# Preliminary

SPECTRALINEAR

# SL23EP08

# Low Jitter and Skew 10 to 220 MHz Zero Delay Buffer (ZDB)

## Key Features

- 10 to 220 MHz operating frequency range
- Low output clock skew: 70ps-typ
- Low output clock Jitter: 50 ps-typ
  - 50 ps-typ at 166MHz, CL=15pF and VDD=3.3V
  - 75 ps-typ at 166MHz, CL=15pF and VDD=2.5V
- Low part-to-part output skew: 150 ps-typ
- 3.3V to 2.5V power supply range
- Low power dissipation:
  - 22 mA-typ at 66MHz and VDD=3.3V
  - 20 mA-typ at 66MHz and VDD=2.5V
- One input drives 8 outputs
- Multiple configurations and drive options
- Select mode to bypass PLL or tri-state outputs
- SpreadThru™ PLL that allows use of SSCG
- Available in 16-pin SOIC and TSSOP packages
- Available in Commercial and Industrial grades

## Applications

- Printers, MFPs and Digital Copiers
- PCs and Work Stations
- Routers, Switchers and Servers
- Datacom and Telecom
- High-Speed Digital Embeded Systems

## Description

The SL23EP08 is a low skew, low jitter and low power Zero Delay Buffer (ZDB) designed to produce up to eight (8) clock outputs from one (1) reference input clock, for high speed clock distribution applications.

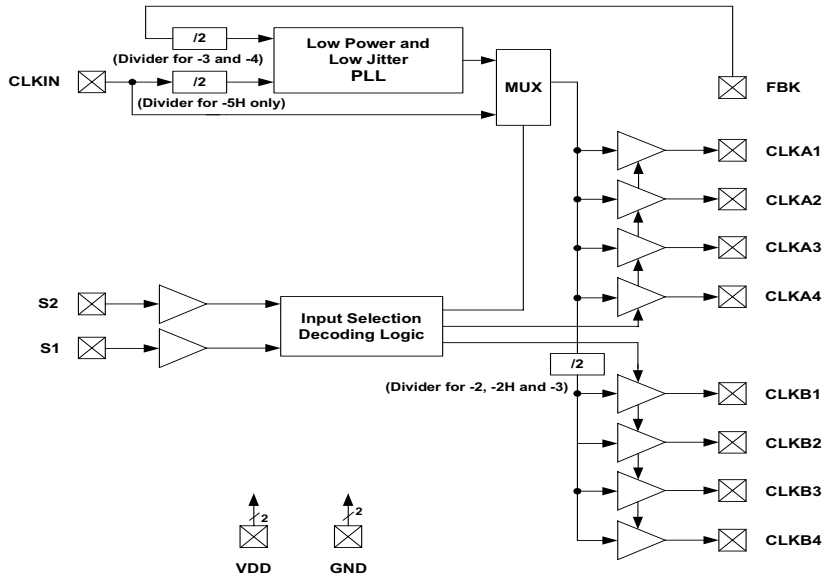
The product has an on-chip PLL and a feedback pin (FBK) which can be used to obtain feedback from any one of the output clocks. The SL23EP08 has two (2) clock driver banks each with four (4) clock outputs. These outputs are controlled by two (2) select input pins S1 and S2. When only four (4) outputs are needed, bank-B output clock buffers can be tri-stated to reduce power dissipation and jitter. The select inputs can also be used to tri-state both banks A and B or drive them directly from the input bypassing the PLL and making the product behave like a Non-Zero Delay Buffer (NZDB). The SL23EP08 offers various X/2,1X, 2X and 4x frequency options at the output clocks. Refer to the "Product Configuration Table" for the details.

The SL23EP08-1H, -2H and 5H versions operates up to 220 MHz and SL23EP08-1, -2, -3 and -4 versions operate up to 133 MHz with CL=15pF output load.

## Benefits

- Up to eight (8) distribution of input clock
- Standard and High-Dirive levels to control impedance level, frequency range and EMI
- Low skew, jitter and power dissipation

## Block Diagram







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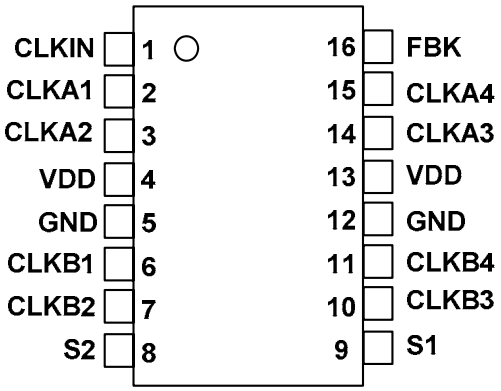
## Pin Configuration




**16-Pin SOIC/TSSOP**

## Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | CLKIN | Input | Reference Frequency Clock Input. 5V tolerant input. Weak pull-down (250kΩ). |
| 2 | CLKA1 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 3 | CLKA2 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 4 | VDD | Power | 3.3V to 2.5V Power Supply. |
| 5 | GND | Power | Power Ground. |
| 6 | CLKB1 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 7 | CLKB2 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 8 | S2 | Input | Select Input, select pin S2. Weak pull-up (250kΩ). |
| 9 | S1 | Input | Select Input, select pin S1. Weak pull-up (250kΩ). |
| 10 | CLKB3 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 11 | CLKB4 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 12 | GND | Power | Power Ground. |
| 13 | VDD | Power | 3.3V to 2.5V Power Supply. |
| 14 | CLKA3 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 15 | CLKA4 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 16 | FBK | Output | PLL Feedback input. |

## General Description

The SL23EP08 is a low skew, low jitter Zero Delay Buffer with very low operating current.

The product includes an on-chip high performance PLL that locks into the input reference clock and produces eight (8) output clock drivers tracking the input reference clock for systems requiring clock distribution.

in addition to FBK pin used for internal PLL feedback, there are two (2) banks with four (4) outputs in each bank, bringing the number of total available output clocks to eight (8).

## Input and output Frequency Range

The input and output frequency range is the same for SL23EP08-1 and -1H versions. For SL23EP08-2, -2H -3, -4 and -5H versions, the output frequency is 1/2x, 1x, 2x, or 4x of the CLKIN as given in the "Available SL23EP08 Configurations" Table 3. But, the frequency range depends on VDD and drive levels as given in the "Electrical Specifications" Tables.

If the input clock frequency is DC (from GND to VDD), this is detected by an input frequency detection circuitry and all eight (8) clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 10 µA supply current.

## SpreadThru™ Feature

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL23EP08 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its reference input to the output clocks. The same spread characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency.

## Select Input Control

The SL23EP08 provides two (2) input select control pins called S1 and S2. This feature enables users to selects various states of output clock banks-A and bank-B, output source and PLL shutdown features as shown in the Table 2.

The S1 (Pin-9) and S2 (Pin-8) inputs include 250 kΩ weak pull-down resistors to GND.

## PLL Bypass Mode

If the S2=1 and S2=0 pins, the on-chip PLL is shutdown and bypassed, and all the eight (8) output clocks of bank A and bank B are driven directly from the reference input clock. In this operation mode SL23EP08 works like a non-ZDB product.

## High and Low-Drive Product Options

The SL23EP08 is offered with high drive "-1H, -2H and -5H" and standard drive "-1, -2, -3 and -4" options. These drive options enable the users to control load levels, frequency range and EMI control. Refer to the AC electrical tables for the details.

SL23EP08-5H is offered only with high drive option. SL23EP08-3 and -4 are offered only with standard drive option.

## Skew and Zero Delay

All outputs should drive the similar load to achieve output-to-output skew and input-to-output delay specifications given in the AC electrical tables. However, Zero delay between input and outputs can be adjusted by changing the loading of FBK pin relative to the banks A and B clocks since FBK is the feedback to the PLL.

## Power Supply Range (VDD)

The SL23EP08 is designed to operate with from 3.3V to 2.5V VDD power supply range. An internal on-chip voltage regulator is used to provide PLL constant power supply of 1.8V, leading to a consistent and stable PLL electrical performance in terms of skew, jitter and power dissipation. The SL2308 I/O is powered by using VDD.

Contact SLI for 1.8V power supply version ZDB called SL23EPL08.

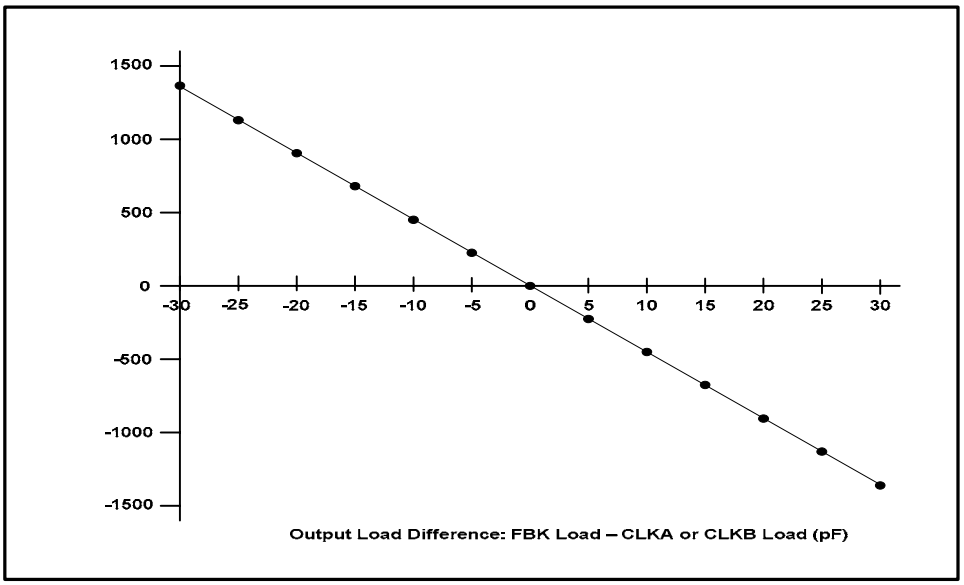



**Figure 1. CLKIN Input to CLKA and CLKB Delay**

| S2 | S1 | Clock A1-A4 | Clock B1-B4 | Output Source | PLL Shutdown and Bypass |
|---|---|---|---|---|---|
| 0 | 0 | Tri-state | Tri-state | PLL | Yes |
| 0 | 1 | Driven | Tri-state | PLL | No |
| 1 | 0 | Driven | Driven | Reference(CLKIN) | Yes |
| 1 | 1 | Driven | Driven | PLL | No |

**Table 2. Select Input Decoding**

| Device | Feedback From | Bank-A Frequency | Bank-B Frequency |
|---|---|---|---|
| SL23EP08-1 and 1H | Bank-A or Bank-B | Reference | Reference |
| SL23EP08-2 and -2H[1] | Bank-A | Reference | Reference/2 |
| SL23EP08-2 and -2H[1] | Bank-B | 2x Reference | Reference |
| SL23EP08-3[1] | Bank-A | 2xReference | Reference[2] |
| SL23EP08-3[1] | Bank-B | 4xReference | 2xReference |
| SL23EP08-4 | Bank-A or Bank-B | 2x Reference | 2x Reference |
| SL23EP08-5H | Bank-A or Bank-B | Reference/2 | Reference/2 |

**Table 3. Available SL23EP08 Configurations**

**Notes:**

1. Outputs are inverted on SL23EP08-2, -2H and -3 in PLL bypass mode when S2=1 and S1=0. Use SL23EP08-1 if non-inverting outputs are required.
2. Output phase is random (0° or 180° with respect to input clock). Use SL23EP08-2 if phase integrity is required.

## Absolute Maximum Ratings

| Description | Condition | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage, VDD | | -0.5 | 4.6 | V |
| All Inputs and Outputs | | -0.5 | VDD+0.5 | V |
| Ambient Operating Temperature | In operation, C-Grade | 0 | 70 | °C |
| Ambient Operating Temperature | In operation, I-Grade | -40 | 85 | °C |
| Storage Temperature | No power is applied | -65 | 150 | °C |
| Junction Temperature | In operation, power is applied | - | 125 | °C |
| Soldering Temperature | | - | 260 | °C |
| ESD Rating (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |

## Operating Conditions (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | VDD+/-10% | 2.97 | 3.3 | 3.63 | V |
| Operating Temperature | TA | Ambient Temperature | 0 | - | 70 | °C |
| Input Capacitance | VIH | Pins 1, 8, 9 and 16 | - | 5 | 7 | pF |

## DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input LOW Voltage | VINL | CLKIN, S2 and S1 pins | – | – | 0.8 | V |
| Input HIGH Voltage | VINH | CLKIN, S2 and S1 pins | 2.0 | – | VDD+0.3 | V |
| Input LOW Current | IINL | 0 < VIN < 0.8V<br>CLKIN, S2 and S1 inputs | – | 25 | 50 | µA |
| Input HIGH Current | IINH | VIN = 2.4 to VDD<br>CLKIN, S2 and S1 inputs | – | – | 50 | µA |
| Output LOW Voltage | VOL | IOL = 8 mA (standard drive) | – | – | 0.4 | V |
| | | IOL = 12 mA (high drive) | – | – | 0.4 | V |
| Output HIGH Voltage | VOH | IOH = –8 mA (standard drive) | 2.4 | – | – | V |
| | | IOH = –12 mA (high drive) | 2.4 | – | – | V |
| Power Down Supply Current | IIDDPD | Measured at CLKIN= GND to VDD or input is floating | – | 8 | 12 | µA |
| Power Supply Current | IDD1 | All Outputs CL=0, 33.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 16 | 20 | mA |
| Power Supply Current | IDD2 | All Outputs CL=0, 66.6 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 22 | 28 | mA |
| Power Supply Current | IDD3 | All Outputs CL=0, 100 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 28 | 36 | mA |
| Power Supply Current | IDD4 | All Outputs CL=0, 133.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 34 | 44 | mA |
| Pull-up and Pull-down Resistors | RPUD | Pins-1/2/3/7/8/9/10/11/14/15<br>250kΩ-typ | 175 | 250 | 325 | kΩ |

## Switching Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Frequency Range | FOUT1 | CL=15pf, -1H and -2H | 10 | - | 220 | MHz |
| | FOUT2 | CL=22pf, -1H and -2H | 10 | - | 200 | MHz |
| | FOUT3 | CL=30pf, -1H and -2H | 10 | - | 135 | MHz |
| | FOUT4 | CL=15pf, -1, -2 and -4 | 10 | - | 200 | MHz |
| | FOUT5 | CL=22pf, -1, -2 and -4 | 10 | - | 135 | MHz |
| | FOUT6 | CL=30pf, -1, -2 and -4 | 10 | - | 100 | MHz |
| Input Duty Cycle | DC1 | Measured at VDD/2, all versions | 30 | 50 | 70 | % |
| Output Duty Cycle | DC2 | CL=30pF, Fout=66 MHz, all versions<br>Measured at VDD/2 | 40 | 50 | 60 | % |

## Switching Electrical Characteristics (C-Grade-Cont.)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| | | | | | | |
|---|---|---|---|---|---|---|
| Output Duty Cycle | DC3 | CL=15pF, Fout=66 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Duty Cycle | DC4 | CL=15pF, Fout=133 MHz, all versions Measured at VDD/2 | 40 | 50 | 60 | % |
| Output Duty Cycle | DC5 | CL=15pF, Fout=166 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Rise/Fall Time | tr/f1 | CL=30pF, -1, -2 and -4 versions | - | - | 2.2 | ns |
| Output Rise/Fall Time | tr/f2 | CL=15pF, -1, -2 and -4 versions | - | - | 1.5 | ns |
| Output Rise/Fall Time | tr/f3 | CL=30pF, -1H and -2H and versions | - | - | 1.5 | ns |
| Output Rise/Fall Time | tr/f4 | CL=15pF, -1H and -2H and versions | - | - | 1.2 | ns |
| Output-to-Output Skew on Same Bank | SKW2 | -1 and -2, measured from 0.8V to 2.0V, and outputs are equally loaded | - | 80 | 150 | ps |
| Output-to-Output Skew on Same Bank | SKW2 | -1H and -2H and -4, measured at VDD/2 and outputs are equally loaded | - | 70 | 150 | ps |
| Output-to-Output Skew Between Bank A and B | SKW3 | -1, -1H, 2H and -4, measured at VDD/2 and outputs are equally loaded | - | 80 | 150 | ps |
| Output-to-Output Skew Between Bank A and B | SKW4 | -2, measured at VDD/2 and outputs are equally loaded | - | 130 | 300 | ps |
| Device-to-Device Skew | SKW5 | All versions, measured at VDD/2 and outputs are equally loaded | - | 150 | 400 | ps |
| Input-to-Output Delay | Dt | All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded and S2=S1=1 | -200 | - | 200 | ps |
| Cycle-to-Cycle Jitter (-1 and -2 Versions) | CCJ1 | Fout=66 MHz and CL=15pF | - | 75 | 150 | ps |
| | | Fout=66MHz and CL=30PF | - | 100 | 200 | ps |
| | | Fout=166MHz and CL=15pF | - | 50 | 100 | ps |
| Cycle-to-Cycle Jitter (-1H, -2H and -4 Versions) | CCJ2 | Fout=66 MHz and CL=15pF | - | 100 | 200 | ps |
| | | Fout=133MHz and CL=30PF | - | 150 | 300 | ps |
| | | Fout=166MHz and CL=15pF | - | 75 | 150 | ps |
| PLL Lock Time | tLOCK | From 0.95VDD and valid clock presented at CLKIN | - | - | 1.0 | ms |

## Operating Conditions (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | VDD+/-10% | 2.97 | 3.3 | 3.63 | V |
| Operating Temperature | TA | Ambient Temperature | -40 | - | 85 | °C |
| Input Capacitance | VIH | Pins 1, 8, 9 and 16 | - | 5 | 8 | pF |

## DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input LOW Voltage | VINL | CLKIN, S2 and S1 pins | – | – | 0.8 | V |
| Input HIGH Voltage | VINH | CLKIN, S2 and S1 pins | 2.0 | – | VDD+0.3 | V |
| Input LOW Current | IINL | 0 < VIN < 0.8V<br>CLKIN, S2 and S1 inputs | – | 25 | 50 | µA |
| Input HIGH Current | IINH | VIN = 2.4 to VDD<br>CLKIN, S2 and S1 inputs | – | – | 50 | µA |
| Output LOW Voltage | VOL | IOL = 8 mA (standard drive) | – | – | 0.4 | V |
| | | IOL = 12 mA (high drive) | – | – | 0.4 | V |
| Output HIGH Voltage | VOH | IOH = –8 mA (standard drive) | 2.4 | – | – | V |
| | | IOH = –12 mA (high drive) | 2.4 | – | – | V |
| Power Down Supply Current | IIDDPD | Measured at CLKIN= GND to VDD or input is floating | – | 12 | 18 | µA |
| Power Supply Current | IDD1 | All Outputs CL=0, 33.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 17 | 22 | mA |
| Power Supply Current | IDD2 | All Outputs CL=0, 66.6 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 24 | 32 | mA |
| Power Supply Current | IDD3 | All Outputs CL=0, 100 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 30 | 40 | mA |
| Power Supply Current | IDD4 | All Outputs CL=0, 133.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 38 | 50 | mA |
| Pull-up and Pull-down Resistors | RPUD | Pins-1/2/3/7/8/9/10/11/14/15<br>250kΩ-typ | 125 | 250 | 375 | kΩ |

## Switching Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 2.5+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Frequency Range | FOUT1 | CL=15pf, -1H and -2H versions | 10 | - | 220 | MHz |
| | FOUT2 | CL=22pf, -1H and -2H versions | 10 | - | 200 | MHz |
| | FOUT3 | CL=30pf, -1H and -2H versions | 10 | - | 135 | MHz |
| | FOUT4 | CL=15pf, -1, -2 and -4 versions | 10 | - | 200 | MHz |
| | FOUT5 | CL=22pf, -1, -2 and -4 versions | 10 | - | 135 | MHz |
| | FOUT6 | CL=30pf, -1, -2 and -4 versions | 10 | - | 100 | MHz |
| Input Duty Cycle | DC1 | Measured at VDD/2, all versions | 30 | 50 | 70 | % |
| Output Duty Cycle | DC2 | CL=30pF, Fout=66 MHz, all versions | 40 | 50 | 60 | % |
| Output Duty Cycle | DC3 | CL=15pF, Fout=66 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Duty Cycle | DC4 | CL=15pF, Fout=133 MHz, all versions Measured at VDD/2 | 40 | 50 | 60 | % |
| Output Duty Cycle | DC5 | CL=15pF, Fout=166 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Rise/Fall Time | tr/f1 | CL=30pF, -1, -2 and -4 versions | - | - | 2.2 | ns |
| Output Rise/Fall Time | tr/f2 | CL=15pF, -1, -2 and -4 versions | - | - | 1.5 | ns |
| Output Rise/Fall Time | tr/f3 | CL=30pF, -1H and -2H and versions | - | - | 1.5 | ns |
| Output Rise/Fall Time | tr/f4 | CL=15pF, -1H and -2H and versions | - | - | 1.2 | ns |
| Output-to-Output Skew on Same Bank | SKW2 | -1 and -2, measured from 0.8V to 2.0V, and outputs are equally loaded | - | 80 | 150 | ps |
| Output-to-Output Skew on Same Bank | SKW2 | -1H and -2H and -4, measured at VDD/2 and outputs are equally loaded | - | 70 | 150 | ps |
| Output-to-Output Skew Between Bank A and B | SKW3 | -1, -1H, 2H and -4, measured at VDD/2 and outputs are equally loaded | - | 80 | 150 | ps |
| Output-to-Output Skew Between Bank A and B | SKW4 | -2, measured at VDD/2 and outputs are equally loaded | - | 130 | 300 | ps |
| Device-to-Device Skew | SKW5 | All versions, measured at VDD/2 and outputs are equally loaded | - | 250 | 500 | ps |
| Input-to-Output Delay | Dt | All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded and S2=S1=1 | -200 | - | 200 | ps |
| Cycle-to-Cycle Jitter (-1 and -2 Versions) | CCJ1 | Fout=66 MHz and CL=15pF | - | 85 | 150 | ps |
| | | Fout=66MHz and CL=30PF | - | 110 | 225 | ps |
| | | Fout=166MHz and CL=15pF | - | 65 | 115 | ps |
| Cycle-to-Cycle Jitter | CCJ2 | Fout=66 MHz and CL=15pF | - | 110 | 225 | ps |

| | | | | | | |
|---|---|---|---|---|---|---|
| (-1H, -2H and -4 Versions) | | Fout=133MHz and CL=30PF | - | 175 | 350 | ps |
| | | Fout=166MHz and CL=15pF | - | 100 | 175 | ps |
| PLL Lock Time | tLOCK | From 0.95VDD and valid CLKIN | - | - | 1.0 | ms |

## Operating Conditions (C-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | VDD+/-10% | 2.25 | 2.5 | 2.75 | V |
| Operating Temperature | TA | Ambient Temperature | 0 | - | 70 | °C |
| Input Capacitance | VIH | Pins 1, 8, 9 and 16 | - | 5 | 7 | pF |

## DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input LOW Voltage | VINL | CLKIN, S2 and S1 pins | – | – | 0.7 | V |
| Input HIGH Voltage | VINH | CLKIN, S2 and S1 pins | 1.7 | – | VDD+0.3 | V |
| Input LOW Current | IINL | 0 < VIN < 0.7V<br>CLKIN, S2 and S1 inputs | – | 25 | 50 | µA |
| Input HIGH Current | IINH | VIN = 1.7 to VDD<br>CLKIN, S2 and S1 inputs | – | – | 50 | µA |
| Output LOW Voltage | VOL | IOL = 6 mA (standard drive) | – | – | 0.3 | V |
| | | IOL = 8 mA (high drive) | – | – | 0.3 | V |
| Output HIGH Voltage | VOH | IOH = – 6 mA (standard drive) | 2.0 | – | – | V |
| | | IOH = – 8 mA (high drive) | 2.0 | – | – | V |
| Power Down Supply Current | IIDDPD | Measured at CLKIN= GND to VDD or input is floating | – | 8 | 12 | µA |
| Power Supply Current | IDD1 | All Outputs CL=0, 33.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 15 | 18 | mA |
| Power Supply Current | IDD2 | All Outputs CL=0, 66.6 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 20 | 25 | mA |
| Power Supply Current | IDD3 | All Outputs CL=0, 100 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 26 | 33 | mA |
| Power Supply Current | IDD4 | All Outputs CL=0, 133.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 32 | 40 | mA |
| Pull-up and Pull-down Resistors | RPUD | Pins-1/2/3/7/8/9/10/11/14/15<br>250kΩ-typ | 125 | 250 | 375 | kΩ |

## Switching Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 2.5+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Frequency Range | FOUT1 | CL=15pf, -1H and -2H | 10 | - | 170 | MHz |
| | FOUT2 | CL=22pf, -1H and -2H | 10 | - | 135 | MHz |
| | FOUT1 | CL=30pf, -1H and -2H | 10 | - | 100 | MHz |
| | FOUT4 | CL=15pf, -1, -2 and -4 | 10 | - | 135 | MHz |
| | FOUT5 | CL=22pf, -1, -2 and -4 | 10 | - | 100 | MHz |
| | FOUT1 | CL=30pf, -1, -2 and -4 | 10 | - | 75 | MHz |
| Input Duty Cycle | DC1 | Measured at VDD/2, all versions | 30 | 50 | 70 | % |

## Switching Electrical Characteristics (C-Grade-Cont.)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

| | | | | | | |
|---|---|---|---|---|---|---|
| Output Duty Cycle | DC2 | CL=15pF, Fout=66 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Duty Cycle | DC3 | CL=15pF, Fout=133 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Duty Cycle | DC4 | CL=15pF, Fout=166 MHz, all versions Measured at VDD/2 | 40 | 50 | 60 | % |
| Output Rise/Fall Time | tr/f1 | CL=30pF, -1, -2 and -4 versions Measured at 0.6 to 1.8V | - | - | 2.0 | ns |
| Output Rise/Fall Time | tr/f2 | CL=15pF, -1, -2 and -4 versions Measured at 0.6 to 1.8V | - | - | 1.6 | ns |
| Output Rise/Fall Time | tr/f3 | CL=30pF, -1H and -2H and versions Measured at 0.6 to 1.8V | - | - | 1.4 | ns |
| Output Rise/Fall Time | tr/f4 | CL=15pF, -1H and -2H and versions Measured at 0.6 to 1.8V | - | - | 1.1 | ns |
| Output-to-Output Skew on Same Bank | SKW2 | -1 and -2, measured from 0.8V to 2.0V, and outputs are equally loaded | - | 80 | 200 | ps |
| Output-to-Output Skew on Same Bank | SKW2 | -1H and -2H and -4, measured at VDD/2 and outputs are equally loaded | - | 70 | 200 | ps |
| Output-to-Output Skew Between Bank A and B | SKW3 | -1, -1H, 2H and -4, measured at VDD/2 and outputs are equally loaded | - | 80 | 200 | ps |
| Output-to-Output Skew Between Bank A and B | SKW4 | -2, measured at VDD/2 and outputs are equally loaded | - | 130 | 350 | ps |
| Device-to-Device Skew | SKW5 | All versions, measured at VDD/2 and outputs are equally loaded | - | 150 | 500 | ps |
| Input-to-Output Delay | Dt | All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded and S2=S1=1 | -250 | - | 250 | ps |

| | | | | | | |
|---|---|---|---|---|---|---|
| Cycle-to-Cycle Jitter (-1, -2 and -4 Versions) | CCJ1 | Fout=66 MHz and CL=15pF | - | 75 | 150 | ps |
| | | Fout=133MHz and CL=15pF | - | 50 | 100 | ps |
| Cycle-to-Cycle Jitter (-1H and -2H Versions) | CCJ2 | Fout=66MHz and CL=15pF | - | 100 | 200 | ps |
| | | Fout=166MHz and CL=15pF | - | 75 | 150 | ps |
| PLL Lock Time | tLOCK | From 0.95VDD and valid clock presented at CLKIN | - | - | 1.0 | ms |

## Operating Conditions (I-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | VDD+/-10% | 2.25 | 2.5 | 2.75 | V |
| Operating Temperature | TA | Ambient Temperature | -40 | - | 85 | °C |
| Input Capacitance | VIH | Pins 1, 8, 9 and 16 | - | 5 | 8 | pF |

## DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input LOW Voltage | VINL | CLKIN, S2 and S1 pins | – | – | 0.7 | V |
| Input HIGH Voltage | VINH | CLKIN, S2 and S1 pins | 1.7 | – | VDD+0.3 | V |
| Input LOW Current | IINL | 0 < VIN < 0.7V<br>CLKIN, S2 and S1 inputs | – | 25 | 50 | µA |
| Input HIGH Current | IINH | VIN = 1.7V to VDD<br>CLKIN, S2 and S1 inputs | – | – | 50 | µA |
| Output LOW Voltage | VOL | IOL = 6 mA (standard drive) | – | – | 0.3 | V |
| | | IOL = 8 mA (high drive) | – | – | 0.3 | V |
| Output HIGH Voltage | VOH | IOH = –6 mA (standard drive) | 2.0 | – | – | V |
| | | IOH = –8 mA (high drive) | 2.0 | – | – | V |
| Power Down Supply Current | IIDDPD | Measured at CLKIN= GND to VDD or input is floating | – | 8 | 12 | µA |
| Power Supply Current | IDD1 | All Outputs CL=0, 33.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 16 | 20 | mA |
| Power Supply Current | IDD2 | All Outputs CL=0, 66.6 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 21 | 28 | mA |
| Power Supply Current | IDD3 | All Outputs CL=0, 100 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 27 | 36 | mA |
| Power Supply Current | IDD4 | All Outputs CL=0, 133.3 MHz CLKIN<br>S2=S1=1 (high), all versions | – | 34 | 44 | mA |
| Pull-up and Pull-down Resistors | RPUD | Pins-1/2/3/7/8/9/10/11/14/15<br>250kΩ-typ | 125 | 250 | 375 | kΩ |

## Switching Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Frequency Range | FOUT1 | CL=15pf, -1H and -2H versions | 10 | - | 175 | MHz |
| | FOUT2 | CL=22pf, -1H and -2H versions | 10 | - | 135 | MHz |
| | FOU3 | CL=30pF, -1H and -2H versions | 10 | - | 100 | MHz |
| | FOUT4 | CL=15pf, -1, -2 and -4 versions | 10 | - | 135 | MHz |
| | FOUT5 | CL=22pf, -1, -2 and -4 versions | 10 | - | 100 | MHz |
| | FOUT6 | CL=30pf, -1, -2 and -4 versions | 10 | - | 75 | MHz |
| Input Duty Cycle | DC1 | Measured at VDD/2, all versions | 30 | 50 | 70 | % |
| Output Duty Cycle | DC2 | CL=30pF, Fout=66 MHz, all versions<br>Measured at VDD/2 | 40 | 50 | 60 | % |

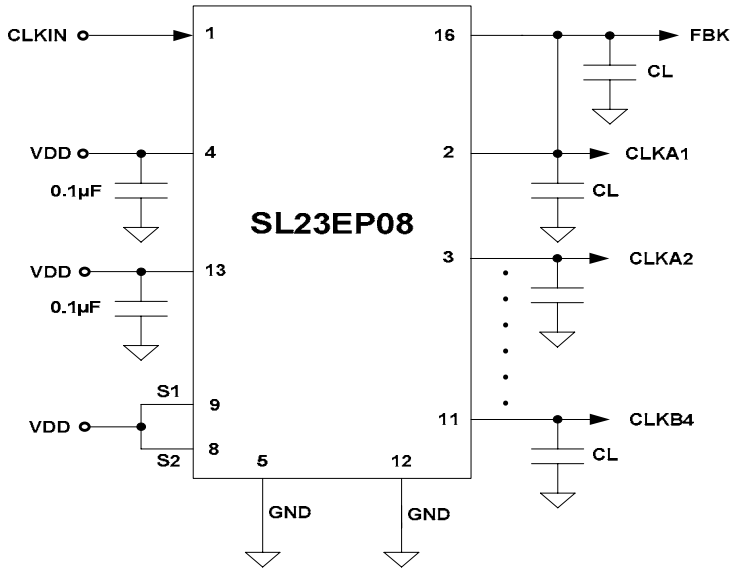
## Switching Electrical Characteristics (I-Grade-Cont.)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

| | | | | | | |
|---|---|---|---|---|---|---|
| Output Duty Cycle | DC3 | CL=15pF, Fout=66 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Duty Cycle | DC4 | CL=15pF, Fout=133 MHz, all versions Measured at VDD/2 | 45 | 50 | 55 | % |
| Output Duty Cycle | DC5 | CL=15pF, Fout=166 MHz, all versions Measured at VDD/2 | 40 | 50 | 60 | % |
| Output Rise/Fall Time | tr/f1 | CL=30pF, -1, -2 and -4 versions Measured at 0.6 to 1.8V | - | - | 2.2 | ns |
| Output Rise/Fall Time | tr/f2 | CL=15pF, -1, -2 and -4 versions Measured at 0.6 to 1.8V | - | - | 1.8 | ns |
| Output Rise/Fall Time | tr/f3 | CL=30pF, -1H and -2H and versions Measured at 0.6 to 1.8V | - | - | 1.5 | ns |
| Output Rise/Fall Time | tr/f4 | CL=15pF, -1H and -2H and versions Measured at 0.6 to 1.8V | - | - | 1.2 | ns |
| Output-to-Output Skew on Same Bank | SKW2 | -1 and -2, measured from 0.8V to 2.0V, and outputs are equally loaded | - | 100 | 220 | ps |
| Output-to-Output Skew on Same Bank | SKW2 | -1H and -2H and -4, measured at VDD/2 and outputs are equally loaded | - | 100 | 220 | ps |
| Output-to-Output Skew Between Bank A and B | SKW3 | -1, -1H, 2H and -4, measured at VDD/2 and outputs are equally loaded | - | 100 | 220 | ps |
| Output-to-Output Skew Between Bank A and B | SKW4 | -2, measured at VDD/2 and outputs are equally loaded | - | 180 | 375 | ps |
| Device-to-Device Skew | SKW5 | All versions, measured at VDD/2 and outputs are equally loaded | - | 275 | 550 | ps |
| Input-to-Output Delay | Dt | All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded and S2=S1=1 | -200 | - | 200 | ps |
| Cycle-to-Cycle Jitter (-1, -2 and -4 Versions) | CCJ1 | Fout=66 MHz and CL=15pF | - | 80 | 175 | ps |
| | | Fout=133MHz and CL=15pF | - | 70 | 150 | ps |
| Cycle-to-Cycle Jitter (-1H and -2H Versions) | CCJ2 | Fout=66 MHz and CL=15pF | - | 70 | 150 | ps |
| | | Fout=166MHz and CL=15pF | - | 60 | 125 | ps |
| PLL Lock Time | tLOCK | From 0.95VDD and valid CLKIN | - | - | 1.0 | ms |

## External Components & Design Considerations

### Typical Application Schematic




### Comments and Recommendations

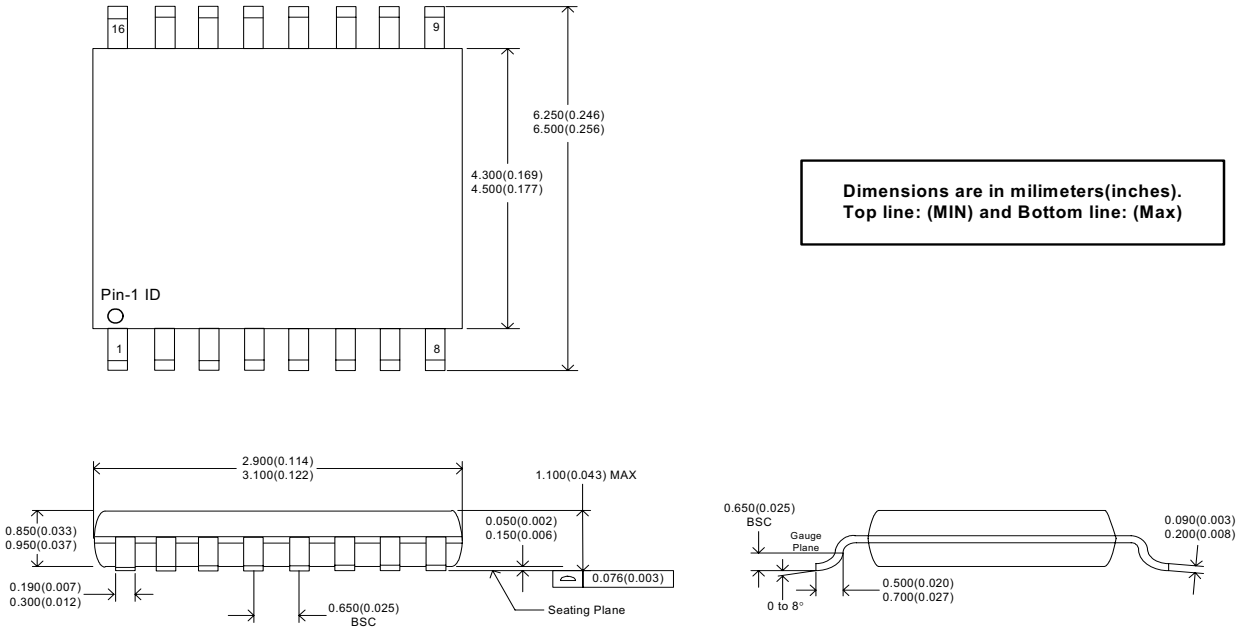
**Decoupling Capacitor:** A decoupling capacitor of 0.1µF must be used between VDD and VSS pins. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

**Series Termination Resistor:** A series termination resistor is recommended if the distance between the output clocks and the load is over 1 ½ inch. The nominal impedance of the clock outputs is given on the page 5. Place the series termination resistors as close to the clock outputs as possible.

**Zero Delay and Skew Control:** All outputs and CLKIN pins should be loaded with the same load to achieve “Zero Delay” between the CLKIN and the outputs. The CLKOUT pin is connected to CLKIN internally on-chip for feedback to PLL. For applications requiring zero input/output delay, the load at the all output pins including the CLKOUT pin must be the same. If any delay adjustment is required, the capacitance at the CLKOUT pin could be increased or decreased to increase or decrease the delay between Bank A and B clocks and CLKIN. For minimum pin-to-pin skew, the external load at all the Bank A and B clocks must be the same.

## Package Outline and Package Dimensions

### 16-Lead TSSOP (4.4mm)

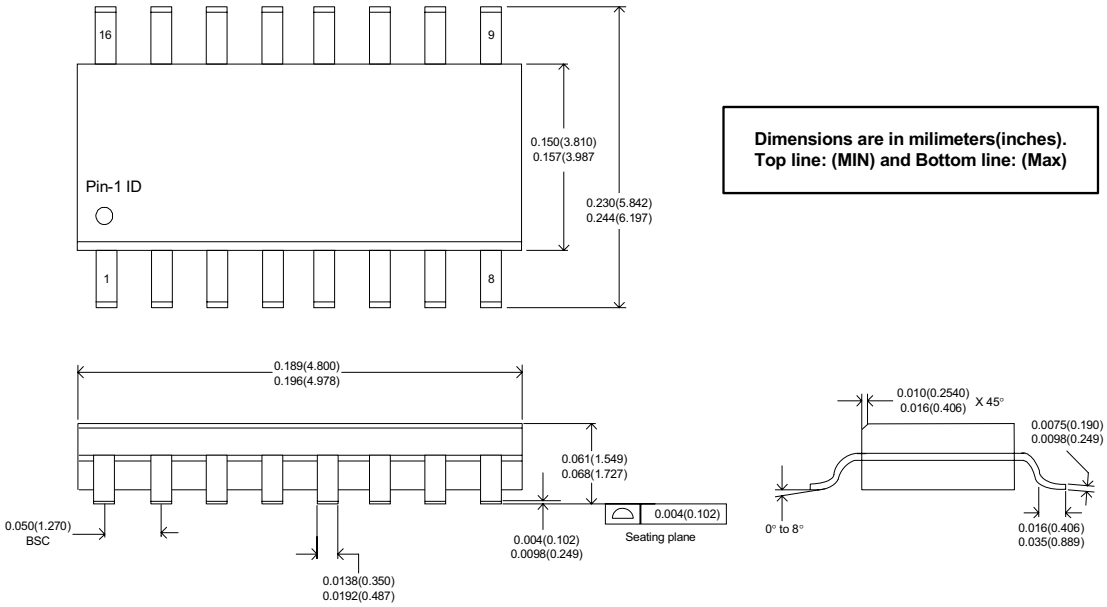



## Thermal Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | θ JA | Still air | - | 80 | - | °C/W |
| | θ JA | 1m/s air flow | - | 70 | - | °C/W |
| | θ JA | 3m/s air flow | - | 68 | - | °C/W |
| Thermal Resistance Junction to Case | θ JC | Independent of air flow | - | 36 | - | °C/W |

## Package Drawing and Dimensions (Cont.)

### 16-Lead SOIC (150 Mil)




## Thermal Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | θ JA | Still air | - | 120 | - | °C/W |
| | θ JA | 1m/s air flow | - | 115 | - | °C/W |
| | θ JA | 3m/s air flow | - | 105 | - | °C/W |
| Thermal Resistance Junction to Case | θ JC | Independent of air flow | - | 60 | - | °C/W |

## Ordering Information [3]

| Ordering Number | Marking | Shipping Package | Package | Temperature |
|---|---|---|---|---|
| SL23EP08SC-1 | SL23EP08SC-1 | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-1T | SL23EP08SC-1 | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-1 | SL23EP08SI-1 | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-1T | SL23EP08SI-1 | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08SC-1H | SL23EP08SC-1H | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-1HT | SL23EP08SC-1H | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-1H | SL23EP08SI-1H | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-1HT | SL23EP08SI-1H | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08ZC-1H | SL23EP08ZC-1H | Tube | 16-pin TSSOP | 0 to 70°C |
| SL23EP08ZC-1HT | SL23EP08ZC-1H | Tape and Reel | 16-pin TSSOP | 0 to 70°C |
| SL23EP08ZI-1H | SL23EP08ZI-1H | Tube | 16-pin TSSOP | -40 to 85°C |
| SL23EP08ZI-1HT | SL23EP08ZI-1H | Tape and Reel | 16-pin TSSOP | -40 to 85°C |
| SL23EP08SC-2 | SL23EP08SC-2 | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-2T | SL23EP08SC-2 | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-2 | SL23EP08SI-2 | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-2T | SL23EP08SI-2 | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08SC-2H | SL23EP08SC-2H | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-2HT | SL23EP08SC-2H | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-4 | SL23EP08SC-4 | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-4T | SL23EP08SC-4 | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-4 | SL23EP08SI-4 | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-4T | SL23EP08SI-4 | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08SC-5H | SL23EP08SC-5H | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-5HT | SL23EP08SC-5H | Tube | 16-pin SOIC | 0 to 70°C |

**Notes:**

3. The SL23EP08 products are RoHS compliant.

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