

**100V P-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$ $T_A = 25^\circ C$
-100V	350m $\Omega$ @ $V_{GS} = -10V$	-1.6
	450m $\Omega$ @ $V_{GS} = -6.0V$	-1.4

**Description and Applications**

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

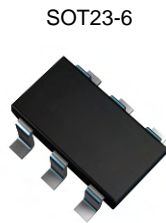
- Motor control
- DC-DC Converters
- Power management functions
- Uninterrupted power supply

**Features and Benefits**

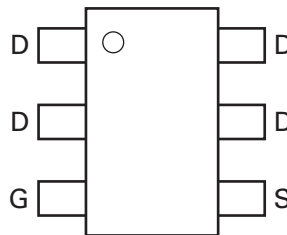
- Fast switching speed
- Low gate drive
- Low input capacitance
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

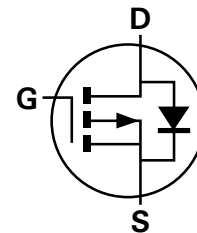
- Case: SOT23-6
- Case Material: Molded Plastic, UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.018 grams (approximate)



Top View



Pin Out - Top View

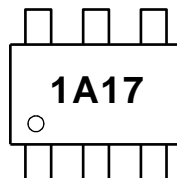


Equivalent Circuit

**Ordering Information**

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMP10A17E6TA	See below	7	8	3,000

**Marking Information**



1A17 = Product Type Marking Code

**Maximum Ratings** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

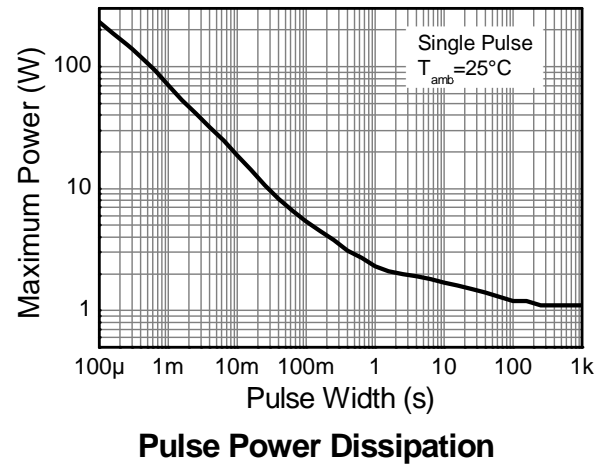
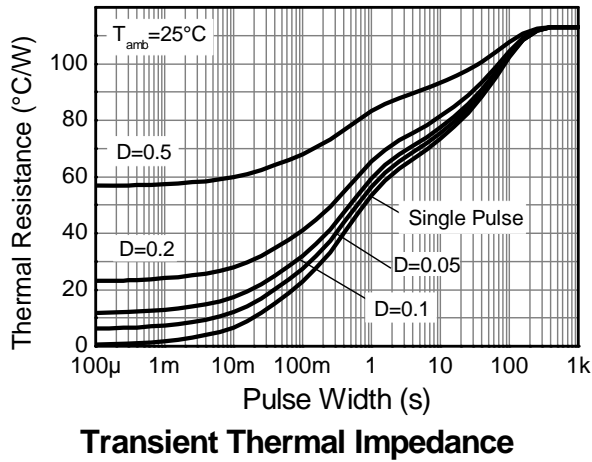
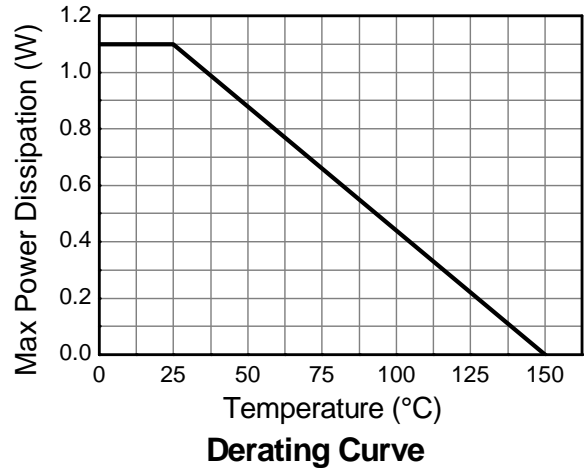
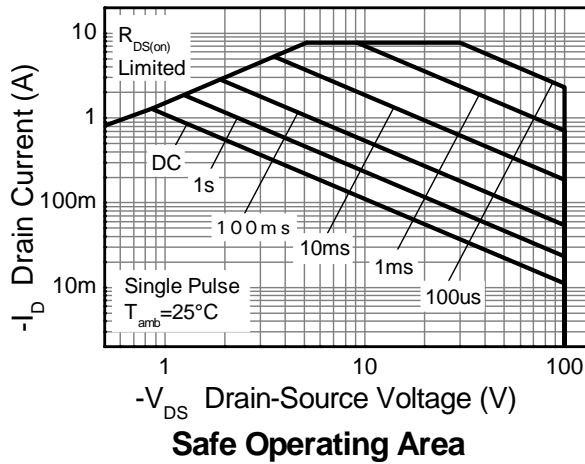
Characteristic			Symbol	Value	Unit	
Drain-Source voltage			$V_{DSS}$	-100	V	
Gate-Source voltage			$V_{GS}$	$\pm 20$	V	
Continuous Drain current	$V_{GS} = 10\text{V}$	(Note 2)	$I_D$	-1.6	A	
		$T_A = 70^\circ\text{C}$ (Note 2)		-1.3		
		(Note 1)		-1.3		
Pulsed Drain current	$V_{GS} = 10\text{V}$	(Note 3)	$I_{DM}$	-7.7	A	
Continuous Source current (Body diode)			(Note 2)	$I_S$	-2.1	A
Pulsed Source current (Body diode)			(Note 3)	$I_{SM}$	-7.7	A

**Thermal Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic		Symbol	Value	Unit
Power dissipation Linear derating factor	(Note 1)	$P_D$	1.1	W mW/ $^\circ\text{C}$
			8.8	
	(Note 2)		1.7 13.7	
Thermal Resistance, Junction to Ambient	(Note 1)	$R_{\theta JA}$	113	$^\circ\text{C/W}$
	(Note 2)		73	
Operating and storage temperature range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

- Notes:
1. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  2. Same as note (1), except the device is measured at  $t \leq 5$  sec.
  3. Same as note (1), except the device is pulsed with  $D = 0.02$  and pulse width 300  $\mu\text{s}$ . The pulse current is limited by the maximum junction temperature.

**Thermal Characteristics**

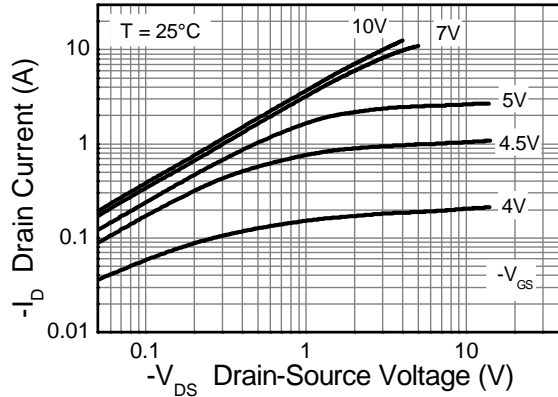


**Electrical Characteristics** @  $T_A = 25^\circ\text{C}$  unless otherwise specified

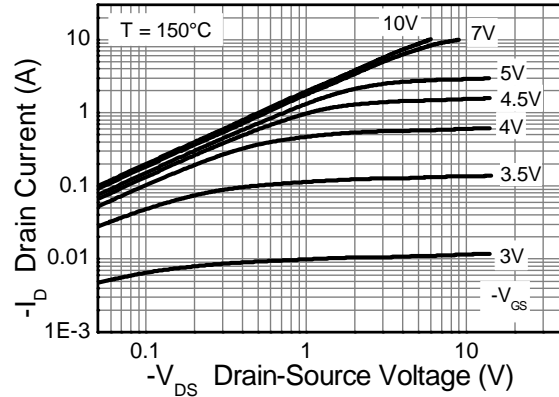
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-100	—	—	V	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-0.5	$\mu\text{A}$	$V_{DS} = -100\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	-2.0	—	-4.0	V	$I_D = -250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 4)	$R_{DS(on)}$	—	—	0.350	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -1.4\text{A}$
				0.450		$V_{GS} = -6\text{V}$ , $I_D = -1.2\text{A}$
Forward Transconductance (Notes 4 & 5)	$g_{fs}$	—	2.8	—	S	$V_{DS} = -15\text{V}$ , $I_D = -1.4\text{A}$
Diode Forward Voltage (Note 4)	$V_{SD}$	—	-0.85	-0.95	V	$I_S = -1.7\text{A}$ , $V_{GS} = 0\text{V}$
Reverse recovery time (Note 5)	$t_{rr}$	—	33	—	ns	$I_S = -1.5\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge (Note 5)	$Q_{rr}$	—	48	—	nC	
<b>DYNAMIC CHARACTERISTICS (Note 5)</b>						
Input Capacitance	$C_{iss}$	—	424	—	pF	$V_{DS} = -50\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	$C_{oss}$	—	36.6	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	29.8	—	pF	
Total Gate Charge (Note 6)	$Q_g$	—	7.1	—	nC	$V_{GS} = -6.0\text{V}$
Total Gate Charge (Note 6)	$Q_g$	—	10.7	—	nC	$V_{GS} = -10\text{V}$ $V_{DS} = -50\text{V}$ $I_D = -1.4\text{A}$
Gate-Source Charge (Note 6)	$Q_{gs}$	—	1.7	—	nC	
Gate-Drain Charge (Note 6)	$Q_{gd}$	—	3.8	—	nC	
Turn-On Delay Time (Note 6)	$t_{D(on)}$	—	3.0	—	ns	$V_{DD} = -50\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -1\text{A}$ , $R_G \cong 6.0\Omega$
Turn-On Rise Time (Note 6)	$t_r$	—	3.5	—	ns	
Turn-Off Delay Time (Note 6)	$t_{D(off)}$	—	13.4	—	ns	
Turn-Off Fall Time (Note 6)	$t_f$	—	7.2	—	ns	

- Notes:
4. Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
  5. For design aid only, not subject to production testing.
  6. Switching characteristics are independent of operating junction temperatures.

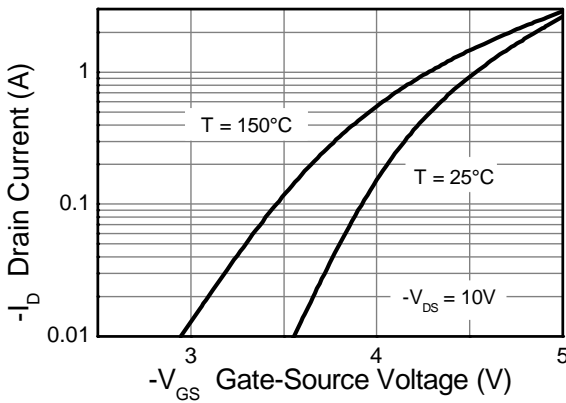
**Typical Characteristics**



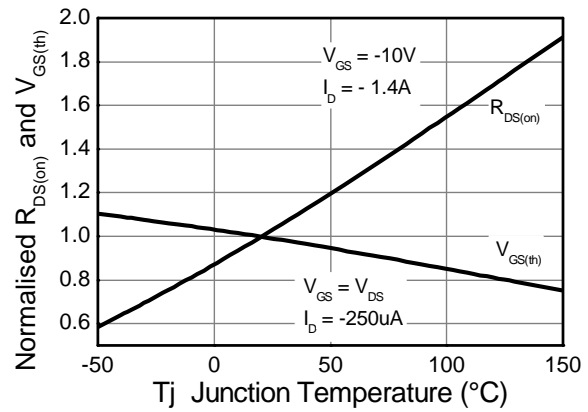
**Output Characteristics**



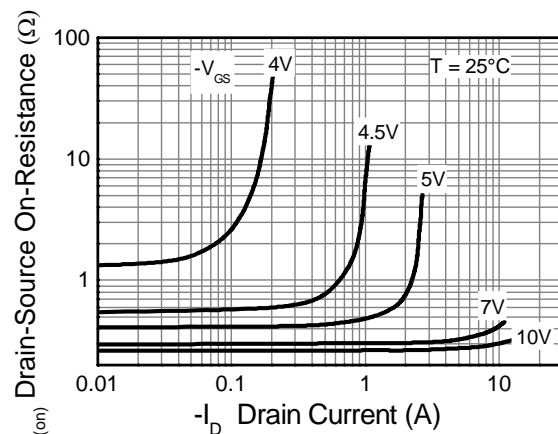
**Output Characteristics**



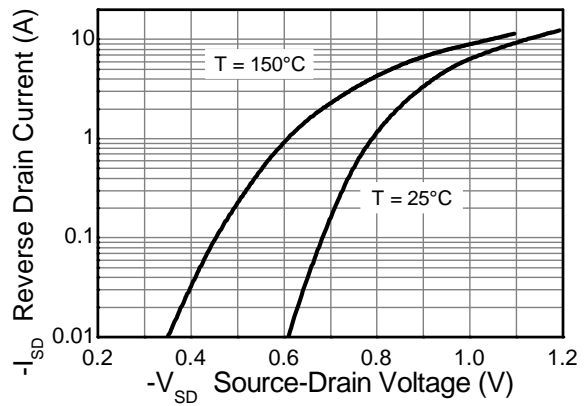
**Typical Transfer Characteristics**



**Normalised Curves v Temperature**

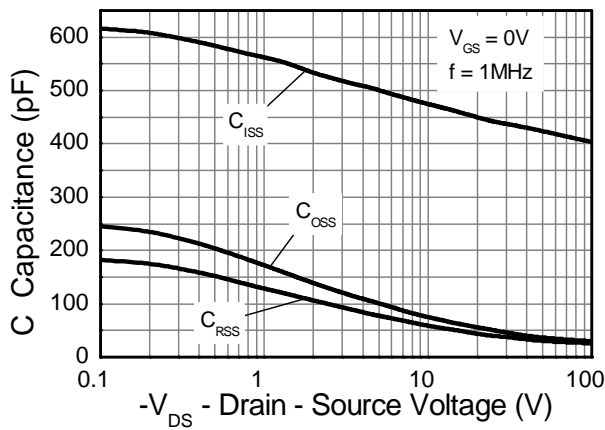


**On-Resistance v Drain Current**

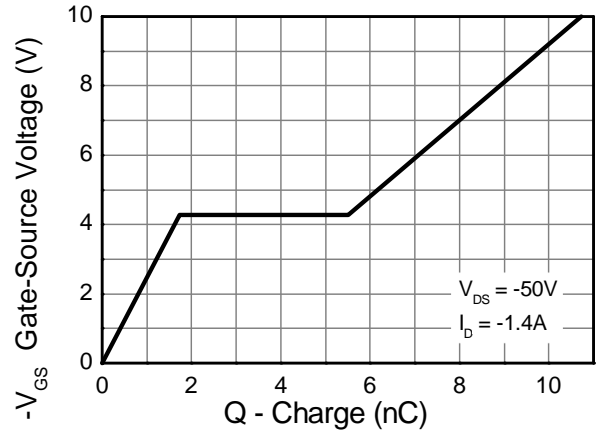


**Source-Drain Diode Forward Voltage**

**Typical Characteristics - continued**

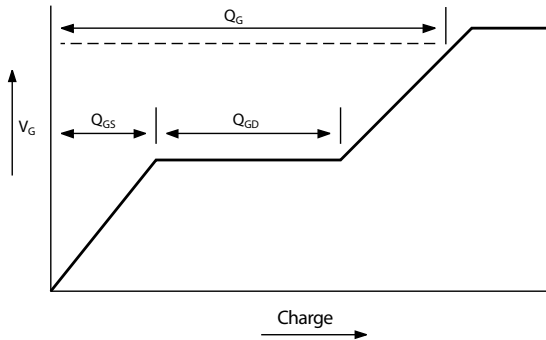


**Capacitance v Drain-Source Voltage**

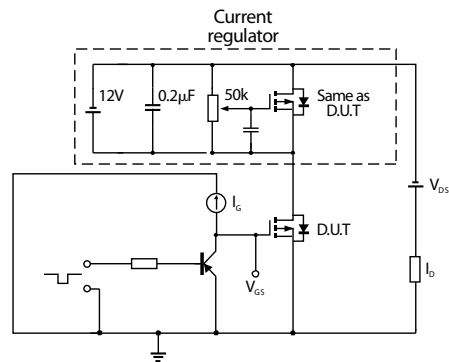


**Gate-Source Voltage v Gate Charge**

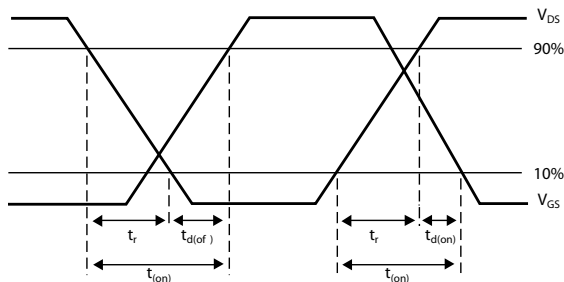
**Test Circuits**



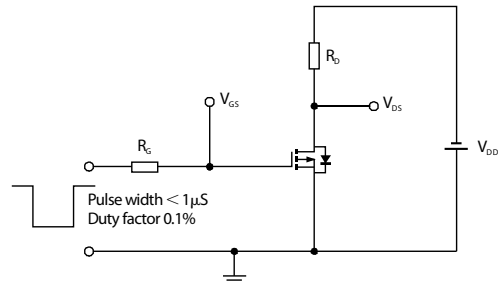
**Basic gate charge waveform**



**Gate charge test circuit**

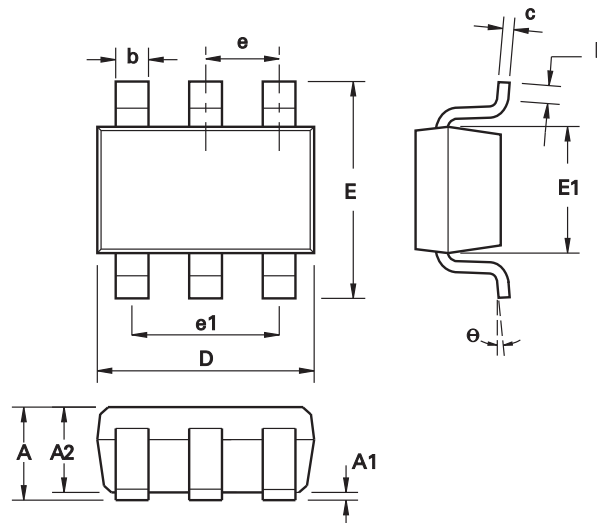


**Switching time waveforms**



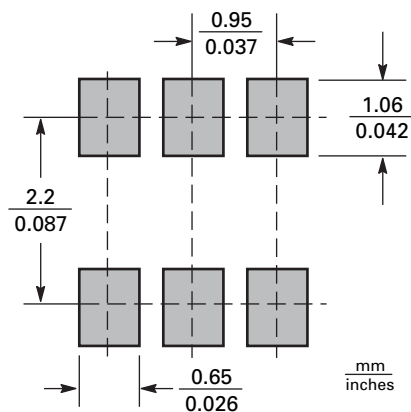
**Switching time test circuit**

**Package Outline Dimensions**



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.45	0.354	0.0570
A1	0.00	0.15	0.00	0.0059
A2	0.90	1.30	0.0354	0.0511
b	0.20	0.50	0.0078	0.0196
C	0.09	0.26	0.0035	0.0102
D	2.70	3.10	0.1062	0.1220
E	2.20	3.20	0.0866	0.1181
E1	1.30	1.80	0.0511	0.0708
L	0.10	0.60	0.0039	0.0236
e	0.95 REF		0.0374 REF	
e1	1.90 REF		0.0748 REF	
$\theta$	0°	30°	0°	30°

**Suggested Pad Layout**



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