



# MICROCHIP MCP6001/1R/1U/2/4

## 1 MHz, Low-Power Op Amp

### Features

- Available in SC-70-5 and SOT-23-5 packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current:  $I_Q = 100 \mu\text{A}$  (typical)
- Phase Margin:  $90^\circ$  (typical)
- Temperature Range:
  - Industrial:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
  - Extended:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Available in Single, Dual and Quad Packages

### Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

### Design Aids

- SPICE Macro Models
- FilterLab<sup>®</sup> Software
- Mindi<sup>™</sup> Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

### Typical Application



### Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and  $90^\circ$  phase margin (typical). It also maintains  $45^\circ$  phase margin (typical) with a 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100  $\mu\text{A}$  (typical) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of  $V_{DD} + 300 \text{ mV}$  to  $V_{SS} - 300 \text{ mV}$ . This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 6.0V.

### Package Types



# MCP6001/1R/1U/2/4

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NOTES:

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
Current at Analog Input Pins ( $V_{IN+}$ , $V_{IN-}$ ) .....	$\pm 2$ mA
Analog Inputs ( $V_{IN+}$ , $V_{IN-}$ ) †† .....	$V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All Other Inputs and Outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage .....	$ V_{DD} - V_{SS} $
Output Short Circuit Current .....	Continuous
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage Temperature .....	$-65^{\circ}C$ to $+150^{\circ}C$
Maximum Junction Temperature ( $T_J$ ) .....	$+150^{\circ}C$
ESD Protection On All Pins (HBM; MM) .....	$\geq 4$ kV; 200V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”.

### DC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^{\circ}C$ ,  $V_{DD} = +1.8V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $V_{CM} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10$  k $\Omega$  to  $V_L$ , and  $V_{OUT} \approx V_{DD}/2$  (refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Input Offset</b>						
Input Offset Voltage	$V_{OS}$	-4.5	—	+4.5	mV	$V_{CM} = V_{SS}$ (Note 1)
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	$\pm 2.0$	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	—	86	—	dB	$V_{CM} = V_{SS}$
<b>Input Bias Current and Impedance</b>						
Input Bias Current:	$I_B$	—	$\pm 1.0$	—	pA	
Industrial Temperature	$I_B$	—	19	—	pA	$T_A = +85^{\circ}C$
Extended Temperature	$I_B$	—	1100	—	pA	$T_A = +125^{\circ}C$
Input Offset Current	$I_{OS}$	—	$\pm 1.0$	—	pA	
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  6$	—	$\Omega  pF$	
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  3$	—	$\Omega  pF$	
<b>Common Mode</b>						
Common Mode Input Range	$V_{CMR}$	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	60	76	—	dB	$V_{CM} = -0.3V$ to $5.3V$ , $V_{DD} = 5V$
<b>Open-Loop Gain</b>						
DC Open-Loop Gain (Large Signal)	$A_{OL}$	88	112	—	dB	$V_{OUT} = 0.3V$ to $V_{DD} - 0.3V$ , $V_{CM} = V_{SS}$
<b>Output</b>						
Maximum Output Voltage Swing	$V_{OL}, V_{OH}$	$V_{SS} + 25$	—	$V_{DD} - 25$	mV	$V_{DD} = 5.5V$ , 0.5V Input Overdrive
Output Short Circuit Current	$I_{SC}$	—	$\pm 6$	—	mA	$V_{DD} = 1.8V$
		—	$\pm 23$	—	mA	$V_{DD} = 5.5V$
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	1.8	—	6.0	V	<b>Note 2</b>
Quiescent Current per Amplifier	$I_Q$	50	100	170	$\mu A$	$I_O = 0$ , $V_{DD} = 5.5V$ , $V_{CM} = 5V$

**Note 1:** MCP6001/1R/1U/2/4 parts with date codes prior to December 2004 (week code 49) were tested to  $\pm 7$  mV minimum/maximum limits.

**2:** All parts with date codes November 2007 and later have been screened to ensure operation at  $V_{DD} = 6.0V$ . However, the other minimum and maximum specifications are measured at 1.8V and 5.5V.

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## AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8$  to  $5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$ , and  $C_L = 60\text{ pF}$  (refer to [Figure 1-1](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>AC Response</b>						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	$G = +1\text{ V/V}$
Slew Rate	SR	—	0.6	—	V/ $\mu\text{s}$	
<b>Noise</b>						
Input Noise Voltage	$E_{ni}$	—	6.1	—	$\mu\text{Vp-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$
Input Noise Voltage Density	$e_{ni}$	—	28	—	nV/ $\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
Input Noise Current Density	$i_{ni}$	—	0.6	—	fA/ $\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$

## TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated,  $V_{DD} = +1.8\text{V to }+5.5\text{V}$  and  $V_{SS} = \text{GND}$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Industrial Temperature Range	$T_A$	-40	—	+85	°C	
Extended Temperature Range	$T_A$	-40	—	+125	°C	
Operating Temperature Range	$T_A$	-40	—	+125	°C	<b>Note</b>
Storage Temperature Range	$T_A$	-65	—	+150	°C	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 5L-SC70	$\theta_{JA}$	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	$\theta_{JA}$	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC (150 mil)	$\theta_{JA}$	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	°C/W	
Thermal Resistance, 8L-DFN (2x3)	$\theta_{JA}$	—	68	—	°C/W	
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	°C/W	

**Note:** The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal Junction Temperature ( $T_J$ ) must not exceed the Absolute Maximum specification of  $+150^\circ\text{C}$ .

## 1.1 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set  $V_{CM}$  and  $V_{OUT}$ ; see Equation 1-1. Note that  $V_{CM}$  is not the circuit's common mode voltage ( $(V_P + V_M)/2$ ), and that  $V_{OST}$  includes  $V_{OS}$  plus the effects (on the input offset error,  $V_{OST}$ ) of temperature, CMRR, PSRR and  $A_{OL}$ .

### EQUATION 1-1:

$$G_{DM} = R_F/R_G$$

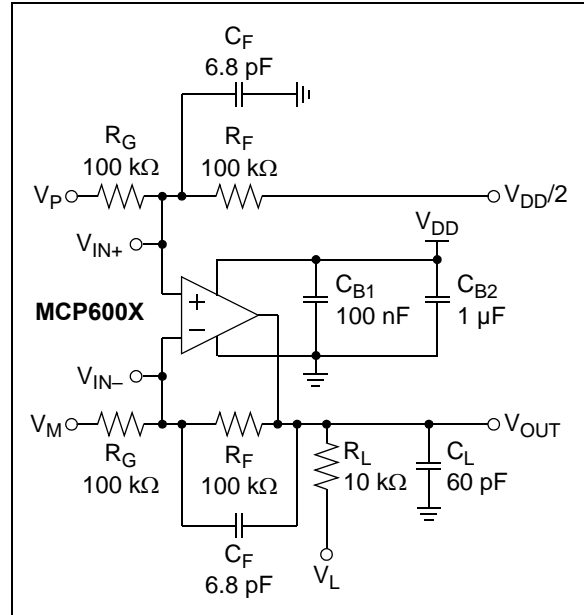
$$V_{CM} = (V_P + V_{DD}/2)/2$$

$$V_{OST} = V_{IN-} - V_{IN+}$$

$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

$G_{DM}$	= Differential Mode Gain	(V/V)
$V_{CM}$	= Op Amp's Common Mode Input Voltage	(V)
$V_{OST}$	= Op Amp's Total Input Offset Voltage	(mV)



**FIGURE 1-1:** AC and DC Test Circuit for Most Specifications.

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NOTES:

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$ , and  $C_L = 60\text{ pF}$ .



**FIGURE 2-1:** Input Offset Voltage.



**FIGURE 2-4:** Input Offset Voltage vs. Common Mode Input Voltage at  $V_{DD} = 1.8\text{V}$ .



**FIGURE 2-2:** Input Offset Voltage Drift.



**FIGURE 2-5:** Input Offset Voltage vs. Common Mode Input Voltage at  $V_{DD} = 5.5\text{V}$ .



**FIGURE 2-3:** Input Offset Quadratic Temp. Co.



**FIGURE 2-6:** Input Offset Voltage vs. Output Voltage.

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**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$ , and  $C_L = 60\text{ pF}$ .



**FIGURE 2-7:** Input Bias Current at  $+85^\circ\text{C}$ .



**FIGURE 2-10:** PSRR, CMRR vs. Frequency.



**FIGURE 2-8:** Input Bias Current at  $+125^\circ\text{C}$ .



**FIGURE 2-11:** Open-Loop Gain, Phase vs. Frequency.



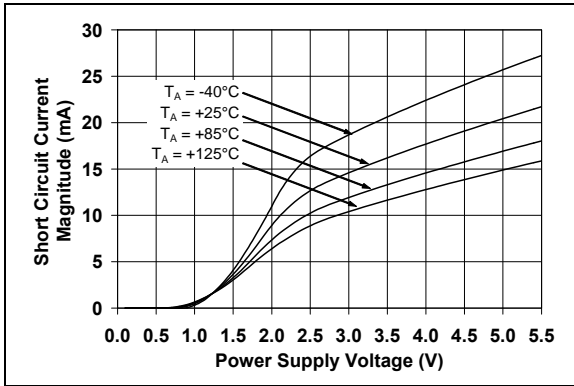
**FIGURE 2-9:** CMRR, PSRR vs. Ambient Temperature.



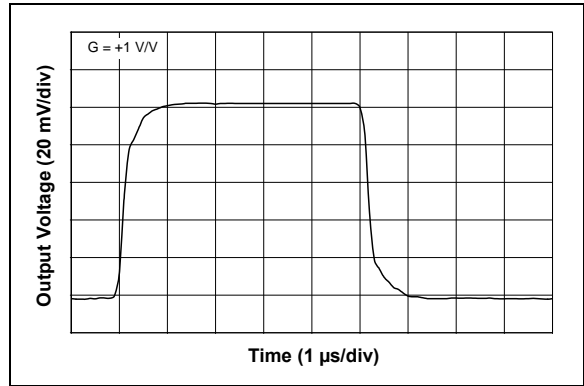
**FIGURE 2-12:** Input Noise Voltage Density vs. Frequency.



**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$ , and  $C_L = 60\text{ pF}$ .



**FIGURE 2-13:** Output Short Circuit Current vs. Power Supply Voltage.



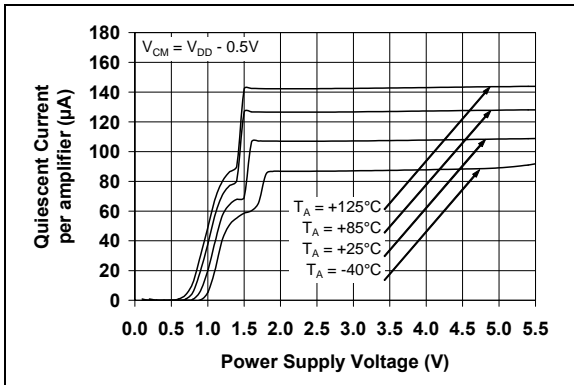
**FIGURE 2-16:** Small-Signal, Non-Inverting Pulse Response.



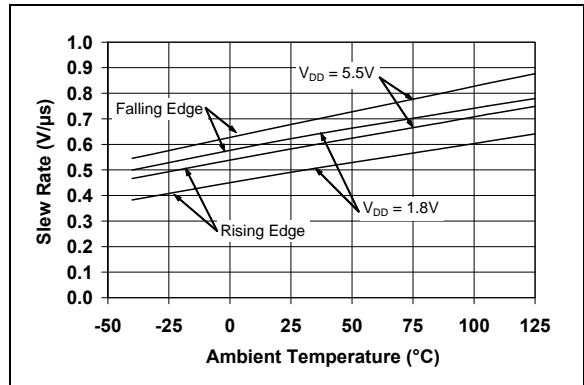
**FIGURE 2-14:** Output Voltage Headroom vs. Output Current Magnitude.



**FIGURE 2-17:** Large-Signal, Non-Inverting Pulse Response.



**FIGURE 2-15:** Quiescent Current vs. Power Supply Voltage.



**FIGURE 2-18:** Slew Rate vs. Ambient Temperature.

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**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$ , and  $C_L = 60\text{ pF}$ .



**FIGURE 2-19:** Output Voltage Swing vs. Frequency.



**FIGURE 2-21:** The MCP6001/2/4 Show No Phase Reversal.



**FIGURE 2-20:** Measured Input Current vs. Input Voltage (below  $V_{SS}$ ).

## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

MCP6001	MCP6001R	MCP6001U	MCP6002		MCP6004	Symbol	Description
SC70-5, SOT-23-5	SOT-23-5	SOT-23-5	MSOP, PDIP, SOIC	DFN 2x3	PDIP, SOIC, TSSOP		
1	1	4	1	1	1	$V_{OUT}, V_{OUTA}$	Analog Output (op amp A)
4	4	3	2	2	2	$V_{IN-}, V_{INA-}$	Inverting Input (op amp A)
3	3	1	3	3	3	$V_{IN+}, V_{INA+}$	Non-inverting Input (op amp A)
5	2	5	8	8	4	$V_{DD}$	Positive Power Supply
—	—	—	5	5	5	$V_{INB+}$	Non-inverting Input (op amp B)
—	—	—	6	6	6	$V_{INB-}$	Inverting Input (op amp B)
—	—	—	7	7	7	$V_{OUTB}$	Analog Output (op amp B)
—	—	—	—	—	8	$V_{OUTC}$	Analog Output (op amp C)
—	—	—	—	—	9	$V_{INC-}$	Inverting Input (op amp C)
—	—	—	—	—	10	$V_{INC+}$	Non-inverting Input (op amp C)
2	5	2	4	4	11	$V_{SS}$	Negative Power Supply
—	—	—	—	—	12	$V_{IND+}$	Non-inverting Input (op amp D)
—	—	—	—	—	13	$V_{IND-}$	Inverting Input (op amp D)
—	—	—	—	—	14	$V_{OUTD}$	Analog Output (op amp D)
—	—	—	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to VSS.

### 3.1 Analog Outputs

The output pins are low-impedance voltage sources.

### 3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

### 3.3 Power Supply Pins

The positive power supply ( $V_{DD}$ ) is 1.8V to 6.0V higher than the negative power supply ( $V_{SS}$ ). For normal operation, the other pins are at voltages between  $V_{SS}$  and  $V_{DD}$ .

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need bypass capacitors.

### 3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the  $V_{SS}$  pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

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NOTES:

## 4.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. This device has high phase margin, which makes it stable for larger capacitive load applications.

### 4.1 Rail-to-Rail Inputs

#### 4.1.1 PHASE REVERSAL

The MCP6001/1R/1U/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-21 shows the input voltage exceeding the supply voltage without any phase reversal.

#### 4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current ( $I_B$ ). The input ESD diodes clamp the inputs when they try to go more than one diode drop below  $V_{SS}$ . They also clamp any voltages that go too far above  $V_{DD}$ ; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.



**FIGURE 4-1:** Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the  $V_{IN+}$  and  $V_{IN-}$  pins (see **Absolute Maximum Ratings** † at the beginning of **Section 1.0 “Electrical Characteristics”**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) from going too far below ground, and the resistors  $R_1$  and  $R_2$  limit the possible current drawn out of the input pins. Diodes  $D_1$  and  $D_2$  prevent the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) from going too far above

$V_{DD}$ , and dump any currents onto  $V_{DD}$ . When implemented as shown, resistors  $R_1$  and  $R_2$  also limit the current through  $D_1$  and  $D_2$ .



**FIGURE 4-2:** Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of resistors  $R_1$  and  $R_2$ . In this case, current through the diodes  $D_1$  and  $D_2$  needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage ( $V_{CM}$ ) is below ground ( $V_{SS}$ ); see Figure 2-20. Applications that are high impedance may need to limit the usable voltage range.

#### 4.1.3 NORMAL OPERATION

The input stage of the MCP6001/1R/1U/2/4 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage ( $V_{CM}$ ), while the other operates at high  $V_{CM}$ . With this topology, the device operates with  $V_{CM}$  up to 0.3V above  $V_{DD}$  and 0.3V below  $V_{SS}$ .

The transition between the two input stages occurs when  $V_{CM} = V_{DD} - 1.1V$ . For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

## 4.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amps is  $V_{DD} - 25 \text{ mV}$  (minimum) and  $V_{SS} + 25 \text{ mV}$  (maximum) when  $R_L = 10 \text{ k}\Omega$  is connected to  $V_{DD}/2$  and  $V_{DD} = 5.5V$ . Refer to Figure 2-14 for more information.

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## 4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer ( $G = +1$ ) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g.,  $> 100$  pF when  $G = +1$ ), a small series resistor at the output ( $R_{ISO}$  in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.



**FIGURE 4-3:** Output resistor,  $R_{ISO}$  stabilizes large capacitive loads.

Figure 4-4 gives recommended  $R_{ISO}$  values for different capacitive loads and gains. The x-axis is the normalized load capacitance ( $C_L/G_N$ ), where  $G_N$  is the circuit's noise gain. For non-inverting gains,  $G_N$  and the Signal Gain are equal. For inverting gains,  $G_N$  is  $1+|\text{Signal Gain}|$  (e.g.,  $-1$  V/V gives  $G_N = +2$  V/V).



**FIGURE 4-4:** Recommended  $R_{ISO}$  values for Capacitive Loads.

After selecting  $R_{ISO}$  for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify  $R_{ISO}$ 's value until the response is reasonable. Bench evaluation and simulations with the MCP6001/1R/1U/2/4 SPICE macro model are very helpful.

## 4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin ( $V_{DD}$  for single-supply) should have a local bypass capacitor (i.e.,  $0.01 \mu\text{F}$  to  $0.1 \mu\text{F}$ ) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e.,  $1 \mu\text{F}$  or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

## 4.5 Unused Op Amps

An unused op amp in a quad package (MCP6004) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



**FIGURE 4-5:** Unused Op Amps.

## 4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12} \Omega$ . A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6001/1R/1U/2/4 family's bias current at  $25^\circ\text{C}$  (typically 1 pA).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.



**FIGURE 4-6:** Example Guard Ring Layout for Inverting Gain.

1. Non-inverting Gain and Unity-Gain Buffer:
  - a. Connect the non-inverting pin ( $V_{IN+}$ ) to the input with a wire that does not touch the PCB surface.
  - b. Connect the guard ring to the inverting input pin ( $V_{IN-}$ ). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
  - a. Connect the guard ring to the non-inverting input pin ( $V_{IN+}$ ). This biases the guard ring to the same reference voltage as the op amp (e.g.,  $V_{DD}/2$  or ground).
  - b. Connect the inverting pin ( $V_{IN-}$ ) to the input with a wire that does not touch the PCB surface.

## 4.7 Application Circuits

### 4.7.1 UNITY-GAIN BUFFER

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity-gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 4-7.



**FIGURE 4-7:** Instrumentation Amplifier with Unity-Gain Buffer Inputs.

### 4.7.2 ACTIVE LOW-PASS FILTER

The MCP6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100x the filter cutoff frequency (or higher) for good performance. It is possible to have the op amp bandwidth 10X higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 4-8 shows a second-order Butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10x higher than the cutoff frequency. The component values were selected using Microchip's FilterLab<sup>®</sup> software.



**FIGURE 4-8:** Active Second-Order Low-Pass Filter.

# MCP6001/1R/1U/2/4

## 4.7.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applications. Figure 4-9 shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in Figure 4-9.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on  $C_1$  is sampled to  $C_2$  for a sample time defined by  $t_{SAMP}$ . At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes,  $C_1$  discharges through  $R_1$  for a time defined by  $t_{CLEAR}$ . At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of  $V_{IN}$  on  $C_1$  for a time defined by  $t_{DETECT}$ .

In order to define  $t_{SAMP}$  and  $t_{CLEAR}$ , it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time ( $\tau$ ) is defined using  $R_1$  ( $\tau = R_1 C_1$ ).  $t_{DETECT}$  is the time that the input signal is sampled on  $C_1$  and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both  $C_1$  and  $C_2$ ), could create slewing limitations as the input voltage ( $V_{IN}$ ) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with an op amp short circuit current of  $I_{SC} = 25 \text{ mA}$  and a load capacitor of  $C_1 = 0.1 \mu\text{F}$ , then:

### EQUATION 4-1:

$$I_{SC} = C_1 \frac{dV_{C1}}{dt}$$

$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$

$$= \frac{25 \text{ mA}}{0.1 \mu\text{F}}$$

$$\frac{dV_{C1}}{dt} = 250 \text{ mV}/\mu\text{s}$$

This voltage rate of change is less than the MCP6001/2/4 slew rate of  $0.6 \text{ V}/\mu\text{s}$ . When the input voltage swings below the voltage across  $C_1$ ,  $D_1$  becomes reverse-biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a  $0.1 \mu\text{F}$  capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than  $40 \mu\text{F}$  and a stabilizing resistor ( $R_{ISO}$ ) needs to be properly selected. (Refer to Section 4.3 "Capacitive Loads").



FIGURE 4-9: Peak Detector with Clear and Sample CMOS Analog Switches.



## 5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6001/1R/1U/2/4 family of op amps.

### 5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6001/1R/1U/2/4 op amps is available on the Microchip web site at [www.microchip.com](http://www.microchip.com). The model was written and tested in official Orcad (Cadence) owned PSPICE. For the other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions can not be guaranteed that it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

### 5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at [www.microchip.com/filterlab](http://www.microchip.com/filterlab), the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

### 5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at [www.microchip.com/mindi](http://www.microchip.com/mindi). This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

### 5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at [www.microchip.com/maps](http://www.microchip.com/maps), the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

### 5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at [www.microchip.com/analogtools](http://www.microchip.com/analogtools).

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

## 5.6 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at [www.microchip.com/appnotes](http://www.microchip.com/appnotes) and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications"*, DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications"*, DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps"*, DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors"*, DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise"*, DS01228
- **AN1297:** *"Microchip 's Op Amp SPICE Macro Models"*

These application notes and others are listed in the design guide:

- *"Signal Chain Design Guide"*, DS21825

## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

5-Lead SC-70 (MCP6001)



Device	I-Temp Code	E-Temp Code
MCP6001	AAN	CDN

Note: Applies to 5-Lead SC-70.

Example: (I-Temp)



OR



Device	I-Temp Code	E-Temp Code
MCP6001	AANN	CDNN

Note: Applies to 5-Lead SC-70.

OR



5-Lead SOT-23 (MCP6001/1R/1U)



Device	I-Temp Code	E-Temp Code
MCP6001	AANN	CDNN
MCP6001R	ADNN	CENN
MCP6001U	AFNN	CFNN

Note: Applies to 5-Lead SOT-23.

Example: (E-Temp)



8-Lead PDIP (300 mil)



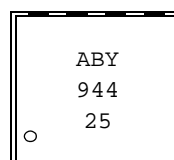
Example:



8-Lead DFN (2 x 3)



Example:



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# MCP6001/1R/1U/2/4

## Package Marking Information (Continued)

8-Lead SOIC (150 mil)



Example:



8-Lead MSOP



Example:



14-Lead PDIP (300 mil) (MCP6004)



Example:



OR



14-Lead SOIC (150 mil) (MCP6004)



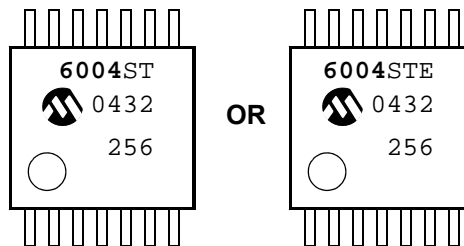
Example:



14-Lead TSSOP (MCP6004)



Example:



## 5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

**Notes:**

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

# MCP6001/1R/1U/2/4

## 5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	$\phi$	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

**Notes:**

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

# MCP6001/1R/1U/2/4

## 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C



## 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123A

# MCP6001/1R/1U/2/4

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

**Notes:**

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	$\alpha$	5°	–	15°
Mold Draft Angle Bottom	$\beta$	5°	–	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

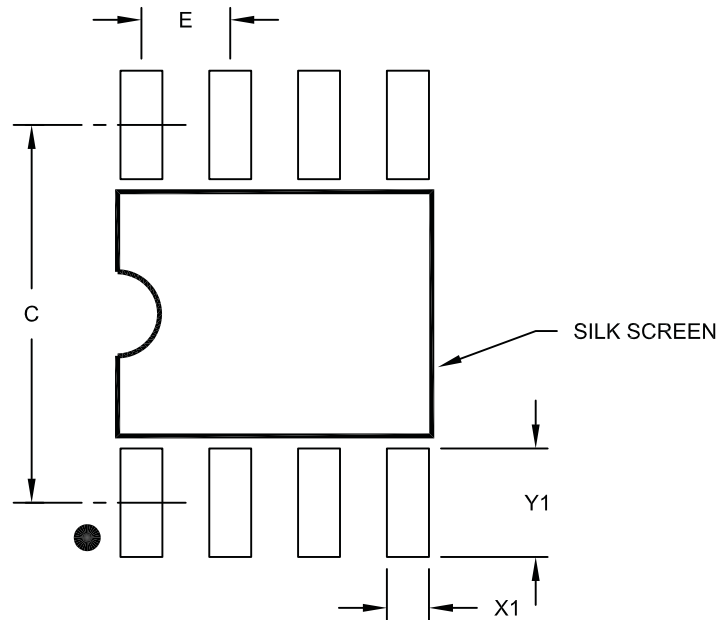
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

# MCP6001/1R/1U/2/4

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		0.65 BSC		
Overall Height	A	-	-	-	1.10
Molded Package Thickness	A2		0.75	0.85	0.95
Standoff	A1		0.00	-	0.15
Overall Width	E		4.90 BSC		
Molded Package Width	E1		3.00 BSC		
Overall Length	D		3.00 BSC		
Foot Length	L		0.40	0.60	0.80
Footprint	L1		0.95 REF		
Foot Angle	$\phi$		0°	-	8°
Lead Thickness	c		0.08	-	0.23
Lead Width	b		0.22	-	0.40

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

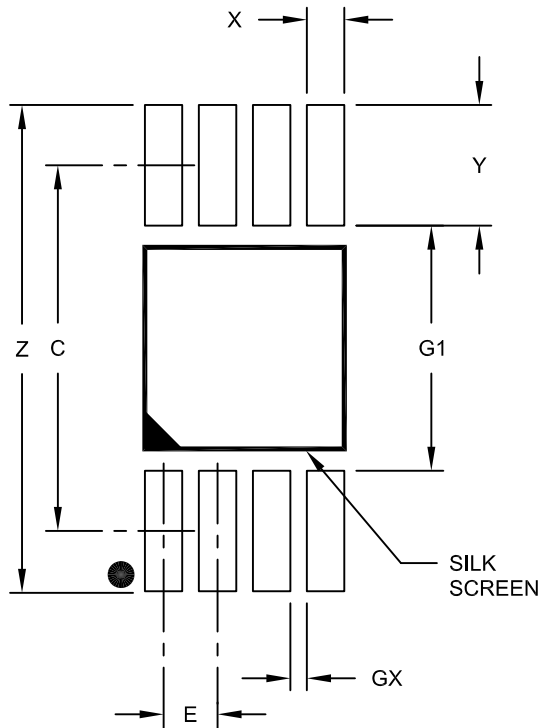
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

# MCP6001/1R/1U/2/4

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C	4.40		
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

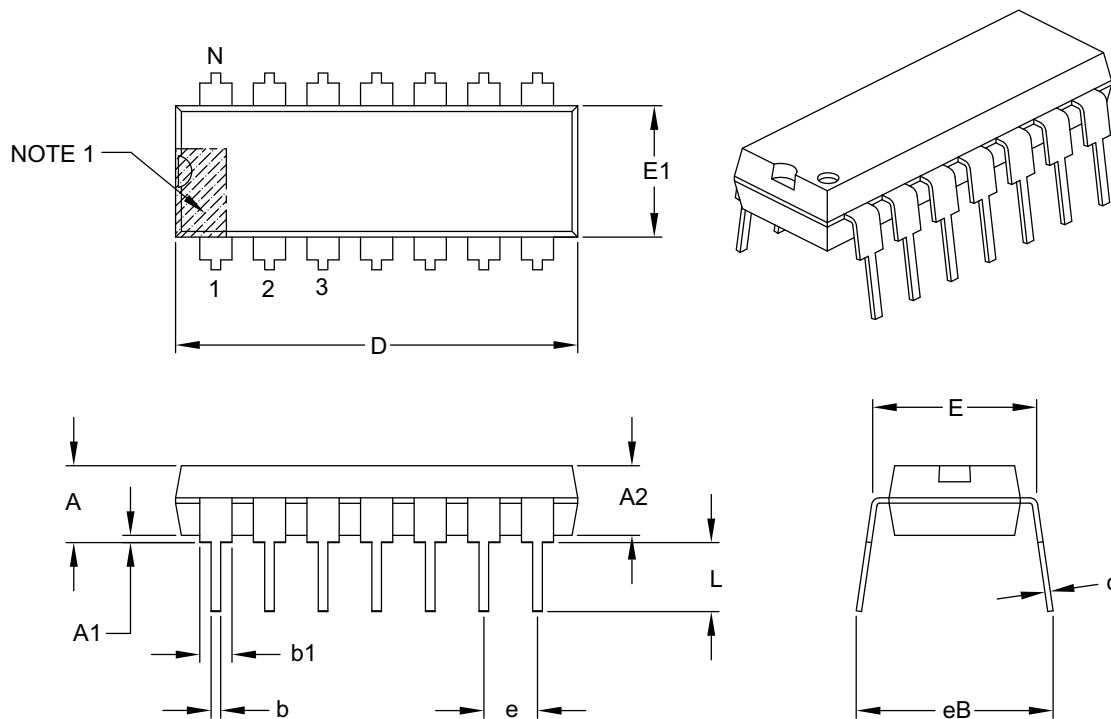
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

# MCP6001/1R/1U/2/4

## 14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

**Notes:**

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

# MCP6001/1R/1U/2/4

## 14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	$\alpha$	5°	–	15°
Mold Draft Angle Bottom	$\beta$	5°	–	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B



# MCP6001/1R/1U/2/4

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

# MCP6001/1R/1U/2/4

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

## 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.45
Distance Between Pads	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

# MCP6001/1R/1U/2/4

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision J (November 2009)

The following is the list of modifications:

1. Added new 2x3 DFN 8-Lead package on page 1.
2. Updated the Temperature Specifications table with 2x3 DFN thermal resistance information.
3. Updated **Section 1.1 “Test Circuits”**.
4. Updated [Figure 2-15](#).
5. Added the 2x3 DFN column to [Table 3-1](#).
6. Added new **Section 3.4 “Exposed Thermal Pad (EP)”**.
7. Updated **Section 5.1 “SPICE Macro Model”**.
8. Updated **Section 5.5 “Analog Demonstration and Evaluation Boards”**.
9. Updated **Section 5.6 “Application Notes”**.
10. Updated **Section 6.1 “Package Marking Information”** with the new 2x3 DFN package marking information.
11. Updated the package drawings.
12. Updated the Product Identification System section with new 2x3 DFN package information.

### Revision H (May 2008)

The following is the list of modifications:

1. **Design Aids:** Name change for Mindi Simulation Tool.
2. **Package Types:** Correct device labeling error.
3. **Section 1.0 “Electrical Characteristics”, DC Electrical Specifications:** Changed “Maximum Output Voltage Swing” condition from 0.9V Input Overdrive to 0.5V Input Overdrive.
4. **Section 1.0 “Electrical Characteristics”, AC Electrical Specifications:** Changed Phase Margin condition from  $G = +1$  to  $G = +1$  V/V.
5. **Section 5.0 “Design AIDS”:** Name change for Mindi Simulation Tool.

### Revision G (November 2007)

The following is the list of modifications:

1. Updated notes to **Section 1.0 “Electrical Characteristics”**.
2. Increased Absolute Maximum Voltage range at input pins.
3. Increased maximum operating supply voltage ( $V_{DD}$ ).
4. Added test circuits.
5. Added [Figure 2-3](#) and [Figure 2-20](#).
6. Added **Section 4.1.1 “Phase Reversal”, Section 4.1.2 “Input Voltage and Current Limits”, Section 4.1.3 “Normal Operation” and Section 4.5 “Unused Op Amps”**.
7. Updated **Section 5.0 “Design AIDS”**,
8. Updated **Section 6.0 “Packaging Information”**
9. Updated Package Outline Drawings.

### Revision F (March 2005)

The following is the list of modifications:

1. Updated **Section 6.0 “Packaging Information”** to include old and new packaging examples.

### Revision E (December 2004)

The following is the list of modifications:

1.  $V_{OS}$  specification reduced to  $\pm 4.5$  mV from  $\pm 7.0$  mV for parts starting with date code YYWW = 0449
2. Corrected package markings in **Section 6.0 “Packaging Information”**.
3. Added Appendix A: Revision History.

### Revision D (May 2003)

- Undocumented changes.

### Revision C (December 2002)

- Undocumented changes.

### Revision B (October 2002)

- Undocumented changes.

### Revision A (June 2002)

- Original data sheet release.

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>XX</u>	
Device	Temperature Range	Package	
Device:	MCP6001T:	Single Op Amp (Tape and Reel) (SC-70, SOT-23)	
	MCP6001RT:	Single Op Amp (Tape and Reel) (SOT-23)	
	MCP6001UT:	Single Op Amp (Tape and Reel) (SOT-23)	
	MCP6002:	Dual Op Amp	
	MCP6002T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)	
	MCP6004:	Quad Op Amp	
	MCP6004T:	Quad Op Amp (Tape and Reel) (SOIC, MSOP)	
Temperature Range:	I = -40°C to +85°C		
	E = -40°C to +125°C		
Package:	LT = Plastic Package (SC-70), 5-lead (MCP6001 only)		
	OT = Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6001, MCP6001R, MCP6001U)		
	MS = Plastic MSOP, 8-lead		
	MC = Plastic DFN, 8-lead		
	P = Plastic DIP (300 mil body), 8-lead, 14-lead		
	SN = Plastic SOIC, (3.99 mm body), 8-lead		
	SL = Plastic SOIC (3.99 mm body), 14-lead		
	ST = Plastic TSSOP (4.4mm body), 14-lead		
			<b>Examples:</b>
			a) MCP6001T-I/LT: Tape and Reel, Industrial Temperature, 5LD SC-70 package
			b) MCP6001T-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
			c) MCP6001RT-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
			d) MCP6001UT-E/OT: Tape and Reel, Extended Temperature, 5LD SOT-23 package.
			a) MCP6002-I/MS: Industrial Temperature, 8LD MSOP package.
			b) MCP6002-I/P: Industrial Temperature, 8LD PDIP package.
			c) MCP6002-E/P: Extended Temperature, 8LD PDIP package.
			d) MCP6002-E/MC: Extended Temperature, 8LD DFN package.
			e) MCP6002-I/SN: Industrial Temperature, 8LD SOIC package.
			f) MCP6002T-I/MS: Tape and Reel, Industrial Temperature, 8LD MSOP package.
			g) MCP6002T-E/MC: Tape and Reel, Extended Temperature, 8LD DFN package.
			a) MCP6004-I/P: Industrial Temperature, 14LD PDIP package.
			b) MCP6004-I/SL: Industrial Temperature, 14LD SOIC package.
			c) MCP6004-E/SL: Extended Temperature, 14LD SOIC package.
			d) MCP6004-I/ST: Industrial Temperature, 14LD TSSOP package.
			e) MCP6004T-I/SL: Tape and Reel, Industrial Temperature, 14LD SOIC package.
			f) MCP6004T-I/ST: Tape and Reel, Industrial Temperature, 14LD TSSOP package.

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NOTES:



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