# bq2204A

# X4 SRAM Nonvolatile Controller Unit

## Features

- Power monitoring and switching for 3-volt battery-backup applications
- Write-protect control
- 2-input decoder for control of up to 4 banks of SRAM
- 3-volt primary cell inputs
- Less than 10ns chip-enable propagation delay
- 5% or 10% supply operation

## General Description

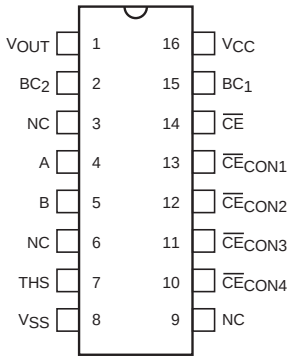
The CMOS bq2204A SRAM Nonvolatile Controller Unit provides all necessary functions for converting up to four banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V $V_{CC}$ input for an out-of-tolerance condition. When out-of-tolerance is detected, the four conditioned chip-enable outputs are forced inactive to write-protect up to four banks of SRAM.

During a power failure, the external SRAMs are switched from the $V_{CC}$ supply to one of two 3V backup supplies. On a subsequent power-up, the SRAMs are write-protected until a power-valid condition exists.

During power-valid operation, a two-input decoder transparently selects one of up to four banks of SRAM.

## Pin Connections




16-Pin Narrow DIP or SOIC

PN220401.eps

## Pin Names

| | |
|---|---|
| $V_{OUT}$ | Supply output |
| $BC_1$–$BC_2$ | 3 volt primary backup cell inputs |
| THS | Threshold select input |
| $\overline{CE}$ | chip-enable active low input |
| $\overline{CE}_{CON1}$–$\overline{CE}_{CON4}$ | Conditioned chip-enable outputs |
| A–B | Decoder inputs |
| NC | No connect |
| $V_{CC}$ | +5 volt supply input |
| $V_{SS}$ | Ground |

## Functional Description

Up to four banks of CMOS static RAM can be battery-backed using the $V_{OUT}$ and conditioned chip-enable output pins from the bq2204A. As $V_{CC}$ slews down during a power failure, the conditioned chip-enable outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are forced inactive independent of the chip-enable input $\overline{CE}$.

This activity unconditionally write-protects the external SRAM as $V_{CC}$ falls below an out-of-tolerance threshold $V_{PFD}$. $V_{PFD}$ is selected by the threshold select input pin, THS. If THS is tied to $V_{SS}$, the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to $V_{CC}$, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to $V_{SS}$ or $V_{CC}$ for proper operation.

If a memory access is in process to any of the four external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time $t_{WPT}$, all four chip-enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

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As the supply continues to fall past $V_{PFD}$, an internal switching device forces $V_{OUT}$ to one of the two external backup energy sources. $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held high by the $V_{OUT}$ energy source.

During power-up, $V_{OUT}$ is switched back to the 5V supply as $V_{CC}$ rises above the backup cell input voltage sourcing $V_{OUT}$. Outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held inactive for time $t_{CER}$ (120ms maximum) after the power supply has reached $V_{PFD}$, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the four $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10ns. The $\overline{CE}$ input is output on one of the four $\overline{CE}_{CON}$ output pins depending on the level of the decode inputs at A and B as shown in the Truth Table.

The A and B inputs are usually tied to high-order address pins so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

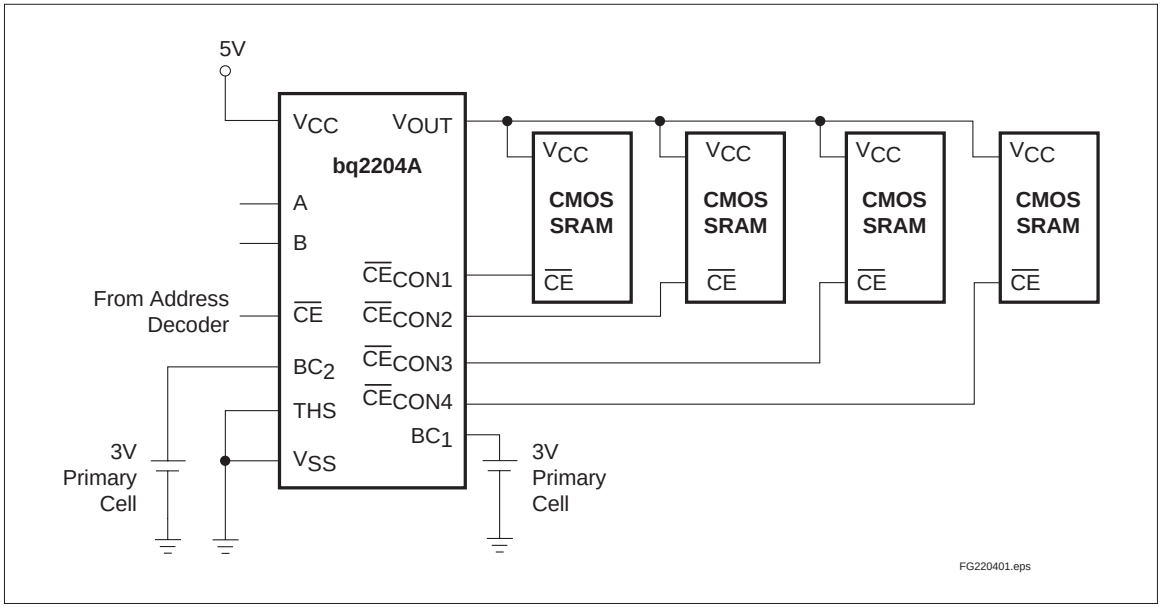



**Figure 1. Hardware Hookup (5% Supply Operation)**

## Energy Cell Inputs—$BC_1$, $BC_2$

Two backup energy source inputs are provided on the bq2204A. The $BC_1$ and $BC_2$ inputs accept a 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If no primary cell is to be used on either $BC_1$ or $BC_2$, the unused input should be tied to $V_{SS}$.

$V_{CC}$ falling below $V_{PFD}$ starts the comparison of $BC_1$ and $BC_2$. The BC input comparison continues until $V_{CC}$ rises above $V_{SO}$. Power to $V_{OUT}$ begins with $BC_1$ and switches to $BC_2$ only when $V_{BC1}$ is less than $V_{BC2}$ minus $V_{BSO}$. The controller alternates to the higher BC voltage only when the difference between the BC input voltages is greater than $V_{BSO}$. Alternating the backup batteries allows one-at-a-time battery replacement and efficient use of both backup batteries.

To prevent battery drain when there is no valid data to retain, $V_{OUT}$ and $\overline{CE}_{CON1-4}$ are internally isolated from $BC_1$ and $BC_2$ by either of the following conditions:

- Initial connection of a battery to $BC_1$ or $BC_2$, or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as $V_{CC}$ crosses both $V_{PFD}$ and $V_{SO}$ during a power-down. See Figure 2. Between these two points in time, $\overline{CE}$ must be brought to the point of (0.48 to 0.52)*$V_{CC}$ and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*$V_{CC}$ at any point between $V_{CC}$ crossing $V_{PFD}$ and $V_{SO}$.

The appropriate battery is connected to $V_{OUT}$ and $\overline{CE}_{CON1–4}$ immediately on subsequent application and removal of $V_{CC}$.

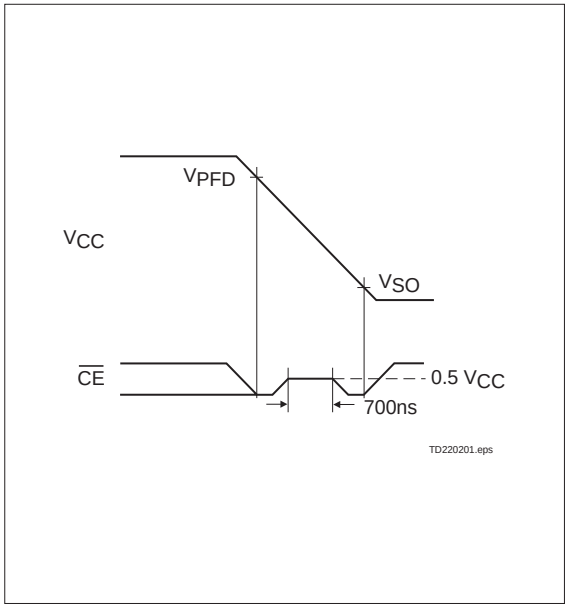



**Figure 2. Battery Isolation Signal**

## Truth Table

| Input | | | Output | | | |
|---|---|---|---|---|---|---|
| $\overline{CE}$ | A | B | $\overline{CE}_{CON1}$ | $\overline{CE}_{CON2}$ | $\overline{CE}_{CON3}$ | $\overline{CE}_{CON4}$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | H | L | H | L | H | H |
| L | L | H | H | H | L | H |
| L | H | H | H | H | H | L |

## Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit | Conditions |
|---|---|---|---|---|
| $V_{CC}$ | DC voltage applied on $V_{CC}$ relative to $V_{SS}$ | -0.3 to +7.0 | V | |
| $V_T$ | DC voltage applied on any pin excluding $V_{CC}$ relative to $V_{SS}$ | -0.3 to +7.0 | V | $V_T \le V_{CC} + 0.3$ |
| $T_{OPR}$ | Operating temperature | 0 to 70 | °C | Commercial |
| | | -40 to +85 | °C | Industrial "N" |
| $T_{STG}$ | Storage temperature | -55 to +125 | °C | |
| $T_{BIAS}$ | Temperature under bias | -40 to +85 | °C | |
| $T_{SOLDER}$ | Soldering temperature | 260 | °C | For 10 seconds |
| $I_{OUT}$ | $V_{OUT}$ current | 200 | mA | |

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## Recommended DC Operating Conditions ($T_A = T_{OPR}$)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.5 | V | THS = $V_{SS}$ |
| | | 4.50 | 5.0 | 5.5 | V | THS = $V_{CC}$ |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V | |
| $V_{IL}$ | Input low voltage | -0.3 | - | 0.8 | V | |
| $V_{IH}$ | Input high voltage | 2.2 | - | $V_{CC}$ + 0.3 | V | |
| $V_{BC1}$, $V_{BC2}$ | Backup cell voltage | 2.0 | - | 4.0 | V | $V_{CC} < V_{BC}$ |
| THS | Threshold select | -0.3 | - | $V_{CC}$ + 0.3 | V | |

**Note:** Typical values indicate operation at $T_A$ = 25°C, $V_{CC}$ = 5V or $V_{BC}$.

## DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CC}$ = 5V ± 10%)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Conditions/Notes |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current | - | - | ± 1 | µA | $V_{IN} = V_{SS}$ to $V_{CC}$ |
| $V_{OH}$ | Output high voltage | 2.4 | - | - | V | $I_{OH}$ = -2.0mA |
| $V_{OHB}$ | $V_{OH}$, BC supply | $V_{BC}$ - 0.3 | - | - | V | $V_{BC} > V_{CC}$, $I_{OH}$ = -10µA |
| $V_{OL}$ | Output low voltage | - | - | 0.4 | V | $I_{OL}$ = 4.0mA |
| $I_{CC}$ | Operating supply current | - | 3 | 6 | mA | No load on outputs. |
| $V_{PFD}$ | Power-fail detect voltage | 4.55 | 4.62 | 4.75 | V | THS = $V_{SS}$ |
| | | 4.30 | 4.37 | 4.50 | V | THS = $V_{CC}$ |
| $V_{SO}$ | Supply switch-over voltage | - | $V_{BC}$ | - | V | |
| $I_{CCDR}$ | Data-retention mode current | - | - | 100 | nA | $V_{OUT}$ data-retention current to additional memory not included. |
| $V_{BC}$ | Active backup cell voltage | - | $V_{BC1}$ | - | V | $V_{BC1} > V_{BC2} + V_{BSO}$ |
| | | - | $V_{BC2}$ | - | V | $V_{BC2} > V_{BC1} + V_{BSO}$ |
| $V_{BSO}$ | Battery switch-over voltage | 0.25 | 0.4 | 0.6 | V | |
| $I_{OUT1}$ | $V_{OUT}$ current | - | - | 160 | mA | $V_{OUT} > V_{CC}$ - 0.3V |
| $I_{OUT2}$ | $V_{OUT}$ current | - | 100 | - | µA | $V_{OUT} > V_{BC}$ - 0.2V |

**Note:** Typical values indicate operation at $T_A$ = 25°C, $V_{CC}$ = 5V or $V_{BC}$.

## Capacitance ($T_A$ = 25°C, F = 1MHz, $V_{CC}$ = 5.0V)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Conditions |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | - | - | 8 | pF | Input voltage = 0V |
| $C_{OUT}$ | Output capacitance | - | - | 10 | pF | Output voltage = 0V |

**Note:** This parameter is sampled and not 100% tested.

## AC Test Conditions

| Parameter | Test Conditions |
|---|---|
| Input pulse levels | 0V to 3.0V |
| Input rise and fall times | 5ns |
| Input and output timing reference levels | 1.5V (unless otherwise specified) |

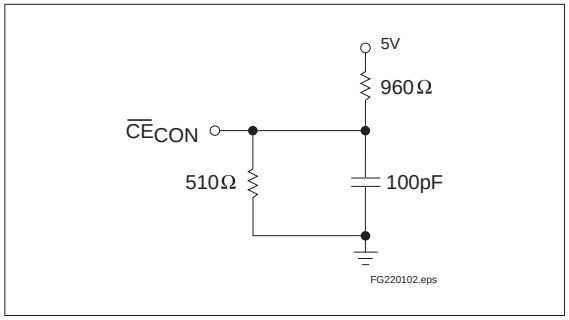



**Figure 3. Output Load**

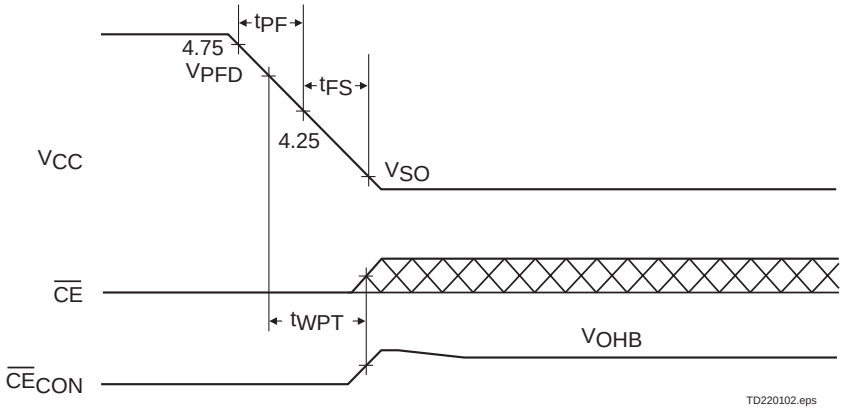
## Power-Fail Control ($T_A = T_{OPR}$)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{PF}$ | $V_{CC}$ slew, 4.75V to 4.25V | 300 | - | - | µs | |
| $t_{FS}$ | $V_{CC}$ slew, 4.25V to $V_{SO}$ | 10 | - | - | µs | |
| $t_{PU}$ | $V_{CC}$ slew, 4.25V to 4.75V | 0 | - | - | µs | |
| $t_{CED}$ | chip-enable propagation delay | - | 7 | 10 | ns | |
| $t_{AS}$ | A,B set up to $\overline{CE}$ | 0 | - | - | ns | |
| $t_{CER}$ | chip-enable recovery | 40 | 80 | 120 | ms | Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up. |
| $t_{WPT}$ | Write-protect time | 40 | 100 | 150 | µs | Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is write-protected. |

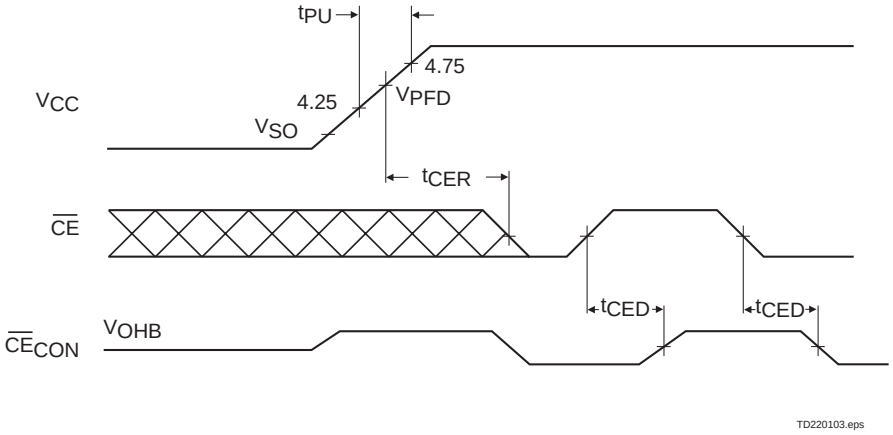
**Note:** Typical values indicate operation at $T_A$ = 25°C, $V_{CC}$ = 5V.

**Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

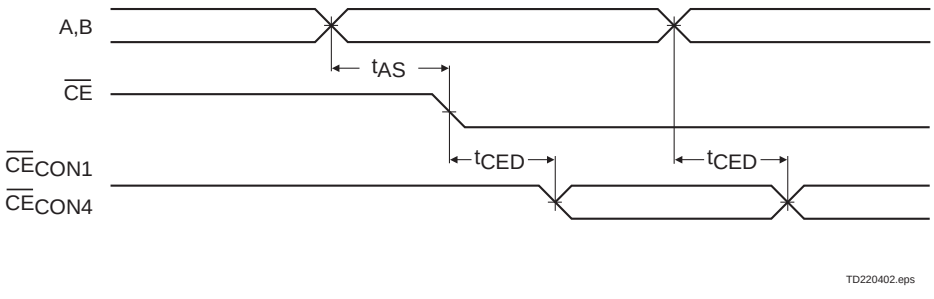
## Power-Down Timing




## Power-Up Timing




## Address-Decode Timing




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## Data Sheet Revision History

| Change No. | Page No. | Description of Change | Nature of Change |
|---|---|---|---|
| 1 | All | bq2204A replaces bq2204. | |
| 1 | 1, 4–5 | 10% tolerance requires the THS pin to be tied to $V_{CC}$, not $V_{OUT}$. | |
| 1 | 3 | Energy cell input selection process alternates between $BC_1$ and $BC_2$. | |

**Note:** Change 1 = Dec. 1992 changes from Sept. 1991

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| BQ2204APN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| BQ2204ASN | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| BQ2204ASN-N | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| BQ2204ASN-NG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| BQ2204ASNG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| BQ2204ASNTR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| BQ2204ASNTRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

(1) The marketing status values are defined as follows:
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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

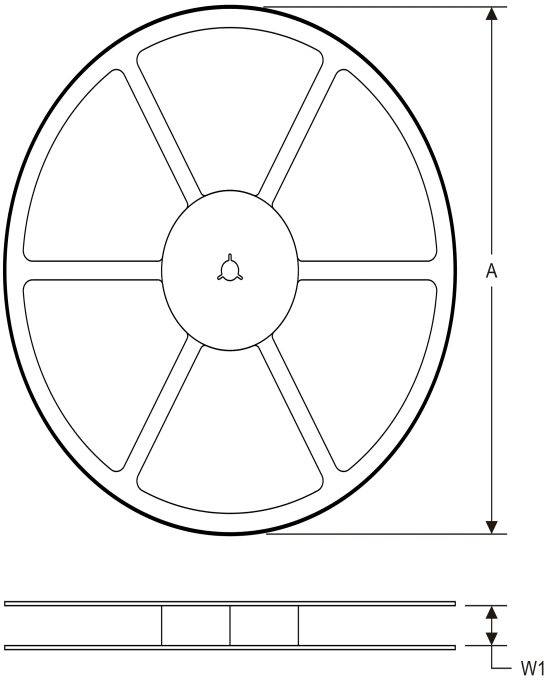
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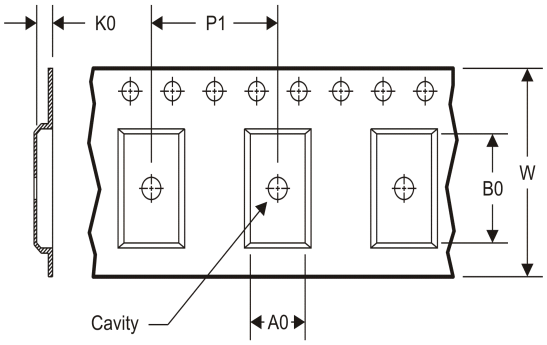
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**REEL DIMENSIONS**




**TAPE DIMENSIONS**



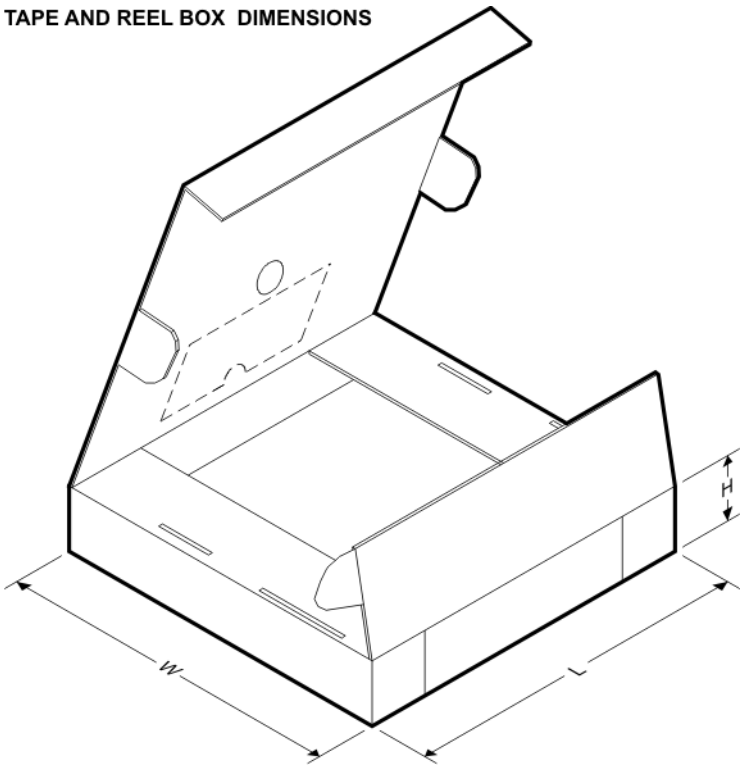

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ2204ASNTR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ2204ASNTR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |

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| RFID | www.ti-rfid.com | | |
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