

NB7V585M

1.8V / 2.5V Differential 2:1 Mux Input to 1:6 CML Clock/Data Fanout Buffer/Translator Multi-Level Inputs w/ Internal Termination

Description

The NB7V585M is a differential 1-to-6 CML clock/data distribution chip featuring a 2:1 Clock/Data input multiplexer with an input select pin. The IN_x/\overline{IN}_x inputs incorporate internal $50\ \Omega$ termination resistors and will accept LVPECL, CML, or LVDS logic levels (see Figure 9). The NB7V585M produces six identical output copies of clock or data operating up to 6 GHz or 10 Gb/s, respectively. As such, NB7V585M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications. The 16 mA differential CML output structure provides matching internal $50\ \Omega$ source terminations, 400 mV output swings when externally terminated with a $50\ \Omega$ resistor to V_{CC} (see Figure 14) and is optimized for low skew and minimal jitter. The NB7V585M is powered with either 1.8 V or 2.5 V supply and is offered in a low profile 5x5 mm 32-pin QFN package.

Application notes, models, and support documentation are available at www.onsemi.com.

The NB7V585M is a member of the GigaComm™ family of high performance clock products.

Features

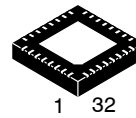
- Maximum Input Data Rate > 10 Gb/s
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 6 GHz
- Random Clock Jitter < 0.8 ps RMS, Max
- Low Skew 1:6 CML Outputs, 20 ps Max
- 2:1 Multi-Level Mux Inputs
- 175 ps Typical Propagation Delay
- 50 ps Typical Rise and Fall Times
- Differential CML Outputs, 330 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 1.71\text{ V to }1.89\text{ V}$
- Internal $50\ \Omega$ Input Termination Resistors
- V_{REFAC} Reference Output
- QFN32 Package, 5 mm x 5 mm
- $-40^\circ\text{C to }+85^\circ\text{C}$ Ambient Operating Temperature
- These are Pb-Free Devices



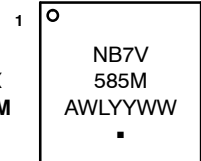
ON Semiconductor®

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MARKING DIAGRAM*



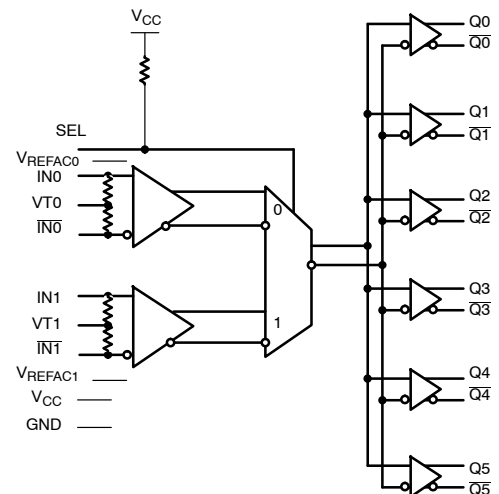
QFN32
MN SUFFIX
CASE 488AM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

SIMPLIFIED LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NB7V585M

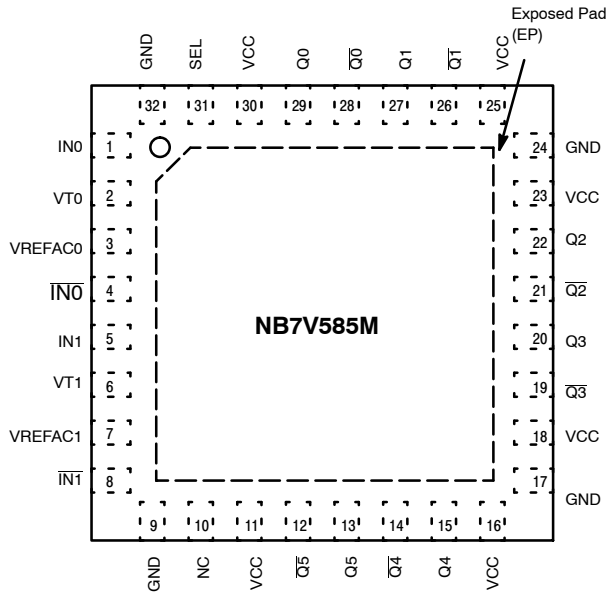


Figure 1. 32-Lead QFN Pinout (Top View)

Table 1. INPUT SELECT FUNCTION TABLE

| SEL* | CLK Input Selected |
|------|--------------------|
| 0 | IN0 |
| 1 | IN1 |

*Defaults HIGH when left open.

Table 2. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|--------------------------|--|----------------------------|---|
| 1,4 5,8 | IN0, $\overline{\text{IN0}}$ IN1, $\overline{\text{IN1}}$ | LVPECL, CML, LVDS Input | Non-inverted, Inverted, Differential Inputs |
| 2,6 | VT0, VT1 | | Internal 100 Ω Center-tapped Termination Pin for IN0/ $\overline{\text{IN0}}$ and IN1/ $\overline{\text{IN1}}$ |
| 31 | SEL | LVTTTL/LVCMOS Input | Input Select pin; LOW for IN0 Inputs, HIGH for IN1 Inputs; defaults HIGH when left open |
| 10 | NC | – | No Connect |
| 11, 16, 18 23, 25, 30 | VCC | – | Positive Supply Voltage. |
| 29, 28 27, 26 | Q0, $\overline{\text{Q0}}$ Q1, $\overline{\text{Q1}}$ | CML Output | Non-inverted, Inverted Differential Outputs (Note 1). |
| 22, 21 20, 19 | Q2, $\overline{\text{Q2}}$ Q3, $\overline{\text{Q3}}$ | CML Output | Non-inverted, Inverted Differential Outputs (Note 1). |
| 15, 14 13, 12 | Q4, $\overline{\text{Q4}}$ Q5, $\overline{\text{Q5}}$ | CML Output | Non-inverted, Inverted Differential Outputs (Note 1). |
| 9, 17, 24, 32 | GND | | Negative Supply Voltage, connected to Ground |
| 3 7 | VREFAC0 VREFAC1 | – | Output Voltage Reference for Capacitor-Coupled Inputs, only |
| – | EP | – | The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board. |

1. In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and if no signal is applied on INn/ $\overline{\text{INn}}$ input, then, the device will be susceptible to self-oscillation. Qn/ $\overline{\text{Qn}}$ outputs have internal 50 Ω source termination resistors.
2. All VCC and GND pins must be externally connected to a power supply for proper operation.

NB7V585M

Table 3. ATTRIBUTES

| Characteristics | | Value |
|--|-----------------------------------|----------------------|
| ESD Protection | Human Body Model Machine Model | > 4 kV > 200 V |
| Input Pullup Resistor (R _{PU}) | | 75 kΩ |
| Moisture Sensitivity (Note 3) | | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 308 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|----------------------|---|---------------------|--|-------------------------------|--------------|
| V _{CC} | Positive Power Supply | GND = 0 V | | 3.0 | V |
| V _{IO} | Input/Output Voltage | GND = 0 V | -0.5 ≤ V _{IO} ≤ V _{CC} + 0.5 | -0.5 to V _{CC} + 0.5 | V |
| V _{INPP} | Differential Input Voltage I _{Nx} - I _{Nx} | | | 1.89 | V |
| I _{IN} | Input Current Through R _T (50 Ω Resistor) | | | ± 40 | mA |
| I _{OUT} | Output Current | Continuous Surge | | 34 40 | mA |
| I _{VFREFAC} | V _{REFAC} Sink/Source Current | | | ± 1.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) (Note 4) | 0 lfpm 500 lfpm | QFN-32 QFN-32 | 31 27 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) (Note 4) | Standard Board | QFN-32 | 12 | °C/W |
| T _{sol} | Wave Solder Pb-Free | | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB7V585M

Table 5. DC CHARACTERISTICS – CML OUTPUT $V_{CC} = 1.8\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C (Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------|----------------|-----|-----|-----|------|
|--------|----------------|-----|-----|-----|------|

POWER SUPPLY CURRENT

| | | | | | |
|----------|--|--|------------|-----|----|
| I_{CC} | Power Supply Current (Inputs and Outputs Open) $V_{CC} = 2.65\text{ V}$ $V_{CC} = 1.89\text{ V}$ | | 235 210 | 260 | mA |
|----------|--|--|------------|-----|----|

CML OUTPUTS (Note 6)

| | | | | | |
|----------|---|--------------------------------|--------------------------------|--------------------------------|----|
| V_{OH} | Output HIGH Voltage $V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$ | $V_{CC} - 40$ 2460 1760 | $V_{CC} - 20$ 2480 1780 | V_{CC} 2500 1800 | mV |
| V_{OL} | Output LOW Voltage $V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$ | $V_{CC} - 500$ 2000 1300 | $V_{CC} - 400$ 2100 1400 | $V_{CC} - 275$ 2200 1500 | mV |

DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED (Note 7) (Figure 6)

| | | | | | |
|-----------|--|----------------|--|----------------|----|
| V_{th} | Input Threshold Reference Voltage Range (Note 8) | 1050 | | $V_{CC} - 100$ | mV |
| V_{IH} | Single-Ended Input HIGH Voltage | $V_{th} + 100$ | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | GND | | $V_{th} - 100$ | mV |
| V_{ISE} | Single-Ended Input Voltage ($V_{IH} - V_{IL}$) | 200 | | 1200 | mV |

V_{REFAC}

| | | | | | |
|-------------|---|----------------|----------------|----------------|----|
| V_{REFAC} | Output Reference Voltage @ 100 μA for Capacitor – Coupled Inputs, Only | $V_{CC} - 625$ | $V_{CC} - 500$ | $V_{CC} - 400$ | mV |
|-------------|---|----------------|----------------|----------------|----|

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Note 9) (Figures 4 and 7)

| | | | | | |
|-----------|--|------|--|----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage (I_N, \bar{I}_N) | 1100 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage (I_N, \bar{I}_N) | GND | | $V_{CC} - 100$ | mV |
| V_{ID} | Differential Input Voltage (I_N, \bar{I}_N) ($V_{IHD} - V_{ILD}$) | 100 | | 1200 | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration, Note 10) (Figure 9) | 1050 | | $V_{CC} - 50$ | mV |
| I_{IH} | Input HIGH Current I_N/\bar{I}_N (V_{TO} / V_{T1} Open) | -150 | | 150 | μA |
| I_{IL} | Input LOW Current I_N/\bar{I}_N (V_{TO} / V_{T1} Open) | -150 | | 150 | μA |

CONTROL INPUT (SEL Pin)

| | | | | | |
|----------|------------------------------------|----------------------|----|----------------------|---------------|
| V_{IH} | Input HIGH Voltage for Control Pin | $V_{CC} \times 0.65$ | | V_{CC} | mV |
| V_{IL} | Input LOW Voltage for Control Pin | GND | | $V_{CC} \times 0.35$ | mV |
| I_{IH} | Input HIGH Current | -150 | 20 | +150 | μA |
| I_{IL} | Input LOW Current | -150 | 5 | +150 | μA |

TERMINATION RESISTORS

| | | | | | |
|------------|--|----|----|----|----------|
| R_{TIN} | Internal Input Termination Resistor (Measured from I_N to V_{Tx}) | 45 | 50 | 55 | Ω |
| R_{TOUT} | Internal Output Termination Resistor | 45 | 50 | 55 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} .
- CML outputs (Q_n/\bar{Q}_n) have internal 50 Ω source termination resistors and must be externally terminated with 50 Ω to V_{CC0} for proper operation.
- V_{th} , V_{IH} , V_{IL} and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

NB7V585M

Table 6. AC CHARACTERISTICS $V_{CC} = 1.8\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C (Note 11)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------------------|--|------------|------------|------------|----------------------|
| f_{MAX} | Maximum Input Clock Frequency, $V_{OUTPP} \geq 200\text{ mV}$ | 6.0 | 7.0 | | GHz |
| $f_{DATAMAX}$ | Maximum Operating Input Data Rate (PRBS23) | 10 | | | Gbps |
| V_{OUTPP} | Output Voltage Amplitude (See Figures 4, Note 15) $f_{in} \leq 4.0\text{ GHz}$ $f_{in} \leq 6.0\text{ GHz}$ | 250 200 | 400 325 | | mV |
| t_{PLH}, t_{PHL} | Propagation Delay to Output Differential @ 1 GHz, Measured at Differential Crosspoint IN_x/IN_x^- to Q_n/Q_n^- SEL to Q_n | 125 | 175 200 | 250 300 | ps |
| $t_{PLH\ TC}$ | Propagation Delay Temperature Coefficient | | 100 | | fs/ $^\circ\text{C}$ |
| t_{SKEW} | Output – Output Skew (Within Device) (Note 12) Device – Device Skew ($t_{pd\ Max} - t_{pd\ min}$) | | | 30 50 | ps |
| t_{DC} | Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{in} \leq 4.0\text{ GHz}$ | 45 | 50 | 55 | % |
| t_{JITTER} | Output Random Jitter (RJ) (Note 13) Deterministic Jitter (DJ) (Note 14) $f_{in} \leq 6.0\text{ GHz}$ $f_{in} \leq 10\text{ Gbps}$ | | 0.2 | 0.8 10 | ps rms ps pk-pk |
| V_{INPP} | Input Voltage Swing (Differential Configuration) (Note 15) | 100 | | 1200 | mV |
| t_r, t_f | Output Rise/Fall Times @ 1 GHz (20% – 80%) $Q_n, \overline{Q_n}$ | | 50 | 65 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 400 mV source, 50% duty cycle clock source. All outputs must be loaded with external 50 Ω to V_{CC} . Input edge rates 40 ps (20% – 80%).
12. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the crosspoint of the outputs.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.
15. Input and output voltage swing is a single-ended measurement operating in differential mode.

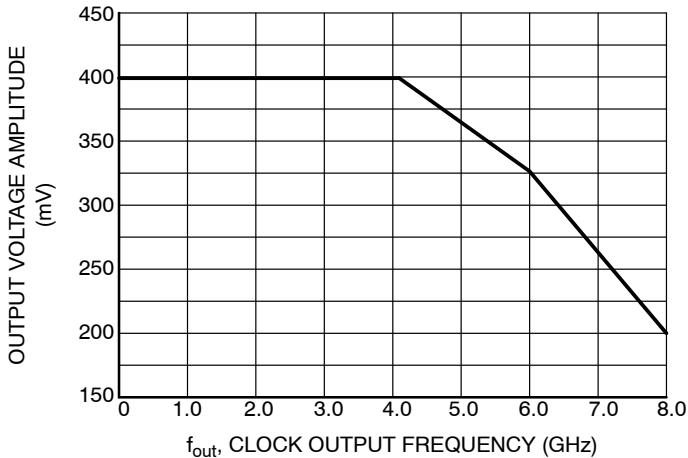


Figure 2. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

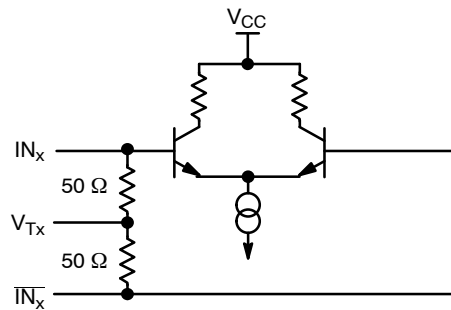


Figure 3. Input Structure

NB7V585M

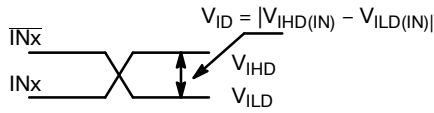


Figure 4. Differential Inputs Driven Differentially

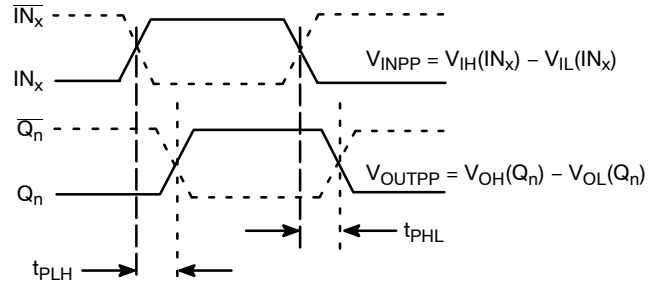


Figure 5. AC Reference Measurement

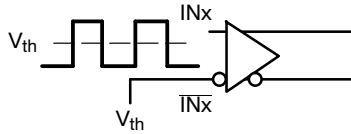


Figure 6. Differential Input Driven Single-Ended

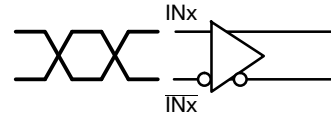


Figure 7. Differential Inputs Driven Differentially

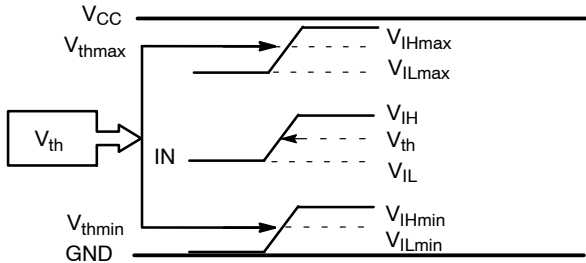


Figure 8. V_{th} Diagram

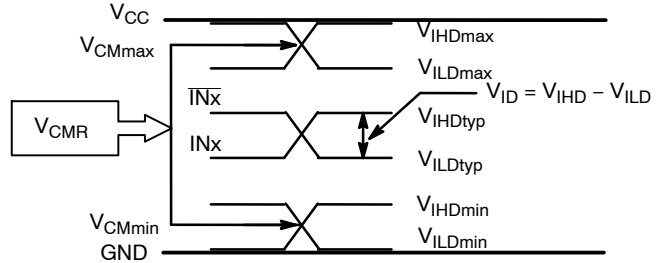


Figure 9. V_{CMR} Diagram

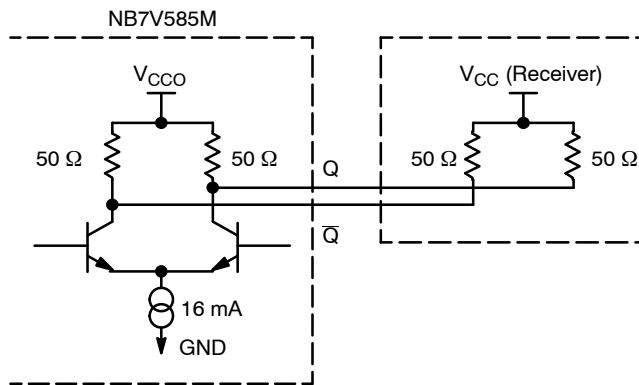


Figure 10. Typical CML Output Structure and Termination

NB7V585M

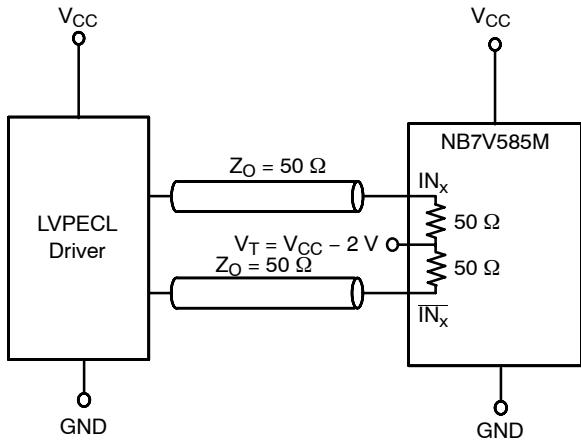


Figure 11. LVPECL Interface

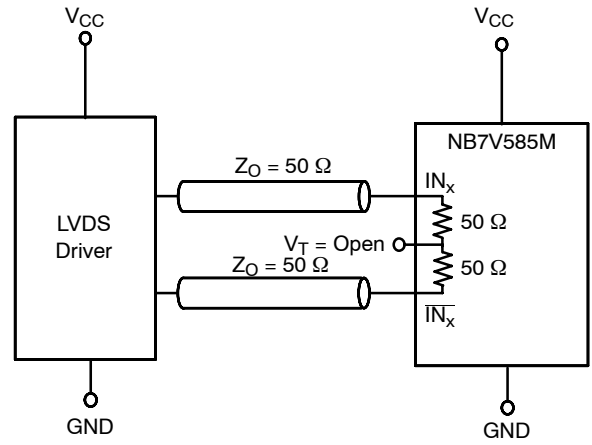


Figure 12. LVDS Interface

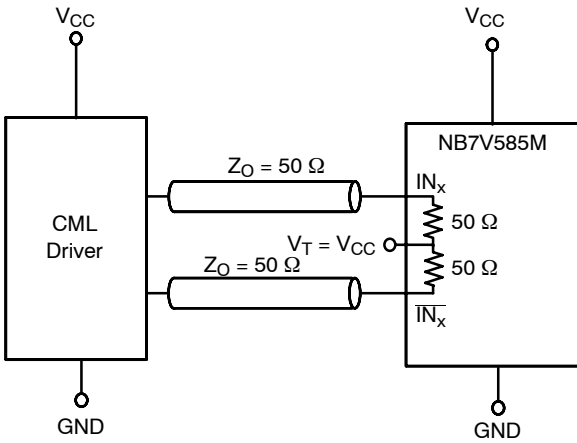


Figure 13. Standard 50 Ω Load CML Interface

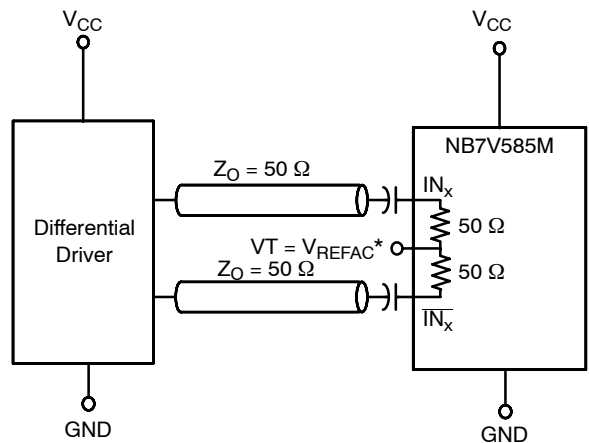


Figure 14. Capacitor-Coupled Differential Interface
(V_T Connected to V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μ F capacitor

ORDERING INFORMATION

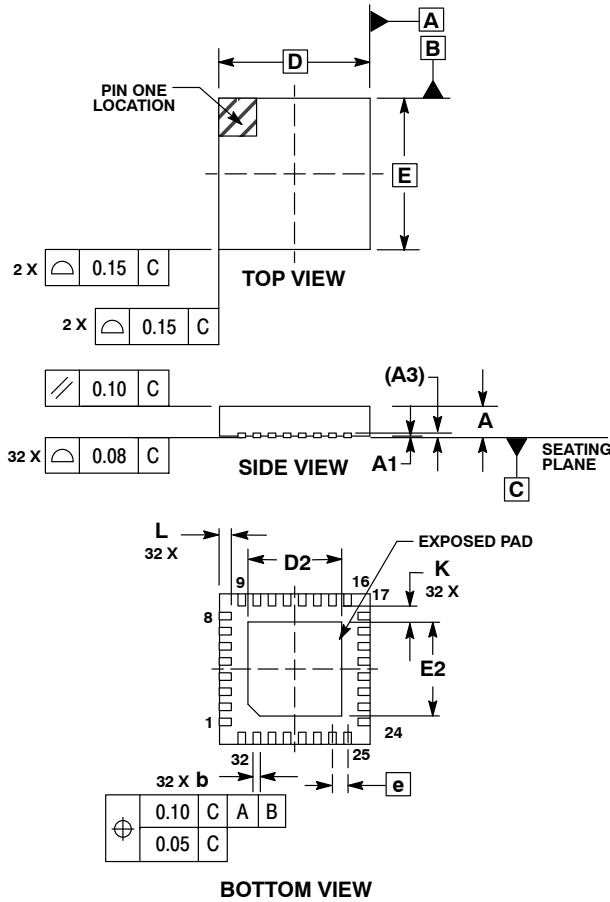
| Device | Package | Shipping† |
|---------------|--------------------|--------------------|
| NB7V585MMNG | QFN32 (Pb-Free) | 74 Units / Rail |
| NB7V585MMNR4G | QFN32 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7V585M

PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P
CASE 488AM-01
ISSUE 0

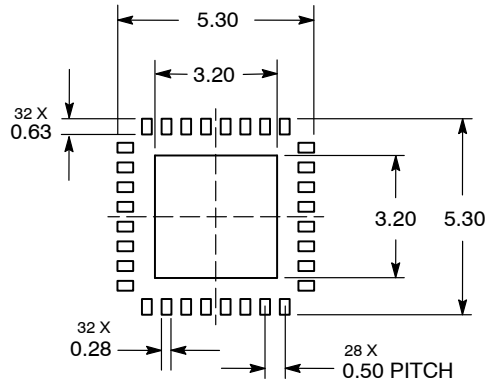


NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | | |
|-------------|-----------|-------|-------|
| DIM | MIN | NOM | MAX |
| A | 0.800 | 0.900 | 1.000 |
| A1 | 0.000 | 0.025 | 0.050 |
| A3 | 0.200 REF | | |
| b | 0.180 | 0.250 | 0.300 |
| D | 5.00 BSC | | |
| D2 | 2.950 | 3.100 | 3.250 |
| E | 5.00 BSC | | |
| E2 | 2.950 | 3.100 | 3.250 |
| e | 0.500 BSC | | |
| K | 0.200 | --- | --- |
| L | 0.300 | 0.400 | 0.500 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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