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January 2016

FDT86244

N-Channel Shielded Gate PowerTrench[®] MOSFET

150 V, 2.8 A, 128 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 128 mΩ at V_{GS} = 10 V, I_D = 2.8 A
- Max $r_{DS(on)}$ = 178 mΩ at V_{GS} = 6 V, I_D = 2.4 A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

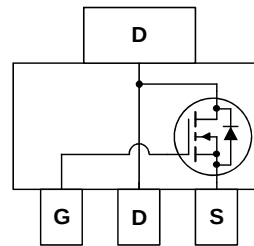
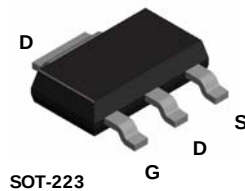


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- Load Switch
- Primary Switch



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	2.8	A
	-Pulsed	12	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	12	mJ
P_D	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.2	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	12	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86244	FDT86244	SOT-223	13 "	12 mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		104		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 2.8\ \text{A}$		106	128	m Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 2.4\ \text{A}$		127	178	
		$V_{GS} = 10\ \text{V}$, $I_D = 2.8\ \text{A}$, $T_J = 125^\circ\text{C}$		196	237	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 2.8\ \text{A}$		12		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 75\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		295	395	pF
C_{oss}	Output Capacitance			33	45	pF
C_{rss}	Reverse Transfer Capacitance			2.4	5	pF
R_g	Gate Resistance			1.0		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ \text{V}$, $I_D = 2.8\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		5.3	11	ns
t_r	Rise Time			1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			9.8	20	ns
t_f	Fall Time			2.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 75\ \text{V}$, $I_D = 2.8\ \text{A}$	4.9	7	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$		2.8	4	nC
Q_{gs}	Total Gate Charge			1.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.3		nC

Drain-Source Diode Characteristics

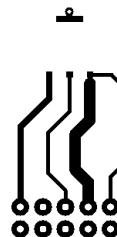
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.8\ \text{A}$ (Note 2)		0.82	1.3	V
t_{rr}	Reverse Recovery Time	$I_F = 2.8\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		48	77	ns
Q_{rr}	Reverse Recovery Charge			44	70	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $55^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b) $118^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Starting $T_J = 25^\circ\text{C}$; N-ch: $L = 1\ \text{mH}$, $I_{AS} = 5\ \text{A}$, $V_{DD} = 135\ \text{V}$, $V_{GS} = 10\ \text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

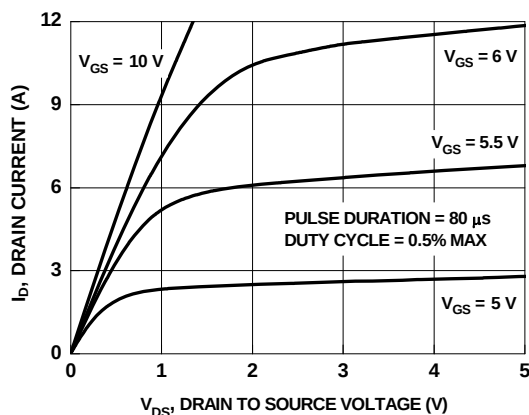


Figure 1. On Region Characteristics

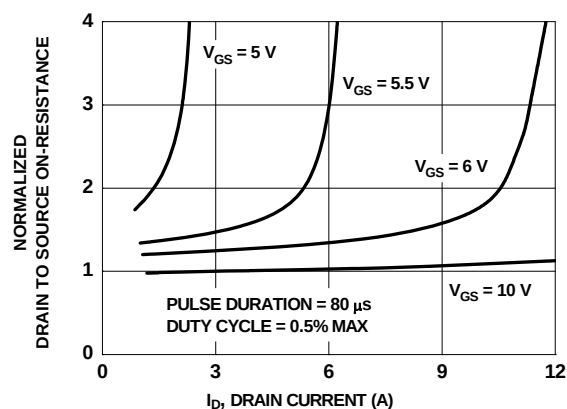


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

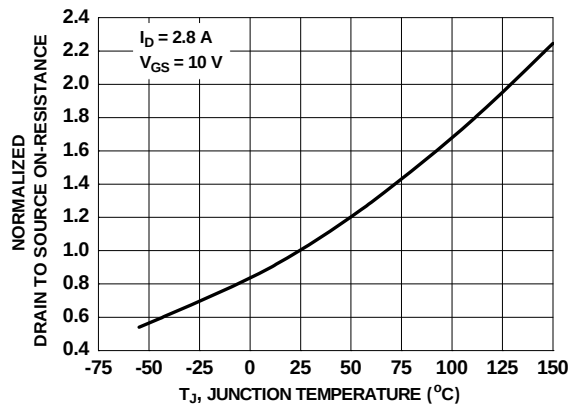


Figure 3. Normalized On Resistance vs Junction Temperature

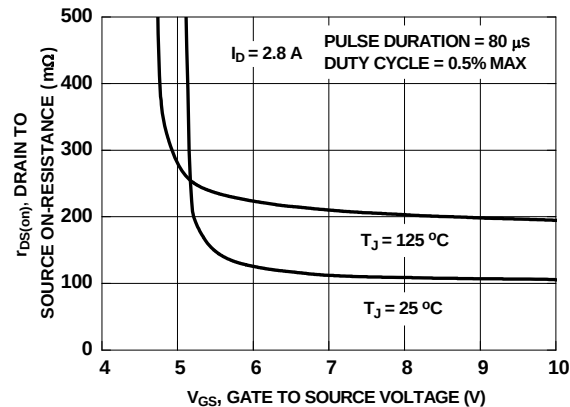


Figure 4. On-Resistance vs Gate to Source Voltage

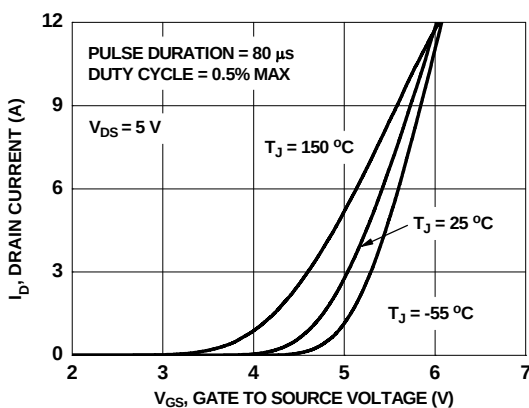


Figure 5. Transfer Characteristics

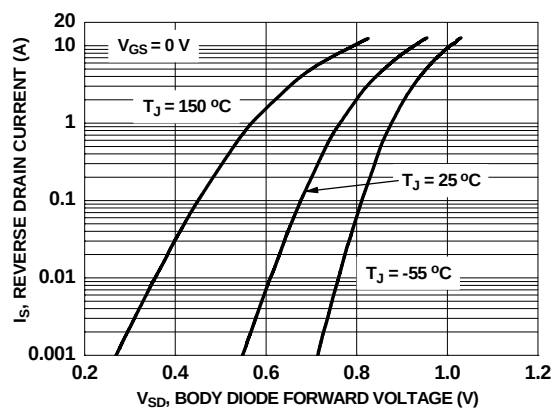


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

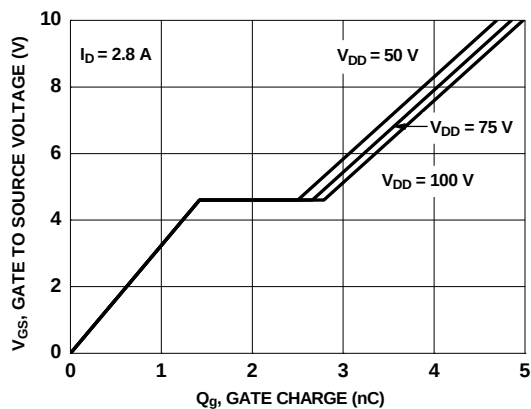


Figure 7. Gate Charge Characteristics

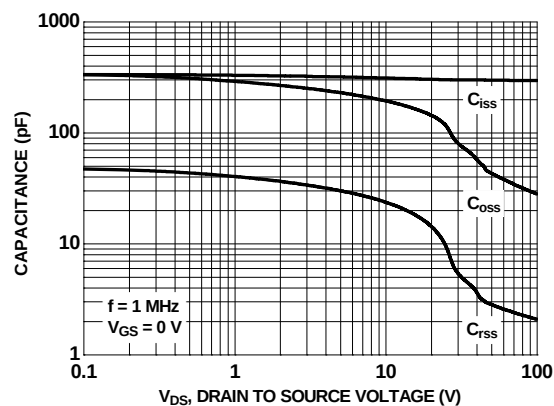


Figure 8. Capacitance vs Drain to Source Voltage

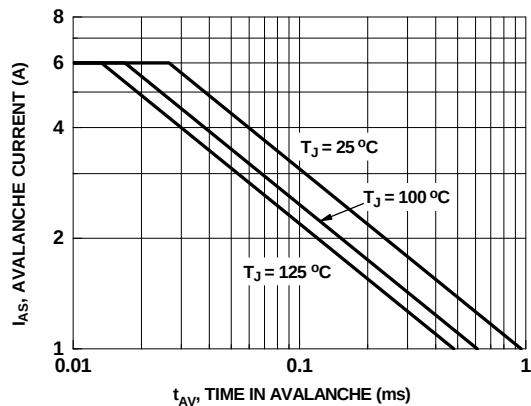


Figure 9. Unclamped Inductive Switching Capability

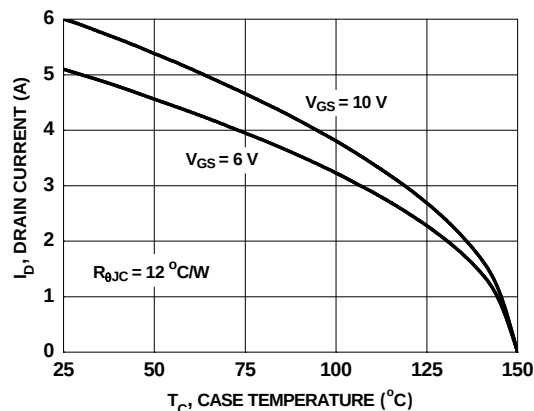


Figure 10. Maximum Continuous Drain Current vs Case Temperature

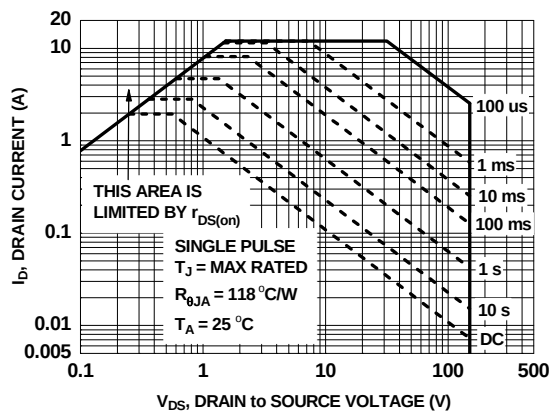


Figure 11. Forward Bias Safe Operating Area

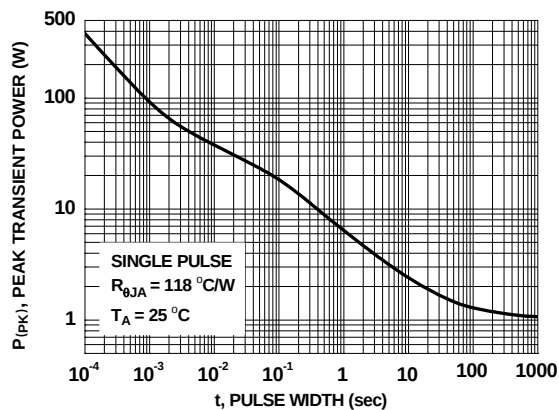


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

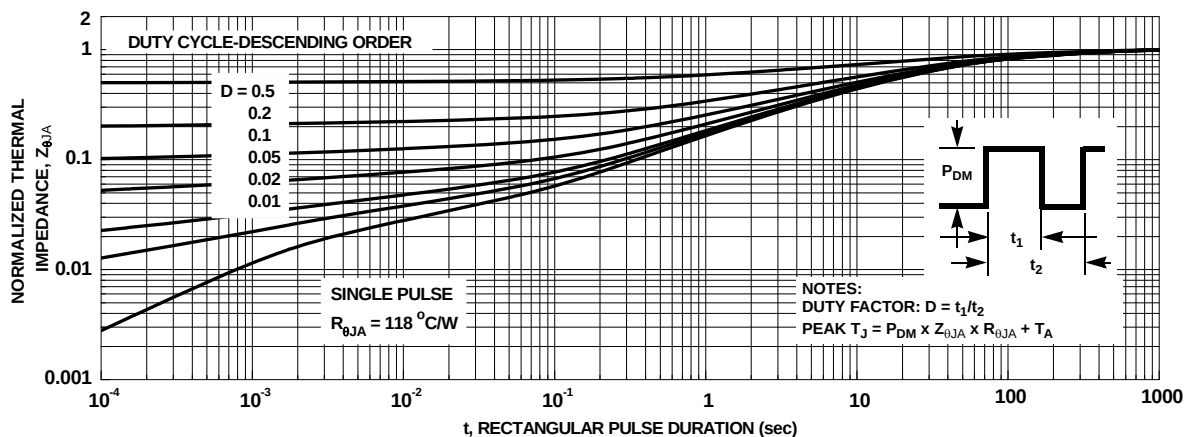


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



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