



25-Bit Configurable Registered Buffer for DDR2

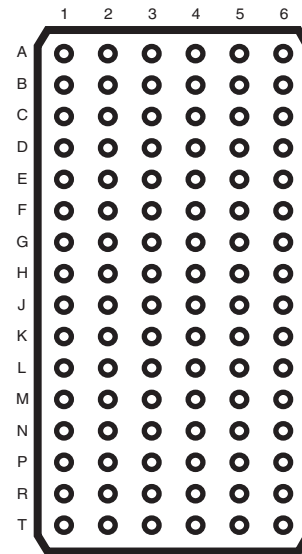
Recommended Application:

- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS97U877
- Ideal for DDR2 400, 533 and 667

Product Features:

- 25-bit 1:1 or 14-bit 1:2 configurable registered buffer
- Supports SSTL_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on C0, C1 and RESET# inputs
- Low voltage operation
V_{DD} = 1.7V to 1.9V
- Available in 96 BGA package
- Drop-in replacement for ICSSSTUA32866
- Green packages available

Pin Configuration



**96 Ball BGA
(Top View)**

Truth Table

| Inputs | | | | | | Outputs | | |
|--------|------------------|------------------|------------------|------------------|----------------------|----------------|----------------|----------------|
| RST# | DCS# | CSR# | CK | CK# | Dn, DODT, DCKE | Qn | QCS# | QODT, QCKE |
| H | L | L | ↑ | ↓ | L | L | L | L |
| H | L | L | ↑ | ↓ | H | H | L | H |
| H | L | L | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | L | H | ↑ | ↓ | L | L | L | L |
| H | L | H | ↑ | ↓ | H | H | L | H |
| H | L | H | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | H | L | ↑ | ↓ | L | L | H | L |
| H | H | L | ↑ | ↓ | H | H | H | H |
| H | H | L | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | H | H | ↑ | ↓ | L | Q ₀ | H | L |
| H | H | H | ↑ | ↓ | H | Q ₀ | H | H |
| H | H | H | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| L | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating | L | L | L |

Ball Assignments

| | DCKE | NC | V _{REF} | V _{DD} | QCKE | NC |
|---|------|------|------------------|-----------------|------|-----|
| A | D2 | D15 | GND | GND | Q2 | Q15 |
| B | D3 | D16 | V _{DD} | V _{DD} | Q3 | Q16 |
| C | DODT | NC | GND | GND | QODT | NC |
| D | D5 | D17 | V _{DD} | V _{DD} | Q5 | Q17 |
| E | D6 | D18 | GND | GND | Q6 | Q18 |
| F | NC | RST# | V _{DD} | V _{DD} | C1 | C0 |
| G | CK | DCS# | GND | GND | QCS# | NC |
| H | CK# | CSR# | V _{DD} | V _{DD} | ZOH | ZOL |
| J | D8 | D19 | GND | GND | Q8 | Q19 |
| K | D9 | D20 | V _{DD} | V _{DD} | Q9 | Q20 |
| L | D10 | D21 | GND | GND | Q10 | Q21 |
| M | D11 | D22 | V _{DD} | V _{DD} | Q11 | Q22 |
| N | D12 | D23 | GND | GND | Q12 | Q23 |
| P | D13 | D24 | V _{DD} | V _{DD} | Q13 | Q24 |
| R | D14 | D25 | V _{REF} | V _{DD} | Q14 | Q25 |
| T | | | | | | |
| | 1 | 2 | 3 | 4 | 5 | 6 |

1:1 Register (C0 = 0, C1 = 0)



Ball Assignments

| | | | | | | |
|---|------|------|------------------|-----------------|-------|-------|
| A | DCKE | NC | V _{REF} | V _{DD} | QCKEA | QCKEB |
| B | D2 | NC | GND | GND | Q2A | Q2B |
| C | D3 | NC | V _{DD} | V _{DD} | Q3A | Q3B |
| D | DODT | NC | GND | GND | QODTA | QODTB |
| E | D5 | NC | V _{DD} | V _{DD} | Q5A | Q5B |
| F | D6 | NC | GND | GND | Q6A | Q6B |
| G | NC | RST# | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | DCS# | GND | GND | QCSA# | QCSB# |
| J | CK# | CSR# | V _{DD} | V _{DD} | ZOH | ZOL |
| K | D8 | NC | GND | GND | Q8A | Q8B |
| L | D9 | NC | V _{DD} | V _{DD} | Q9A | Q9B |
| M | D10 | NC | GND | GND | Q10A | Q10B |
| N | D11 | NC | V _{DD} | V _{DD} | Q11A | Q11B |
| P | D12 | NC | GND | GND | Q12A | Q12B |
| R | D13 | NC | V _{DD} | V _{DD} | Q13A | Q13B |
| T | D14 | NC | V _{REF} | V _{DD} | Q14A | Q14B |
| | 1 | 2 | 3 | 4 | 5 | 6 |

1:2 Register A (C0 = 0, C1 = 1)

Ball Assignments

| | | | | | | |
|---|------|------|------------------|-----------------|-------|-------|
| A | D1 | NC | V _{REF} | V _{DD} | Q1A | Q1B |
| B | D2 | NC | GND | GND | Q2A | Q2B |
| C | D3 | NC | V _{DD} | V _{DD} | Q3A | Q3B |
| D | D4 | NC | GND | GND | Q4A | Q4B |
| E | D5 | NC | V _{DD} | V _{DD} | Q5A | Q5B |
| F | D6 | NC | GND | GND | Q6A | Q6B |
| G | NC | RST# | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | DCS# | GND | GND | QCSA# | QCSB# |
| J | CK# | CSR# | V _{DD} | V _{DD} | ZOH | ZOL |
| K | D8 | NC | GND | GND | Q8A | Q8B |
| L | D9 | NC | V _{DD} | V _{DD} | Q9A | Q9B |
| M | D10 | NC | GND | GND | Q10A | Q10B |
| N | DODT | NC | V _{DD} | V _{DD} | QODTA | QODTB |
| P | D12 | NC | GND | GND | Q12A | Q12B |
| R | D13 | NC | V _{DD} | V _{DD} | Q13A | Q13B |
| T | DCKE | NC | V _{REF} | V _{DD} | QCKEA | QCKEB |
| | 1 | 2 | 3 | 4 | 5 | 6 |

1:2 Register B (C0 = 1, C1 = 1)

General Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VDD operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR-II DIMM load. **ICSSSTUA32864B** operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going high, and CK# going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

The device supports low-power standby operation. When the reset input (RST#) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when RST# is low all registers are reset, and all outputs are forced low. The LVCMOS RST# and Cn inputs must always be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, RST# must be held in the low state during power up.

In the DDR-II RDIMM application, RST# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RST# until the input receivers are fully enabled, the design of the **ICSSSTUA32864B** must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both DCS# and CSR# inputs and will gate the Qn outputs from changing states when both DCS# and CSR# inputs are high. If either DCS# or CSR# input is low, the Qn outputs will function normally. The RST input has priority over the DCS# and CSR# control and will force the outputs low. If the DCS#-control functionality is not desired, then the CSR# input can be hardwired to ground, in which case, the setup-time requirement for DCS# would be the same as for the other D data inputs. Package options include 96-ball LFBGA (MO-205CC).

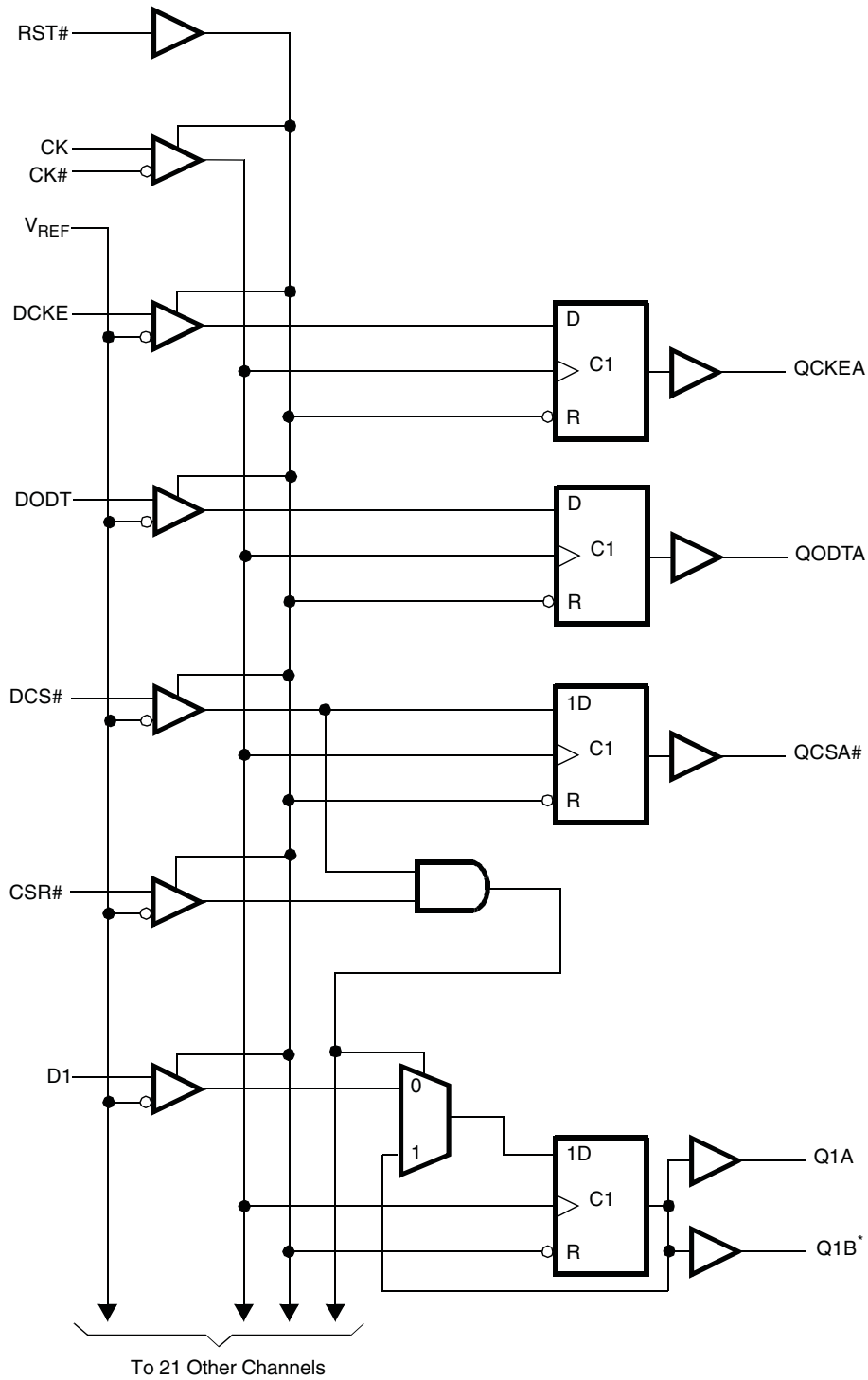


Ball Assignment

| Terminal Name | Description | Electrical Characteristics |
|------------------|---|----------------------------|
| GND | Ground | Ground input |
| V _{DD} | Power supply voltage | 1.8V nominal |
| V _{REF} | Input reference voltage | 0.9V nominal |
| Z _{OH} | Reserved for future use | Input |
| Z _{OL} | Reserved for future use | Input |
| CK | Positive master clock input | Differential input |
| CK# | Negative master clock input | Differential input |
| C0, C1 | Configuration control inputs | LVC MOS inputs |
| RST# | Asynchronous reset input - resets registers and disables V _{REF} data and clock differential-input receivers | LVC MOS input |
| CSR#, DCS# | Chip select inputs - disables D1 - D24 outputs switching when both inputs are high | SSTL ₁₈ input |
| D1 - D25 | Data input - clock in on the crossing of the rising edge of CK and the falling edge of CK# | SSTL ₁₈ input |
| DODT | The outputs of this register bit will not be suspended by the DCS# and CSR# control | SSTL ₁₈ input |
| DCKE | The outputs of this register bit will now be suspended by the DCS# and CSR# control | SSTL ₁₈ input |
| Q1 - Q25 | Data outputs that are suspended by the DCS# and CSR# control | 1.8V CMOS |
| QCS# | Data output that will not be suspended by the DCS# and CSR# control | 1.8V CMOS |
| QODT | Data output that will not be suspended by the DCS# and CSR# control | 1.8V CMOS |
| QCKE | Data output that will not be suspended by the DCS# and CSR# control | 1.8V CMOS |

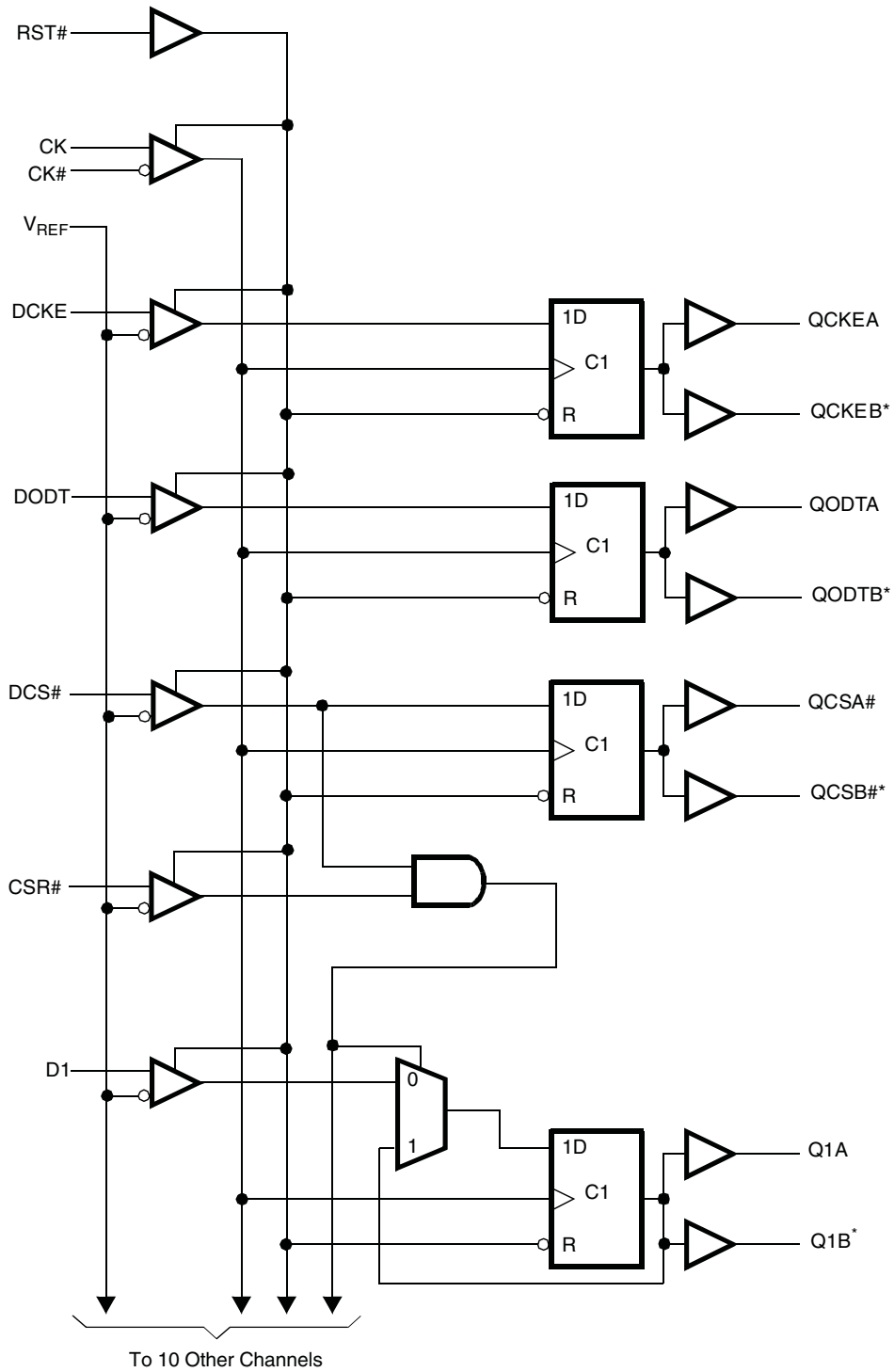


Block Diagram for 1:1 mode (positive logic)





Block Diagram for 1:2 mode (positive logic)



*Note: Disabled in 1:1 configuration



Absolute Maximum Ratings

| | |
|--|---------------------|
| Storage Temperature | -65°C to +150°C |
| Supply Voltage | -0.5V to 2.5V |
| Input Voltage ^{1,2} | -0.5V to +2.5V |
| Output Voltage ^{1,2} | -0.5V to VDD + 0.5V |
| Input Clamp Current | ±50 mA |
| Output Clamp Current | ±50mA |
| Continuous Output Current | ±50mA |
| VDD or GND Current/Pin | ±100mA |
| Package Thermal Impedance ³ | 36°C |

Notes:

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This value is limited to 2.5V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

| PARAMETER | DESCRIPTION | | MIN | TYP | MAX | UNITS | |
|----------------------|--------------------------------|-------------------|--------------------------|-----------------------|--------------------------|-------|----|
| V _{DD} | I/O Supply Voltage | | 1.7 | 1.8 | 1.9 | V | |
| V _{REF} | Reference Voltage | | 0.49 x V _{DD} | 0.5 x V _{DD} | 0.51 x V _{DD} | | |
| V _{TT} | Termination Voltage | | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 | | |
| V _I | Input Voltage | | 0 | | V _{DD} | | |
| V _{IH (DC)} | DC Input High Voltage | Data Inputs | V _{REF} + 0.125 | | | | |
| V _{IH (AC)} | AC Input High Voltage | | V _{REF} + 0.250 | | | | |
| V _{IL (DC)} | DC Input Low Voltage | | | | V _{REF} - 0.125 | | |
| V _{IL (AC)} | AC Input Low Voltage | | | | V _{REF} - 0.250 | | |
| V _{IH} | Input High Voltage Level | RESET#, C0, C1 | 0.65 x V _{DD} | | | | |
| V _{IL} | Input Low Voltage Level | | | | 0.35 x V _{DD} | | |
| V _{ICR} | Common mode Input Range | CLK, CLK# | 0.675 | | 1.125 | | |
| V _{ID} | Differential Input Voltage | | 0.600 | | | | |
| I _{OH} | High-Level Output Current | | | | -8 | | mA |
| I _{OL} | Low-Level Output Current | | | | 8 | | |
| T _A | Operating Free-Air Temperature | | 0 | | 70 | °C | |

¹Guaranteed by design, not 100% tested in production.

Note: Reset# and Cn inputs must be held at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless Reset# is low.



Electrical Characteristics - DC

T_A = 0 - 70°C; V_{DD} = 1.8 +/-0.1V (unless otherwise stated)

| SYMBOL | PARAMETERS | CONDITIONS | V _{DD} | MIN | TYP | MAX | UNITS |
|------------------|--|---|-----------------|-----|-----|------|-----------------------|
| V _{IK} | | I _I = -18mA | | | | -1.2 | V |
| V _{OH} | | I _{OH} = -6mA | 1.7V | 1.2 | | | |
| V _{OL} | | I _{OL} = 6mA | 1.7V | | | 0.5 | |
| I _I | All Inputs | V _I = V _{DD} or GND | 1.9V | -5 | | 5 | μA |
| I _{DD} | Standby (Static) | RESET# = GND | 1.9V | | | 100 | μA |
| | Operating (Static) | V _I = V _{IH(AC)} or V _{IL(AC)} , RESET# = V _{DD} | | | | 40 | |
| I _{DDD} | Dynamic operating (clock only) | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK# switching 50% duty cycle. | 1.8V | | 39 | | μ/clock MHz |
| | Dynamic Operating (per each data input) 1:1 mode | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK# switching 50% duty cycle. One data | | | 19 | | μA/ clock MHz/data |
| | Dynamic Operating (per each data input) 1:2 mode | input switching at half clock frequency, 50% duty cycle | | | 35 | | |
| C _i | Data Inputs | V _I = V _{REF} ±350mV | | 2.5 | | 3.5 | pF |
| | CLK and CLK# | V _{ICR} = 1.25V, V _{I(PP)} = 360mV | | 2 | | 3 | |
| | RESET# | V _I = V _{DD} or GND | | | 2.5 | | |

Notes:

1 - Guaranteed by design, not 100% tested in production.



Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

| SYMBOL | PARAMETERS | | MIN | MAX | UNITS |
|-------------|---|--|------|-----|-------|
| f_{clock} | Clock frequency | | | 410 | MHz |
| t_W | Pulse duration, CK, CK High or Low | | 1 | | ns |
| t_{ACT} | Differential inputs active time (See notes 1 and 2) | | | 10 | ns |
| t_{INACT} | Differential inputs inactive time (See notes 1 and 3) | | | 15 | ns |
| | Setup time | DCS before CK, CK↓, CSR high; CSR before CK, CK↓, DCS high | 0.7 | | ns |
| t_{SU} | Setup time | DCS before CK, CK↓, CSR Low | 0.5 | | ns |
| | | DODT, DCKE and data before CK, CK↓ | 0.5 | | ns |
| t_h | Hold time | DCS, DODT, DCKE and data after CK, CK↓ | 0.50 | | ns |
| | | PAR_IN after CK, CK↓ | 0.50 | | ns |

- Notes:**
- 1 - Guaranteed by design, not 100% tested in production.
 - 2 - For data signal input slew rate of 1V/ns.
 - 3 - For data signal input slew rate of 0.5V/ns and < 1V/ns.
 - 4 - CLK/CLK# signal input slew rate of 1V/ns.

Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

| SYMBOL | From (Input) | To (Output) | $V_{DD} = 1.8V \pm 0.1V$ | | | UNITS |
|---------------|--------------|-------------|--------------------------|-----|-----|-------|
| | | | MIN | TYP | MAX | |
| f_{max} | | | 410 | | | MHz |
| t_{PDM}^1 | CLK, CLK# | Q | 1.1 | | 1.9 | ns |
| t_{PDMSS}^2 | CLK, CLK# | Q | | | 2 | |
| t_{phi} | RESET# | Q | | | 3 | ns |

- Notes: 1. Includes 350ps test-load transmission-line delay
 2. Guaranteed by design, not 100% tested in production.

Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range (See figure 7)

| PARAMETER | $V_{DD} = 1.8V \pm 0.1V$ | | UNIT |
|--------------------|--------------------------|-----|------|
| | MIN | MAX | |
| dV/dt_r | 1 | 4 | V/ns |
| dV/dt_f | 1 | 4 | V/ns |
| dV/dt_{Δ}^1 | | 1 | V/ns |

1. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

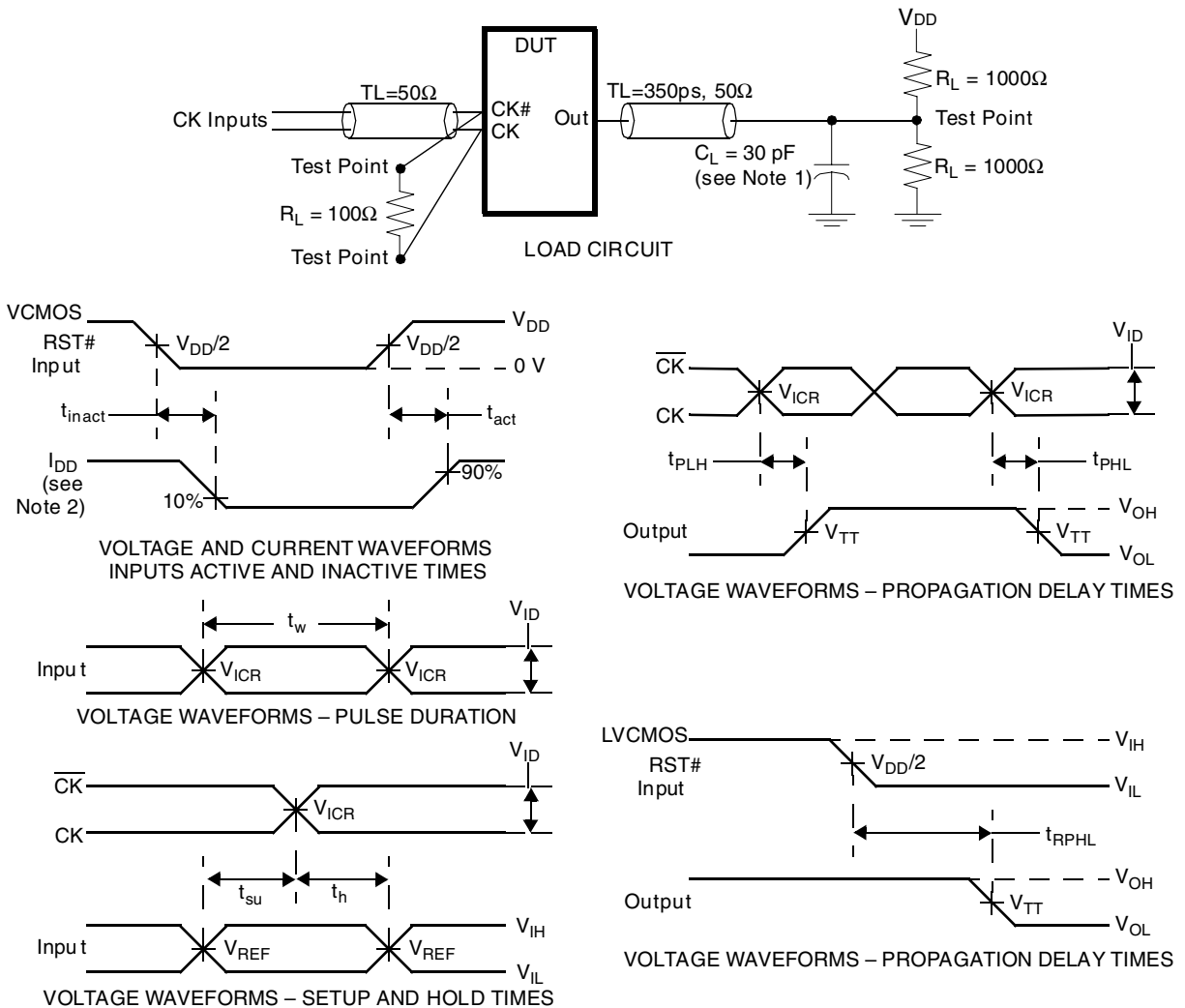
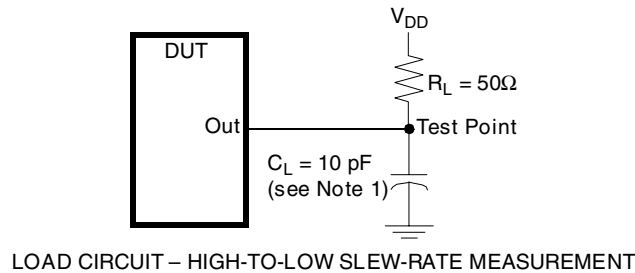
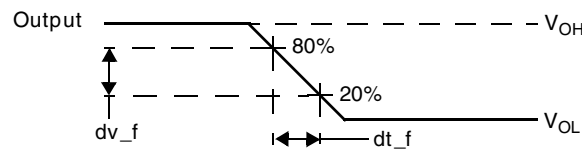


Figure 6— Parameter Measurement Information ($V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$)

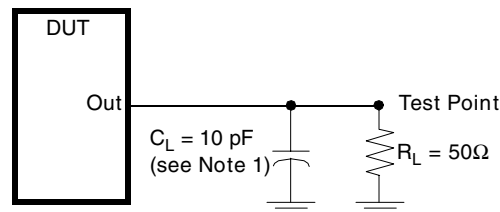
- Notes:
1. C_L includes probe and jig capacitance.
 2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_o = 0\text{ mA}$.
 3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\Omega$, input slew rate = $1\text{ V/ns} \pm 20\%$ (unless otherwise specified).
 4. The outputs are measured one at a time with one transition per measurement.
 5. $V_{REF} = V_{DD}/2$
 6. $V_{IH} = V_{REF} + 250\text{ mV}$ (ac voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
 7. $V_{IL} = V_{REF} - 250\text{ mV}$ (ac voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVCMOS input.
 8. $V_{ID} = 600\text{ mV}$
 9. t_{PLH} and t_{PHL} are the same as t_{PDM} .



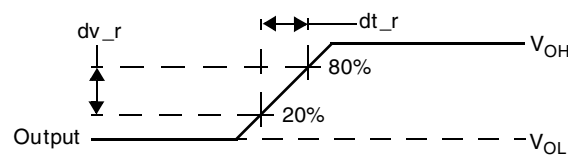
LOAD CIRCUIT – HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS – HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT – LOW-TO-HIGH SLEW-RATE MEASUREMENT

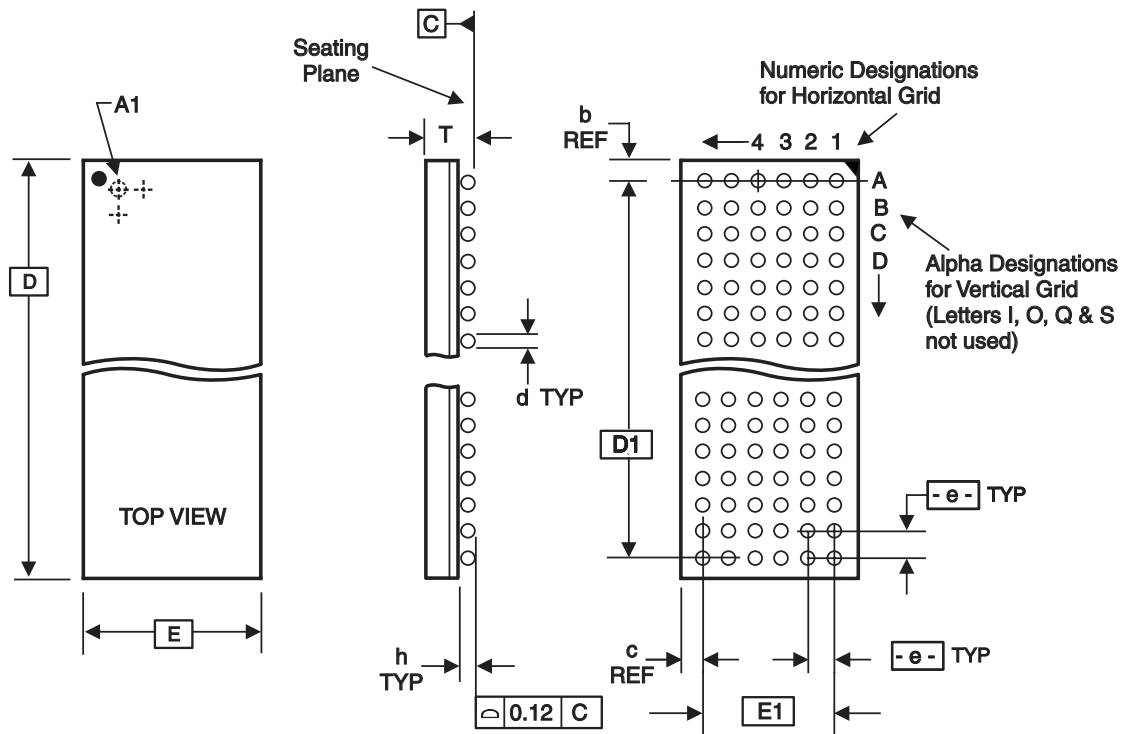


VOLTAGE WAVEFORMS – LOW-TO-HIGH SLEW-RATE MEASUREMENT

Figure 7 — Output Slew-Rate Measurement Information ($V_{DD} = 1.8V \pm 0.1V$)

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz$, $Z_O = 50\Omega$, input slew rate = $1 V/ns \pm 20\%$ (unless otherwise specified).



ALL DIMENSIONS IN MILLIMETERS

| D | E | T | e | BALL GRID | | Max. TOTAL | d | h | REF. DIMENSIONS | |
|-----------|----------|-----------|----------|-----------|------|------------|-----------|-----------|-----------------|-------|
| | | | | HORIZ | VERT | | | | b | c |
| 13.50 Bsc | 5.50 Bsc | 1.30/1.50 | 0.80 Bsc | 6 | 16 | 96 | 0.40/0.50 | 0.25/0.41 | 0.75 | 0.75 |
| 11.50 Bsc | 5.00 Bsc | /1.2 | 0.65 Bsc | 6 | 16 | 96 | 0.38/0.48 | 0.27/0.37 | 0.875 | 0.875 |

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

* Source Ref.: JEDEC Publication 95, MO-205

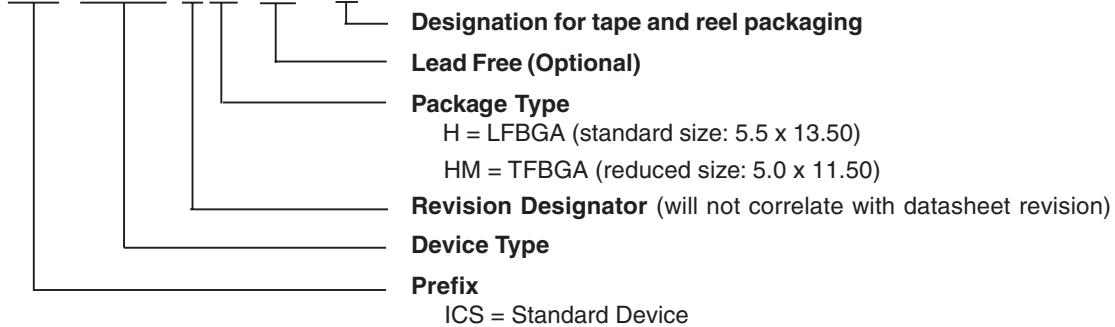
10-0055C

Ordering Information

ICSSSTUA32864Bz(LF)T

Example:

ICS XXXX y z (LF) - T





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Электрон
Связь**

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Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331