

# NB3L8504S

## 2.5 V / 3.3 V 1:4 Differential Input to LVDS Fanout Buffer / Translator

### Description

The NB3L8504S is a differential 1:4 LVDS fanout buffer/translator with OE control for each differential output. The differential inputs which can be driven by either a differential or single-ended input, can accept various logic level standards such as LVPECL, LVDS, HSTL, HCSL and SSTL. These signals are then translated to four identical LVDS copies of the input up to 700 MHz. As such, the NB3L8504S is ideal for Clock distribution applications that require low skew.

The NB3L8504S is offered in the TSSOP-16 package.

### Features

- Four Differential LVDS Outputs
- Each Differential Output has OE Control
- 700 MHz Maximum Output Frequency
- 660 ps Max Output Rise and Fall Times, LVCMOS
- Translates Differential Input to LVDS Levels
- Additive Phase Jitter RMS: < 100 fs Typical
- 50 ps Maximum Output Skew
- 350 ps Maximum Part-to-part Skew
- 1.3 ns Maximum Propagation Delay
- Operating Range:  $V_{CC} = 2.5 V \pm 5\%$  or  $3.3 V \pm 10\%$
- $-40^{\circ}C$  to  $+85^{\circ}C$  Ambient Operating Temperature
- 16-Pin TSSOP, 4.4 mm x 5.0 mm x 0.925 mm
- These are Pb-Free Devices

### Applications

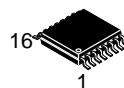
- Telecom
- Ethernet
- Networking
- SONET



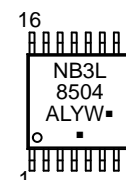
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### MARKING DIAGRAM\*



TSSOP-16  
DT SUFFIX  
CASE 948F



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

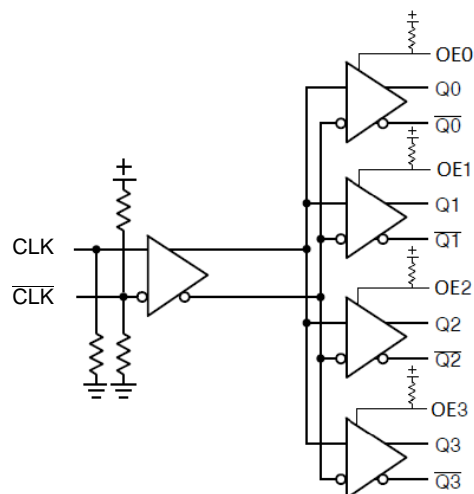


Figure 1. Logic Diagram

### ORDERING INFORMATION

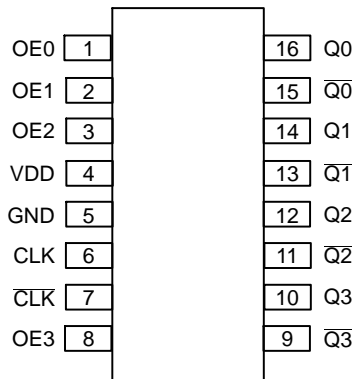
See detailed ordering and shipping information on page 9 of this data sheet.

# NB3L8504S

**Table 1. PIN DESCRIPTIONS AND CHARACTERISTICS**

Pin	Name	I/O	Description
1	OE0	LVTTL/LVCMOS Input	Output Enable pin for Q0, $\overline{Q0}$ outputs. Defaults High when left open; internal pull-up resistor.
2	OE1	LVTTL/LVCMOS Input	Output Enable pin for Q1, $\overline{Q1}$ outputs. Defaults High when left open; internal pull-up resistor.
3	OE2	LVTTL/LVCMOS Input	Output Enable pin for Q2, $\overline{Q2}$ outputs. Defaults High when left open; internal pull-up resistor.
4	VDD	Power	3.3 V / 2.5 V Positive Supply Voltage.
5	GND	Power	3.3 V / 2.5 V Negative Supply Voltage.
6	CLK	Multi-Level Input	Non-inverting differential Clock input. Defaults Low when left open; internal pull-down resistor.
7	$\overline{\text{CLK}}$	Multi-Level Input	Inverting differential Clock input. Defaults to VDD/2 when left open; internal pull-up and pull-down resistors.
8	OE3	LVTTL/LVCMOS Input	Output Enable pin for Q3, $\overline{Q3}$ outputs. Defaults High when left open; internal pull-up resistor.
9	$\overline{Q3}$	LVDS Output	Inverting differential Clock output.
10	Q3	LVDS Output	Non-inverting differential Clock output.
11	$\overline{Q2}$	LVDS Output	Inverting differential Clock output.
12	Q2	LVDS Output	Non-inverting differential Clock output.
13	$\overline{Q1}$	LVDS Output	Inverting differential Clock output.
14	Q1	LVDS Output	Non-inverting differential Clock output.
15	$\overline{Q0}$	LVDS Output	Inverting differential Clock output.
16	Q0	LVDS Output	Non-inverting differential Clock output.

1. All VDD and GND pins must be externally connected to a power supply for proper operation.



**Figure 2. NB3L8504S Pinout, 16-pin TSSOP (Top View)**

**Table 2. OUTPUT ENABLE FUNCTION TABLE**

OE[3:0]	Outputs – Q[0:3], $\overline{Q}$ [0:3]
LOW	High Impedance
HIGH (Default)	Active

# NB3L8504S

**Table 3. ATTRIBUTES**

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R <sub>PU</sub> – Input Pull-up Resistor R <sub>PD</sub> – Input Pull-down Resistor		50 kΩ 50 kΩ
C <sub>IN</sub> – Input Capacitance		4 pF
R <sub>IN</sub> – Input Impedance		10 kΩ
Moisture Sensitivity (Note 2)	TSSOP–16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count		371
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition		Rating	Unit
V <sub>DD</sub>		GND = 0 V		4.6	V
V <sub>IN</sub>		GND = 0 V		–0.5 to V <sub>DD</sub> +0.5	V
I <sub>out</sub>	Continuous Current Surge Current	LVDS Outputs		10 15	mA mA
I <sub>OSC</sub>	Output Short Circuit Current Line-to-Line (Q to $\bar{Q}$ ) Line-to-GND (Q or $\bar{Q}$ to GND)	Q or $\bar{Q}$ Q to $\bar{Q}$ to GND	Continuous Continuous	12 24	mA mA
T <sub>A</sub>	Operating Temperature Range	TSSOP–16		–40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			–65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	TSSOP–16 TSSOP–16	138 108	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	(Note 3)	TSSOP–16	33 – 36	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NB3L8504S

**Table 5. DC CHARACTERISTICS**  $V_{DD} = 2.5\text{ V} \pm 5\%$  or  $3.3\text{ V} \pm 10\%$ ;  $GND = 0\text{ V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
--------	----------------	-----	-----	-----	------

**POWER SUPPLY / CURRENT** (Note 4)

$V_{DD}$	Power Supply Voltage	$V_{DD} = 3.3\text{ V}$ $V_{DD} = 2.5\text{ V}$	2.97 2.375	3.3 2.5	3.63 2.625	V
$I_{DD}$	Power Supply Current for $V_{DD}$			41	50	mA

**LVDS OUTPUTS** (Note 5)

$V_{OD}$	Differential Output Voltage (Figure 12) (Notes 6 and 7)	250	350	450	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change (Figure 12) (Notes 6 and 7)			50	mV
$V_{OS}$	Offset Voltage (Figure 13) (Notes 6 and 7)	1075	1250	1375	mV
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change (Figure 13) (Notes 6 and 7)			50	mV
$V_{OH}$	Output HIGH Voltage		1425	1600	mV
$V_{OL}$	Output LOW Voltage	900	1075		mV

**DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (see Figure 5 & 6) (Note 11)

$V_{IHD}$	Differential Input HIGH Voltage	500		$V_{DD} - 850$	mV
$V_{ILD}$	Differential Input LOW Voltage	-300		$V_{IHD} - 150$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	150		1300	mV
$V_{IHCMR}$	Input Common Mode Voltage Range (Differential Configuration) (Note 10) (Figure 7)	$GND + 0.5$		$V_{DD} - 850$	mV
$I_{IH}$	Input HIGH Current, $V_{DD} = V_{IN} = 3.63\text{ V}$	CLK, CLK		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current, $V_{DD} = 3.63\text{ V}$ , $V_{IN} = 0\text{ V}$	CLK CLK	-5 -150		$\mu\text{A}$

**LVC MOS – OE Control Inputs**

$V_{IH}$	Input HIGH Voltage	2.0		$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage	-0.3		0.8	V
$I_{IH}$	Input HIGH Current, $V_{DD} = V_{IN} = 3.63\text{ V}$			5	$\mu\text{A}$
$I_{IL}$	Input LOW Current, $V_{DD} = 3.63\text{ V}$ , $V_{IN} = 0\text{ V}$		-150		$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input pins open and output pins loaded with  $R_L = 100\ \Omega$  across differential.
5. LVDS outputs require  $100\ \Omega$  receiver termination resistor between diff. pair. See Figure 14.
6.  $V_{OS\ max} + \frac{1}{2} V_{OD\ max}$ . Also see Figures 12 and 13.
7.  $V_{OS\ min} - \frac{1}{2} V_{OD\ max}$ . Also see Figures 12 and 13.
8.  $V_{IH}$ ,  $V_{IL}$ ,  $V_{th}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.
9.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.
10.  $V_{IHCMR\ max}$  varies 1:1 with  $V_{DD}$ ,  $V_{IHCMR\ min}$  varies 1:1 with  $GND$ .
11.  $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{IHCMR}$  parameters must be complied with simultaneously.

# NB3L8504S

**Table 6. AC CHARACTERISTICS**  $V_{DD} = 2.5\text{ V} \pm 5\%$  or  $3.3\text{ V} \pm 10\%$ ;  $GND = 0\text{ V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (Note 12) (Figure 10)

Symbol	Characteristic	Min	Typ	Max	Unit
$f_{MAX}$	Input Clock Frequency $V_{OUTPP} \geq 250\text{ mV}$ @ $V_{INPPmax}$			700	MHz
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) $f_{in} \leq 700\text{ MHz}$ (See Figure 3)	250	350		mV
tpd	Differential Input to Differential Output Propagation Delay at $f_{MAX}$ @ $V_{DD} = 3.3\text{ V}$	0.9		1.3	ns
tjit( $\phi$ )	Additive Phase Jitter RMS (Figure 4) Integration Range: 12 kHz – 20 MHz $f_{out} = 156.25\text{ MHz}$ $f_{out} = 100\text{ MHz}$		0.07 0.10	0.08 0.105	ps
t <sub>SKEW(o-o)</sub>	Output-to-output Skew (Note 14) (Figure 8)			50	ps
T <sub>SKEW(pp)</sub>	Part-to-part Skew (Note 14)			350	ps
t <sub>r</sub> / t <sub>f</sub>	Output Rise/Fall Times @ 50 MHz, 20% – 80%	180	350	660	ps
t <sub>DC</sub>	Output Clock Duty Cycle (Input Duty Cycle = 50%)	45	50	55	%
$V_{INPP}$	Input Voltage Swing (Differential Configuration) (Note 13)	150		1300	mV

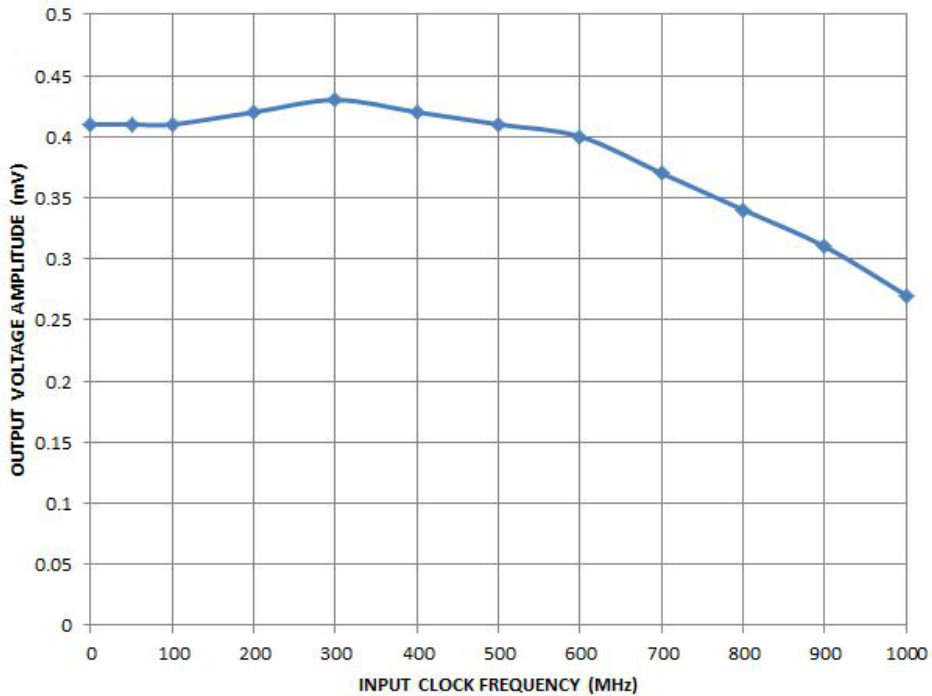
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured by forcing a 50% duty cycle clock source. All LVDS output loading with an external  $R_L = 100\ \Omega$  across Q &  $\bar{Q}$ .

13.  $V_{INPP(max)}$  cannot exceed  $V_{DD}$ . Input voltage swing is a single-ended measurement operating in differential mode.

14. Skew is measured between outputs under identical transition at 50 MHz.



**Figure 3. Output Voltage Amplitude ( $V_{OUTPP}$ ) vs. Input Clock Frequency ( $f_{in}$ ) and Temperature (@  $V_{DD} = 2.5\text{ V}$ )**

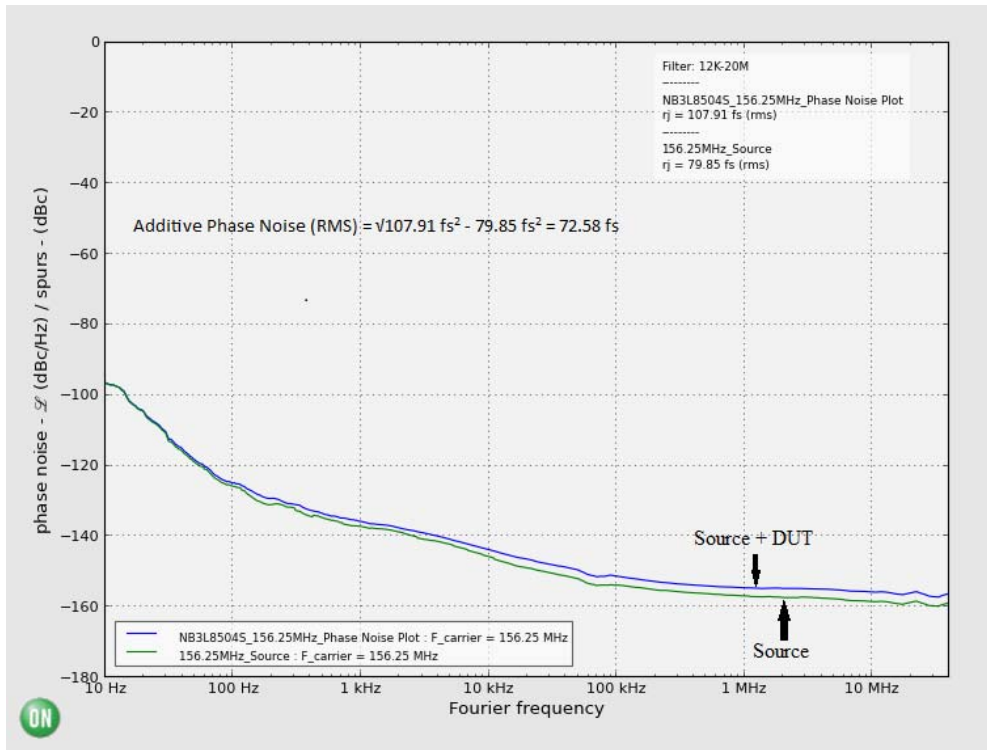


Figure 4. Additive Phase Jitter

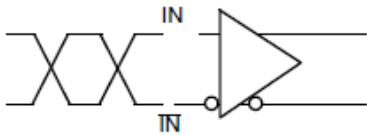


Figure 5. Differential Inputs Driven Differentially

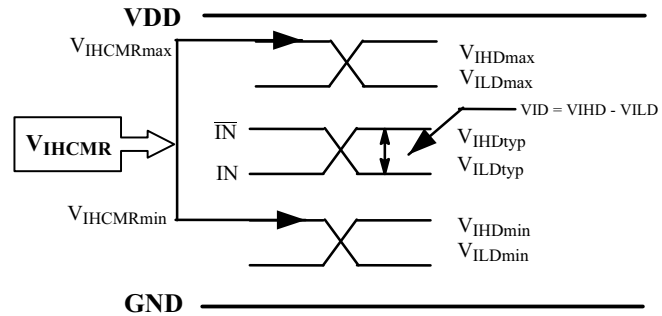


Figure 7. VIHCMR Diagram

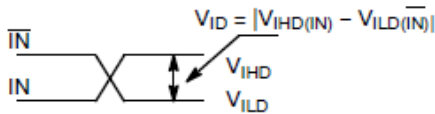


Figure 6. Differential Inputs Driven Differentially

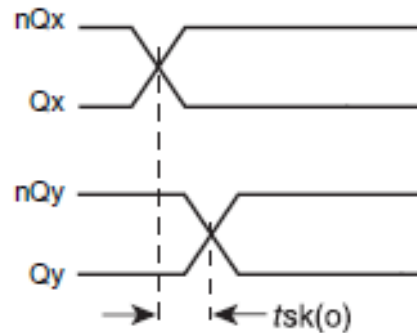


Figure 8. Output-to-Output Skew

# NB3L8504S

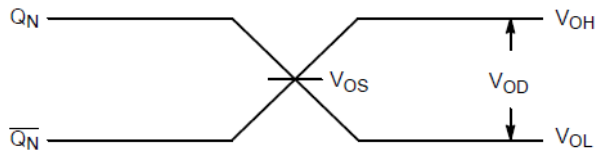


Figure 9. LVDS Output

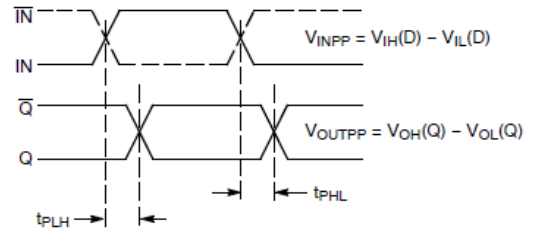


Figure 10. AC Reference Measurements

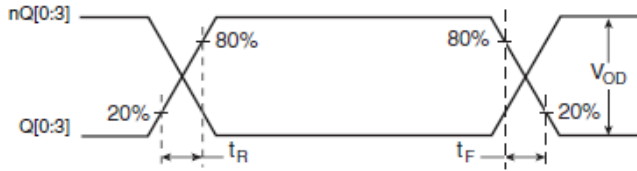


Figure 11. LVDS Output

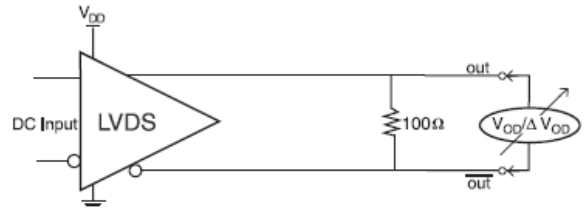


Figure 12.  $V_{OD}$  and  $\Delta V_{OD}$

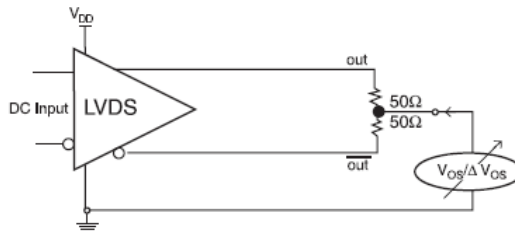


Figure 13.  $V_{OS}$  and  $\Delta V_{OS}$

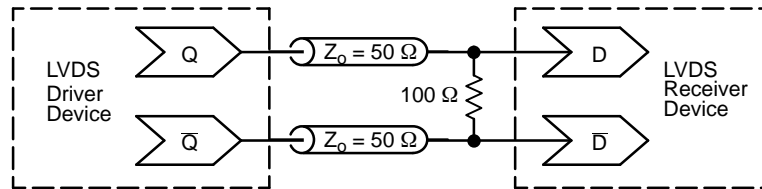


Figure 14. Typical LVDS Termination for Output Driver and Device Evaluation

# NB3L8504S

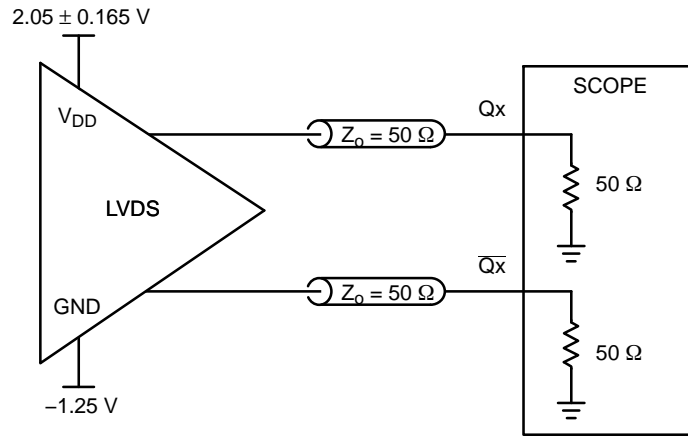


Figure 15. Typical Test Setup and Termination for Evaluation. The  $V_{DD} = 2.05 \text{ V} \pm 0.165 \text{ V}$  and GND of  $-1.25$  Split Supply Allows a Direct Connection to an Oscilloscope  $50 \Omega$  Input Module

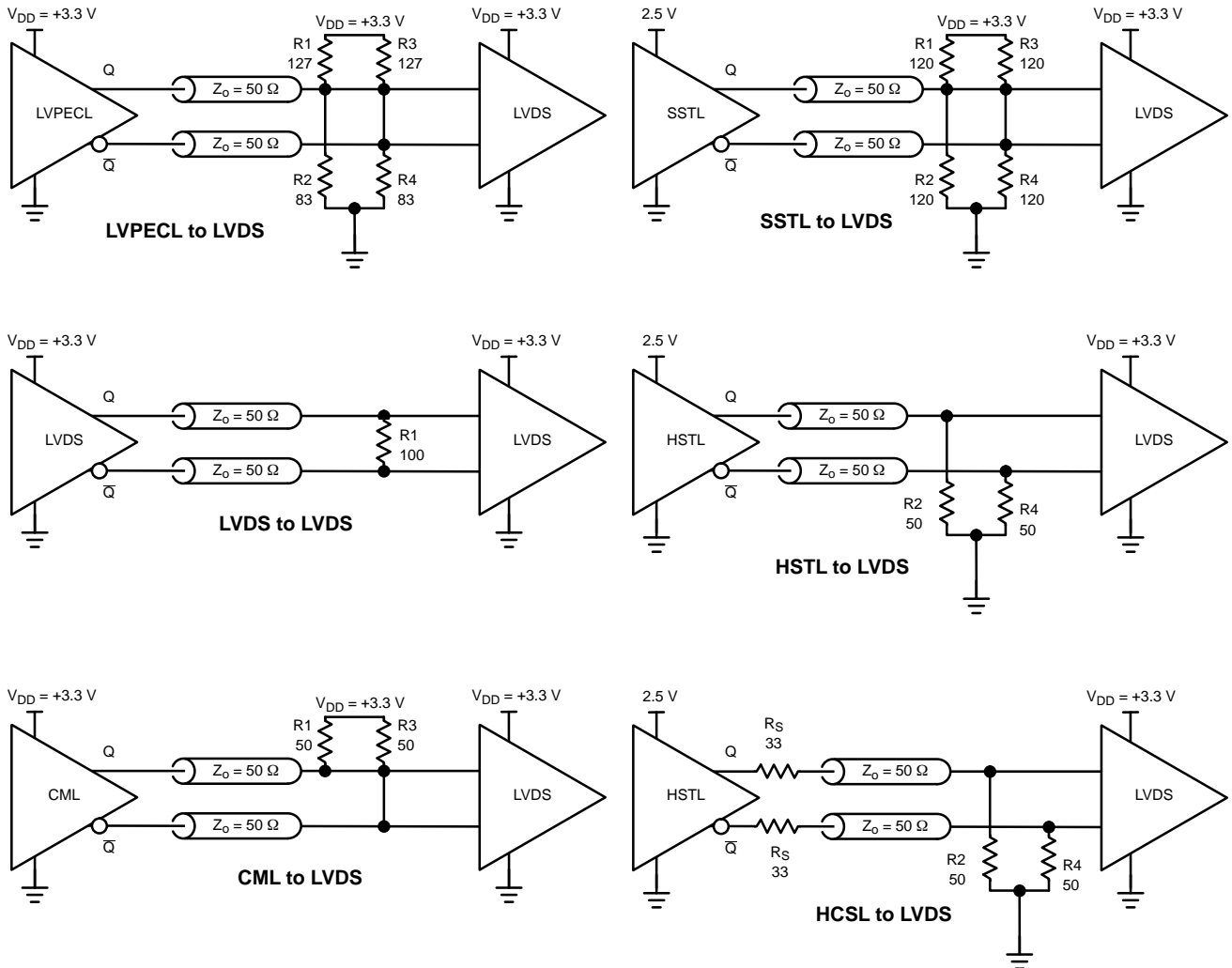
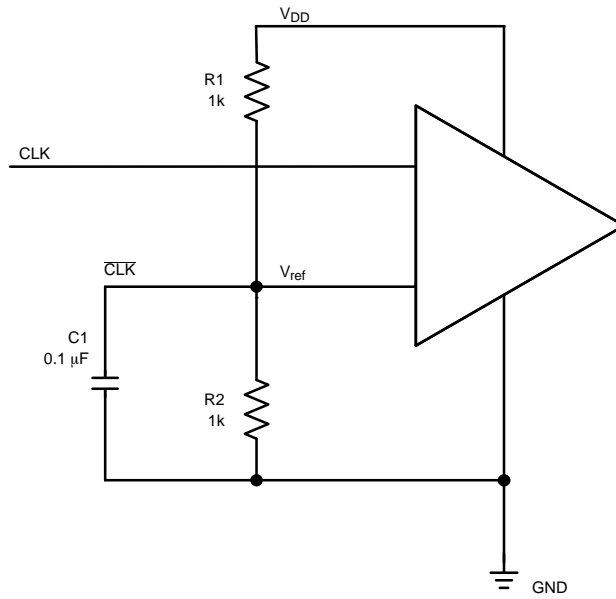


Figure 16. Differential Input Interface from LVPECL, CML, LVDS, HSTL, SSTL or HCSL



# NB3L8504S



**Figure 17. Differential Input Driven Single-ended**

**Differential Clock Input to Accept Single-ended Input**

Figure 17 shows how the CLK input can be driven by a single-ended Clock signal. C1 is connected to the  $V_{ref}$  node

as a bypass capacitor. Locate these components close the device pins. R1 and R2 must be adjusted to position  $V_{ref}$  to the center of the input swing on CLK.

**Table 7. ORDERING INFORMATION**

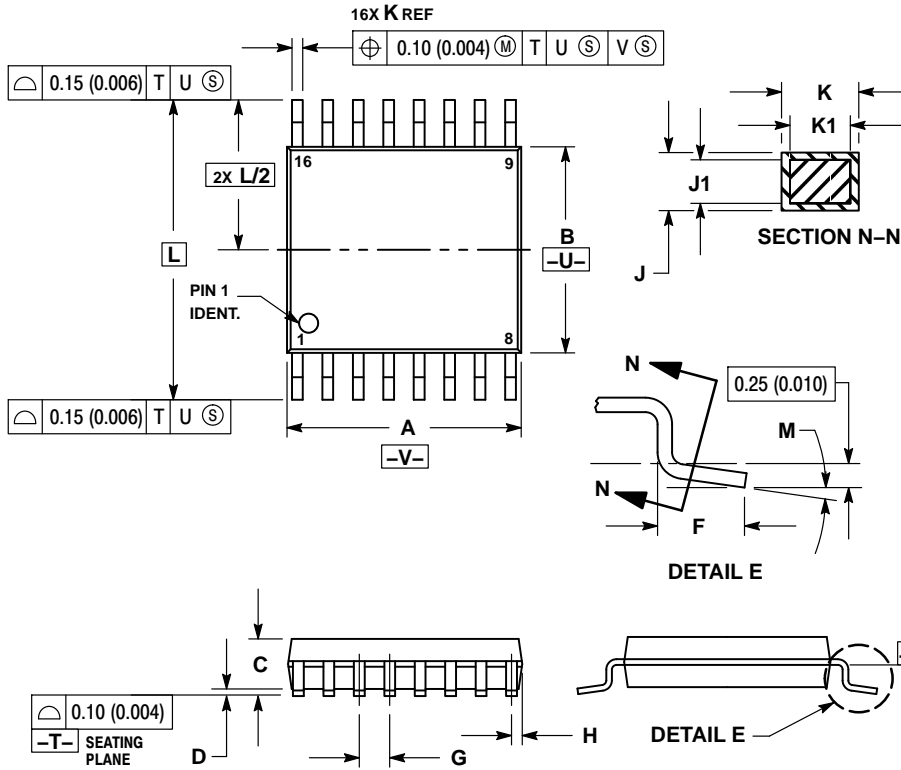
Device	Package	Shipping
NB3L8504SDTG	TSSOP-16 (Pb-Free)	96 Units / Tube
NB3L8504SDTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NB3L8504S

## PACKAGE DIMENSIONS

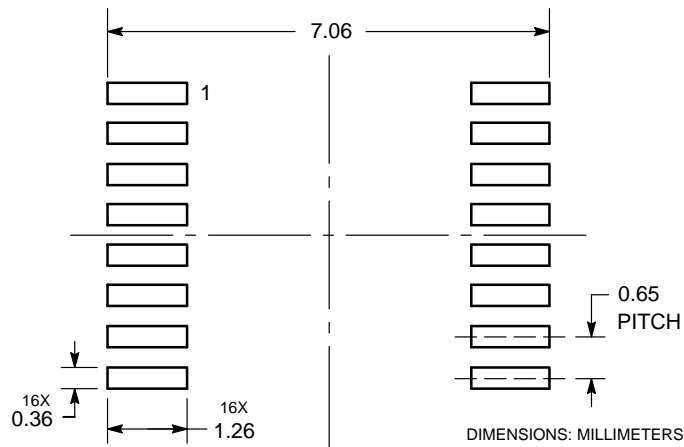
TSSOP-16  
DT SUFFIX  
CASE 948F  
ISSUE B




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative



## Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

### Наши контакты:

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331