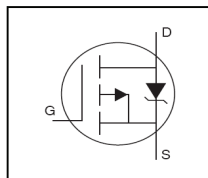
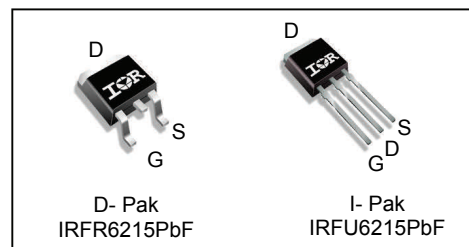


- P-Channel
- 175°C Operating Temperature
- Surface Mount (IRFR6215)
- Straight Lead (IRFU6215)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

HEXFET® Power MOSFET



V_{DSS}	-150V
R_{DS(on)}	0.295Ω
I_D	-13A



G	D	S
Gate	Drain	Source

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFU6215PbF	I-Pak	Tube	75	IRFU6215PbF
IRFR6215PbF	D-Pak	Tube	75	IRFR6215PbF
		Tape and Reel Left	3000	IRFR6215TRL PbF

Absolute Maximum Ratings

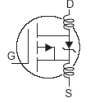
Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ -10V	-13	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ -10V	-9.0	
I _{DM}	Pulsed Drain Current ①⑥	-44	
P _D @ T _C = 25°C	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②⑥	310	mJ
I _{AR}	Avalanche Current ①⑥	-6.6	A
E _{AR}	Repetitive Avalanche Energy ①⑥	11	mJ
dv/dt	Peak Diode Recovery dv/dt③	5.0	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	1.4	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount) ⑦	—	50	
R _{θJA}	Junction-to-Ambient	—	110	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

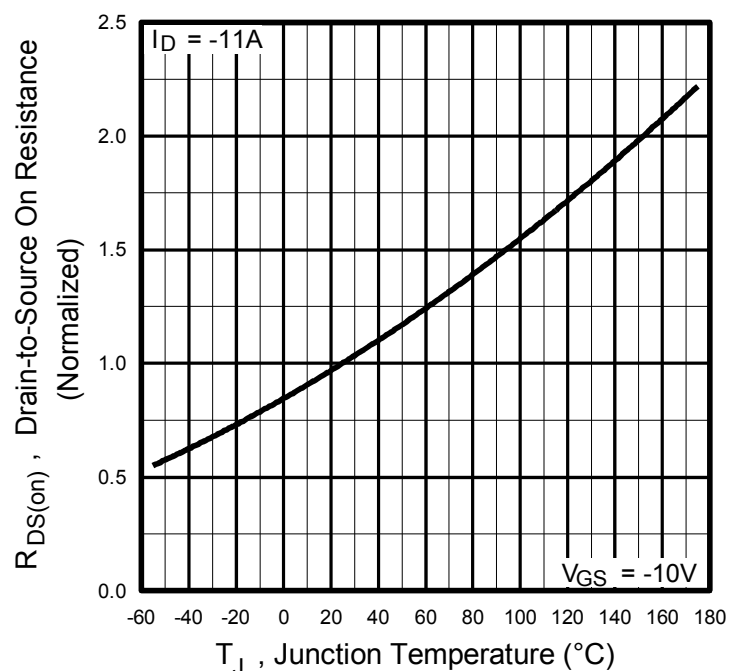
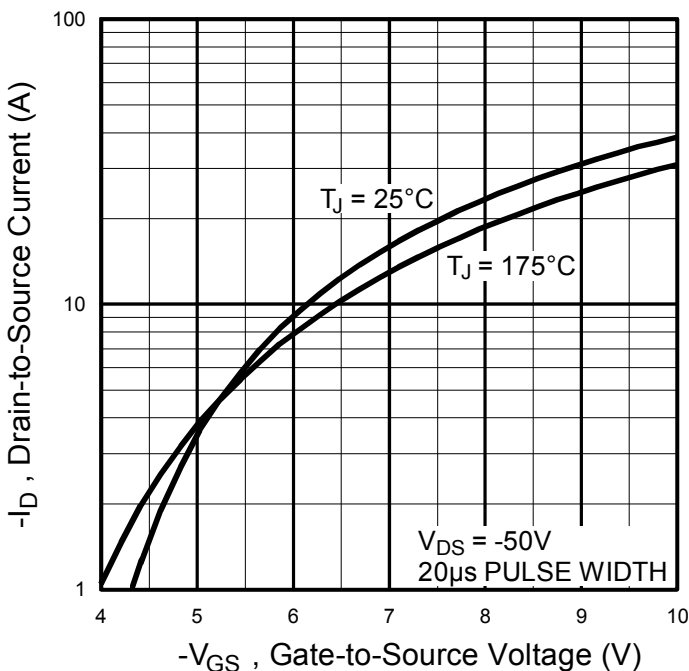
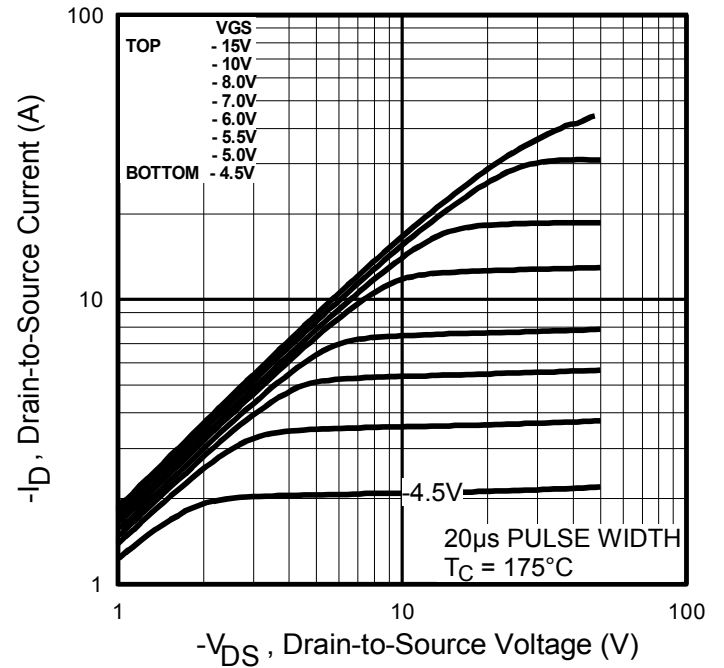
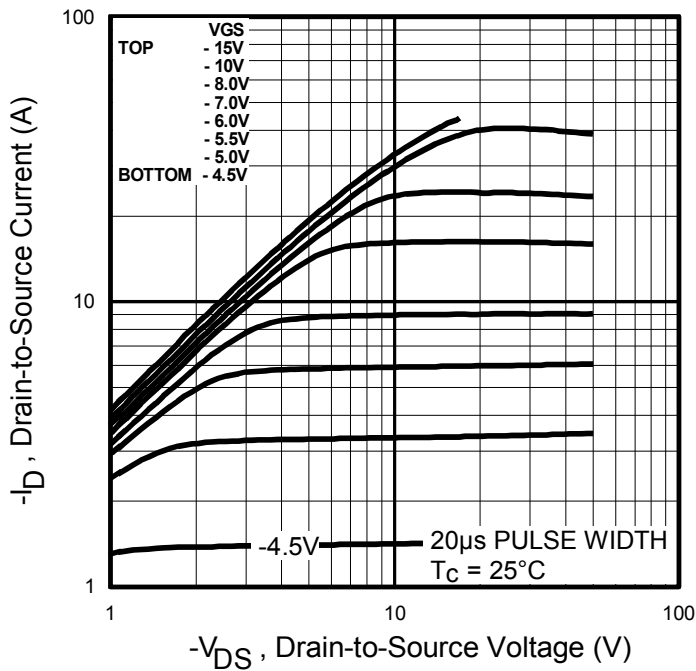
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-150	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.295	Ω	$V_{GS} = -10V, I_D = -6.6A$ ④
		—	—	0.58		$V_{GS} = -10V, I_D = -6.6A$ ④ $T_J = 150^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Trans conductance	3.6	—	—	S	$V_{DS} = -50V, I_D = -6.6A$ ⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -150V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -120V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	—	66	nC	$I_D = -6.6A$
Q_{gs}	Gate-to-Source Charge	—	—	8.1		$V_{DS} = -120V$
Q_{gd}	Gate-to-Drain Charge	—	—	35		$V_{GS} = -10V$, See Fig. 6 and 13 ④ ⑥
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = -75V$
t_r	Rise Time	—	36	—		$I_D = -6.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	53	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	37	—		$R_D = 12\Omega$, See Fig. 10 ④ ⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead ,6mm (0.25in.) from package and center of die contact⑤
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	860	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	220	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	130	—		$f = 1.0MHz$, See Fig. 5 ⑥


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-13	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ① ⑥	—	—	-44		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	$T_J = 25^\circ\text{C}, I_S = -6.6A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	160	240	ns	$T_J = 25^\circ\text{C}, I_F = -6.6A$
Q_{rr}	Reverse Recovery Charge	—	1.2	1.7	μC	$di/dt = 100A/\mu s$ ④ ⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig.11)
- ② starting $T_J = 25^\circ\text{C}$, $L = 14mH$, $R_G = 25\Omega$, $I_{AS} = -6.6A$. (See Fig.12)
- ③ $I_{SD} \leq -6.6A$, $di/dt \leq -620A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ This is applied for I-PAK, LS of D-PAK is measured between lead and center of die contact.
- ⑥ Uses IRF6215 data and test conditions.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.



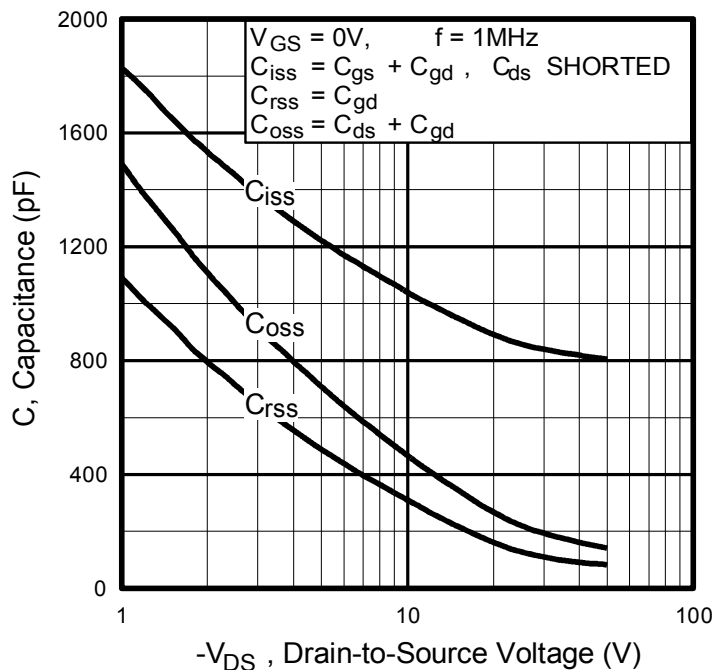


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

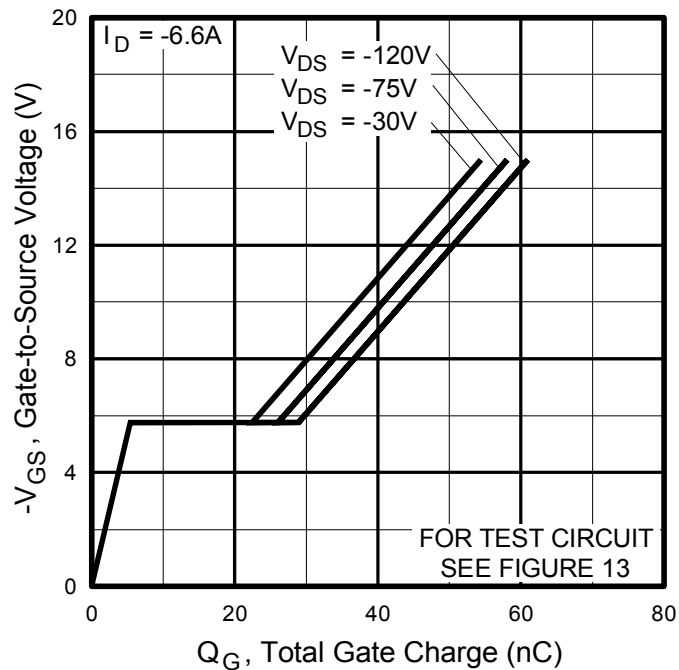


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

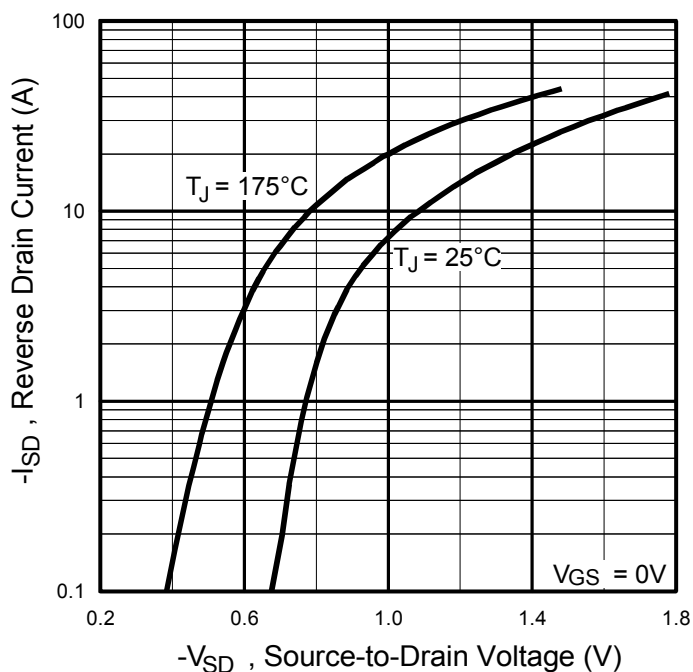


Fig. 7 Typical Source-to-Drain Diode
Forward Voltage

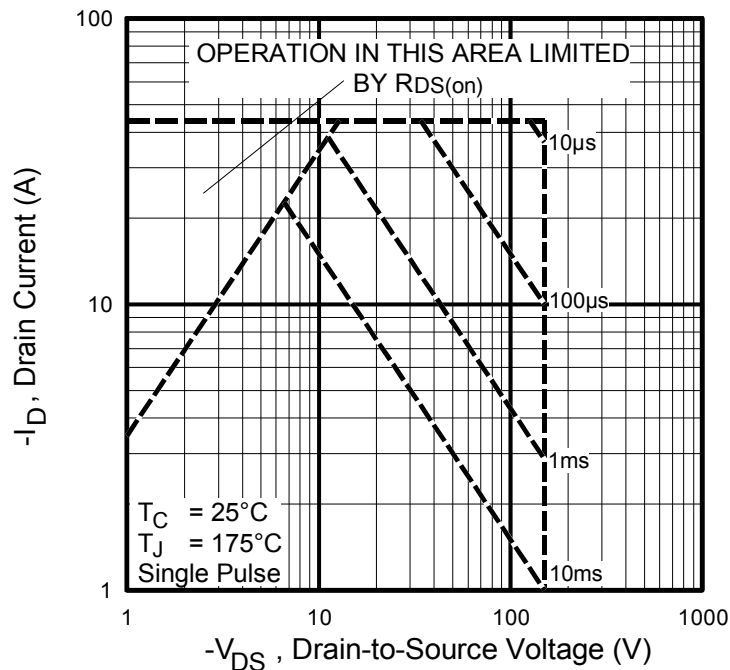
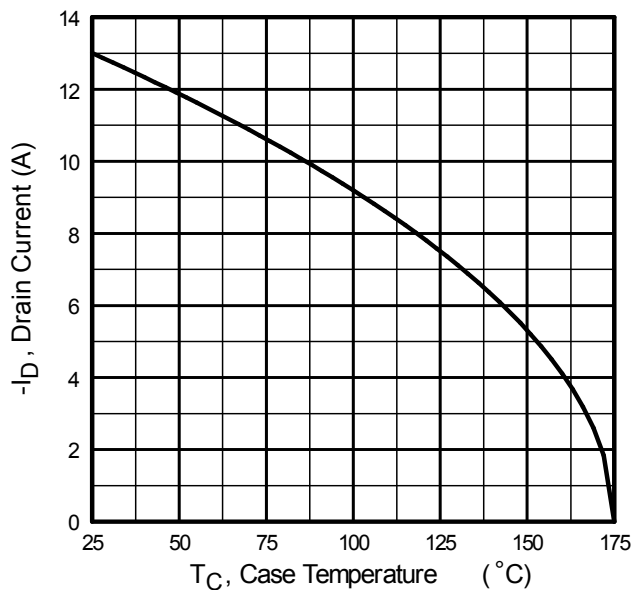
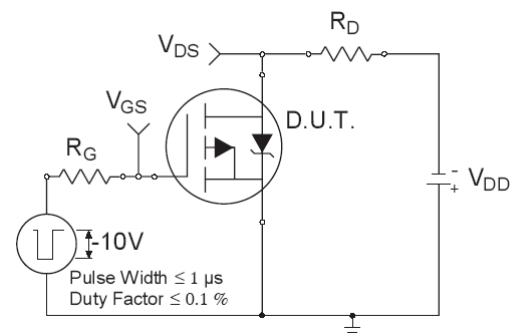
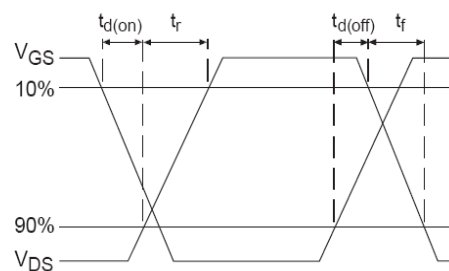
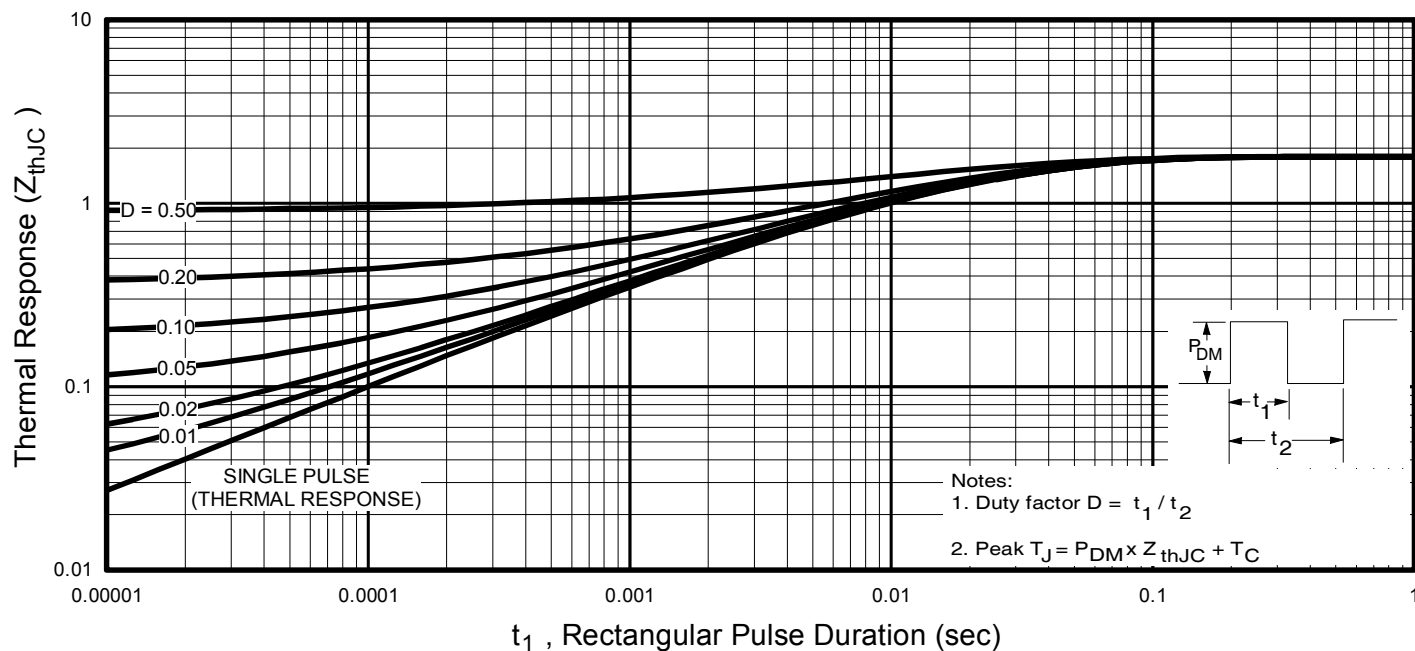


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

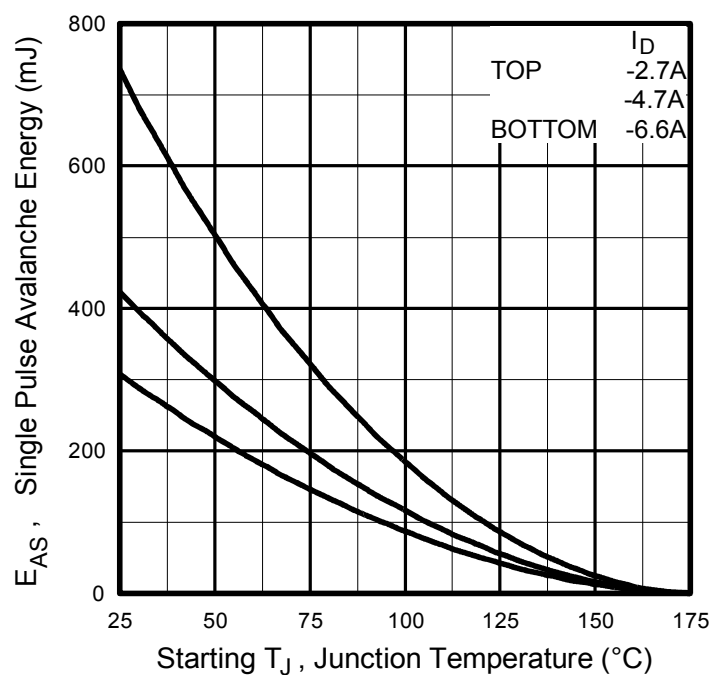
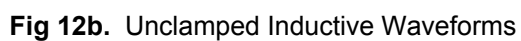
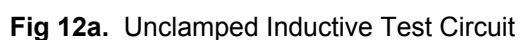


Fig 12c. Maximum Avalanche Energy vs. Drain Current

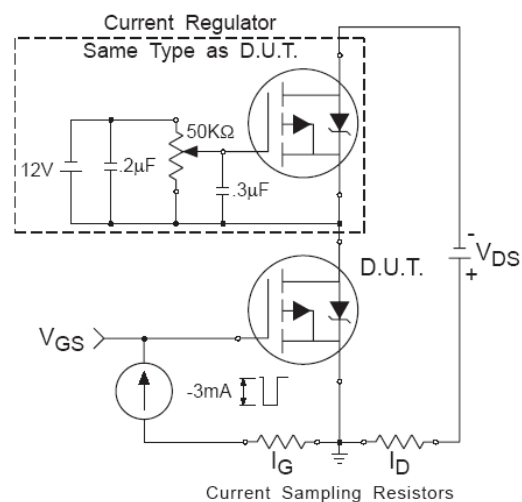
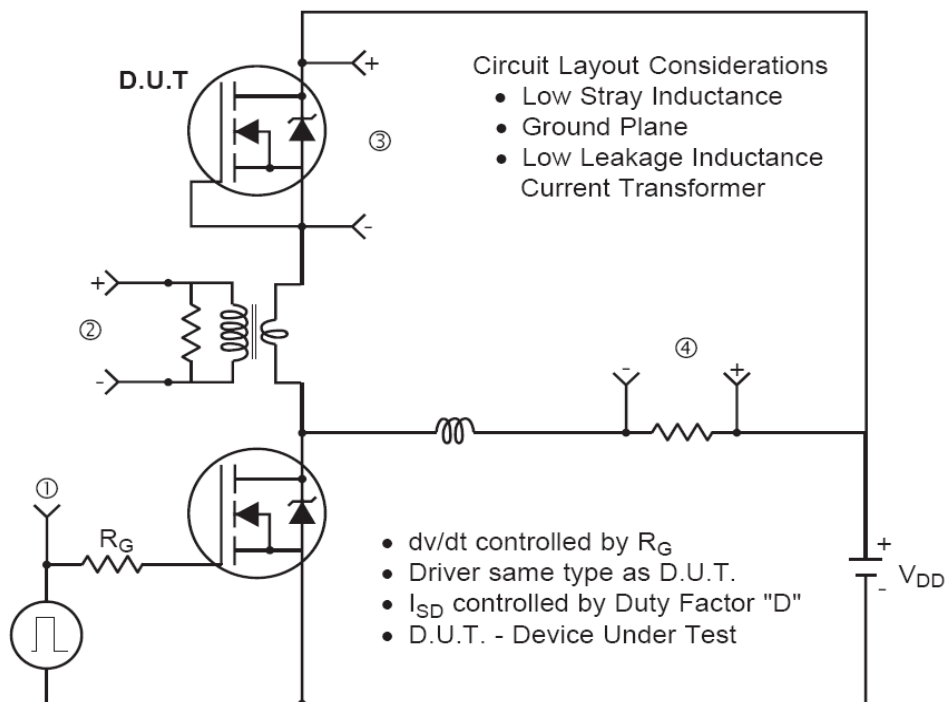


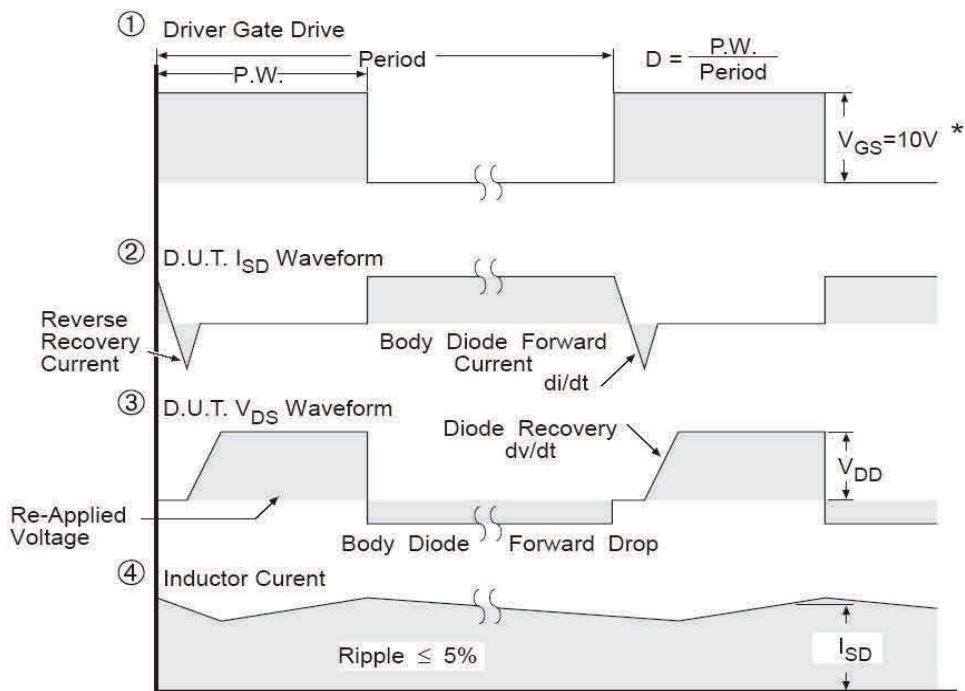
Fig 13a. Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



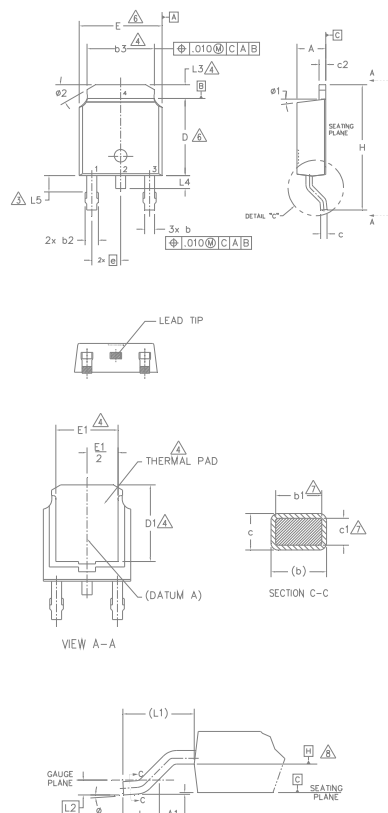
* Reverse Polarity of D.U.T for P-Channel



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	7
A1	—	0.13	—	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	4
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	7
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	
c2	0.46	0.89	.018	.035	6
D	5.97	6.22	.235	.245	
D1	5.21	—	.205	—	4
E	6.35	6.73	.250	.265	
E1	4.32	—	.170	—	6
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	4
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		3
L3	0.89	1.27	.035	.050	
L4	—	1.02	—	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

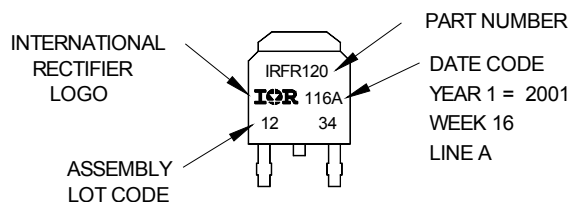
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

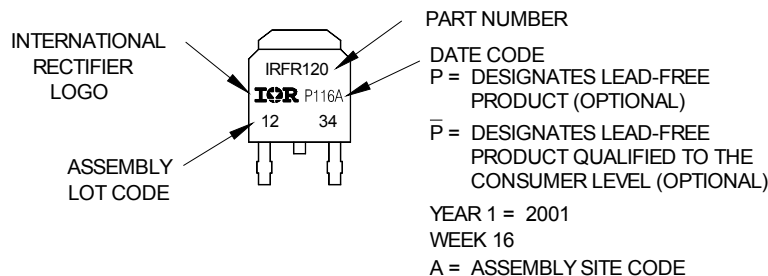
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON VW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

"P" in assembly line position indicates
"Lead-Free" qualification to the consumer-level

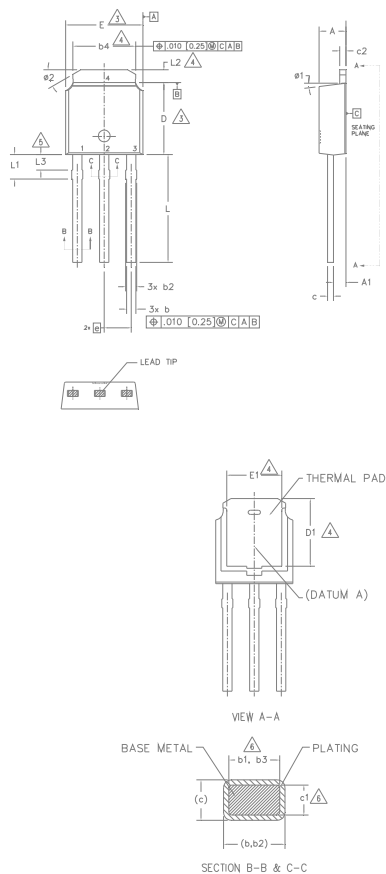


OR



Note: For the most current drawing please refer to Infineon's web site www.infineon.com

I-Pak (TO-251AA) Package Outline Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5.- LEAD DIMENSION UNCONTROLLED IN L3.
- 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	
b4	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	—	.205	—	4
E	6.35	6.73	.250	.265	3
E1	4.32	—	.170	—	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	
L3	0.89	1.52	.035	.060	4
ø1	0"	15"	0"	15"	5
ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

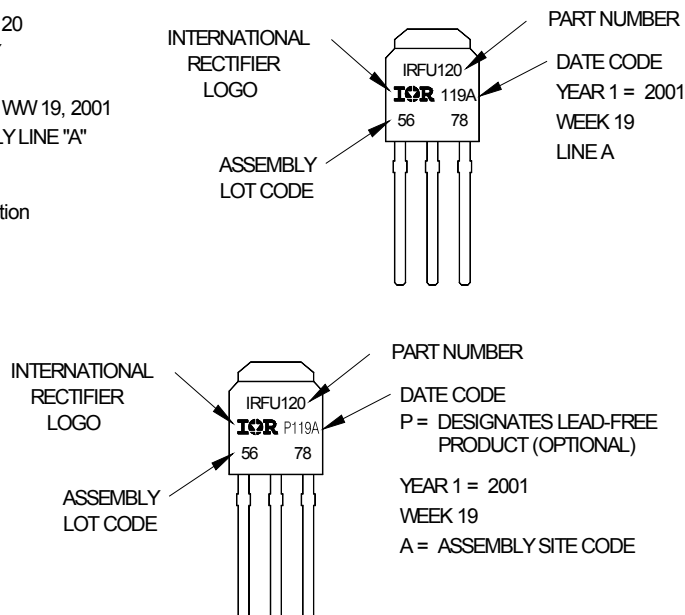
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 2001
IN THE ASSEMBLY LINE "A"

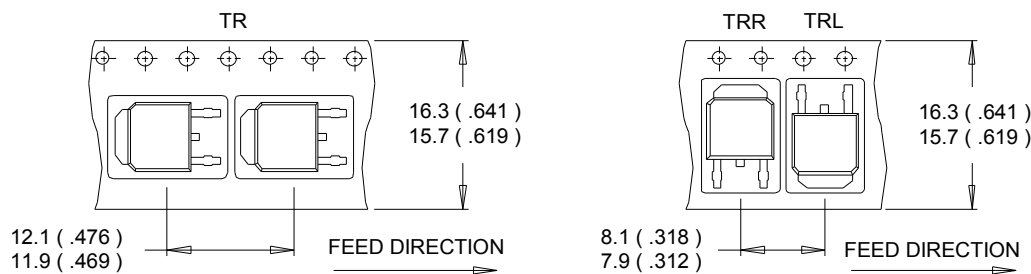
Note: "P" in assembly line position
indicates Lead-Free

OR



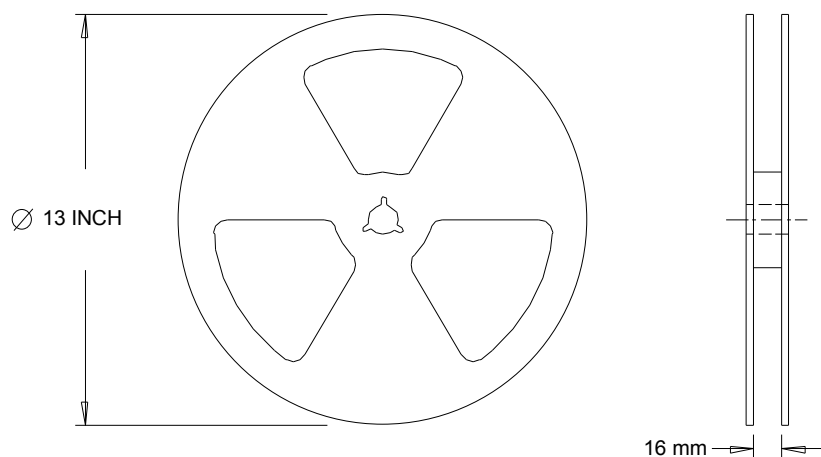
Note: For the most current drawing please refer to Infineon's web site www.infineon.com

D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	D-Pak	MSL1
	I-Pak	(per JEDEC J-STD-020D) ^{††}
RoHS Compliant	Yes	

[†] Qualification standards can be found at Infineon's web site www.infineon.com

^{††} Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
5/31/2016	- Updated datasheet with corporate template. - Added disclaimer on last page.

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Document reference

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Наши контакты:

Телефон: +7 812 627 14 35

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Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331