

### DESCRIPTION

Demonstration circuit 2512A is a gasket adapter board that allows DC718-compatible data converter eval boards to interface with FPGA boards that have an HSMC connector, such as the SoCkit Cyclone 5 SoC development board from Arrow Electronics.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2512A>

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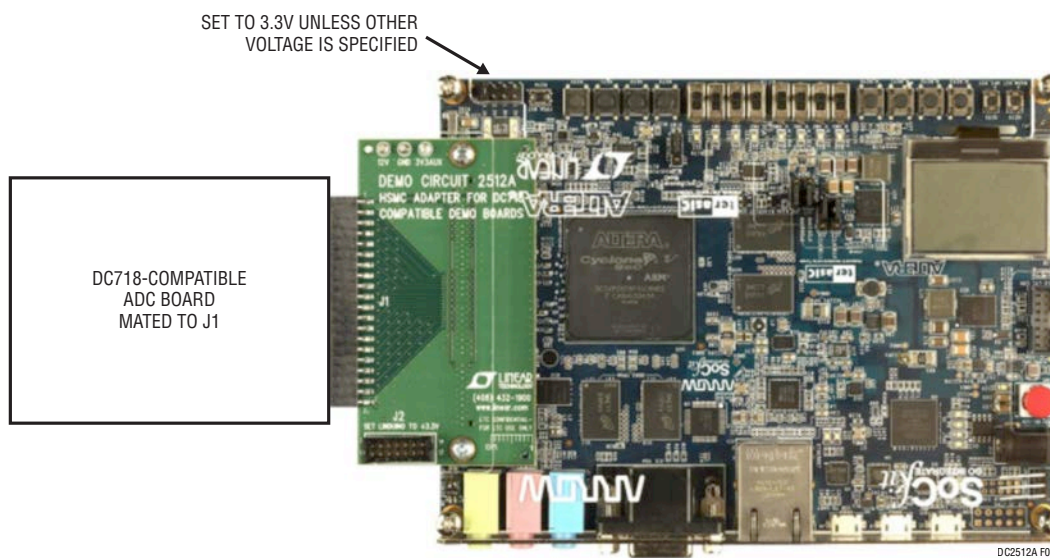


Figure 1. Basic Connections

## QUICK START PROCEDURE

DC2512A was designed to mate to the Arrow SoCkit board. DC2512A may work with other HSMC-compatible FPGA boards, but the pin connections and voltages should be verified.

Carefully mate the HSMC connector on the reverse side of the DC2512A to the SoCkit board. Use high-quality, 5mm spacers such as Harwin R30-6200514, and M3 × 12 or 4-40 × 1/2" pan-head screws.

Most FPGA loads intended for use with the DC2512A require 3.3V I/O voltage. Unless the test script or other experiment documentation indicates otherwise, set the

SoCkit's I/O voltage to 3.3V by placing the JP2 jumper on the SoCkit board in the 3.3V position (closest to the edge of the board). Mate the ADC demo board to J1 on DC2512A. Observe proper power-sequencing: the best practice is to power up the SoCkit before applying power to the ADC demo board.

A complete example of a typical evaluation setup is covered in the blog, "Data Converter Evaluation with the Arrow / Altera SoCkit FPGA board":

<http://www.linear.com/solutions/7704>

## EXTERNAL CONNECTIONS

Mapping of individual pins is shown in Table 1.

**J1:** 2x40, 0.1" (2.54mm) receptacle, compatible with ADC demo boards that are used with the DC718 capture board. Signals include conversion clock, up to 18 data lines, I<sup>2</sup>C signals for identification, and 3.3V auxiliary power.

**J2:** 2x7 QuikEval™/Linduino® connector. Not used for basic ADC evaluation. Allows the FPGA board to control

QuikEval-compatible demo boards for experiments or application development.

**J3, J4:** Test pads for additional HSMC signals.

**12V, GND, 3.3V Turret Posts:** 12V and 3.3V, supplied through the HSMC connector. May be used to power additional circuitry, refer to SoCkit documentation for maximum current. Do NOT apply power to these points.

**Table 1. Pin Mapping**

DC2512A HEADER/PIN	DC2512A SIGNAL NAME	HSMC SIGNAL NAME	SoCkit FPGA PIN NO.
		HSMC_CLK_IN0	PIN_J14
		HSMC_CLKIN_n1	PIN_AB27
		HSMC_CLKIN_n2	PIN_G15
J1, Pin 3	CCLK+	HSMC_CLKIN_p1	PIN_AA26
		HSMC_CLKIN_p2	PIN_H15
		HSMC_CLK_OUT0	PIN_AD29
J3, Pin 29		HSMC_CLKOUT_p1	PIN_E7
J3, Pin 31		HSMC_CLKOUT_n1	PIN_E6
		HSMC_CLKOUT_p2	PIN_A11
		HSMC_CLKOUT_n2	PIN_A10
J2, Pin 4	SCK/SCL	HSMC_D[0]	PIN_C10
J2, Pin 7	MOSI/SDA	HSMC_D[1]	PIN_H13
J2, Pin 6	CS#	HSMC_D[2]	PIN_C9
J2, Pin 5	MISO	HSMC_D[3]	PIN_H12
J1, Pin 1	SCL	HSMC_SCL	PIN_AA28
J1, Pin 2	SDA	HSMC_SDA	PIN_AE29
J1, Pin 37	D0	HSMC_RX_p[0]	PIN_G12

## EXTERNAL CONNECTIONS

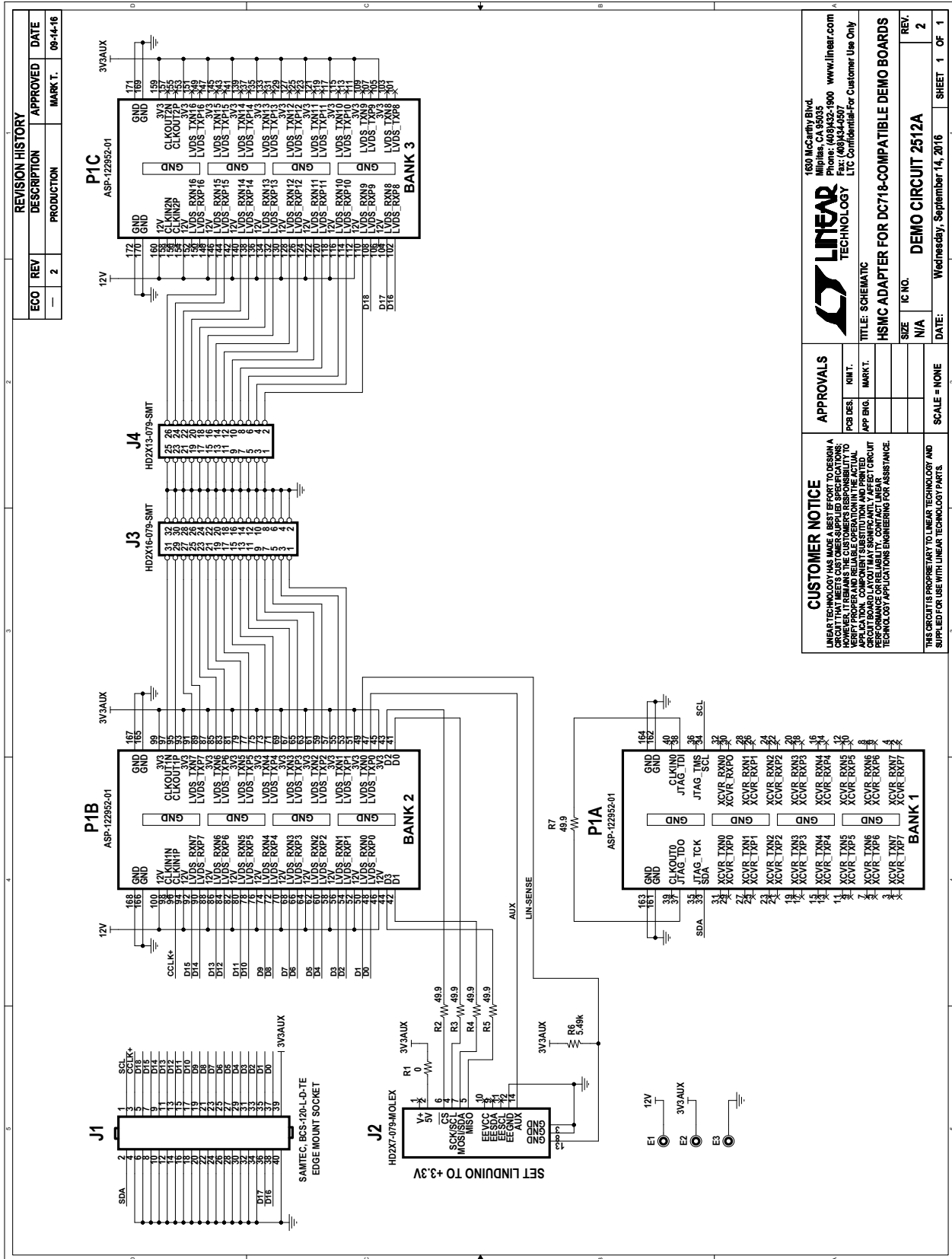
DC2512A HEADER/PIN	DC2512A SIGNAL NAME	HSMC SIGNAL NAME	SoCkit FPGA PIN NO.
J1, Pin 35	D1	HSMC_RX_n[0]	PIN_G11
J1, Pin 33	D2	HSMC_RX_p[1]	PIN_K12
J1, Pin 31	D3	HSMC_RX_n[1]	PIN_J12
J1, Pin 29	D4	HSMC_RX_p[2]	PIN_G10
J1, Pin 27	D5	HSMC_RX_n[2]	PIN_F10
J1, Pin 25	D6	HSMC_RX_p[3]	PIN_J10
J1, Pin 23	D7	HSMC_RX_n[3]	PIN_J9
J1, Pin 21	D8	HSMC_RX_p[4]	PIN_K7
J1, Pin 19	D9	HSMC_RX_n[4]	PIN_K8
J1, Pin 17	D10	HSMC_RX_p[5]	PIN_J7
J1, Pin 15	D11	HSMC_RX_n[5]	PIN_H7
J1, Pin 13	D12	HSMC_RX_p[6]	PIN_H8
J1, Pin 11	D13	HSMC_RX_n[6]	PIN_G8
J1, Pin 9	D14	HSMC_RX_p[7]	PIN_F9
J1, Pin 7	D15	HSMC_RX_n[7]	PIN_F8
J1, Pin 38	D16	HSMC_RX_p[8]	PIN_F11
J1, Pin 36	D17	HSMC_RX_n[8]	PIN_E11
J1, Pin 5	D18	HSMC_RX_p[9]	PIN_B6
J4, Pin 2		HSMC_RX_n[9]	PIN_B5
J4, Pin 4		HSMC_RX_p[10]	PIN_E9
J4, Pin 6		HSMC_RX_n[10]	PIN_D9
J4, Pin 8		HSMC_RX_p[11]	PIN_E12
J4, Pin 10		HSMC_RX_n[11]	PIN_D12
J4, Pin 12		HSMC_RX_p[12]	PIN_D11
J4, Pin 14		HSMC_RX_n[12]	PIN_D10
J4, Pin 16		HSMC_RX_p[13]	PIN_C13
J4, Pin 18		HSMC_RX_n[13]	PIN_B12
J4, Pin 20		HSMC_RX_p[14]	PIN_F13
J4, Pin 22		HSMC_RX_n[14]	PIN_E13
J4, Pin 24		HSMC_RX_p[15]	PIN_H14
J4, Pin 26		HSMC_RX_n[15]	PIN_G13
		HSMC_RX_p[16]	PIN_F15
		HSMC_RX_n[16]	PIN_F14
		HSMC_TX_p[0]	PIN_A9
		HSMC_TX_n[0]	PIN_A8
J3, Pin 1		HSMC_TX_p[1]	PIN_E8
J3, Pin 3		HSMC_TX_n[1]	PIN_D7
J3, Pin 5		HSMC_TX_p[2]	PIN_G7
J3, Pin 7		HSMC_TX_n[2]	PIN_F6
J3, Pin 9		HSMC_TX_p[3]	PIN_D6
J3, Pin 11		HSMC_TX_n[3]	PIN_C5
J3, Pin 13		HSMC_TX_p[4]	PIN_D5

# DEMO MANUAL DC2512A

## PARTS LIST

DC2512A HEADER/PIN	DC2512A SIGNAL NAME	HSMC SIGNAL NAME	SoCkit FPGA PIN NO.
J3, Pin 15		HSMC_TX _n[4]	PIN_C4
J3, Pin 17		HSMC_TX _p[5]	PIN_E3
J3, Pin 19		HSMC_TX _n[5]	PIN_E2
J3, Pin 21		HSMC_TX _p[6]	PIN_E4
J3, Pin 23		HSMC_TX _n[6]	PIN_D4
J3, Pin 25		HSMC_TX _p[7]	PIN_C3
J3, Pin 27		HSMC_TX _n[7]	PIN_B3
		HSMC_TX _p[8]	PIN_E1
		HSMC_TX _n[8]	PIN_D1
		HSMC_TX _p[9]	PIN_D2
		HSMC_TX _n[9]	PIN_C2
		HSMC_TX _p[10]	PIN_B2
		HSMC_TX _n[10]	PIN_B1
		HSMC_TX _p[11]	PIN_A4
		HSMC_TX _n[11]	PIN_A3
		HSMC_TX _p[12]	PIN_A6
		HSMC_TX _n[12]	PIN_A5
		HSMC_TX _p[13]	PIN_C7
		HSMC_TX _n[13]	PIN_B7
		HSMC_TX _p[14]	PIN_C8
		HSMC_TX _n[14]	PIN_B8
		HSMC_TX _p[15]	PIN_C12
		HSMC_TX _n[15]	PIN_B11
		HSMC_TX _p[16]	PIN_B13
		HSMC_TX _n[16]	PIN_A13

SCHEMATIC DIAGRAM



REVISION HISTORY			
ECO	REV	DESCRIPTION	APPROVED DATE
—	2	PRODUCTION	MARK T. 09-14-16

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**LINEAR TECHNOLOGY**

TITLE: SCHEMATIC  
HSMC ADAPTER FOR DC718-COMPATIBLE DEMO BOARDS

APPROVALS

PCB DES.	REV. T.	MARK T.
APP ENG.	MARK T.	

SIZE: N/A  
IC NO.: DEMO CIRCUIT 2512A  
DATE: Wednesday, September 14, 2016  
SHEET: 1 OF 1

REVISION: 2

SCALE: NONE

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# DEMO MANUAL DC2512A

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