

Datasheet



# Capacitive Controller ICs Capacitive Switch Controller ICs



3.0 to 3.6V (Typ.)

-25 to 85°C (Typ.)

3.5mA (Typ.

without load)

16msec (Typ.)

# BU21072MUV / BU21078MUV

# General Description

BU21072MUV/BU21078MUV is a capacitive sensor controller for switch operation.

In addition to a regular simple switch, support matrix switches which are arranged in the matrix sensors. If external noise and temperature drift are detected, the automatic self-calibration is operated. Include LED controller with PWM function.

#### Features

- 10 capacitive sensor ports. (BU21072MUV)
  12 capacitive sensor ports. (BU21078MUV)
- Supported Matrix switches.
  Maximum 16 switches. (BU21072MUV) Maximum 36 switches. (BU21078MUV)
- Automatic self-calibration.
- Held touch detection.
- LED controller with PWM function.
- Inform the detected result of switch operation by interrupt.
- 2-wire serial bus interface.
- 3.3V single power supply.
- Built-in Power-On-Reset and Oscillator.

#### Applications

- Appliance that require multiple switches.
- Information appliance as printer.
- AV appliance as digital TV and HDD recorder.
- Notebook PC.

#### Typical Application Circuit

## Key Specifications

- Input voltage range
- Operating temperature range
  - Operating current
- Scan rate
- Scannale

BU21078MUV :

#### Packages

BU21072MUV : VQFN024V4040

VQFN028V5050

- 4.00 mm×4.00 mm×1.00 mm
- 5.00 mm×5.00 mm×1.00 mm





VQFN024V4040

VQFN028V5050



Fig.1 Typical Application Circuit

oProduct structure : Silicon monolithic integrated circuit oThis product is not designed protection against radioactive rays

#### Overview

BU21072MUV/BU21078MUV is a capacitive sensor controller for switch operation.

Included blocks are AFE (Analog Front End) detecting capacitance, A/D converter, MPU, LED ports with PWM function, 2-wire serial bus interface compatible with I2C protocol, power-on-reset, oscillator. Operate with a 3.0 to 3.6V single power supply.

The results that detected switch operations (Touch/Release/Hold) are held to each register. An interrupt is send from INT port to the host when a register is updated by detected operations. If external noise and temperature drift are detected, run automatic self-calibration. Without periodical polling, offer the reduction of the host load.

LED ports are able to be applied PWM function. PWM function offers fade-in / fade-out brightness control.

Simple switch

One sensor is assigned to one switch. Each simple switch has the registers of detected Touch/Release/Hold operations. Simple switches support to multi-detect Touch/Release/Hold. Unused simple switches are maskable.

Matrix switches

The cross points of the sensors which are arranged in a matrix are able to assigned to individual switches. Each matrix switch has the registers of detected Touch/Release/Hold operations. Matrix switches do not support to multi-detect Touch/Release/Hold. Not used matrix switches are maskable. BU21072MUV supports 16 matrix switches configured by 4x4 sensors, and BU21078MUV supports 36 matrix switches configured by 6x6 sensors.

•Automatic self-calibration

BU21072MUV/BU21078MUV has observed the situation surrounding the sensor based on the detection result. If external noise and temperature drift are detected, the automatic self-calibration is operated for the stable detection result.

•LED controller with PWM timers

LED controller is High active. Each LED port is assigned to a choice of four PWM timers. If the situation surrounding the sensor is changed by the switching LED, it is useable that calibration is operated by sending LED control command.

Host interface

BU21072MUV/BU21078MUV is slave device for the host device. 2-wire serial bus is compatible with I2C protocol. Slave Address : 0x5C(BU21072MUV) , 0x5D(BU21078MUV)

# Pin Configurations



Fig.2 Pin configuration of BU21072MUV



Fig.3 Pin configuration of BU21078MUV

## Pin Descriptions

Number		Name	Туре	Function	Note	Power	Initial	l/O Equivalence
BU21072MUV	BU21078MUV						Condition	Circuit
-	1	SIN12	Ain	Capacitive Touch Sensor 12		AVDD	Hi-Z	Fig.4
2	2	SIN2	Ain	Capacitive Touch Sensor 2		AVDD	Hi-Z	Fig.4
-	3	SIN11	Ain	Capacitive Touch Sensor11		AVDD	Hi-Z	Fig.4
3	4	SIN1	Ain	Capacitive Touch Sensor 1		AVDD	Hi-Z	Fig.4
4	5	SIN0	Ain	Capacitive Touch Sensor 0		AVDD	Hi-Z	Fig.4
5	6	AVDD	Power	LDO output for analog blocks		VDD	-	-
6	7	VDD	Power	Power		-	-	-
7	8	DVDD	Power	LDO output for digital blocks		VDD	-	-
8	9	VSS	GND	Ground		-	-	-
9	10	TEST	In	Test input	Must be tied to Ground	VDD	-	Fig.5
10	11	SCL	InOut	Host I/F clock input		VDD	Hi-Z	Fig.5
11	12	SDA	InOut	Bi-directional Host I/F Data		VDD	Hi-Z	Fig.5
12	13	INT	Out	Interrupt output	Active High Interrupt	VDD	"L"	Fig.6
13	14	LED0	Out	LED control with PWM output 0	Active High	VDD	Hi-Z	Fig.6
14	15	LED1	Out	LED control with PWM output 1	Active High	VDD	Hi-Z	Fig.6
15	16	LED2	Out	LED control with PWM output 2	Active High	VDD	Hi-Z	Fig.6
16	17	LED3	Out	LED control with PWM output 3	Active High	VDD	Hi-Z	Fig.6
17	18	LED4	Out	LED control with PWM output 4	Active High	VDD	Hi-Z	Fig.6
18	19	LED5	Out	LED control with PWM output 5	Active High	VDD	Hi-Z	Fig.6
-	20	LED6	Out	LED control with PWM output 6	Active High	VDD	"L"	Fig.6
-	21	LED7	Out	LED control with PWM output 7	Active High	VDD	"L"	Fig.6
19	-	SIN9	Ain	Capacitive Touch Sensor 9		AVDD	Hi-Z	Fig.4
20	-	SIN8	Ain	Capacitive Touch Sensor 8		AVDD	Hi-Z	Fig.4
21	22	SIN7	Ain	Capacitive Touch Sensor 7		AVDD	Hi-Z	Fig.4
22	23	SIN6	Ain	Capacitive Touch Sensor 6		AVDD	Hi-Z	Fig.4
-	24	SIN13	Ain	Capacitive Touch Sensor 13		AVDD	Hi-Z	Fig.4
23	25	SIN5	Ain	Capacitive Touch Sensor 5		AVDD	Hi-Z	Fig.4
-	26	SIN14	Ain	Capacitive Touch Sensor 14		AVDD	Hi-Z	Fig.4
24	27	SIN4	Ain	Capacitive Touch Sensor 4		AVDD	Hi-Z	Fig.4
1	28	SIN3	Ain	Capacitive Touch Sensor 3		AVDD	Hi-Z	Fig.4

Initial Condition is at that power-on-reset is active.

# ●I/O Equivalence Circuits



Fig.4 I/O equivalence circuit (a)







Fig.6 I/O equivalence circuit (c)

## Block Diagram



Fig.7 Block Diagram

#### Description of Blocks

•Sensor AFE, C/V Converter

Convert from capacitance to voltage following the order of sensors.

•A/D

Convert from voltage to the detected result the digital value.

- •LDO28 2.73V output LDO for Sensor AFE, C/V Converter and A/D.
- •LDO15
- 1.5V output LDO for OSC and digital blocks.
- •OSC

Ring oscillator as the system clock.

POR

Power-On-Reset monitoring VDD as the system reset.

MPU

Based on the detection result, detect switch operations (Touch/Release/Hold) and run Auto-calibration. Inform by the INT port to the host about that the switch operations are detected. Control LED ports by the commands from the host.

•PROM

Program ROM for the included MPU.

- •WRAM
  - Work RAM for the included MPU.
- •HOST I/F

2-wire serial bus interface compatible with I2C protocol.

•AFE\_CNT

Sequencer of Sensor AFE, C/V converter and A/D.

•PWM\_CNT

PWM timers for the LED ports.

•LEDDRV

LED port drivers. •WDTR

Watchdog Timer Reset. It releases the system reset after 1 sec from that MPU cannot clear WDTR. (If MPU cannot clear WDTR, MPU is hang-up.)

# ●Absolute Maximum Ratings (Ta = 25°C)

Param	eter	Symbol	Rating	Unit
Power supply volta	ge	VDD	-0.5 to 7.0	V
Input voltage		V <sub>IN</sub>	-0.5 to VDD + 0.3	V
Storage temperatu	re range	T <sub>stg</sub>	-55 to 125	°C
Dower dissinction	BU21072MUV	Р	272 *1	m)//
Power dissipation	BU21078MUV	Pd	304 *2	mW
Maximum junction	temperature	T <sub>jmax</sub>	125	°C

\*1 \*2 Derated by 2.72mW/°C over 25°C. (IC only). Derated by 3.04mW/°C over 25°C. (IC only).

# Recommended Operating Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	VDD	3.0 to 3.6	V
Operating temperature range	T <sub>opr</sub>	-20 to 85	°C

# ●Electrical Characteristics (Ta = 25°C, VDD = 3.3V, VSS = 0V)

Parameter	Symbol	Rating			Unit	Condition	
	Symbol	Min.	Тур.	Max.	Unit	Condition	
Input High voltage	V <sub>IH</sub>	VDD x 0.7	-	VDD + 0.3	V		
Input Low voltage	VIL	VSS - 0.3	-	VDD x 0.3	V		
Output High voltage	V <sub>OH</sub>	VDD - 0.5	-	VDD	V	I <sub>OH</sub> = -4mA	
Output Low voltage	V <sub>OL</sub>	VSS	-	VSS + 0.5	V	I <sub>OL</sub> = 4mA	
Oscillator clock frequency	f <sub>osc</sub>	45	50	55	MHz		
DVDD LDO output voltage	V <sub>DVDD</sub>	1.35	1.50	1.65	V		
AVDD LDO output voltage	VAVDD	2.63	2.73	2.83	V		
Power-on-reset release voltage		2.25	-	2.55	V		
Power-on-reset detect voltage		2.10	-	2.40	V		
Operating current	I <sub>DD</sub>	-	3.5	-	mA	Without load of sensors.	

# Timing Charts

Host interface

2-wire serial bus. Compatible with I2C protocol. Supports slave mode only. Slave Address = 0x5C (BU21072MUV) Slave Address = 0x5D (BU21078MUV) Supports Standard-mode (data transfer rate of 100 kbit/s) and Fast-mode (data transfer rate of 400 kbit/s). Supports sequential read.



Fig.8 2-wire serial bus data format



Fig.9	2-wire serial	bus timing chart
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Parameter	Symbol	Standard-mode		Fast-mode		Linit
Parameter	Symbol	MIN	MAX	MIN	MAX	Unit
Hold time (repeated) START condition	f <sub>SCL</sub>	0	100	0	400	kHz
LOW period of the SCL clock	t <sub>HD;STA</sub>	4.0	-	0.6	-	usec
HIGH period of the SCL clock	t <sub>LOW</sub>	4.7	-	1.3	-	usec
Data hold time	t <sub>HIGH</sub>	4.0	-	0.6	-	usec
Data set-up time	t <sub>HD;DAT</sub>	0.1	3.45	0.1	0.9	usec
Set-up time for a repeated START condition	t <sub>su;dat</sub>	0.25	-	0.1	-	usec
Set-up time for STOP condition	t <sub>SU;STA</sub>	4.7	-	0.6	-	usec
Bus free time between a STOP and START condition	t <sub>su;sтo</sub>	4.0	-	0.6	-	usec
Hold time (repeated) START condition	t <sub>BUF</sub>	4.7	-	1.3	-	usec

# BU21072MUV / BU21078MUV

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#### Scan rate

After scan each sensor in time series, MPU convert to the switch operations from the detected results. The number of sensor ports is difference between BU21072MUV and BU21078MUV, but one scan rate is the same. One scan rate is about 16msec at typical.



#### Fig.11 Timing chart of scan rate

#### •Power on sequence

Power supply pin is VDD only. AVDD and DVDD are supplied by each LDO included BU21072/78MUV, so that have no priority about power on sequence. When VDD reaches to the effective voltage, power-on-reset which initializes the digital block is released.

Power-On-Reset monitoring VDD, so it should be set to proper value of decoupling capacitor and VDD rise time, so as to rise to the proper voltage (DVDD $\rightarrow$ VDD).



Fig.12 Arrangement of external decoupling capacitors

When power-on-reset is released, MPU starts initial sequence. Inform by the INT port to the host that the initialization has been completed. After verify that the initialization has completed, the host will need to resend the command to the IC. In the case that WDTR is released as well, MPU starts initial sequence. If WDTR has released, all registers have been initialized. So the host will need to resend the command to the IC.





Fig.13 Timing chart of power on sequence

# •Application Examples

BU21072MUV /BU21078MUV offer two method of switch. One is simple switch, another is matrix switch. The number of the maximum matrix switches is 16 by BU21072MUV, and 36 by BU21078MUV.





Fig.15 Application example 1 (8-simple switches, 3-LEDs with BU21072MUV)



Fig.16 Application example 2 (36-matrix switches, 4-LEDs with BU21078MUV)



Fig.17 Application example 3 (16-matrix switches, 2-simple switches, 6-LEDs with BU21072MUV)

## Operational Notes

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

#### (7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

## (10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

#### (11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

#### (12) Rush current

The IC with some power supplies has a capable of rush current due to procedure and delay at power-on. Pay attention to the capacitance of the coupling capacitors and the wiring pattern width and routing of the power supply and the GND lines.

## Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

# •Ordering Information



#### Line-up

Sensor ports	Package	Orderable Part Number
10ch	VQFN024V4040	BU21072MUV-E2
12ch	VQFN028V5050	BU21078MUV-E2

# Physical Dimension Tape and Reel Information

VQFN024V4040



# VQFN028V5050



#### • Marking Diagrams (TOP VIEW)



#### Revision History

Date	Revision	Changes
12.Mar.2012	001	New Release

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