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# FDMS4D4N08C

## N-Channel Shielded Gate PowerTrench® MOSFET 80 V, 123 A, 4.3 mΩ

### Features

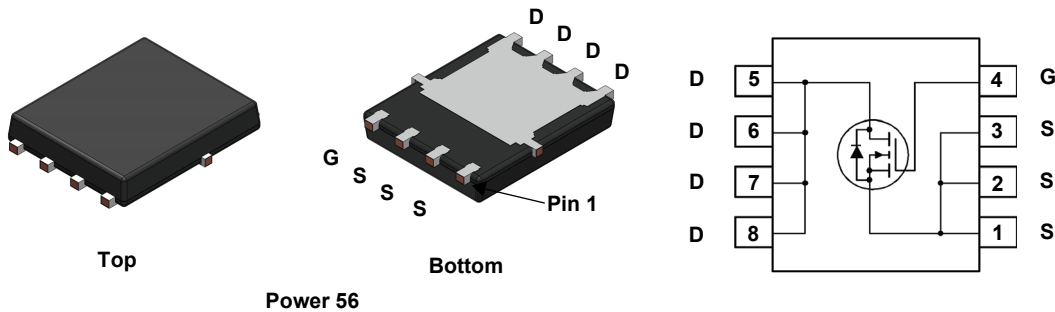
- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 4.3 mΩ at  $V_{GS} = 10$  V,  $I_D = 44$  A
- Max  $r_{DS(on)}$  = 10.4 mΩ at  $V_{GS} = 6$  V,  $I_D = 22$  A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

### General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

### Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



Power 56

### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	80	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 5)	123	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	78	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	17	
	-Pulsed (Note 4)	498	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	486	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	125	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS4D4N08C	FDMS4D4N08C	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		63		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}$ , $V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$ , $V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-8.2		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 44\ \text{A}$		3.7	4.3	m $\Omega$
		$V_{GS} = 6\ \text{V}$ , $I_D = 22\ \text{A}$		5.7	10.4	
		$V_{GS} = 10\ \text{V}$ , $I_D = 44\ \text{A}$ , $T_J = 125^\circ\text{C}$		5.9	7.2	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\ \text{V}$ , $I_D = 44\ \text{A}$		98		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 40\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$		2920	4090	pF
$C_{oss}$	Output Capacitance			1045	1465	pF
$C_{rss}$	Reverse Transfer Capacitance			35	50	pF
$R_g$	Gate Resistance		0.1	1.3	2.5	$\Omega$

### Switching Characteristics

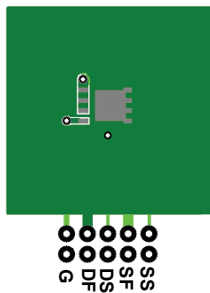
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\ \text{V}$ , $I_D = 44\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GEN} = 6\ \Omega$		17	31	ns
$t_r$	Rise Time			7	15	ns
$t_{d(off)}$	Turn-Off Delay Time			25	40	ns
$t_f$	Fall Time			5	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 40\ \text{V}$ , $I_D = 44\ \text{A}$	40	56	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $6\ \text{V}$		25	35	nC
$Q_{gs}$	Gate to Source Charge			13		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			8		nC
$Q_{oss}$	Output Charge	$V_{DD} = 40\ \text{V}$ , $V_{GS} = 0\ \text{V}$		60		nC
$Q_{sync}$	Total Gate Charge Sync.	$V_{DS} = 0\ \text{V}$ , $I_D = 44\ \text{A}$		35		nC

### Drain-Source Diode Characteristics

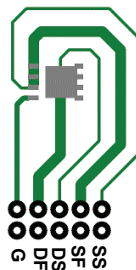
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = 2.1\ \text{A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\ \text{V}$ , $I_S = 44\ \text{A}$ (Note 2)		0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 22\ \text{A}$ , $di/dt = 300\ \text{A}/\mu\text{s}$		26	42	ns
$Q_{rr}$	Reverse Recovery Charge			44	71	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 22\ \text{A}$ , $di/dt = 1000\ \text{A}/\mu\text{s}$		20	32	ns
$Q_{rr}$	Reverse Recovery Charge			106	169	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\ \text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\ \text{in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



50  $^\circ\text{C}/\text{W}$  when mounted on a  $1\ \text{in}^2$  pad of 2 oz copper



125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 486 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3\ \text{mH}$ ,  $I_{AS} = 18\ \text{A}$ ,  $V_{DD} = 80\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ . 100% test at  $L = 0.1\ \text{mH}$ ,  $I_{AS} = 51\ \text{A}$ .

4. Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

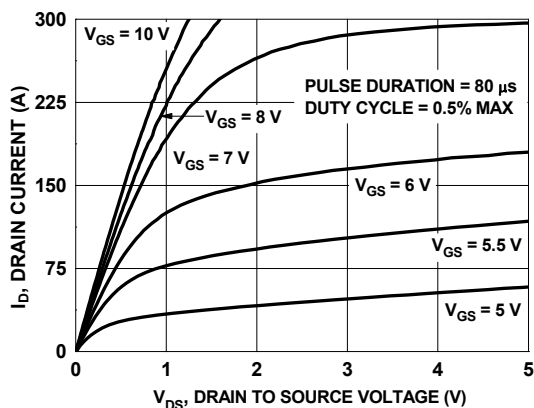


Figure 1. On Region Characteristics

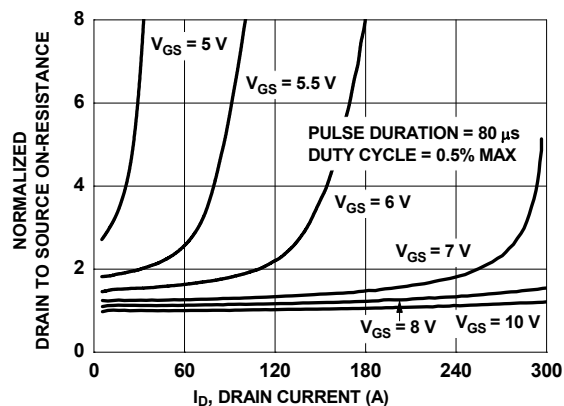


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

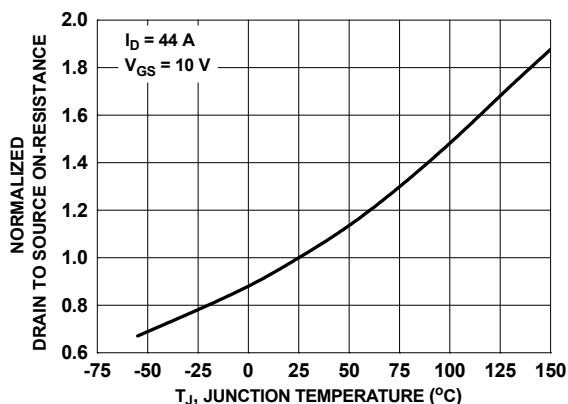


Figure 3. Normalized On Resistance vs. Junction Temperature

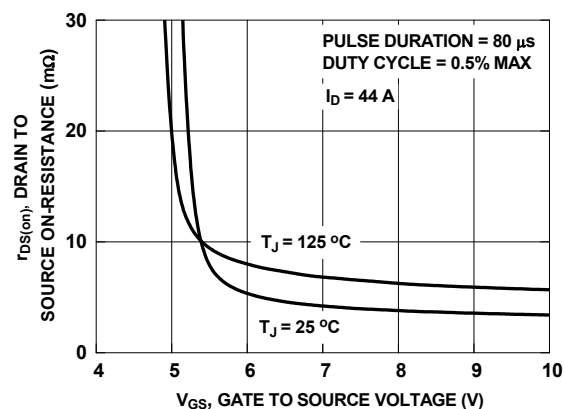


Figure 4. On-Resistance vs. Gate to Source Voltage

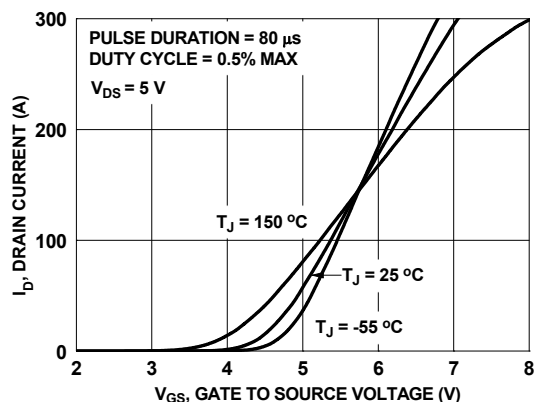


Figure 5. Transfer Characteristics

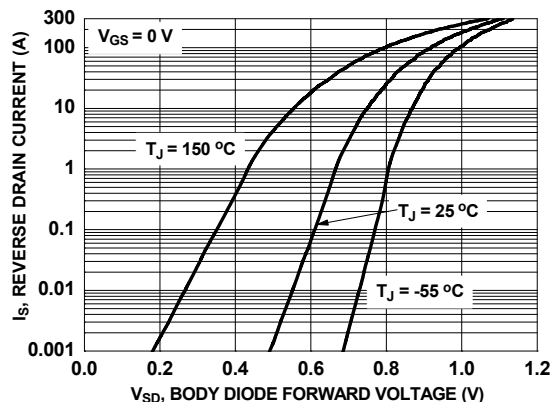


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

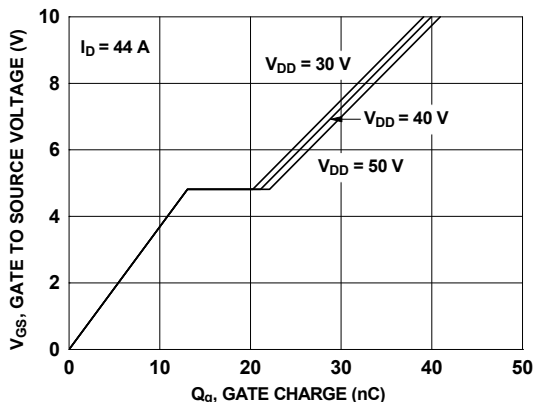


Figure 7. Gate Charge Characteristics

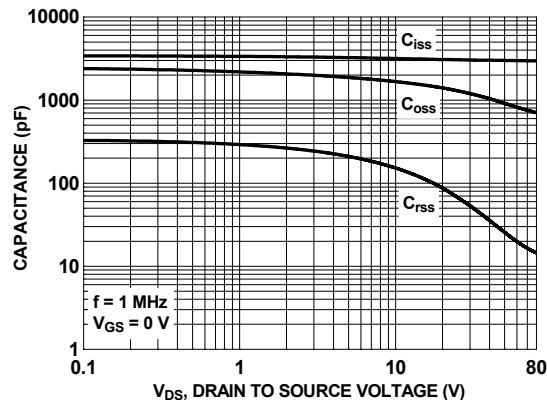


Figure 8. Capacitance vs. Drain to Source Voltage

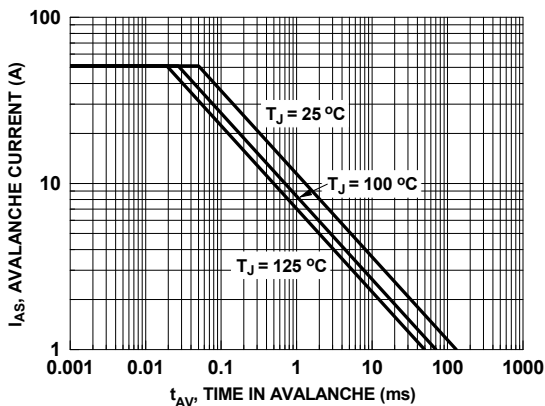


Figure 9. Unclamped Inductive Switching Capability

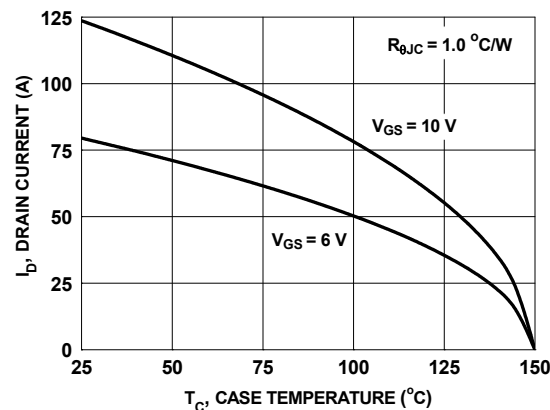


Figure 10. Maximum Continuous Drain Current vs Case Temperature

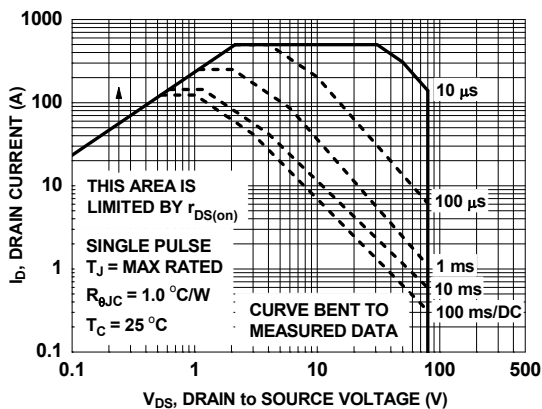


Figure 11. Forward Bias Safe Operating Area

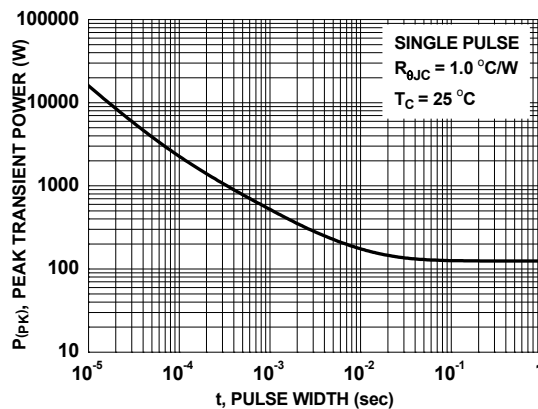
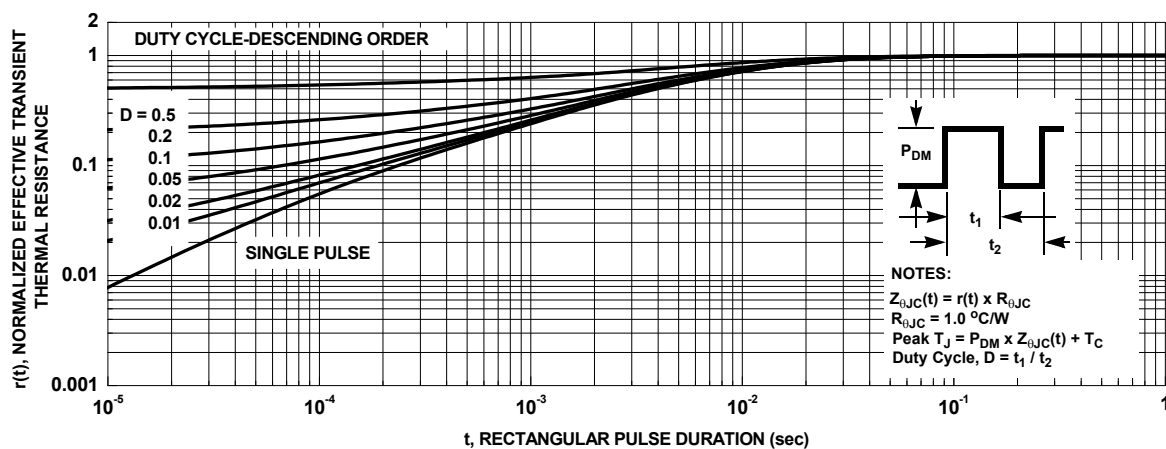


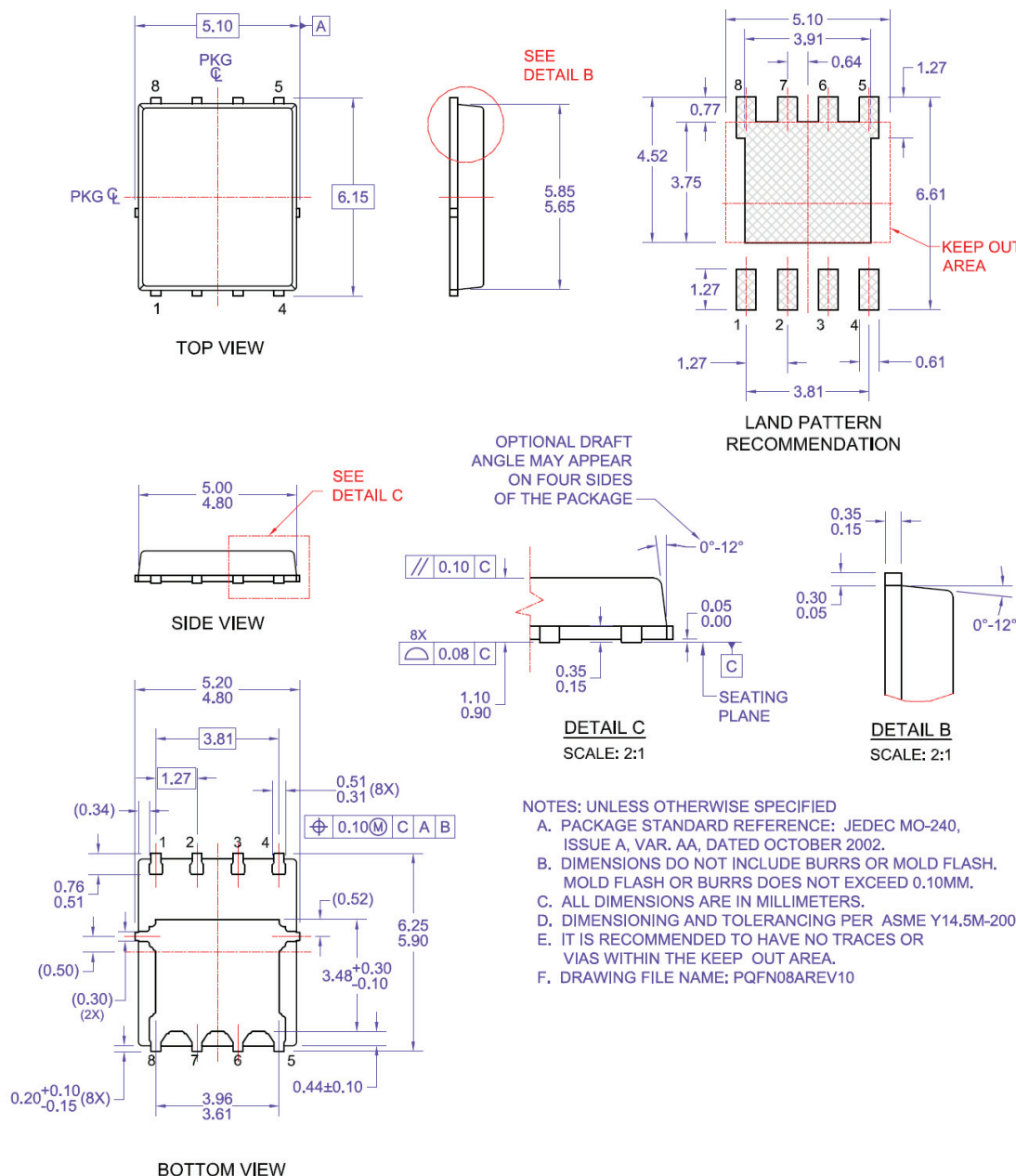
Figure 12. Single Pulse Maximum Power Dissipation

# **Typical Characteristics** $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout

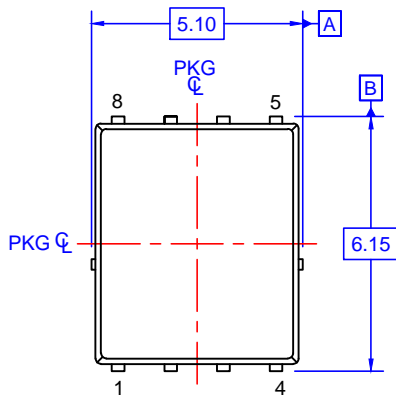


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  - ALL DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - DRAWING FILE NAME: PQFN08AREV10

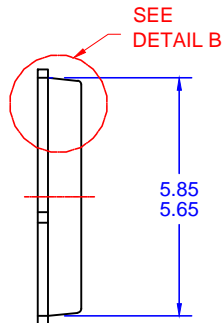
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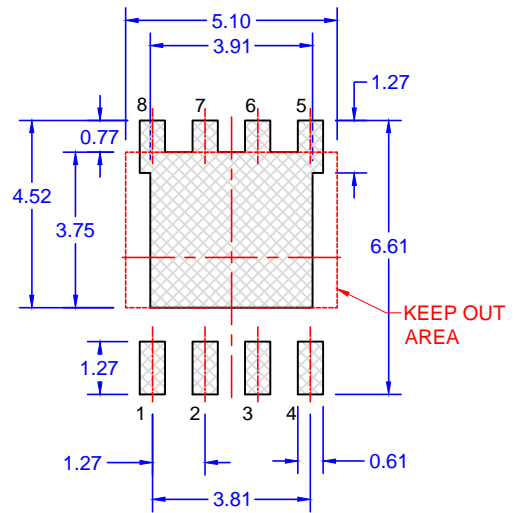
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CASE 483AE  
ISSUE A



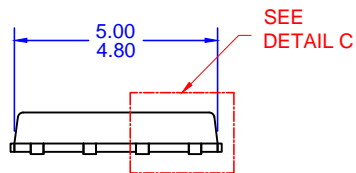
TOP VIEW



SEE  
DETAIL B



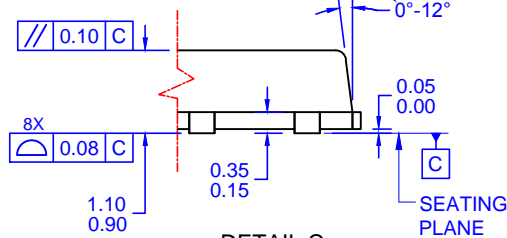
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SIDE VIEW

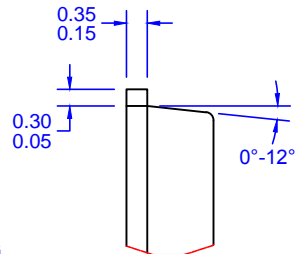
SEE  
DETAIL C

OPTIONAL DRAFT  
ANGLE MAY APPEAR  
ON FOUR SIDES  
OF THE PACKAGE



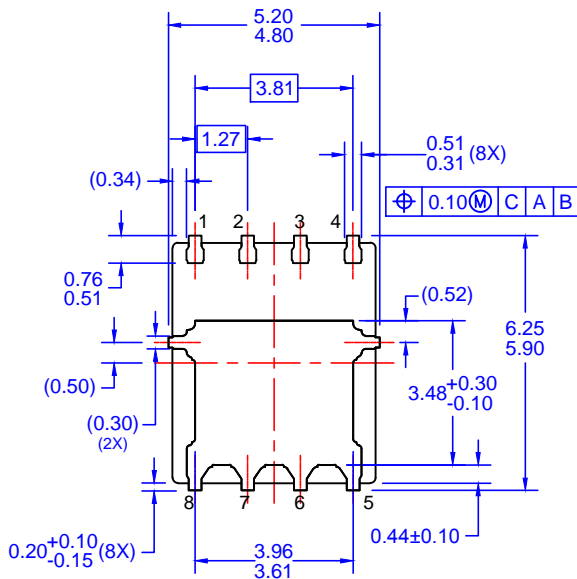
DETAIL C

SCALE: 2:1



DETAIL B

SCALE: 2:1



BOTTOM VIEW

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