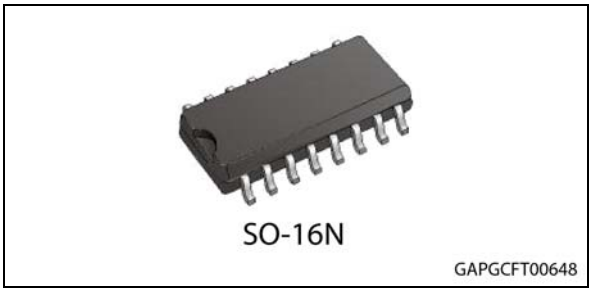
VNH5200AS-E

Fully integrated H-bridge motor driver for automotive applications

Datasheet - production data



Features

Type	$R_{DS(on)}$	I_{out}	V_{CCmax}
VNH5200AS-E	200 mΩ typ (per leg)	8 A	41 V

- Automotive qualified
- Output current: 8 A
- 3 V CMOS-compatible inputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Protection against loss of ground and loss of V_{CC}
- Current sense output proportional to motor current
- Output protected against short to ground and short to V_{CC}
- Package: ECOPACK®

Description

The VNH5200AS-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches.

Both switches are designed using STMicroelectronics' well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dies are assembled in SO-16N package on electrically isolated leadframes.
Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals IN_A and IN_B can directly interface the microcontroller to select the motor direction and the brake condition. The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enables one leg of the bridge. Each $DIAG_A/EN_A$ provides a feedback digital diagnostic signal as well. The normal operating condition is explained in the truth table. The CS pin allows to monitor the motor current by delivering a current proportional to its value.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-16N	VNH5200AS-E	VNH5200ASTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

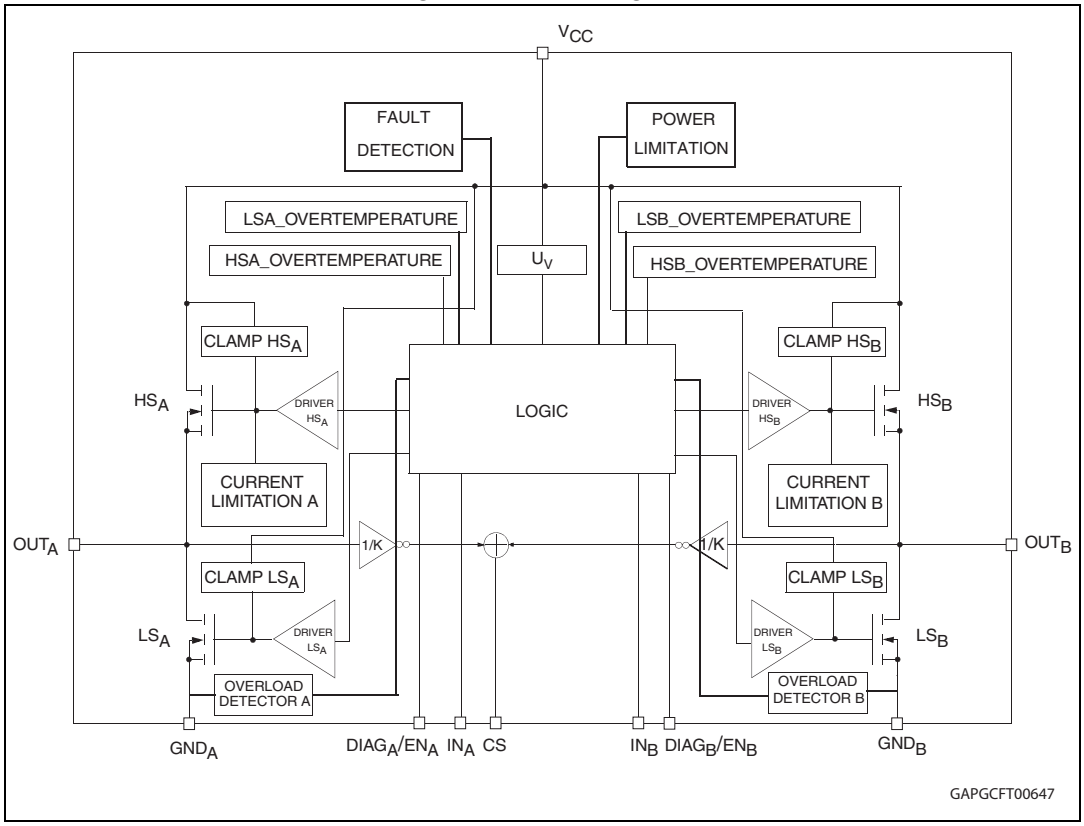


Table 2. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table.
Undervoltage	Shuts down the device for battery voltage lower than 5V.
High-side and low-side clamp voltage	Protect the high-side and the low-side switches from the high voltage on the battery line.
High-side and low-side driver	Drive the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge.
Current limitation	Limits the motor current in case of short circuit.
High-side and low-side overtemperature protection	In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die.
Low-side overload detector	Detects when low side current exceeds shutdown current and latches off the concerned Low side.

Table 2. Block description (continued)

Name	Description
Fault detection	Signalizes the abnormal behaviour of the switch (output shorted to ground or output shorted to battery) by pulling down the concerned ENx/DIAGx pin.
Power limitation	Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.

Figure 2. Configuration diagram (top view)

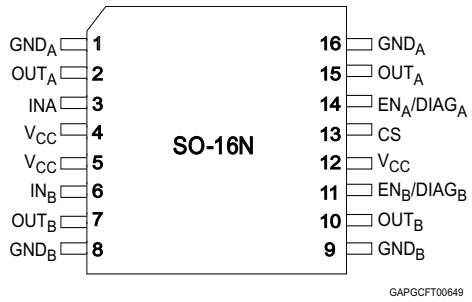


Table 3. Suggested connections for unused and not connected pins

Connection / pin	Current sense	OUTx	INPUTx, DIAGx/ENx
Floating	Not allowed	X	X
To ground	Through 1 kΩ resistor	Not allowed	Through 10 kΩ resistor

Table 4. Pin definitions and functions

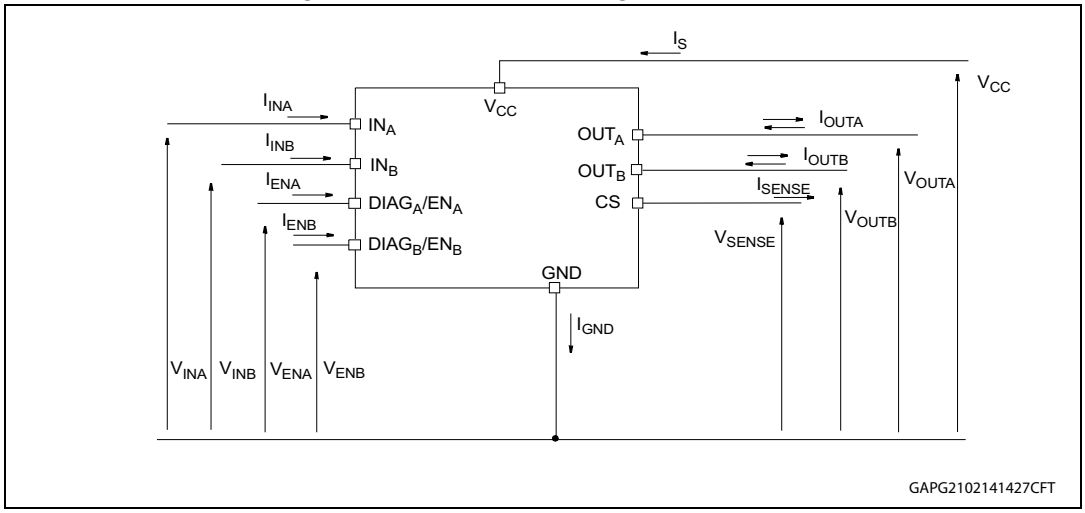
Pin N°	Symbol	Function
1, 16	GND_A	Source of low-side switch A
2, 15	OUT_A	Source of high-side switch A / drain of low-side switch A
3	IN_A	Clockwise input
4, 5, 12	V_{CC}	Power supply voltage
6	IN_B	Counter clockwise input
7, 10	OUT_B	Source of high-side switch B / drain of low-side switch B
8, 9	GND_B	Source of low-side switch B
11	$EN_B/DIAG_B$	Status of high-side and low-side switches B. Open drain output.
13	CS	Output of current sense
14	$EN_A/DIAG_A$	Status of high-side and low-side switches A. Open drain output.

Table 5. Pin functions description

Name	Description
V_{CC}	Battery connection.
GND	Power ground.
OUT_A OUT_B	Power connections to the motor.
IN_A IN_B	Voltage controlled input pins with hysteresis, CMOS-compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V_{CC}, brake to GND, clockwise and counterclockwise).
$EN_A/DIAG_A$ $EN_B/DIAG_B$	Open drain bidirectional logic pins.These pins must be connected to an external pull up resistor. When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a high-side FET or excessive ON-state voltage drop across a low-side FET), these pins are pulled low by the device (see *Table 14: Truth table in fault conditions (detected on OUTA)*).
CS	Analog current sense output. This output delivers a current proportional to the motor current. The information can be read back as an analog voltage across an external resistor.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 6: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+ 40	V
I_{max}	Maximum output current (continuous)	Internally limited	A
I_R	Reverse output current (continuous)	-15	A
I_{IN}	Input current (IN_A and IN_B pins)	+/- 10	mA
I_{EN}	Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	+/- 10	mA
V_{CS}	Current sense maximum voltage	V_{CC}-40/+V_{CC}	V
V_{ESD}	Electrostatic discharge (Human body model: R=1.5 kΩ, C=100 pF)	2	kV
T_c	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C
I_{GND}	DC reverse ground pin current	200	mA

2.2 Thermal data

Table 7. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (per leg)	TBD	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 15*	°C/W

2.3 Electrical characteristics

Values specified in this section are for V_{CC} = 9 V up to 18 V; -40 °C < T_j < 150°C, unless otherwise specified.

Table 8. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5		18	V
I_S	Supply current	Off-state with all fault cleared and ENx = 0 (standby) IN_A = IN_B = 0; T_j = 25°C; V_{CC} = 13 V		3	6	µA
		Off-state with all fault cleared and ENx = 0 (standby) IN_A = IN_B = 0; V_{CC} = 13 V; T_j = -40°C to 150°C			10	µA
		Off-state (no standby) IN_A = IN_B = 0; ENx = 5 V; T_j = -40°C to 150°C			5	mA
		On-state: IN_A or IN_B = 5 V		3	6	mA
R_{ONHS}	Static high-side resistance	I_{OUT} = 2 A; T_j = 25°C		110		mΩ
		I_{OUT} = 2 A; T_j = -40 to 150°C			250	mΩ
R_{ONLS}	Static low-side resistance	I_{OUT} = 2 A; T_j = 25°C		75		mΩ
		I_{OUT} = 2 A; T_j = -40°C to 150°C			150	mΩ
V_f	Free-wheeling diode forward voltage	I_{OUT} = -2 A; T_j = 150°C		0.7	0.9	V
$I_{L(off)}$	High-side off-state output current (per channel)	T_j = 25°C; V_{OUTX} = EN_X = 0 V; V_{CC} = 13 V	0		3	µA
		T_j = 125°C; V_{OUTX} = EN_X = 0 V; V_{CC} = 13 V	0		5	µA

Table 9. Logic inputs (IN_A, IN_B, EN_A, EN_B)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)			0.9	V
V_{IH}	Input high level voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)	2.1			V
V_{IHYST}	Input hysteresis voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)	0.15			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5	6.3	7.5	V
		I_{IN} = -1 mA	-1.0	-0.7	-0.3	V
I_{INL}	Input current	V_{IN} = 0.9 V	1			µA
I_{INH}	Input current	V_{IN} = 2.1 V			10	µA
V_{DIAG}	Enable output low level voltage	Fault operation ($DIAG_X/EN_X$ pin acts as an output pin); I_{EN} = 1 mA			0.4	V

Table 10. Switching (V_{CC} = 13 V, R_{LOAD} = 6.5 Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	Input rise time < 1µs (see *Figure 6*)		50		µs
$t_{d(off)}$	Turn-off delay time	Input rise time < 1µs (see *Figure 6*)		120		µs
t_r	Rise time	See *Figure 5*		0.8		µs
t_f	Fall time	See *Figure 5*		33		µs
t_{DEL}	Delay time during change of operating mode		200	400	1600	µs

Table 11. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{USD}	Undervoltage shutdown			4	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
I_{LIM_H}	High-side current limitation		8	12	16	A
I_{SD_LS}	Shutdown LS current		8	15	23	A
V_{CLPH}	High-side clamp voltage (V_{CC} to OUT_A = 0 or OUT_B = 0)	I_{OUT} = 100 mA; t_{clamp} = 1 ms	41	46	52	V
V_{CLPLS}	Low-side clamp voltage (OUT_A = V_{CC} or OUT_B = V_{CC} to GND)	I_{OUT} = 100 mA; t_{clamp} = 1 ms	41	46	52	V
T_{TSD_HS}	High-side thermal shutdown temperature	V_{IN} = 2.1 V	150	175	200	°C
T_{TR_HS}	High-side thermal reset temperature		135			°C
T_{HYST_HS}	High-side thermal hysteresis (T_{SD_HS} - T_{R_HS})			7		°C
T_{TSD_LS}	Low-side thermal shutdown temperature	V_{IN} = 0 V	150	175	200	°C
V_{CLP}	Total clamp voltage (V_{CC} to GND)	I_{OUT} = 100 mA; t_{clamp} = 1 ms	41	46	52	V
t_{SD_LS}	Time to shutdown for the low-side			10		µs

Table 12. Current sense (9 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.075 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	990	1600	2330	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	860	1450	2000	
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C	890	1140	1270	
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	900	1080	1300	
dK_0/K_0 (1)	Analog sense current drift	I_{OUT} = 0.075 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	-20		20	%
dK_1/K_1 (1)	Analog sense current drift	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	-30		30	%
dK_2/K_2 (1)	Analog sense current drift	I_{OUT} = 2 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C	-14		14	%
dK_3/K_3 (1)	Analog sense current drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	-14		14	%
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 2 A; R_{SENSE} = 10 KΩ	5			V

Table 12. Current sense (9 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{IN} = 0 V; T_j = -40°C to 150°C	0		5	µA
		V_{IN} = 5 V; T_j = -40°C to.150°C	0		5	µA

1. Analog sense current drift is deviation of factor K for a given device over (-40 °C to 150 °C and 9 V < V_{CC} < 18 V) with respect to its value measured at T_J = 25 °C, V_{CC} = 13 V.

Figure 4. Definition of delay time

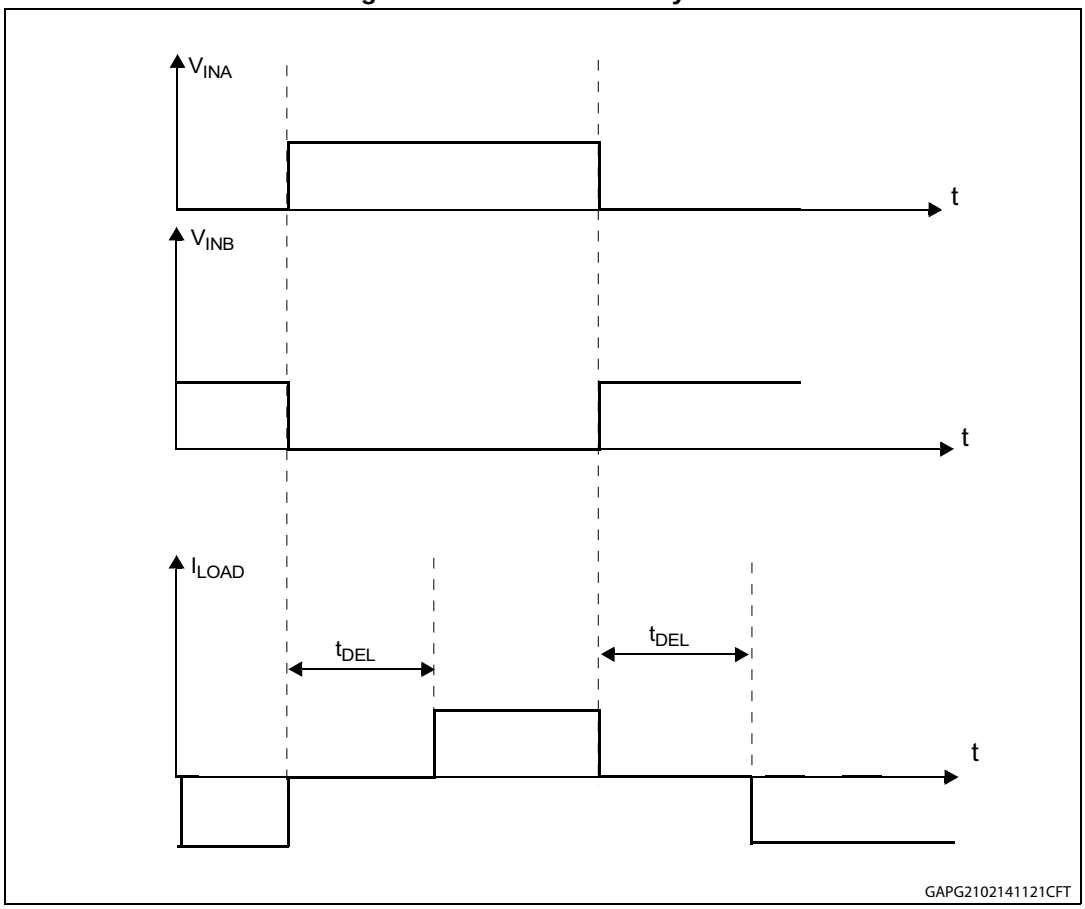


Figure 5. Definition of the low-side switching times

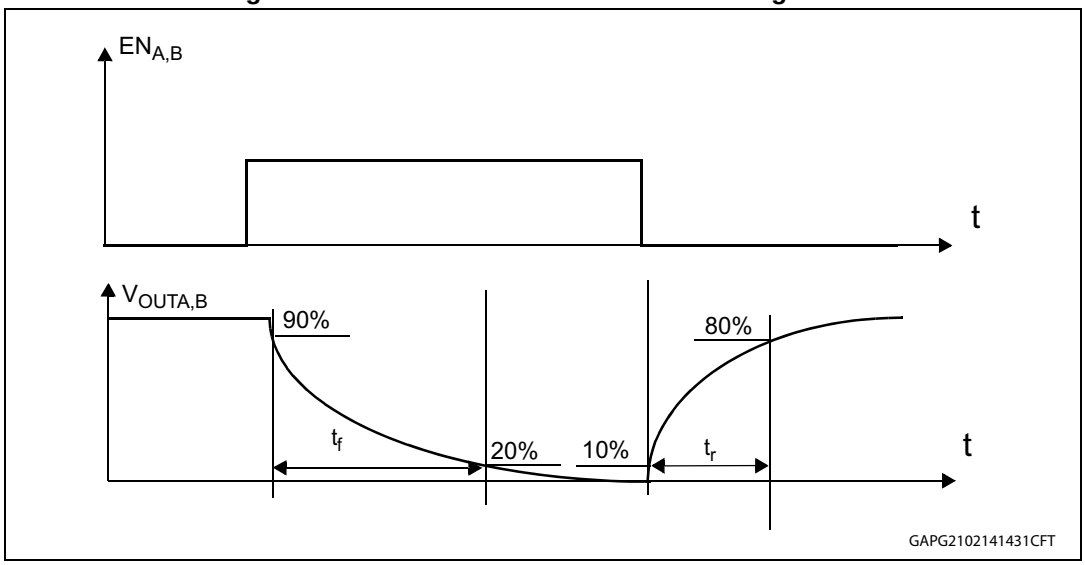


Figure 6. Definition of the high-side switching times

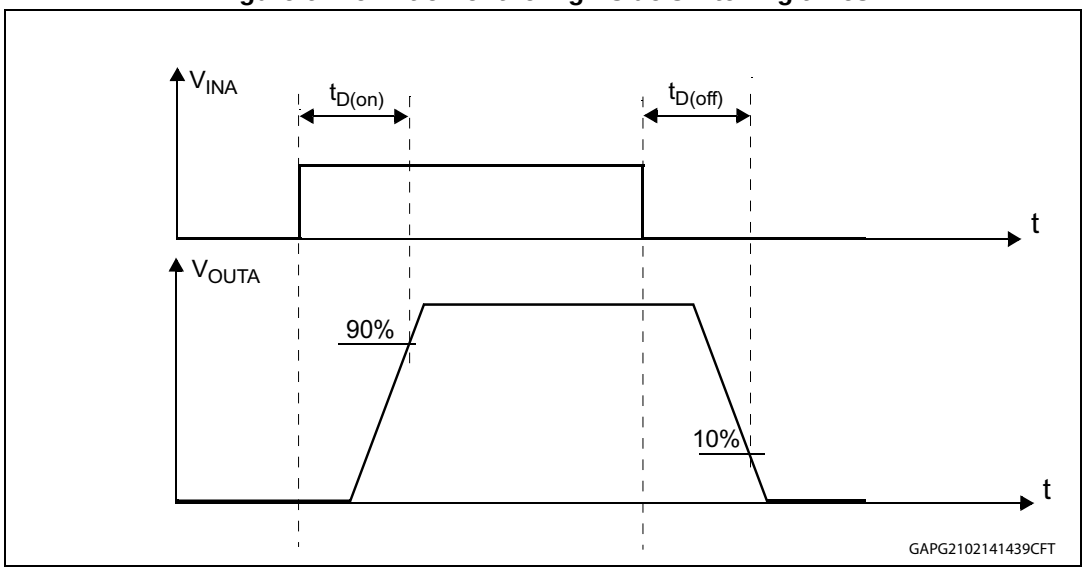


Table 13. Truth table in normal operating conditions

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS	Operating mode
1	1	1	1	H	H	High Imp.	Brake to V_{CC}
	0				L	$I_{SENSE} = I_{OUT}/K$	Clockwise (CW)
0	1			L	H		Counterclockwise (CCW)
	0				L	High Imp.	Brake to GND

Table 14. Truth table in fault conditions (detected on OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS (V_{CSD}=0V)
1	1	0	1	OPEN	H	High Imp.
	0				L	
0	1				H	I_{OUTB}/K
	0				L	High Imp.
X	X		0		OPEN	
		Fault Information		Protection Action		

Note: In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

Table 15. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 16. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 17. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 7. Waveforms in full-bridge operation (part 1)

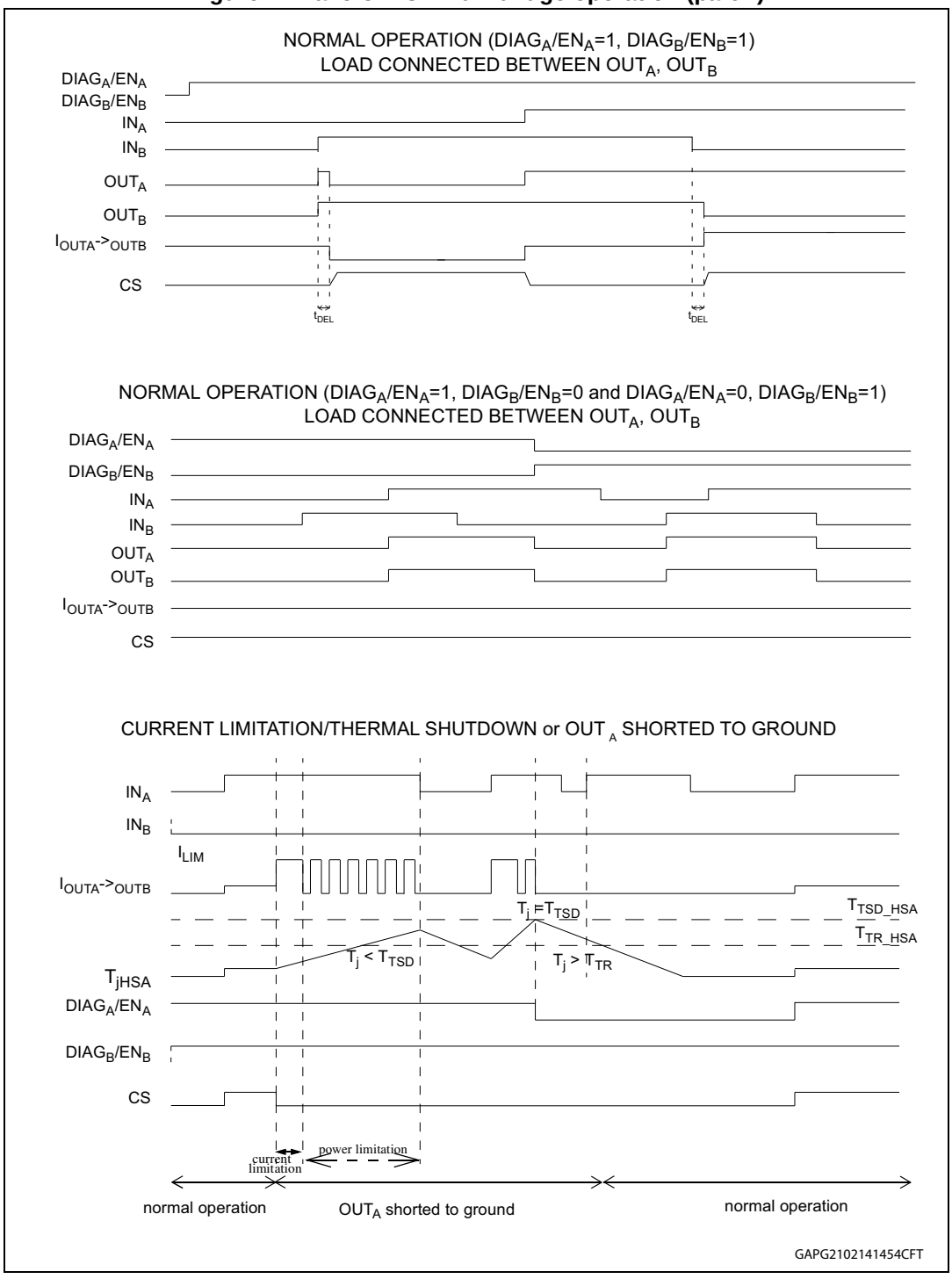
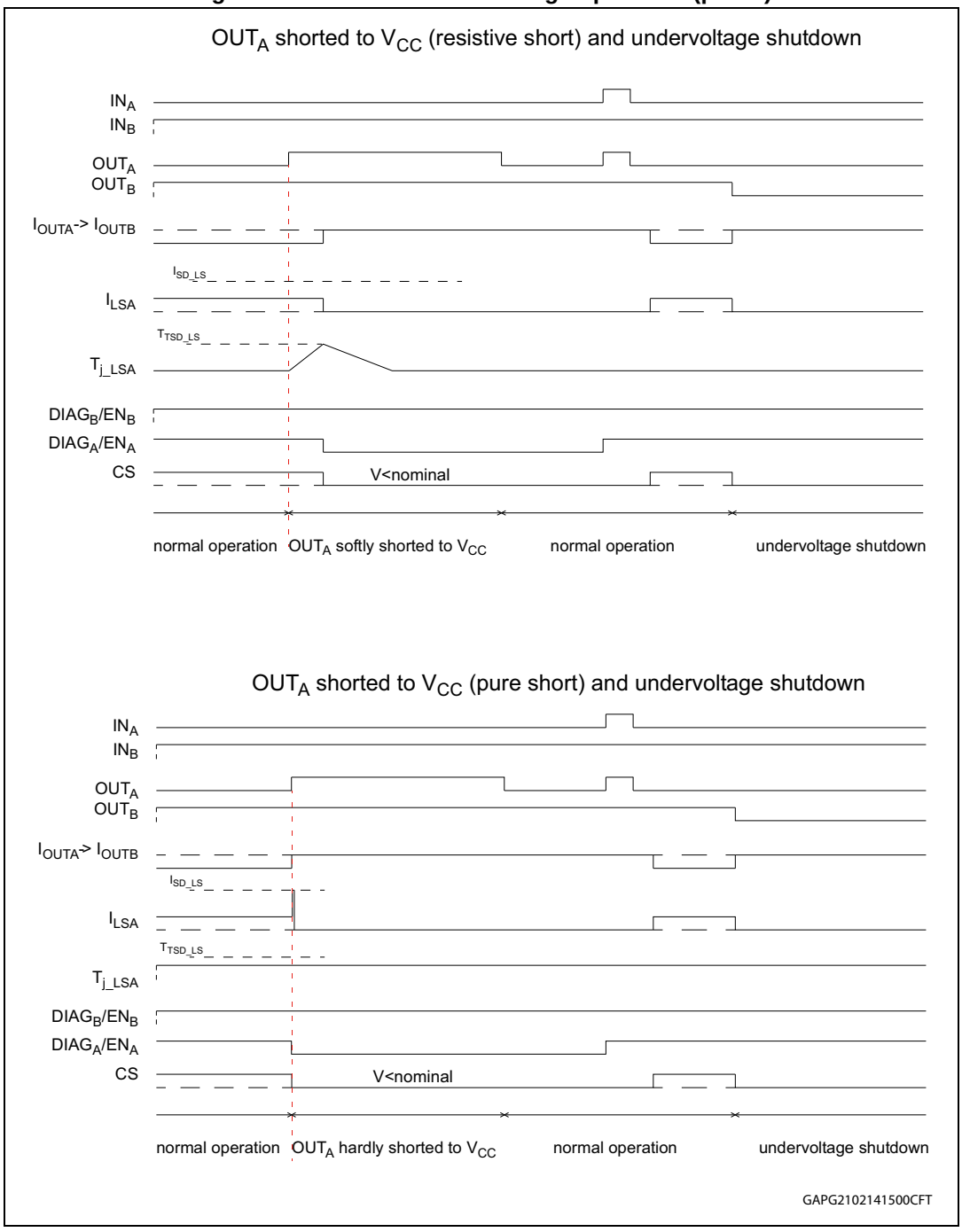


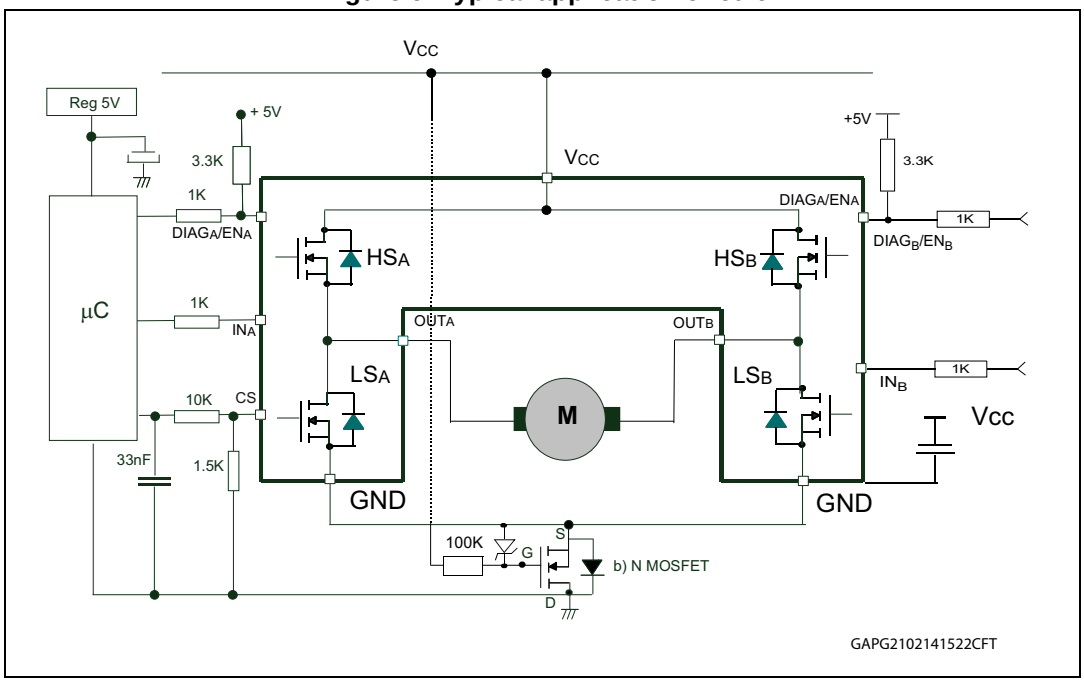
Figure 8. Waveforms in full-bridge operation (part 2)



3 Application information

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

Figure 9. Typical application circuit



Note: The value of the blocking capacitor (C) depends on the application conditions. Stored energy of the motor inductance may fly back into the blocking capacitor, if the bridge driver goes into 3-state. This causes a hazardous overvoltage if the capacitor is not big enough. As basic orientation, 500 µF per 10 A load current is recommended.

In case of a fault condition the $DIAG_X/EN_X$ pin is considered as an output pin by the device.

The fault conditions are:

- Overtemperature on one or both high-sides
- Short to battery condition on the output (overcurrent detection on the low-side Power MOSFET)

Possible origins of fault conditions may be:

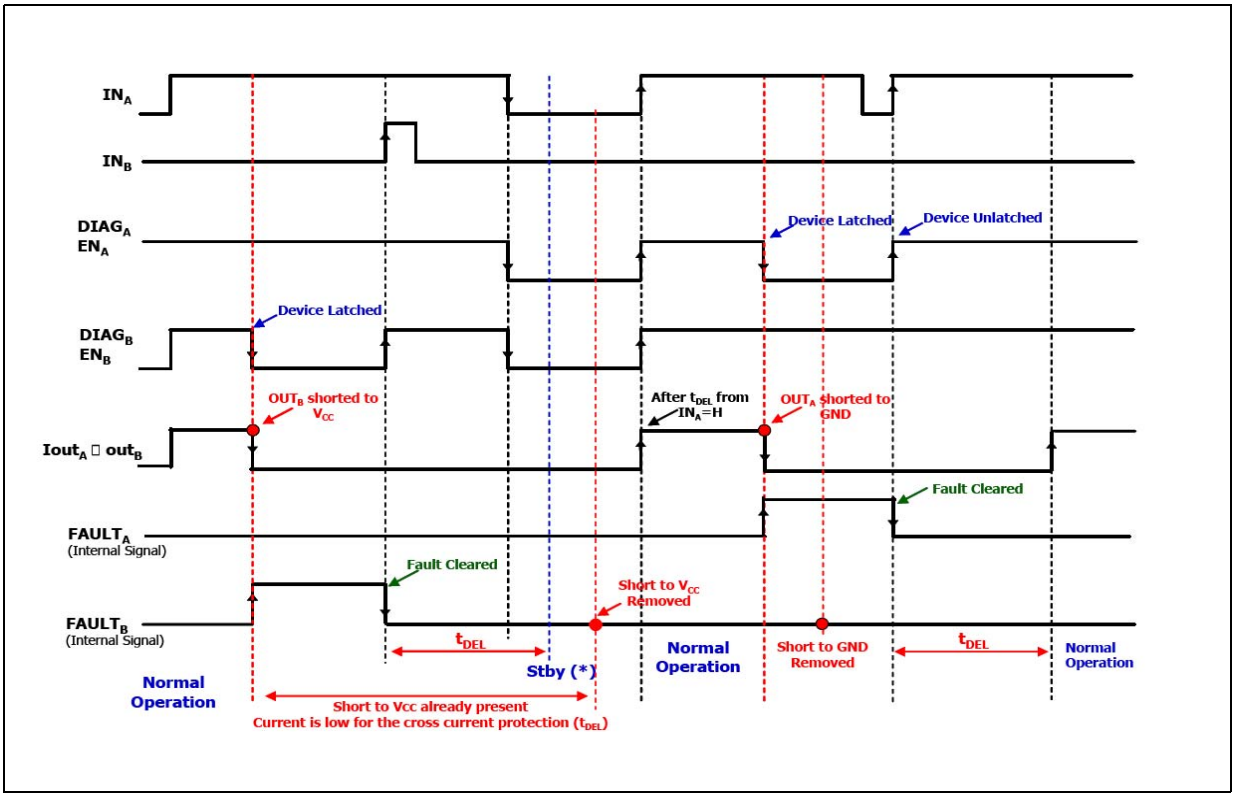
OUT_A is shorted to ground $\rightarrow$ overtemperature detection on high-side A

OUT_A is shorted to V_{CC} $\rightarrow$ low-side Power MOSFET overcurrent detection

When a fault condition is detected, the user can identify which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn on the respective output (OUT_X) again, the input signal must rise from low to high level.

Figure 10. Behavior in fault condition (how a fault can be cleared)



Note: In case the fault condition is not removed, the procedure for unlatching and sending the device in Stby mode is:

- Clear the fault in the device (toggle: IN_A if EN_A = 0 or IN_B if EN_B = 0)

- Pull low all inputs and Diag/EN pins within t_{DEL}.

If the Diag/En pins are already low the fault can be cleared simply by toggling the input. The device enters in stby mode as soon as the fault is cleared.

3.1 Reverse battery protection

Three possible solutions can be considered:

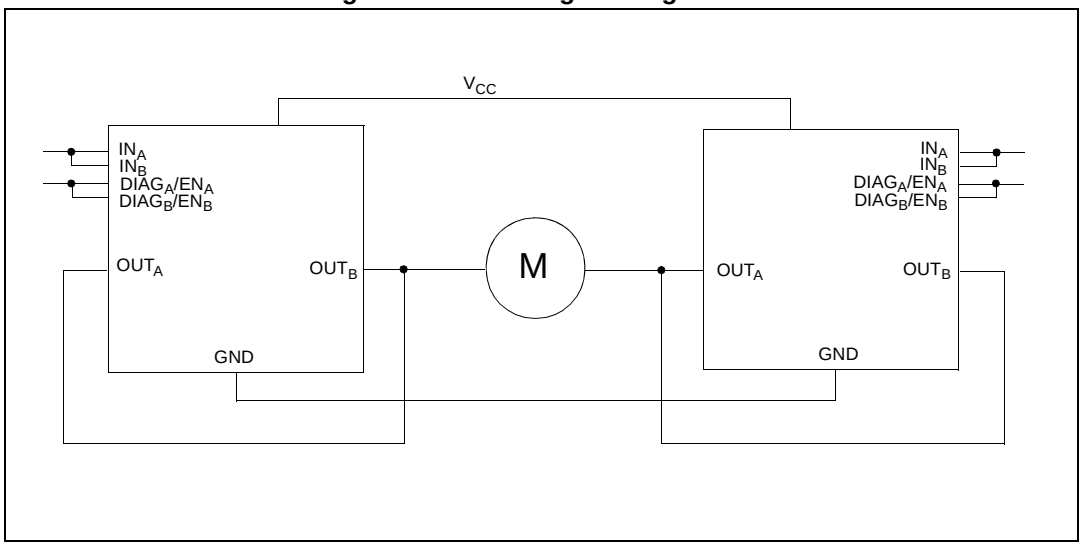
- A Schottky diode D connected to V_{CC} pin
- An N-channel MOSFET connected to the GND pin (see *Figure 9: Typical application circuit*)
- A P-channel MOSFET connected to the V_{CC} pin

The device sustains no more than -15 A in reverse battery conditions because of the two Body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH5200AS-E is pulled down to the V_{CC} line (approximately -1.5 V).

Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through microcontroller I/Os, series resistor is:

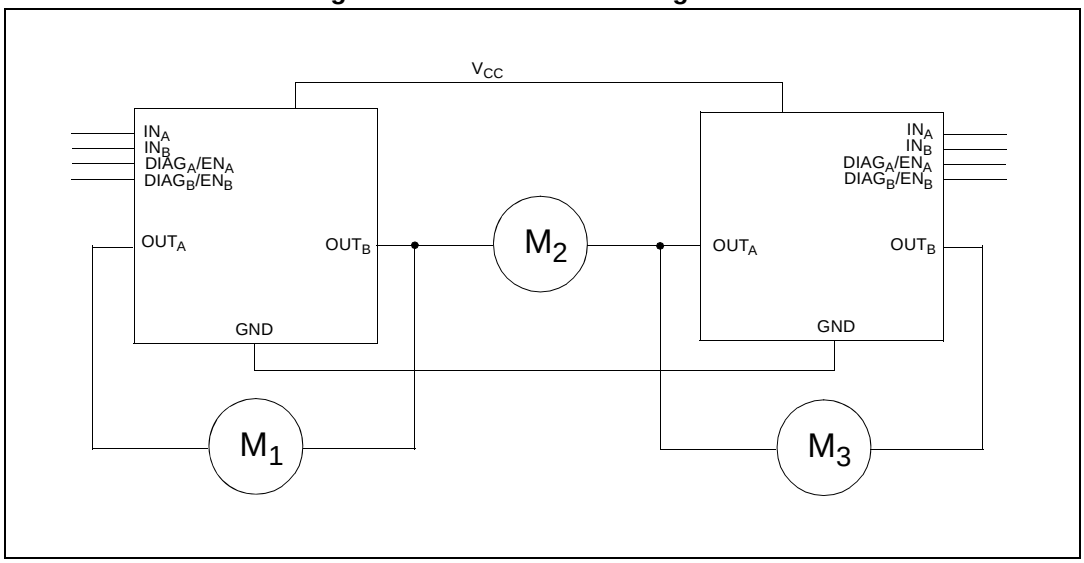
$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

Figure 11. Half-bridge configuration



Note: The VNH5200AS-E can be used as a high power half-bridge driver achieving an On resistance per leg of 90 mΩ.

Figure 12. Multi-motors configuration

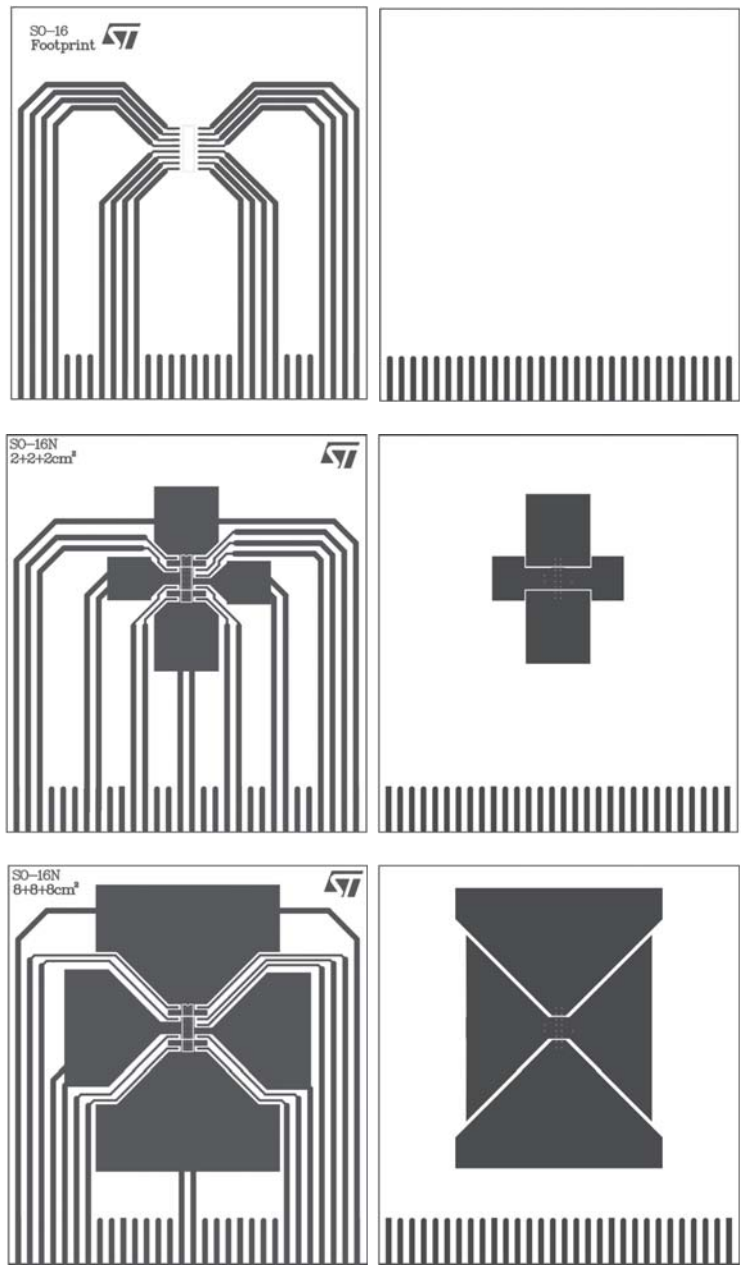


Note: The VNH5200AS-E can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor must be driven at a time. $DIAG_X/EN_X$ pins allow to put unused half-bridges in high impedance.

4 Package and PCB thermal data

4.1 PCB characteristics

Figure 13. PCB layout (top and bottom): footprint, 2+2+2 cm^2, 8+8+8 cm^2



Note: Board finish thickness 1.6 mm +/- 10%, double layer, dimensions 77x86 mm, material FR4; Cu thickness 70µm (both front and back side); Thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm.

4.2 Package thermal data

4.2.1 Thermal characterization in steady state conditions

Figure 14. Chipset configuration in steady state conditions

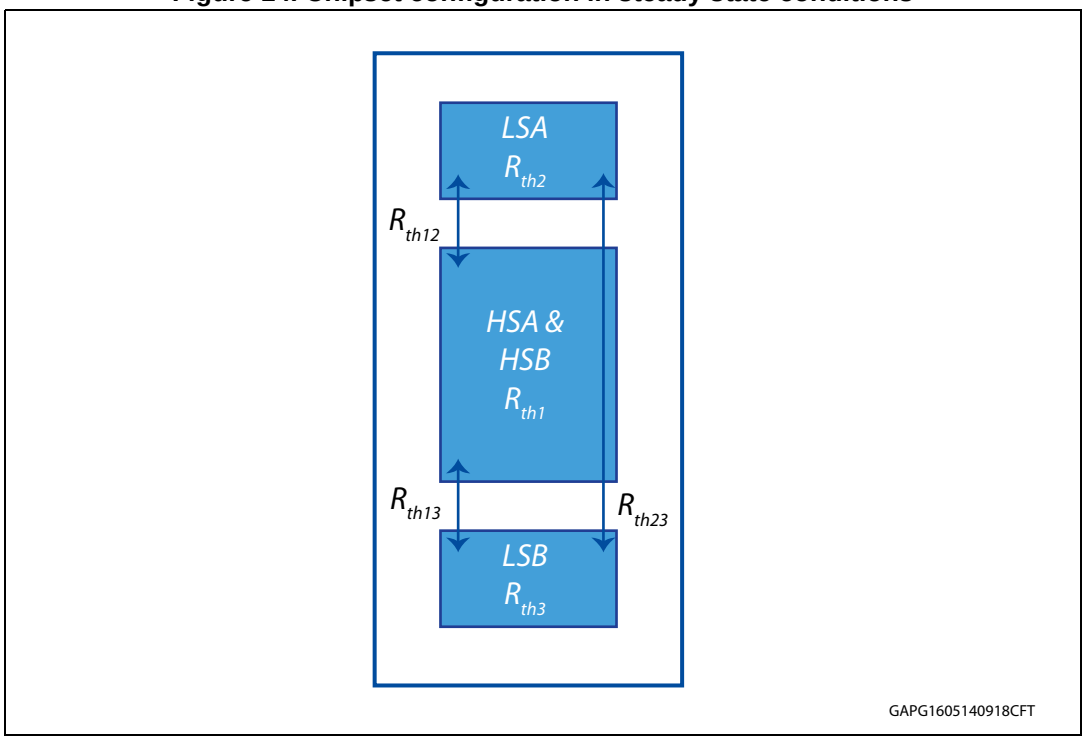


Figure 15. Auto and mutual $R_{thj\text{-}amb}$ vs. PCB heat-sink area in open box free air condition

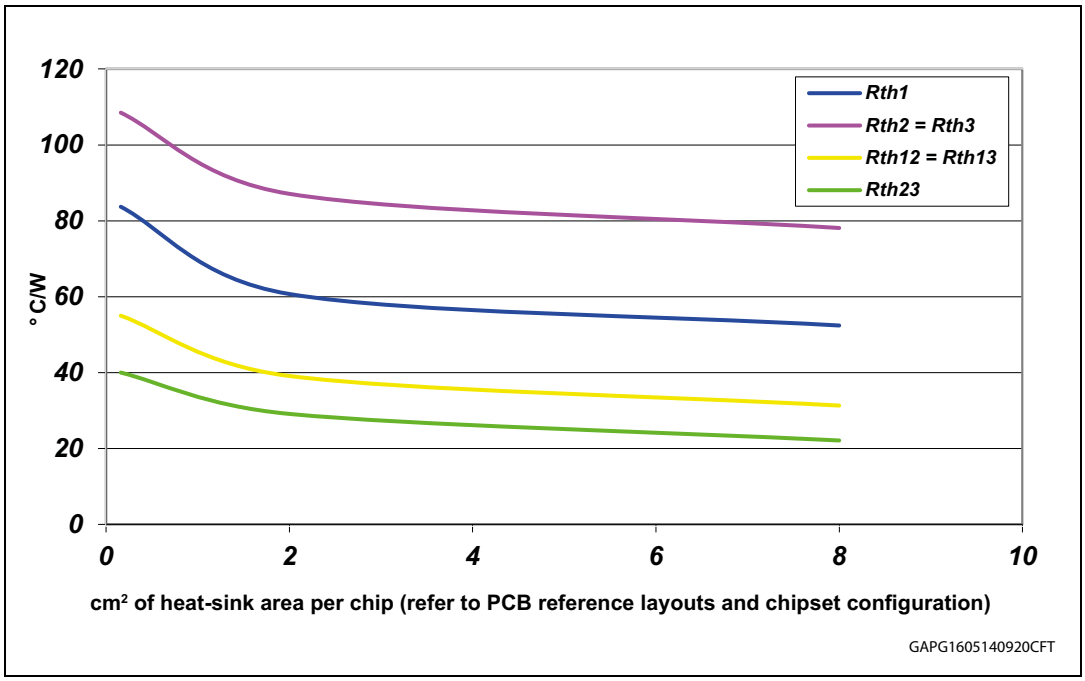


Table 18. Thermal model for junction temperature calculation in steady-state conditions

HS_A	HS_B	LS_A	LS_B	T_{jHSAB}	T_{jLSA}	T_{jLSB}
ON	OFF	OFF	ON	$P_{dHSA} \cdot R_{th1} + P_{dLSB} \cdot R_{th13} + T_{amb}$	$P_{dHSA} \cdot R_{th12} + P_{dLSB} \cdot R_{th23} + T_{amb}$	$P_{dHSA} \cdot R_{th13C} + P_{dLSB} \cdot R_{th3} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHSB} \cdot R_{th1} + P_{dLSA} \cdot R_{th12} + T_{amb}$	$P_{dHSB} \cdot R_{th12} + P_{dLSA} \cdot R_{th2} + T_{amb}$	$P_{dHSAB} \cdot R_{th13} + P_{dLSA} \cdot R_{th23} + T_{amb}$

4.2.2 Thermal characterization during transients

$T_{hs} = Pd_{hs} \cdot Z_{hs} + Z_{hsls} \cdot (Pd_{lsA} + Pd_{lsB}) + T_{amb}$

$T_{lsA} = Pd_{lsA} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{lsB} \cdot Z_{lsls} + T_{amb}$

$T_{lsB} = Pd_{lsB} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{lsA} \cdot Z_{lsls} + T_{amb}$

Figure 16. Chipset configuration during transients

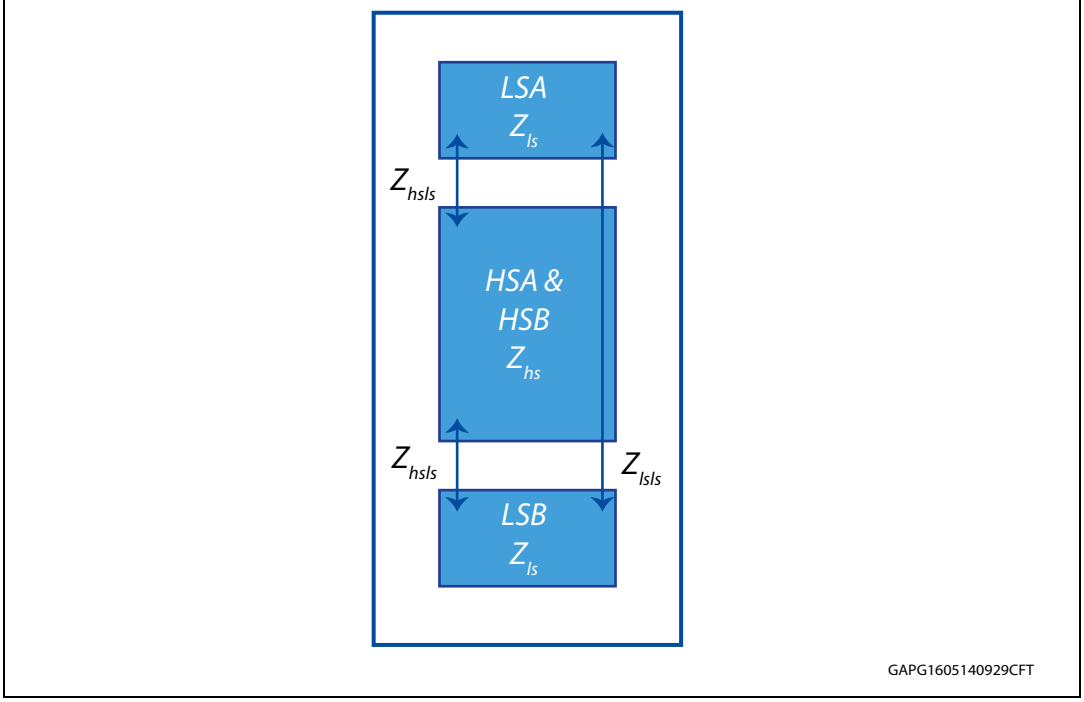


Figure 17. HSD thermal impedance junction ambient single pulse

Figure 18. LSD thermal impedance junction ambient single pulse

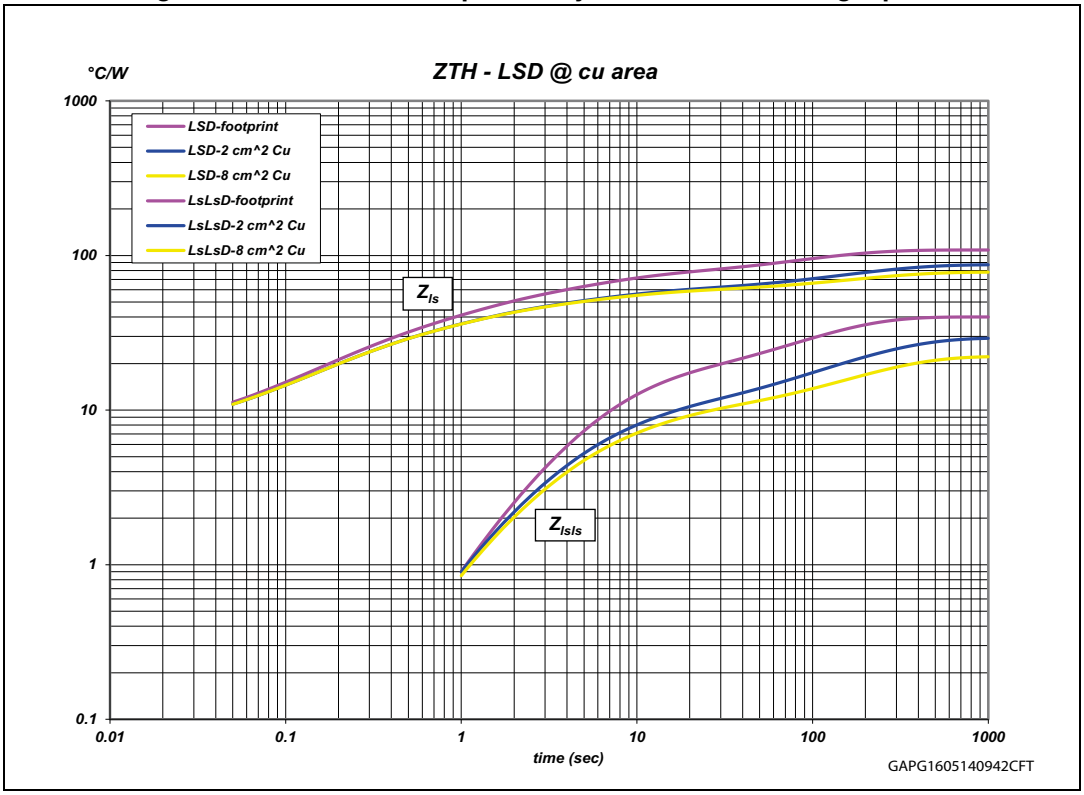


Figure 19. Electrical equivalent model

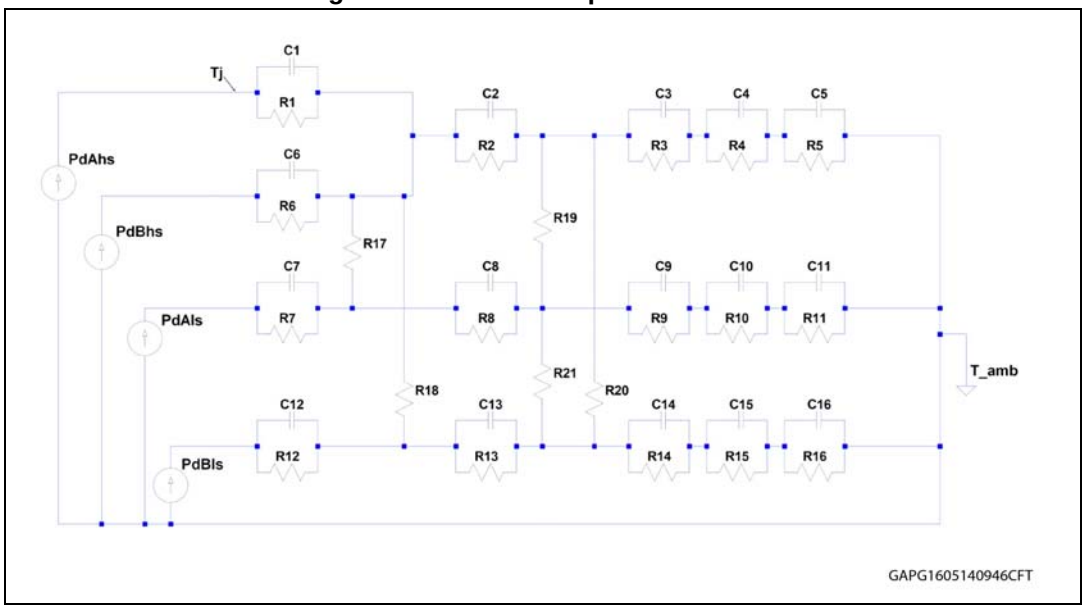


Table 19. Thermal parameters

Heat-sink area per chip (cm^2)	Footprint	2	8
R1 (°C/W)	4.5		
R2 (°C/W)	14		
R3 (°C/W)	26	18	18
R4 (°C/W)	42	12	12
R5 (°C/W)	75	48	32
R6 (°C/W)	4.5		
R7 (°C/W)	6.5		
R8 (°C/W)	14		
R9 (°C/W)	35		
R10 (°C/W)	68	48	48
R11 (°C/W)	103	100	68
R12 (°C/W)	6.5		
R13 (°C/W)	14		
R14 (°C/W)	35		
R15 (°C/W)	68	48	48
R16 (°C/W)	103	100	68
R17 (°C/W)	150	120	120
R18 (°C/W)	150	120	120
R19 (°C/W)	180	150	150
R20 (°C/W)	180	150	150

Table 19. Thermal parameters (continued)

Heat-sink area per chip (cm^2)	Footprint	2	8
R21 (°C/W)	4000	2000	2000
C1 (W·s/°C)	0.001		
C2 (W·s/°C)	0.02		
C3 (W·s/°C)	0.15		
C4 (W·s/°C)	0.2	0.5	1
C5 (W·s/°C)	1.5	2	6
C6 (W·s/°C)	0.001		
C7 (W·s/°C)	0.0005		
C8 (W·s/°C)	0.015		
C9 (W·s/°C)	0.04		
C10 (W·s/°C)	0.08	0.15	0.15
C11 (W·s/°C)	1	2.5	3
C12 (W·s/°C)	0.0005		
C13 (W·s/°C)	0.015		
C14 (W·s/°C)	0.04		
C15 (W·s/°C)	0.08	0.15	0.15
C16 (W·s/°C)	1	2.5	3

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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5.2 SO-16N mechanical data

Figure 20. SO-16N package dimensions

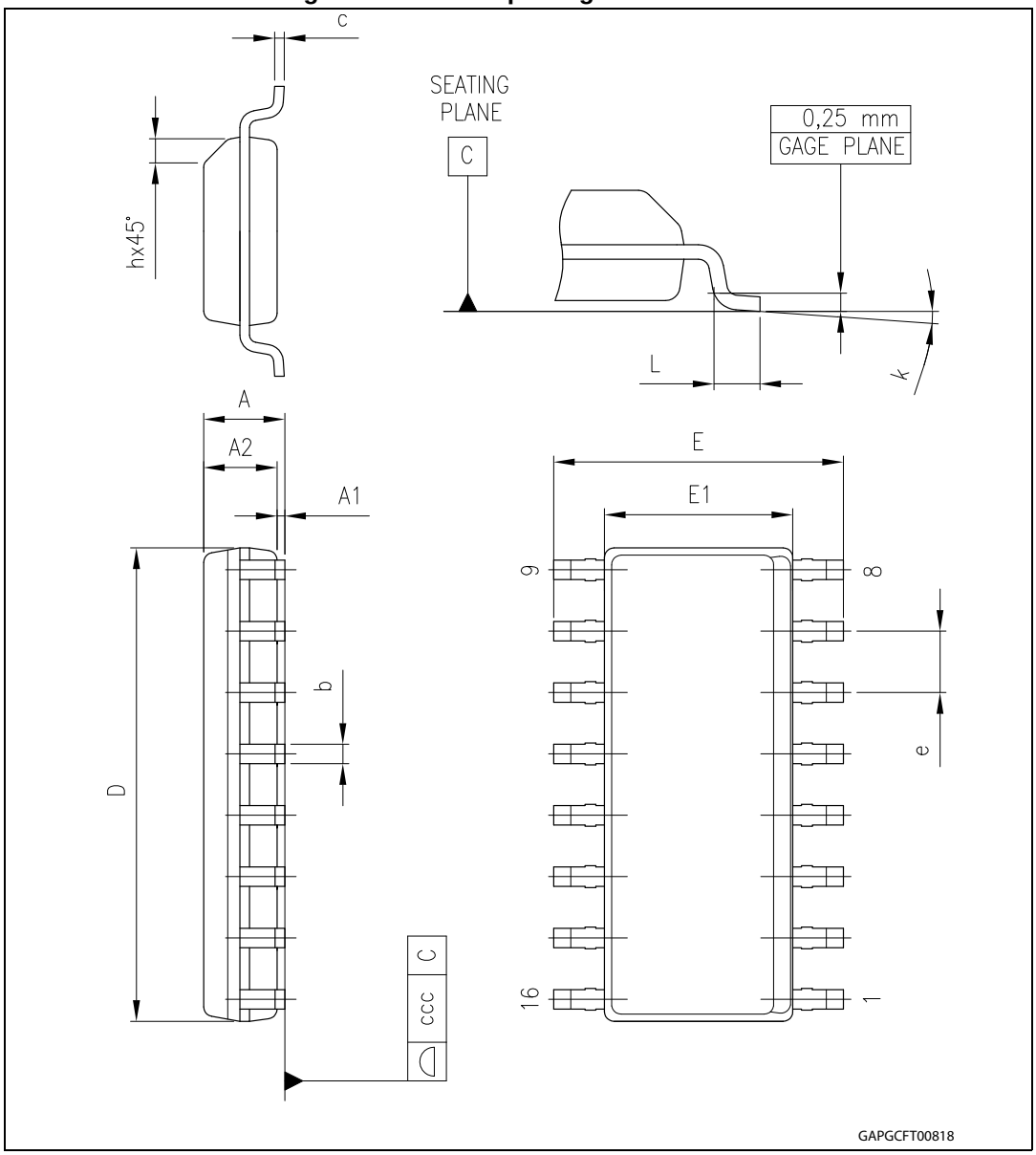

Table 20. SO-16N mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8
ccc			0.10

6 Revision history

Table 21. Document revision history

Date	Revision	Changes
03-Jul-2012	1	Initial release.
20-Mar-2013	2	Updated *Figure 2: Configuration diagram (top view)* Added *Table 3: Suggested connections for unused and not connected pins* *Table 4: Pin definitions and functions*: – pins 11 and 14: updated symbol and functions *Table 8: Power section*: – R_{ONHS}, R_{ONLS}: updated values – I_{RM}: removed row *Table 10: Switching (VCC = 13 V, RLOAD = 6.5 W)*: – t_r, t_f: updated values – t_{rr}: removed row *Table 11: Protections and diagnostics*: – V_{USD}, I_{SD_LS}: updated values – T_{TSD_HS}, T_{TR_HS}, T_{HYST_HS}: updated symbol name and parameter – T_{TSD_LS}: updated test conditions *Table 12: Current sense (9 V < VCC < 18 V)*: – K_0, K_1, K_2, K_3, dK_2/K_2, dK_3/K_3: updated values – V_{SENSE}: updated test conditions – I_{SENSE0}: removed test conditions and updated value Added *Figure 5: Definition of the low-side switching times*
14-June-2013	3	Updated *Description* and *Table 8*.
18-Sep-2013	4	Updated disclaimer.
26-Feb-2014	5	Updated *Features* list Added *Figure 4: Definition of delay time* Updated *Figure 5: Definition of the low-side switching times* Added *Section 2.4: Waveforms* and *Chapter 3: Application information*
16-May-2014	6	Updated document title Added *Chapter 4: Package and PCB thermal data*
14-Apr-2015	7	*Table 8: Power section*: – R_{ONHS}, R_{ONLS}: updated value *Table 12: Current sense (9 V < VCC < 18 V)*: – K_x, dK_x/K_x: updated values

Table 21. Document revision history (continued)

Date	Revision	Changes
21-Oct-2015	8	*Table 6: Absolute maximum ratings*: – I_{GND}: removed row *Table 8: Power section*: – V_f: updated parameter *Table 11: Protections and diagnostics*: – V_{CLPH}, V_{CLPLS}, V_{CLP}: updated test conditions *Table 12: Current sense (9 V < VCC < 18 V)*: – K_0, K_1, K_2, K_3: updated values *Table 20: SO-16N mechanical data*: – ccc: updated values
11-Nov-2015	9	*Table 6: Absolute maximum ratings*: – I_{GND}: added row

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