

## 1.5A Dual Open-Drain MOSFET Drivers

### Features:

- Independently Programmable Rise and Fall Times
- Low Output Impedance – 7Ω Typ.
- High Speed  $t_R$ ,  $t_F$  – <30 nsec with 1000 pF Load
- Short Delay Times – <30 nsec
- Wide Operating Range:
  - 4.5V to 18V
- Latch-Up Protected: Will Withstand > 500 mA Reverse Current (Either Polarity)
- Input Withstands Negative Swings Up to -5V

### Applications:

- Motor Controls
- Driving Bipolar Transistors
- Driver for Non-overlapping Totem Poles
- Reach-Up/Reach-Down Driver

### Device Selection Table

Part Number	Package	Temp. Range
TC4404COA	8-Pin SOIC	0°C to +70°C
TC4404CPA	8-Pin PDIP	0°C to +70°C
TC4404EOA	8-Pin SOIC	-40°C to +85°C
TC4404EPA	8-Pin PDIP	-40°C to +85°C
TC4404MJA	8-Pin CERDIP	-55°C to +125°C
TC4405COA	8-Pin SOIC	0°C to +70°C
TC4405CPA	8-Pin PDIP	0°C to +70°C
TC4405EOA	8-Pin SOIC	-40°C to +85°C
TC4405EPA	8-Pin PDIP	-40°C to +85°C
TC4405MJA	8-Pin CERDIP	-55°C to +125°C

### General Description:

The TC4404/TC4405 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the totem-pole output have been left separated so that individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of drain-current-limiting resistors in the pull-up and/or pull-down sections, allowing the user to define the rates of rise and fall for a capacitive load; or a reduced output swing, if driving a resistive load, or to limit base current, when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 nsec for a 1000 pF load.

For driving MOSFETs in motor-control applications, where slow-ON/fast-OFF operation is desired, these devices are superior to the previously used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-ON, while maintaining fast turn-OFF and maximum noise immunity for an OFF device.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other Microchip drivers. They allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-OFF. By proper positioning of the resistor, either npn or pnp transistors can be driven.

For driving many loads in low-power regimes, these drivers, because they eliminate shoot-through currents in the output stage, require significantly less power at higher frequencies, and can be helpful in meeting low-power budgets.

### Package Type



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Because neither drain in an output is dependent on the other, these devices can also be used as open-drain buffer/drivers where both drains are available in one device, thus minimizing chip count. Unused open drains should be returned to the supply rail that their device sources are connected to (pull-downs to ground, pull-ups to  $V_{DD}$ ), to prevent static damage. In addition, in situations where timing resistors or other means of limiting crossover currents are used, like drains may be paralleled for greater current carrying capacity.

These devices are built to operate in the most demanding electrical environments. They will not latch-up under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings\*

Supply Voltage .....	+22V
Power Dissipation ( $T_A \leq 70^\circ\text{C}$ )	
PDIP .....	730 mW
CERDIP .....	800 mW
SOIC .....	470 mW
Package Thermal Resistance	
PDIP $R_{\theta J-A}$ .....	125°C/W
PDIP $R_{\theta J-C}$ .....	45°C/W
CERDIP $R_{\theta J-A}$ .....	150°C/W
CERDIP $R_{\theta J-C}$ .....	55°C/W
SOIC $R_{\theta J-A}$ .....	155°C/W
SOIC $R_{\theta J-C}$ .....	45°C/W
Operating Temperature Range	
C Version .....	0°C to +70°C
E Version .....	-40°C to +85°C
M Version .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## TC4404/TC4405 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: $T_A = +25^\circ\text{C}$ , with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ , unless otherwise noted.						
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
<b>Input</b>						
$V_{IH}$	Logic 1, High Input Voltage	2.4	—	—	V	
$V_{IL}$	Logic 0, Low Input Voltage	—	—	0.8	V	
$I_{IN}$	Input Current	-1	—	1	$\mu\text{A}$	$0\text{V} \leq V_{IN} \leq V_{DD}$
<b>Output</b>						
$V_{OH}$	High Output Voltage	$V_{DD} - 0.025$	—	—	V	
$V_{OL}$	Low Output Voltage	—	—	0.025	V	
$R_O$	Output Resistance	—	7	10	$\Omega$	$I_{OUT} = 10\text{ mA}$ , $V_{DD} = 18\text{V}$ ; Any Drain
$I_{PK}$	Peak Output Current (Any Drain)	—	1.5	—	A	Duty cycle $\leq 2\%$ , $t \leq 300\ \mu\text{sec}$
$I_{DC}$	Continuous Output Current (Any Drain)	—	—	100	mA	
$I_R$	Latch-Up Protection (Any Drain) Withstand Reverse Current	—	>500	—	mA	Duty cycle $\leq 2\%$ , $t \leq 300\ \mu\text{sec}$
<b>Switching Time (Note 1)</b>						
$t_R$	Rise Time	—	25	30	nsec	Figure 3-1, $C_L = 1000\ \text{pF}$
$t_F$	Fall Time	—	25	30	nsec	Figure 3-1, $C_L = 1000\ \text{pF}$
$t_{D1}$	Delay Time	—	15	30	nsec	Figure 3-1, $C_L = 1000\ \text{pF}$
$t_{D2}$	Delay Time	—	32	50	nsec	Figure 3-1, $C_L = 1000\ \text{pF}$
<b>Power Supply</b>						
$I_S$	Power Supply Current	—	—	4.5	mA	$V_{IN} = 3\text{V}$ (Both Inputs)
		—	—	0.4		$V_{IN} = 0\text{V}$ (Both Inputs)

**Note 1:** Switching times ensured by design.

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## TC4404/TC4405 ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Over operating temperature range with  $4.5V \leq V_{DD} \leq 18V$ , unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
$V_{IH}$	Logic 1, High Input Voltage	2.4	—	—	V	
$V_{IL}$	Logic 0, Low Input Voltage	—	—	0.8	V	
$I_{IN}$	Input Current	-10	—	10	$\mu A$	$0V \leq V_{IN} \leq V_{DD}$
<b>Output</b>						
$V_{OH}$	High Output Voltage	$V_{DD} - 0.025$	—	—	V	
$V_{OL}$	Low Output Voltage	—	—	0.025	V	
$R_O$	Output Resistance	—	9	12	$\Omega$	$I_{OUT} = 10 \text{ mA}$ , $V_{DD} = 18V$ ; Any Drain
$I_{PK}$	Peak Output Current (Any Drain)	—	1.5	—	A	Duty cycle $\leq 2\%$ , $t \leq 300 \mu\text{sec}$
$I_{DC}$	Continuous Output Current (Any Drain)	—	—	100	mA	
$I_R$	Latch-Up Protection (Any Drain) Withstand Reverse Current	—	>500	—	mA	Duty cycle $\leq 2\%$ , $t \leq 300 \mu\text{sec}$
<b>Switching Time (Note 1)</b>						
$t_R$	Rise Time	—	—	40	nsec	Figure 3-1, $C_L = 1000 \text{ pF}$
$t_F$	Fall Time	—	—	40	nsec	Figure 3-1, $C_L = 1000 \text{ pF}$
$t_{D1}$	Delay Time	—	—	40	nsec	Figure 3-1, $C_L = 1000 \text{ pF}$
$t_{D2}$	Delay Time	—	—	60	nsec	Figure 3-1, $C_L = 1000 \text{ pF}$
<b>Power Supply</b>						
$I_S$	Power Supply Current	—	—	8	mA	$V_{IN} = 3V$ (Both Inputs)
		—	—	0.6		$V_{IN} = 0V$ (Both Inputs)

**Note 1:** Switching times ensured by design.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin No. (8-Pin PDIP, SOIC, CERDIP)	Symbol	Description
1	V <sub>DD</sub>	Supply input, 4.5V to 18V.
2	IN A	Control input A, TTL/CMOS compatible input.
3	IN B	Control input A, TTL/CMOS compatible input.
4	GND	Ground.
5	B BOTTOM	Output B, pull-down.
6	B TOP	Output B, pull-up.
7	A BOTTOM	Output A, pull-down.
8	A TOP	Output A, pull-up.

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## 3.0 APPLICATIONS INFORMATION

### 3.1 Circuit Layout Guidelines

Avoid long power supply and ground traces (added inductance causes unwanted voltage transients). Use power and ground planes wherever possible.

In addition, it is advisable that low ESR bypass capacitors (4.7  $\mu$ F or 10  $\mu$ F tantalum) be placed as close to the driver as possible. The driver should be physically located as close to the device it is driving as possible to minimize the length of the output trace.



**FIGURE 3-1:** Switching Time Test Circuit

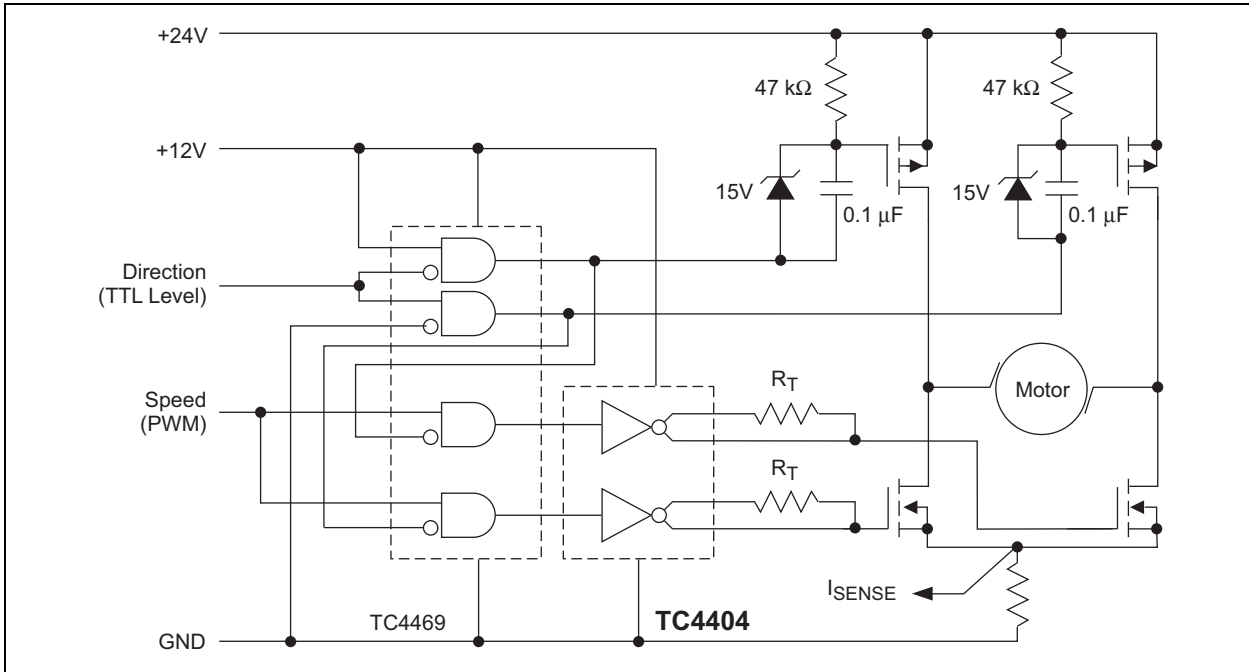
### 3.2 Typical Applications



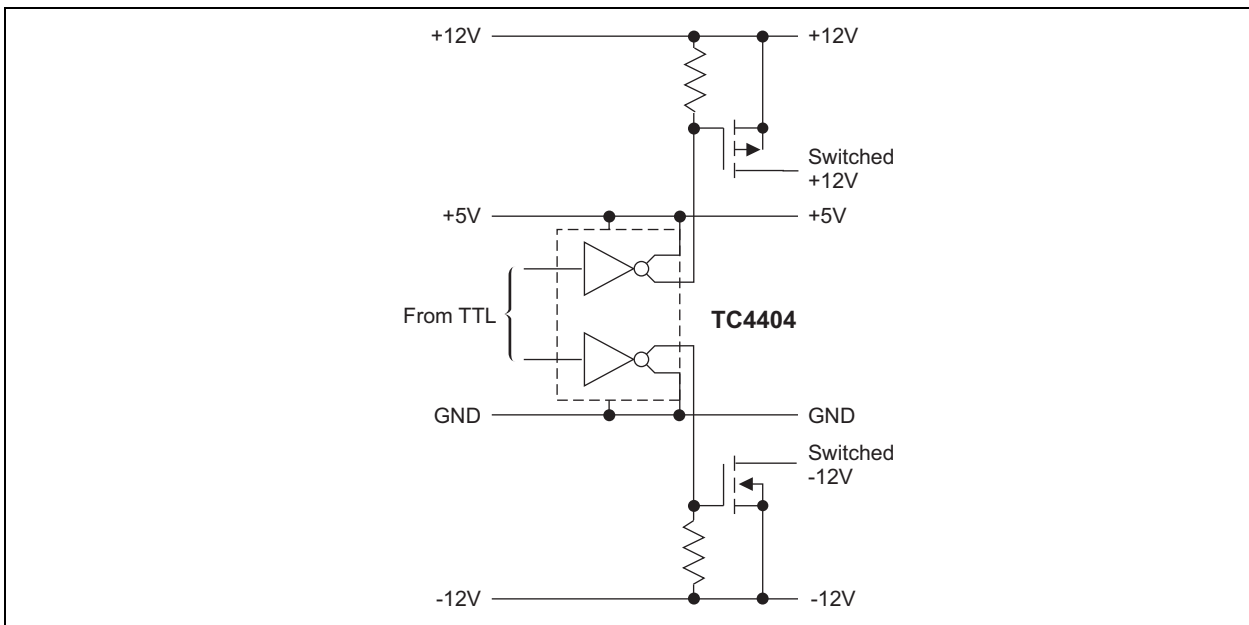
**FIGURE 3-2:** Zero Crossover Current Totem-Pole Switch



**FIGURE 3-3:** Driving Bipolar Transistors



**FIGURE 3-4:** Servo Motor Control



**FIGURE 3-5:** Reach-Up and Reach-Down Driving

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## 4.0 TYPICAL CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.





## TYPICAL CHARACTERISTICS (CONTINUED)



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## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

Package marking data not available at this time.

### 5.2 Taping Form



## 5.3 Package Dimensions

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

### 8-Pin Plastic DIP



Dimensions: inches (mm)

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## Package Dimensions (Continued)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

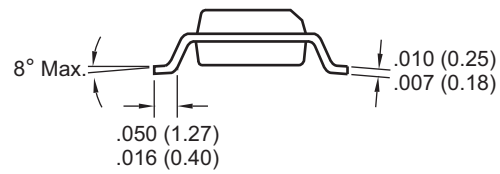
### 8-Pin Cerdip (Narrow)



Dimensions: inches (mm)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

## 8-Pin SOIC



Dimensions: inches (mm)

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## 6.0 REVISION HISTORY

### Revision D (December 2012)

Added a note to each package outline drawing.

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