

### General Description

The MIC705, MIC706, MIC707, and MIC708 are inexpensive microprocessor supervisory circuit that monitors power supplies in microprocessor based systems. The circuit functions include a watchdog timer, microprocessor reset, backup battery switchover, power failure warning and a debounced manual reset input.

The MIC705 and MIC706 offer a watchdog timer function while the MIC707 and MIC708 have an active high reset output in addition to the active low reset output.

Supply voltage monitor levels of 4.65V and 4.4V are available. The MIC705 and MIC707 have a nominal reset threshold level of 4.65V while the MIC706 and MIC708 have a 4.4V nominal threshold level. When the supply voltage drops below the respective reset threshold level, /RESET is asserted.

### Features

- Debounced manual reset input is TTL/CMOS Compatible
- Watchdog timer, 1.6s (MIC705/706)
- 4.65V or 4.40V Precision Voltage Monitor
- Early power fail warning or low battery detect

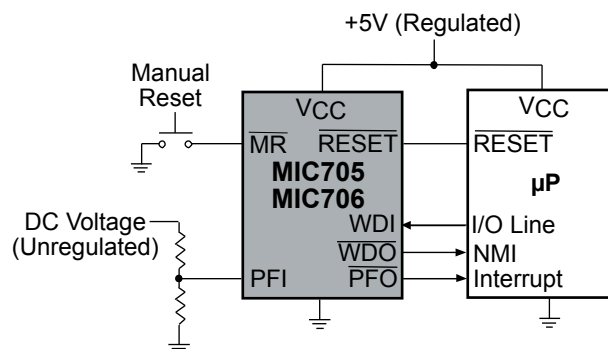
### Applications

- Automotive systems
- Intelligent systems
- Critical microprocessor power monitoring
- Battery powered computers
- Computers
- Controllers

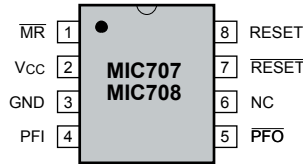
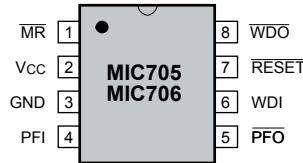
### Ordering Information

| Part Number |          | Temperature Range | Package    |
|-------------|----------|-------------------|------------|
| Standard    | Pb-Free  |                   |            |
| MIC70_N     | MIC70_NY | -40°C to +85°C    | 8-Pin PDIP |
| MIC70_M     | MIC70_MY | -40°C to +85°C    | 8-Pin SOIC |

### Typical Application



## Pin Configuration



**8-Pin PDIP Package**  
**8-Pin SOIC Package**

## Pin Description

| Pin Number<br>MIC705/06 | Pin Number<br>MIC707/08 | Pin Name        | Pin Function  |
|-------------------------|-------------------------|-----------------|---|
| 1                       | 1                       | /MR             | Manual Reset Input forces /RESET to assert when pulled below 0.8V. An internal pull-up current of 250 $\mu$ A on this input forces it high when left floating. this input can also be driven from TTL or CMOS logic.  |
| 2                       | 2                       | V <sub>CC</sub> | Primary supply input, +5V   |
| 3                       | 3                       | GND             | IC ground pin, 0V reference   |
| 4                       | 4                       | PFI             | Power Fail Input. Internally connected to the power fail comparator which is referenced to 1.25V. The Power Fail Output (/PFO) remains high if PFI is above 1.25V. PFI should be connected to GND or V <sub>OUT</sub> if the power fail comparator is not used.   |
| 5                       | 5                       | /PFO            | Power Fail Output. The power fail comparator is independent of all other function on this device.   |
| 6                       | N/A                     | WDI             | Watch Dog Input. The WDI input monitors microprocessor activity, an internal watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, /WDO is forced to active low. the watchdog function can be disabled by floating the WDI pin.  |
| N/A                     | 6                       | N/C             | Not Internally Connected  |
| 7                       | 7                       | /RESET          | /RESET is asserted if either V <sub>CC</sub> goes below the reset threshold voltage or by low signal on the manual reset input (/MR). /RESET remains asserted for one reset timeout period (200ms) after V <sub>CC</sub> exceeds the reset threshold voltage or after the manual reset pin transition from low to high. The watchdog timer will not assert /RESET unless /WDO is connected to /MR |
| 8                       | N/A                     | /WDO            | Output for the Watchdog Timer. The watchdog timer resets itself with each transition o the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, /WDO is forced low. /WDO will also be forced low id V <sub>CC</sub> is below the reset threshold voltage and will remain low until V <sub>CC</sub> returns to a valid level.                           |
| N/A                     | 8                       | RESET           | RESET is the compliment of /RESET and is asserted if either V <sub>CC</sub> goes below the reset threshold voltage or by a low signal on the manual reset input (/MR). RESET is suitable for microprocessor systems that use active high reset.   |

**Absolute Maximum Ratings<sup>(1)</sup>**

|   |                               |
|---|-------------------------------|
| Terminal Voltage                            |                               |
| $V_{CC}$ .....                              | -0.3V to +6.0V                |
| All other inputs .....                      | -0.3V to ( $V_{OUT} + 0.3V$ ) |
| Input Current                               |                               |
| $V_{CC}$ , Gnd .....                        | 25mA                          |
| Output Current (all outputs) .....          | 20mA                          |
| Lead Temperature (soldering, 10 sec.) ..... | 300°C                         |
| Storage Temperature .....                   | -65°C to +150°C               |

**Operating Ratings<sup>(2)</sup>**

|                                |                |
|--------------------------------|----------------|
| Operating Temperature Range    |                |
| MIC70_N .....                  | -40°C to +85°C |
| MIC70_M .....                  | -40°C to +85°C |
| Power Dissipation (PDIP) ..... | 475mW          |
| Power Dissipation (SOP) .....  | 400mW          |

**Electrical Characteristics<sup>(3)</sup>**

$V_{CC} = 4.75V$  to  $5.5V$  for MIC705/07;  $V_{CC} = 4.5V$  to  $5.5V$  for MIC706/08;  $T_A$  = Operating Temperature Range, **bold** values indicate  $-40^\circ C \leq T_A \leq +85^\circ C$ ; unless noted

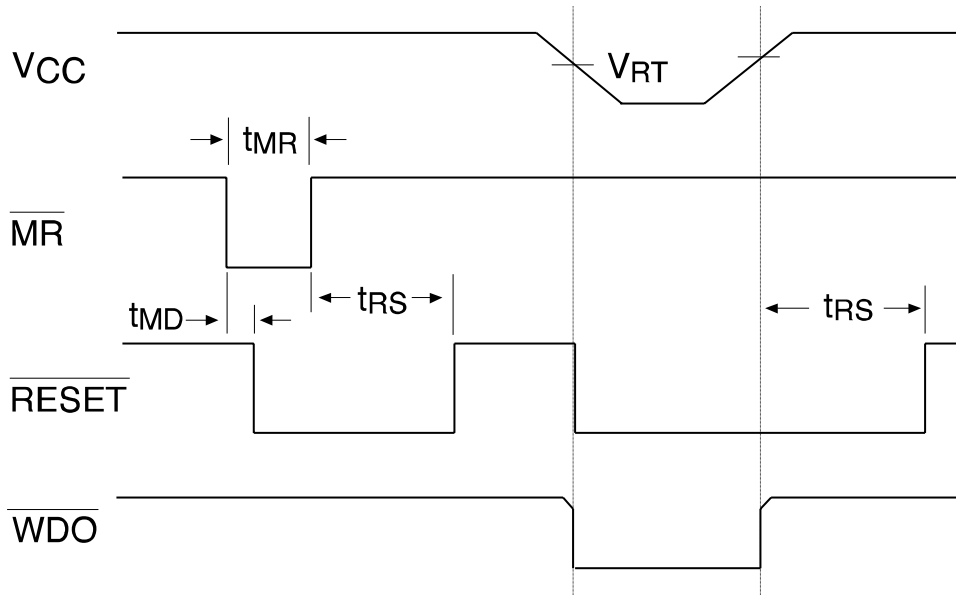
| Parameter                           | Conditions  | Min.            | Typ.      | Max        | Units              |
|-------------------------------------|---|-----------------|-----------|------------|--------------------|
| Operating Voltage Range, $V_{CC}$   | MIC70_  | 1.4             |           | 5.5        | V                  |
| Supply Current                      | MIC70_  |                 |           | 60         | $\mu A$            |
| Reset Voltage Threshold             | MIC705, MIC707  | 4.50            | 4.65      | 4.75       | V                  |
|                                     | MIC706, MIC708  | 4.25            | 4.4       | 4.5        | V                  |
| Reset Threshold Hysteresis          |   |                 | 40        |            | mV                 |
| Reset Pulse Width, $t_{RS}$         |   | 140             | 200       | 280        | ms                 |
| /RESET Output Voltage               | $I_{Source} = 80\mu A$<br>$I_{Sink} = 3.2mA$<br>MIC70_C, $I_{Sink} = 50\mu A$ , $V_{CC} = 1.4V$ | $V_{CC} - 1.5V$ |           | 0.4<br>0.3 | V<br>V             |
| RESET Output Voltage                | $I_{Source} = 80\mu A$<br>$I_{Sink} = 3.2mA$  | $V_{CC} - 1.5V$ |           | 0.4        | V<br>V             |
| Watchdog Timeout Period, $t_{WD}$   |   | 1.0             | 1.6       | 2.25       | sec                |
| WDI Minimum Input Pulse, $t_{WP}$   | $V_{IL} = 0.4V$ , $V_{IH} = 80\%$ of $V_{CC}$   | 50              |           |            | ns                 |
| WDI Threshold Voltage               | $V_{IH}$ , $V_{CC} = 5V$<br>$V_{IL}$ , $V_{CC} = 5V$  | 3.5             |           | 0.8        | V<br>V             |
| WDI Input Current                   | WDI = 0V<br>WDI = $V_{CC}$  | -150            | -50<br>50 | 150        | $\mu A$<br>$\mu A$ |
| WDO Output Voltage                  | $I_{Source} = 800\mu A$<br>$I_{Sink} = 1.2mA$   | $V_{CC} - 1.5V$ |           | 0.4        | V<br>V             |
| /MR Pull-Up Current                 | /MR = 0V  | 100             | 250       | 600        | $\mu A$            |
| /MR Pulse Width, $t_{MR}$           |   | 150             |           |            | ns                 |
| /MR Input Threshold                 | $V_{IL}$<br>$V_{IH}$  | 2.0             |           | 0.8        | V<br>V             |
| /MR to Reset Output Delay, $t_{MD}$ |   |                 |           | 250        | ns                 |
| PFI Input Threshold                 | $V_{CC} = 5V$   | 1.2             | 1.25      | 1.3        | V                  |
| PFI Input Current                   |   | -25             | 0.01      | +25        | nA                 |
| /PFO Output Voltage                 | $I_{Sink} = 3.2mA$<br>$V_{CC} = 5V$ , $I_{Source} = 800\mu A$                                   | $V_{CC} - 1.5V$ |           | 0.4        | V<br>V             |

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating rating.

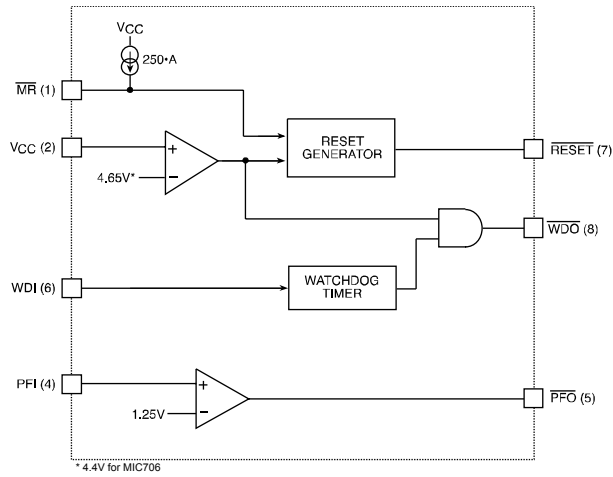
**Note 3.** Specification for packaged product only.

# Timing Diagram

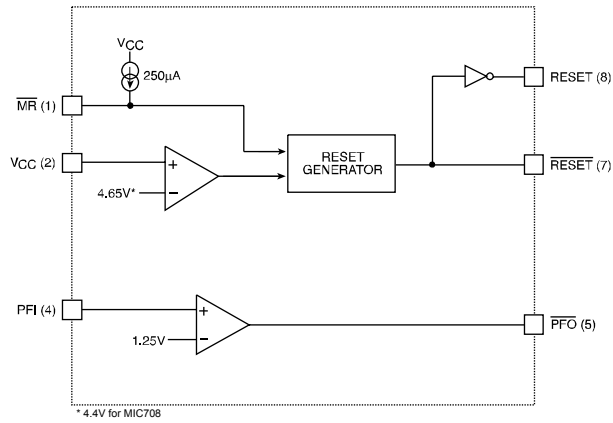


Timing Diagram for Reset

# Block Diagrams



**MIC705/MIC706 Block diagram**



**MIC707/MIC708 Block diagram**

## Applications Information

### Battery Switchover Section

The MIC691/693 monitors the supply voltage applied to the  $V_{CC}$  pin. Whenever  $V_{CC}$  falls below the reset threshold voltage and  $V_{BATT}$ , the device enters battery-backup mode. When this happens, the auxiliary supply on  $V_{BATT}$  is routed through a low impedance PMOS switch to the  $V_{OUT}$  pin. The  $V_{OUT}$  pin is capable of sourcing up to 25mA when in the backup mode.  $V_{CC}$  is routed to  $V_{OUT}$  through a large PMOS switch during normal operation ( $V_{CC} > V_{BATT}$ ) and can source continuous currents of up to 250mA.  $V_{OUT}$  can be used to drive CMOS RAM. The BATT ON Pin can be used to indicate the status of battery backup mode or as the base drive for an external pass transistor when  $V_{OUT}$  has to source more than 25mA in battery-backup mode.  $V_{CC}$  is connected to  $V_{OUT}$  and the substrate whenever  $V_{CC}$  exceeds the reset threshold. If  $V_{BATT}$  is connected to a voltage source that is greater than 0.6V above  $V_{CC}$ , the parasitic diode of the  $V_{BATT}$  switch will conduct from the  $V_{BATT}$  to the substrate.

### Microprocessor Reset

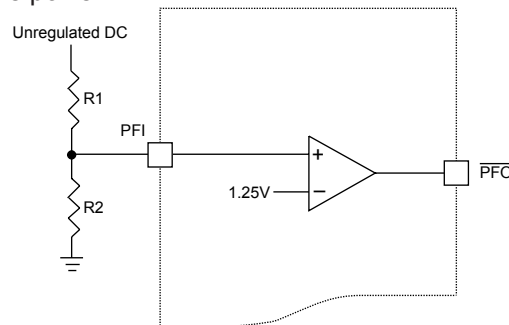
The  $/RESET$  pin is asserted whenever  $V_{CC}$  falls below the reset threshold voltage. The reset pin remains asserted for a period of 200ms after  $V_{CC}$  has risen above the reset threshold voltage. The reset timeout period can also be selected by the end user, see Table 1. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure.  $/RESET$  will remain valid with  $V_{CC}$  as low as 1.4V and when auxiliary power is connected to  $V_{BATT}$  ( $V_{BATT} > 2.0V$ ), the reset pin will remain valid with  $V_{CC}$  from 0V to 5.5V.

### Chip Enable Gating

The MIC691/693 also include memory protection circuitry which inhibits the writing of memory during a power fail condition. During normal operation, chip enable transitions are gated through a series transmission gate from  $/CE IN$  to  $/CE OUT$ . The typical propagation delay through the chip enable gating circuitry is 2ns.  $/CE OUT$  follows  $/CE IN$  unless  $V_{CC}$  drops below the reset threshold voltage, at which time  $/CE OUT$  will remain high until  $V_{CC}$  returns to a valid level. EEPROMs can be write protected in a similar manner by connecting the  $/CE OUT$  pin to the store or write input.

### Power Fail Warning

An additional comparator which is independent of the other functions on the MIC691/693 is provided for early warning of power failure. An external voltage divider can be used to compare unregulated DC to an internal 1.25V reference. The voltage divider ratio on the input of the power-fail comparator (PFI) can be chosen so as to trip the power fail comparator a few milliseconds before  $V_{CC}$  falls below the maximum reset threshold voltage. The output of the power-fail comparator ( $/PFO$ ) can be used to interrupt the microprocessor when used in this mode and execute shut-down procedures prior to power loss. Hysteresis can be added to this comparator with external resistors, as is commonly done with any comparator. When  $V_{CC} < V_{BATT} - 1.2V$  (typ.), the power-fail comparator is turned off and  $/PFO$  is pulled low in order to conserve power.

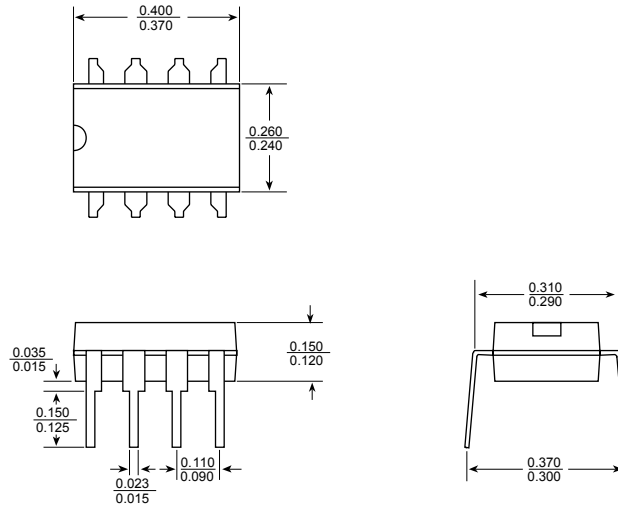


**Power Fail Comparator**

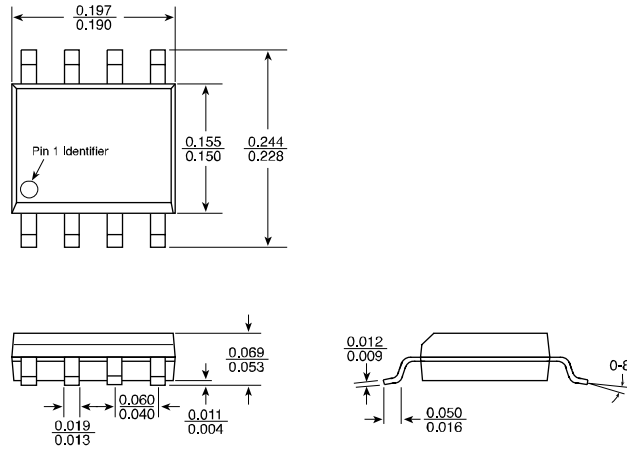
### Watchdog Timer

The microprocessor can be monitored by connecting the WDI pin (watchdog input) to a bus line or an I/O line. If a transition doesn't occur on the WDI pin within the watchdog timeout (Table 1.), the microprocessor is reset.  $/RESET$  will remain asserted for 200ms when this occurs. A minimum pulse of 100ns or any transition low-to-high or high-to-low on the WDI pin will reset the watchdog timer. The output of the watchdog timer (WDO) will remain high, if WDI sees a valid transition within the watchdog period or if  $V_{CC}$  falls below the reset threshold as the watchdog timer is disabled when this happens.

**Package Information**



**8-Pin PDIP (N)**



**8-Pin SOIC (M)**

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