# Green Hybrid Digital Four Phase PWM Controller for Intel VR12.5™ CPUs

## ISL95820

The ISL95820 Pulse Width Modulation (PWM) controller IC provides a complete low-cost solution for Intel VR12.5™ compliant microprocessor core power supplies. It provides the control and protection for a Voltage Regulator (VR). The VR incorporates 3 integrated drivers and can operate in 4-, 3-, 2- or 1-phase configurations. The VR uses a serial control bus to communicate with the CPU and achieve lower cost and smaller board area.

The VR utilizes Intersil's Robust Ripple Regulator R3 Technology™. The R3™ modulator has many advantages compared to traditional modulators, including faster transient response, variable switching frequency in response to load transients, and improved light load efficiency due to diode emulation mode with load-dependent low switching frequency.

The ISL95820 has several other key features. It supports either DCR current sensing with a single NTC thermistor for DCR temperature compensation, or more precise resistor current sensing if desired. The output comes with remote voltage sense, programmable $V_{BOOT}$ voltage, $I_{MAX}$, voltage transition slew rate and switching frequency, adjustable overcurrent protection and Power-Good signal.

## Features

- Serial data bus
- SMBus/PMBus/$I^2C$ interface with SVID conflict free
- Configurable 4-, 3-, 2- or 1-phase for the output using three integrated gate drivers
- Green Hybrid Digital R3™ modulator
  - Excellent transient response
  - Phase shedding with power state selection
  - Diode emulation in single-phase for high light-load efficiency
- 0.5% system accuracy over-temperature
- Supports multiple current sensing methods
  - Lossless inductor DCR current sensing
  - Precision resistor current sensing
- Differential remote voltage sensing
- Programmable $V_{BOOT}$ voltage at start-up
- Resistor programmable $I_{MAX}$, load line, diode emulation, slope compensation, and switching frequency
- Adaptive body diode conduction time reduction

## Applications

- Intel VR12.5 desktop computers

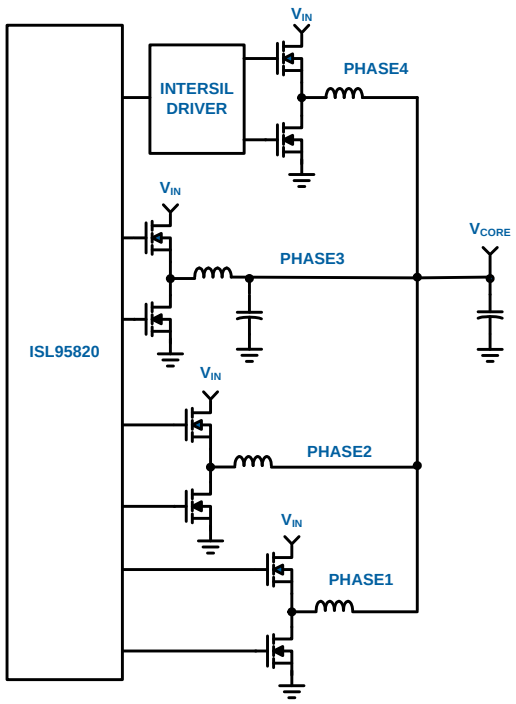


**FIGURE 1. SIMPLIFIED APPLICATION CIRCUIT**

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# Ordering Information

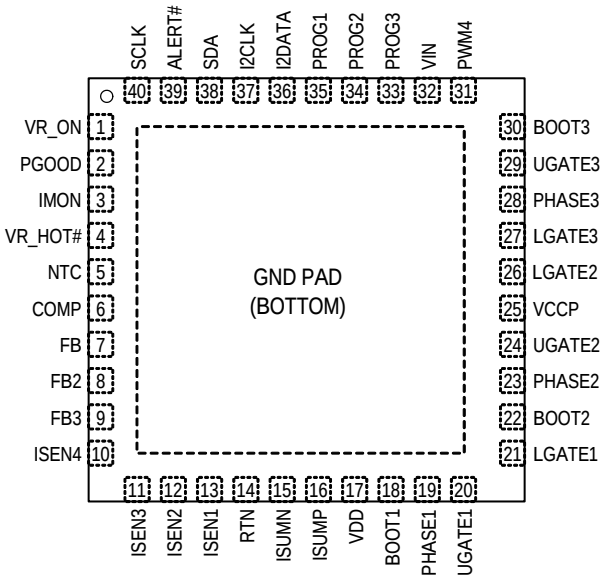
| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL95820CRTZ | ISL9582 0CRTZ | 0 to +70 | 40 Ld 5x5 TQFN | L40.5x5 |
| ISL95820IRTZ | ISL9582 0IRTZ | -40 to +85 | 40 Ld 5x5 TQFN | L40.5x5 |
| ISL95820EVAL1Z | Evaluation Board | | | |

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL95820. For more information on MSL please see techbrief TB363.

# Pin Configuration

ISL95820
(40 LD TQFN)
TOP VIEW



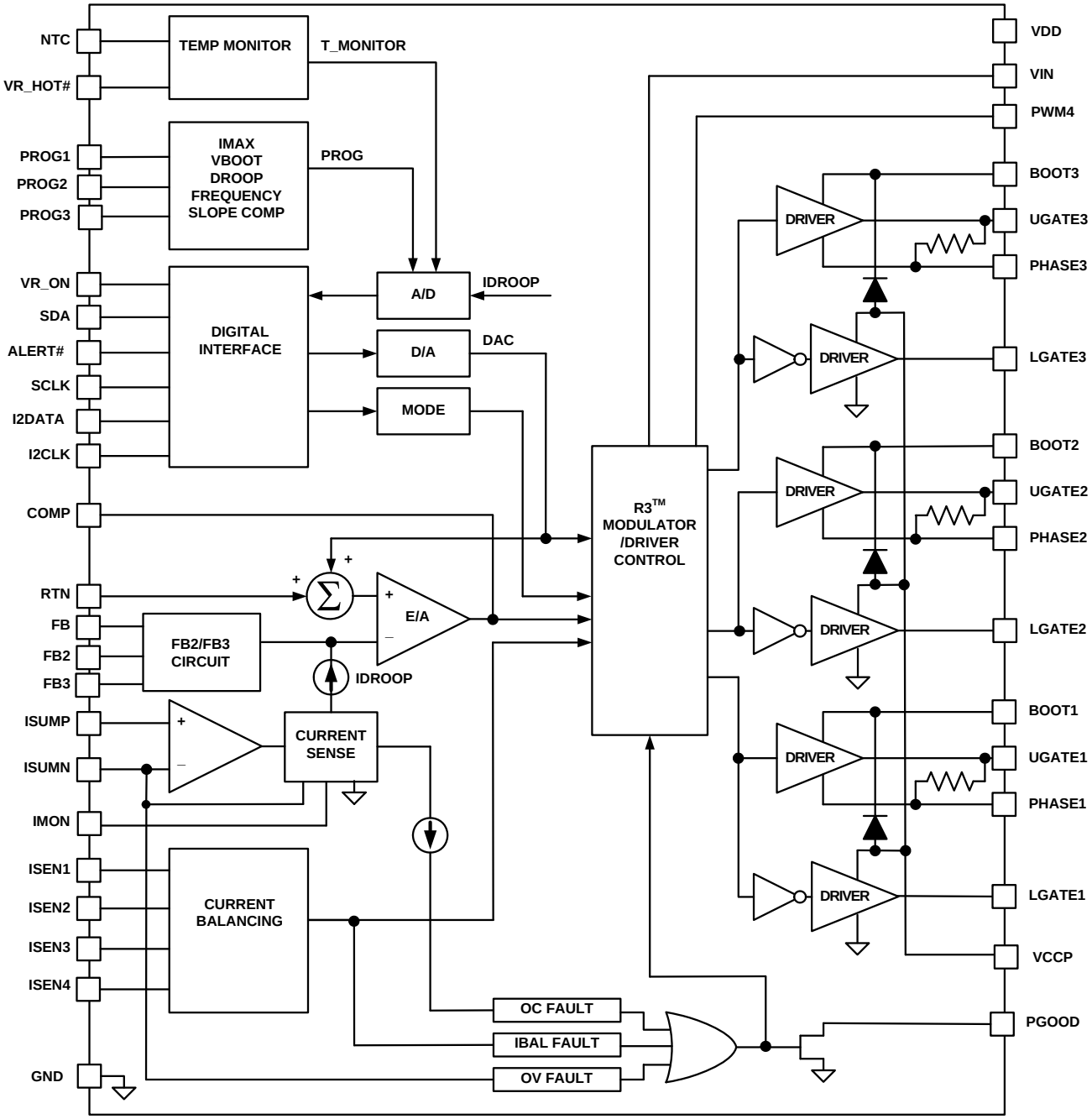
# Pin Descriptions

| PIN # | SYMBOL | DESCRIPTION |
|---|---|---|
| BOTTOM PAD | GND | Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pad. It should also be used as the thermal pad for heat removal. |
| 1 | VR_ON | Controller enable input. A high level logic signal on this pin enables the controller. |
| 2 | PGOOD | Power-Good open-drain output indicating when VR is able to supply regulated voltage. Pull-up externally to VDD or to a lower supply, such as 3.3V. |
| 3 | IMON | VR output current monitor. IMON sources a current proportional to the regulator output current. A resistor to ground determines the scaling of the IMON voltage to output current. |
| 4 | VR_HOT# | Open drain thermal overload output indicator. Part of the communication bus with the CPU. |
| 5 | NTC | The thermistor input to VR_HOT# circuit. Use it to monitor VR temperature. |
| 6 | COMP | This pin is the output of the VR error amplifier. It provides error amplifier feedback to the compensation network. |
| 7 | FB | This pin is the inverting input of the VR error amplifier. A DAC-derived voltage equal to the VID reference voltage is connected internally to the non-inverting error amplifier input. |
| 8 | FB2 | There is an internal switch between FB pin and FB2 pin. The switch is off (open) when VR is in 1-phase mode and is on (closed) otherwise. The components connecting to FB2 are used to adjust the compensation in 1-phase mode to achieve optimum performance for VR. |
| 9 | FB3 | There is an internal switch between pins FB and FB3. The switch will be on (closed) in droop mode (whenever programmable output DC loadline operation is enabled), and off (open) when no-droop mode is selected. The purpose is to include a resistor in parallel with the fixed droop resistor when droop is active, and to isolate that resistor when droop is inactive. This parallel resistor increases the open-loop gain of the compensator while droop is active. The effective droop (output DC loadline) programming resistance is the parallel combination of these two resistors. |
| 10 | ISEN4 | Individual current sensing for Phase4. When ISEN4 is pulled to VDD (5V), the controller will disable VR Phase 4. This signal is used to monitor for and to correct phase current imbalance. |
| 11 | ISEN3 | Individual current sensing for Phase3. When ISEN4 and ISEN3 is pulled to VDD (5V), the controller will disable VR Phases 4 and 3. Do not disable Phase 3 without also disabling Phase 4. This signal is used to monitor for and to correct phase current imbalance. |
| 12 | ISEN2 | Individual current sensing for Phase 2. When ISEN4, ISEN3 and ISEN2 are pulled to VDD (5V), the controller will disable VR Phases 4, 3 and 2. Do not disable Phase 2 without also disabling Phases 3 and 4. This signal is used to monitor for and to correct phase current imbalance. |
| 13 | ISEN1 | Individual current sensing for Phase 1. This signal is used to monitor for and to correct phase current imbalance. |
| 14 | RTN | Remote ground (return) voltage sensing. Part of the differential remote VR voltage sense network. |
| 15, 16 | ISUMN and ISUMP | VR droop current sensing inputs. |
| 17 | VDD | +5V bias power. |
| 18 | BOOT1 | Phase 1 internal gate driver high-side MOSFET bootstrap capacitor connection. Connect an MLCC capacitor between the BOOT1 and the PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT1 pin each time the PHASE1 pin drops below VCCP minus the voltage dropped across the internal boot diode. |
| 19 | PHASE1 | Current return path for Phase 1 high-side MOSFET gate driver. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase1. |
| 20 | UGATE1 | Output of Phase 1 high-side MOSFET gate driver. Connect the UGATE1 pin to the gate of Phase 1 high-side MOSFET. |
| 21 | LGATE1 | Output of Phase 1 low-side MOSFET gate driver. Connect the LGATE1 pin to the gate of Phase 1 low-side MOSFET. |
| 22 | BOOT2 | Phase 2 internal gate driver high-side MOSFET bootstrap capacitor connection. Connect an MLCC capacitor between the BOOT2 and the PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT2 pin, each time the PHASE2 pin drops below VCCP minus the voltage dropped across the internal boot diode. |
| 23 | PHASE2 | Current return path for Phase 2 high-side MOSFET gate driver. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 2. |
| 24 | UGATE2 | Output of Phase 2 high-side MOSFET gate driver. Connect the UGATE2 pin to the gate of Phase 2 high-side MOSFET. |
| 25 | VCCP | Input voltage bias for the internal gate drivers. Connect +5V or +12V to the VCCP pin. Decouple with at least 1µF of an MLCC capacitor. Diode Emulation Mode must be disabled (using PROG2 pin resistor) for +5V driver operation. |

## Pin Descriptions (Continued)

| PIN # | SYMBOL | DESCRIPTION |
|---|---|---|
| 26 | LGATE2 | Output of Phase 2 low-side MOSFET gate driver. Connect the LGATE2 pin to the gate of Phase 2 low-side MOSFET. |
| 27 | LGATE3 | Output of Phase 3 low-side MOSFET gate driver. Connect the LGATE3 pin to the gate of Phase 3 low-side MOSFET. |
| 28 | PHASE3 | Current return path for Phase 3 high-side MOSFET gate driver. Connect the PHASE3 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 3. |
| 29 | UGATE3 | Output of Phase 3 high-side MOSFET gate driver. Connect the UGATE3 pin to the gate of Phase 3 high-side MOSFET. |
| 30 | BOOT3 | Phase 3 internal gate driver high-side MOSFET bootstrap capacitor connection. Connect an MLCC capacitor between the BOOT3 and the PHASE3 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT3 pin, each time the PHASE3 pin drops below VCCP minus the voltage dropped across the internal boot diode. |
| 31 | PWM4 | PWM output for Phase 4. Phase 4 requires an external gate driver device. The Intersil ISL6625A driver is recommended. |
| 32 | VIN | Input supply voltage, used for feed-forward. Connect this pin to the input voltage of the output drive stages. |
| 33 | PROG3 | A resistor from the PROG3 pin to GND programs the internal modulator slope compensation and switching frequency. |
| 34 | PROG2 | A resistor from the PROG2 pin to GND programs the initial power-up voltage ($V_{BOOT}$), enables/disables the DC loadline (droop) function, and enables/disables diode emulation mode (DEM) in Power States 2 and 3 (PS2 and PS3). |
| 35 | PROG1 | A resistor from PROG1 pin to GND programs $I_{MAX}$, the designed nominal maximum load current of the VR. The value of $I_{MAX}$ establishes the scaling of the reported VR output current, which can be read via the SVID or PMBus interfaces. The PROG1 resistor is chosen such that the reported $I_{MAX}$ current is FFh when the output current is equal to the maximum load current. |
| 36, 37 | I2DATA, I2CLK | Interface of SMBus/PMBus/$I^2C$. Tie to VCC with 4.7kΩ pull-up resistor when not used. |
| 38, 39, 40 | SDA, ALERT#, SCLK, | SVID communication bus between the CPU and the VR. |

# Block Diagram



# Typical Application Circuit

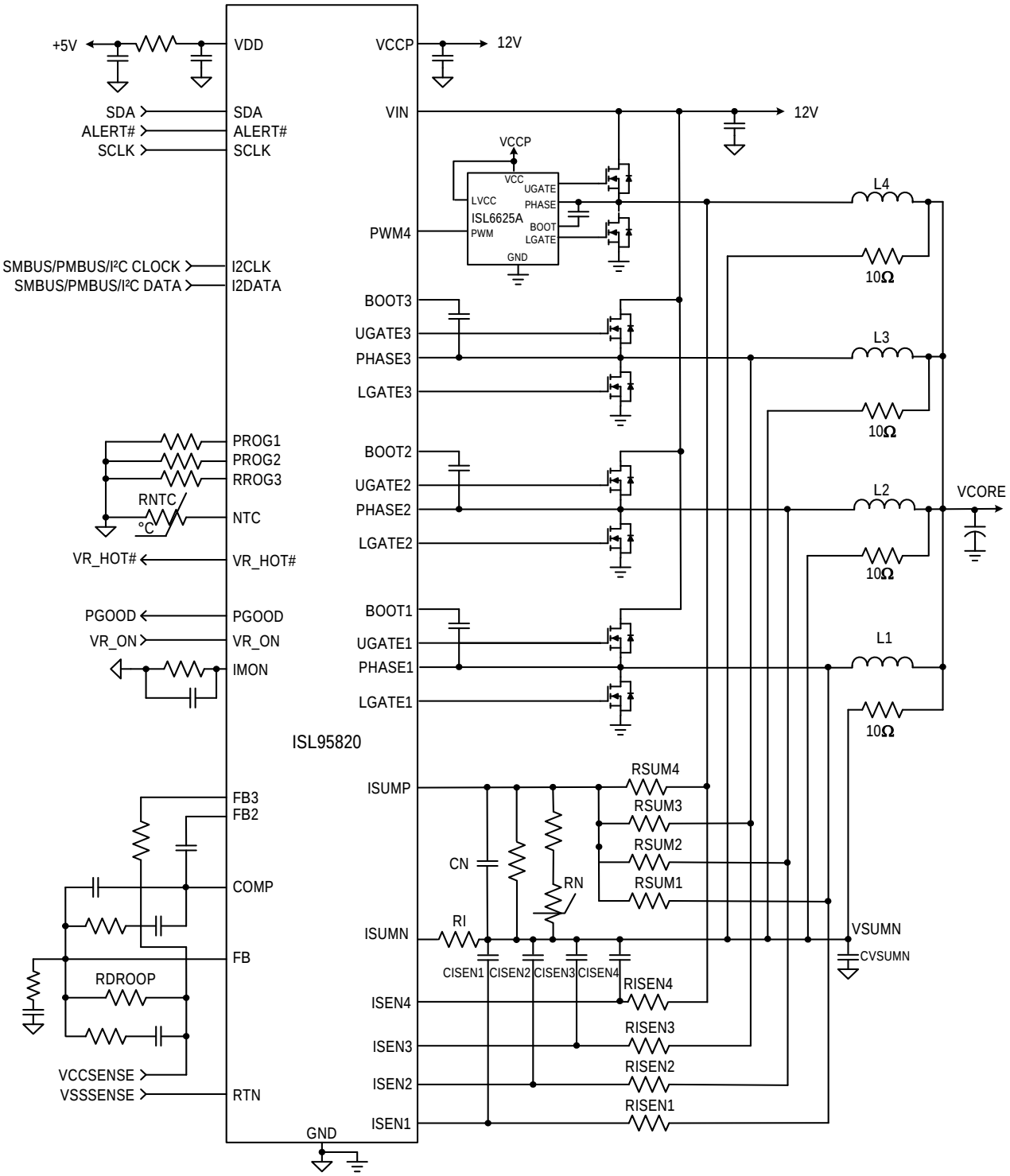



FIGURE 2. TYPICAL ISL95820 APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

## Absolute Maximum Ratings

VDD . . . . . -0.3V to +7V
VIN . . . . . +28V
VCCP . . . . . +15V
BOOT . . . . . -0.3V to +36V
UGATE . . . . . $V_{PHASE}$ - 0.3$V_{DC}$ to $V_{BOOT}$ + 0.3V
$V_{PHASE}$ - 3.5V (<100ns Pulse Width, 2µJ) to $V_{BOOT}$ + 0.3V
LGATE . . . . . GND - 0.3$V_{DC}$ to $V_{VCCP}$ + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to $V_{VCCP}$ + 0.3V
PHASE . . . . . GND - 0.3$V_{DC}$ to 25$V_{DC}$
GND - 8V (<400ns, 20µJ) to 30V (<200ns, $V_{BOOT}$ - GND < 36V)
Open Drain Outputs, PGOOD, VR_HOT#, ALERT# . . . . . -0.3V to +7V
All Other Pins . . . . . -0.3V to VDD + 0.3V

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 40 Ld TQFN Package (Notes 4, 5) . . . . . | 31 | 3 |

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C

## Recommended Operating Conditions

Supply Voltage, VDD . . . . . +5V ±5%
Input Voltage, VIN (Note 6) . . . . . +4.5V to 20.0V
Driver Supply Voltage, VCCP (Note 6) . . . . . +4.5V to +13.2V
Ambient Temperature
CRTZ . . . . . 0°C to +70°C
IRTZ . . . . . -40°C to +85°C
Junction Temperature
CRTZ . . . . . 0°C to +125°C
IRTZ . . . . . -40°C to +125°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.
6. It is recommended that VIN+VCCP not exceed 24V nominally. For VCCP < 7V, Diode Emulation Mode (DEM) **must** be disabled using the PROG2 pin programming resistor.

## Electrical Specifications

Operating Conditions: $V_{DD}$ = 5V, $T_A$ = 0°C to +70°C (ISL95820CRTZ), $T_A$ = -40°C to +85°C (ISL95820IRTZ), $f_{SW}$ = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature ranges.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **INPUT POWER SUPPLIES** | | | | | | |
| VDD Supply Current | $I_{VDD}$ | $V_{VDD}$ = 5V; VR_ON = 1V | | 6.4 | **8.0** | mA |
| | | $V_{VDD}$ = 5V; VR_ON = 0V | | | **125** | µA |
| VIN Supply Current | $R_{VIN}$ | $V_{VIN}$ = 25V; VR_ON = 1V | | 600 | | kΩ |
| | $I_{VIN}$ | $V_{VIN}$ = 25V; VR_ON = 0V | | | **1** | µA |
| VCCP No Load Switching Supply Current | $I_{VCCP}$ | $V_{VCCP}$ = 12V; $f_{sw}$ = $f_{sw_}$300k; Phases 1-3 active; $C_{BOOT1,2,3}$ = 0.1µF | | 8 | | mA |
| | | $V_{VCCP}$ = 12V; Phases inactive | | 0.72 | **1.5** | mA |
| **POWER-ON-RESET THRESHOLDS** | | | | | | |
| VDD Power-On-Reset Threshold | $VDD\_POR_r$ | $V_{VDD}$ rising | **4.3** | 4.35 | **4.5** | V |
| | $VDD\_POR_f$ | $V_{VDD}$ falling | **4.0** | 4.15 | **4.3** | V |
| VIN Power-On-Reset Threshold | $VIN\_POR_r$ | $V_{VIN}$ rising | **3.75** | 4.00 | **4.5** | V |
| | $VIN\_POR_f$ | $V_{VIN}$ falling | **3.05** | 3.50 | **3.7** | V |
| VCCP Power-On-Reset Threshold | $VCCP\_POR_r$ | $V_{VCCP}$ rising | **4.0** | 4.30 | **4.5** | V |
| | $VCCP\_POR_f$ | $V_{VCCP}$ falling | **3.45** | 3.90 | **4.1** | V |
| **SYSTEM AND REFERENCES** | | | | | | |
| Maximum Output Voltage | $V_{OUT(MAX)}$ | VID = [10110101] | | 2.3 | | V |
| Minimum Output Voltage | $V_{OUT(MIN)}$ | VID = [00000001] | | 0.5 | | V |
| Fast Slew Rate (for VID changes) | | | **10** | 12 | | mV/µs |
| Slow Slew Rate (for VID changes) | | | **2.5** | 3 | | mV/µs |

**Electrical Specifications** Operating Conditions: $V_{DD}$ = 5V, $T_A$ = 0°C to +70°C (ISL95820CRTZ), $T_A$ = -40°C to +85°C (ISL95820IRTZ), $f_{SW}$ = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature ranges. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| System Accuracy | CRTZ Error ($V_{OUT}$) | No load; closed loop, active mode range, VID = 1.00V to 2.3V, | **-0.5** | | **+0.5** | % |
| | | VID = 0.80V to 0.99V | **-5** | | **+5** | mV |
| | | VID = 0.5V to 0.79V | **-8** | | **+8** | mV |
| | IRTZ Error ($V_{OUT}$) | No load; closed loop, active mode range, VID = 1.00V to 2.3V | **-0.8** | | **+0.8** | % |
| | | VID = 0.8V to 0.99V | **-8** | | **+8** | mV |
| | | VID = 0.5V to 0.79V | **-10** | | **+10** | mV |
| Internal $V_{BOOT}$ | | CRTZ | **1.64** | 1.65 | **1.66** | V |
| | | | **1.69** | 1.70 | **1.71** | V |
| | | | **1.74** | 1.75 | **1.76** | V |
| | | IRTZ | **1.635** | 1.65 | **1.665** | V |
| | | | **1.685** | 1.70 | **1.715** | V |
| | | | **1.735** | 1.75 | **1.765** | V |
| **CHANNEL FREQUENCY** | | | | | | |
| 200kHz Configuration | $f_{sw\_}200k$ | | **180** | 200 | **220** | kHz |
| 300kHz Configuration | $f_{sw\_}300k$ | | **275** | 300 | **325** | kHz |
| 450kHz Configuration | $f_{sw\_}450k$ | | **410** | 450 | **490** | kHz |
| **AMPLIFIERS** | | | | | | |
| Current-Sense Amplifier Input Offset | CRTZ | $I_{FB}$ = 0A | **-0.2** | | **+0.2** | mV |
| | IRTZ | $I_{FB}$ = 0A | **-0.3** | | **+0.3** | mV |
| Error Amp DC Gain | $A_{V0}$ | | | 119 | | dB |
| Error Amp Gain-Bandwidth Product | GBW | $C_L$ = 20pF | | 17 | | MHz |
| **ISEN** | | | | | | |
| ISEN Offset Voltage | | Maximum of $I_{SEN}$ - Minimum of $I_{SEN}$ | | | **1** | mV |
| ISEN Input Bias Current | | | | 20 | | nA |
| **GATE DRIVER BOOTSTRAP SWITCHES (Phases 1-3)** | | | | | | |
| On-resistance | $R_F$ | | | 40 | | Ω |
| Reverse Leakage | $I_R$ | $V_{VDDP}$ = 12V, $V_{VR\_ON}$ = 0, BOOT and PHASE connected and total current measured | | 0.2 | | µA |
| **GATE DRIVER OUTPUTS (Phases 1-3)** | | | | | | |
| UGATE Pull-Up Resistance | $R_{UGPU}$ | 250mA Source Current | | 3.70 | | Ω |
| UGATE Source Current | $I_{UGSRC}$ | UGATE - PHASE = 2.5V | | 1.30 | | A |
| UGATE Pull-Down Resistance | $R_{UGPD}$ | 250mA Sink Current | | 1.41 | | Ω |
| UGATE Sink Current | $I_{UGSNK}$ | UGATE - PHASE = 2.5V | | 1.27 | | A |
| LGATE Pull-Up Resistance | $R_{LGPU}$ | 250mA Source Current | | 2.75 | | Ω |
| LGATE Source Current | $I_{LGSRC}$ | LGATE - VSSP = 2.5V | | 1.75 | | A |
| LGATE Pull-Down Resistance | $R_{LGPD}$ | 250mA Sink Current | | 0.60 | | Ω |
| LGATE Sink Current | $I_{LGSNK}$ | LGATE - VSSP = 2.5V | | 2.14 | | A |

**Electrical Specifications** Operating Conditions: $V_{DD}$ = 5V, $T_A$ = 0°C to +70°C (ISL95820CRTZ), $T_A$ = -40°C to +85°C (ISL95820IRTZ), $f_{SW}$ = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature ranges. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| UGATE to LGATE Deadtime | $t_{UGFLGR}$ | UGATE falling to LGATE rising, no load, $V_{VDDP}$ = 7V | | 59 | | ns |
| LGATE to UGATE Deadtime | $t_{LGFUGR}$ | LGATE falling to UGATE rising, no load, $V_{VDDP}$ = 7V | | 37 | | ns |
| **PWM4 (Phase 4)** | | | | | | |
| PWM4 Output Low | $V_{0L}$ | Sinking 5mA | | | **1.0** | V |
| PWM4 Output High | $V_{0H}$ | Sourcing 5mA | | 4.5 | | V |
| PWM4 Tri-State Leakage | | PWM = 2.5V | | 1 | | µA |
| **PROTECTION** | | | | | | |
| Overvoltage Threshold | $OV_H$ | $V_{SEN}$ > setpoint for >1µs, SET_OV = 00h | | VID + 300mV | | V |
| | | $V_{SEN}$ > setpoint for >1µs, SET_OV = 01h | | 3.3 | | V |
| Current Imbalance Threshold | | One $I_{SEN}$ above another ISEN for >3.2ms | | 19 | | mV |
| Overcurrent Threshold (See Table 1 for configuration and PS*n* dependencies.) | OCP_TH | PS0 in 4-, 3-, 2-, 1-Phase configuration, or any PSx in 1-Phase configuration | **54** | 60 | **66** | µA |
| | | PS1 in 3-Phase configuration | **36** | 40 | **44** | µA |
| | | PS1 in 4-Phase configuration PS1/2/3 in 2-Phase configuration | **27** | 30 | **33** | µA |
| | | PS2/3 in 4-, 3-Phase configuration | **18** | 20 | **22** | µA |
| NTC Source Current | | NTC = 1.3V | **54** | 60 | **66** | µA |
| NTC VR_HOT# Trip Voltage, TZ 7Fh to TZ FFh Threshold | | NTC voltage forced, voltage falling threshold | **0.881** | 0.893 | **0.905** | V |
| NTC Thermal Alert# Trip Voltage, TZ 3Fh to TZ 7Fh Threshold | | NTC voltage forced, voltage falling threshold | **0.92** | 0.932 | **0.944** | V |
| NTC VR_HOT# Reset Voltage, TZ 7Fh to TZ 3Fh Threshold | | NTC voltage forced, voltage rising threshold | **0.923** | 0.936 | **0.948** | V |
| NTC Thermal Alert# Reset Voltage, TZ 3Fh to TZ 1Fh Threshold | | NTC voltage forced, voltage rising threshold | **0.96** | 0.974 | **0.986** | V |
| **POWER-GOOD AND PROTECTION MONITORS** | | | | | | |
| PGOOD Low Voltage | $V_{OL}$ | $I_{PGOOD}$ = 4mA | | 0.15 | **0.4** | V |
| PGOOD Leakage Current | $I_{OH}$ | PGOOD = 3.3V | | | **1** | µA |
| PGOOD Delay | tpgd | Time from VR_ON high to PGOOD high; $V_{BOOT}$ = 1.7V | | 3 | | ms |
| VR_HOT# Low Resistance | | $I_{VR\_HOT\#}$ = 10mA | | 7 | **12** | Ω |
| VR_HOT# Leakage Current | | $V_{VR\_HOT\#}$ = 5V | | | **1** | µA |
| ALERT# Low Resistance | | $I_{ALERT\#}$ = 10mA | | 7 | **12** | Ω |
| ALERT# Leakage Current | | $V_{ALERT}$ = 5V | | | **1** | µA |
| **LOGICAL AND SERIAL INTERFACE** | | | | | | |
| VR_ON Input Low | $V_{IL}$ | | | | **0.3** | V |
| VR_ON Input High | $V_{IH}$ | CRTZ | **0.7** | | | V |
| | $V_{IH}$ | IRTZ | **0.75** | | | V |

**Electrical Specifications** Operating Conditions: $V_{DD}$ = 5V, $T_A$ = 0°C to +70°C (ISL95820CRTZ), $T_A$ = -40°C to +85°C (ISL95820IRTZ), $f_{SW}$ = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature ranges. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| VR_ON Leakage Current | $I_{VR\_ON}$ | VR_ON = 0V | **-1** | 0 | | µA |
| | | VR_ON = 1V | | 3.5 | **6** | µA |
| SCLK Maximum Speed | | | | 42 | | MHz |
| SCLK Minimum Speed | | | | 13 | | MHz |
| SCLK, SDA Leakage | | VR_ON = 0V, SCLK and SDA = 0V and 1V | **-1** | | **1** | µA |
| | | VR_ON = 1V, SCLK and SDA = 1V | **-2** | | **1** | µA |
| | | VR_ON = 1V, SDA = 0V | **-26** | –21 | **–16** | µA |
| | | VR_ON = 1V, SCLK= 0V | **-52** | –42 | **–32** | µA |
| SDA Low Resistance | | $I_{SDA}$ = 10mA | | 7 | **12** | Ω |
| $I^2CLK$ Maximum Speed | | | **400** | | | kHz |
| $I^2CLK$ Minimum Speed | | | | | **50** | kHz |
| $I^2C$ Timeout | | | **25** | 30 | **35** | ms |
| $I^2DATA$ Low Resistance | | $I_{I2DATA}$ = 4mA | | 28 | **40** | Ω |
| $I^2CLK$, $I^2DATA$ Leakage | | VR_ON = 0V, $I^2CLK$ and $I^2DATA$ = 0V and 1V | **-1** | | **1** | µA |
| | | VR_ON = 1V, $I^2CLK$ and $I^2DATA$ = 1V | **-2** | | **1** | µA |
| | | VR_ON = 1V, $I^2DATA$ = 0V | **-1** | | **1** | µA |
| | | VR_ON = 1V, $I^2CLK$= 0V | **-1** | | **1** | µA |

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

# Theory of Operation

The ISL95820 is a 1-, 2-, 3-, or 4-phase PWM controller for the Intel microprocessor VR12.5 core voltage regulator. The ISL95820 is designed to be compliant to Intel VR12.5 specifications with SerialVID Features. The SMBus/PMBus/$I^2C$ can be programmed with the Embedded Controller. The system parameters and SVID required registers are programmable with two dedicated pins. This greatly simplifies the system design for various platforms and lowers inventory complexity and cost by using a single device.

## Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. Multiphase converters overcome the daunting technical challenges in producing a cost-effective and thermally viable single-phase converter. The ISL95820 controller reduces the complexity of multiphase implementation by integrating vital functions, including integrated drivers for three phases, direct interface for a fourth external driver device, and requiring minimal output components. The "Typical Application Circuit" on page 7 provides the top level views of multiphase power conversion using the ISL95820 controller.

## Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with the other channels. For the example of a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times that of the ripple frequency of any one phase, as illustrated in Figure 3. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and to supply the DC load current.

The ripple current of a multiphase converter is less than that of a single-phase converter supplying the same load. To understand why, examine Equation 1, which represents an individual channel's peak-to-peak inductor current.

$$I_{P\text{-}P} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, $V_{IN}$ and $V_{OUT}$ are the input and output voltages respectively, L is the single-channel inductor value, and $F_{SW}$ is the switching frequency.

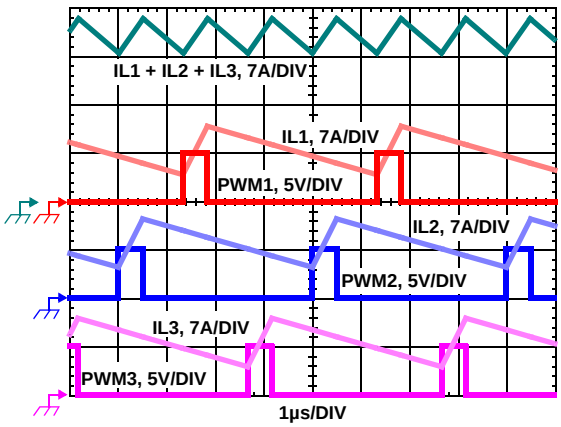



FIGURE 3. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

In a multiphase converter, the output capacitor current is the superposition of the ripple currents from each of the individual phases. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N (symmetrically phase-shifted inductor currents) in Equation 2, the peak-to-peak overall ripple current ($I_{C(P\text{-}P)}$) decreases with the increase in the number of channels, as shown in Figure 4, which introduces the concept of the Ripple Current Multiplier ($K_{RCM}$). At the (steady state) duty cycles for which the ripple current, and thus the $K_{RCM}$, is zero, the turn-off of one phase corresponds exactly with the turn-on of another phase, resulting in the sum of all phase currents being always the (constant) load current, and therefore there is no ripple current in this case.

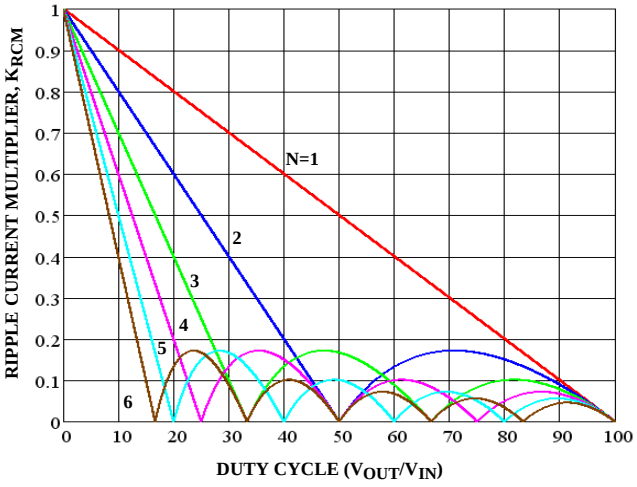



FIGURE 4. RIPPLE CURRENT MULTIPLIER vs DUTY CYCLE

Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and the summed inductor ripple current. Increased ripple frequency and lower ripple amplitude mean that the designer can use lower saturation-current inductors and fewer or less costly output capacitors for any performance specification.

$$I_{C(P-P)} = \frac{V_{OUT}}{L \cdot F_{SW}} K_{RCM} \quad \text{(EQ. 2)}$$

$$K_{RCM} = \frac{(N \cdot D - m + 1) \cdot (m - (N \cdot D))}{N \cdot D}$$

$$\text{for} \quad m - 1 \le N \cdot D \le m$$

$$m = \text{ROUNDUP}(N \cdot D, 0)$$

Another benefit of interleaving is to reduce the input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitors. Figure 5 example illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

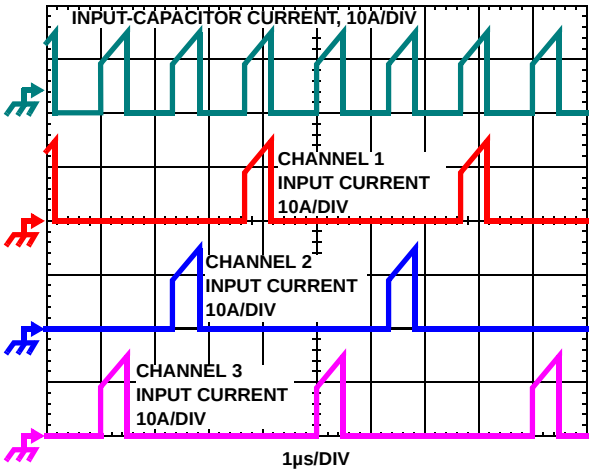



**FIGURE 5. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER**

The converter depicted in Figure 5 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

A more detailed exposition of input capacitor design is provided in “Input Capacitor Selection” on page 20.

## Multiphase R3™ Modulator

The Intersil ISL95820 multiphase regulator uses the patented R3™ (Robust Ripple Regulator™) modulator. The R3™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 6 shows the conceptual multiphase R3™ modulator circuit, and Figure 7 illustrates the operational principles.

The internal modulator uses a master clock circuit to generate the clocks for the slave circuits, one per phase. The R3™ modulator master oscillator slews between two voltage signals, the COMP voltage (the output of the voltage sense error amplifier) and VW (Voltage Window), a voltage positively offset from COMP by an offset voltage that is dependent on the nominal switching frequency. The modulator discharges the master clock ripple capacitor $C_{rm}$ with a current source equal to $g_m V_o$, where $g_m$ is a gain factor, dependent on nominal switching frequency, and also on number of active phases. $C_{rm}$ voltage $V_{crm}$ is a sawtooth waveform traversing between the VW and COMP voltages. It resets (charges quickly) to VW when it discharges (with discharge current $g_m V_o$) to COMP and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the active slave circuits. If VR is in 4-phase mode, the master clock signal will be distributed to the four phases 90° out-of-phase, in 3-phase mode distributed to the three phases 120° out-of-phase, and in 2-phase mode distributed to Phases 1 and 2 180° out-of-phase. If VR is in 1-phase mode, the master clock signal will be distributed to Phase 1 only and will be the Clock1 signal.

Each slave circuit has its own ripple capacitor $C_{rsn}$, whose voltage mimics the inductor ripple current. A $g_m$ amplifier converts the inductor voltage (or alternatively, series sense resistor voltage, indicative of that phase’s inductor current) into a current source to charge and discharge $C_{rsn}$. The slave circuit turns on its PWM pulse upon receiving its respective clock signal Clock*n*, and the current source *charges* $C_{rsn}$ with a current proportional to its respective positive inductor voltage. When $C_{rsn}$ voltage $V_{Crsn}$ rises to VW, the slave circuit turns off the PWM pulse, and the current source then *discharges* $C_{rsn}$, with a current proportional to its respective now-negative inductor voltage. $C_{rsn}$ discharges until the next Clock*n* pulse, and the cycle repeats.

Since the modulator works with the $V_{crsn}$, which are large-amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL95820 uses an error amplifier that allows the controller to maintain a 0.5% output voltage accuracy.

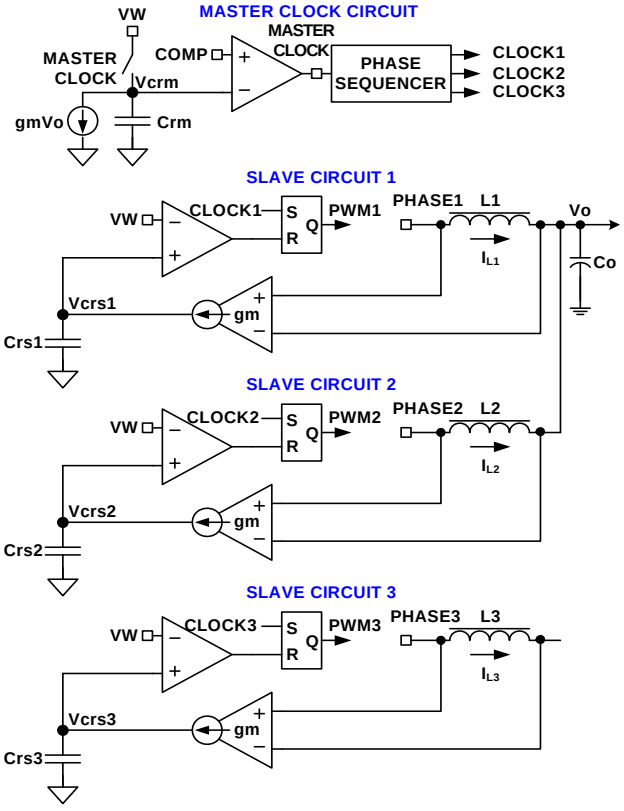



**FIGURE 6. R3™ MODULATOR CIRCUIT AT 3-PHASE MODE**

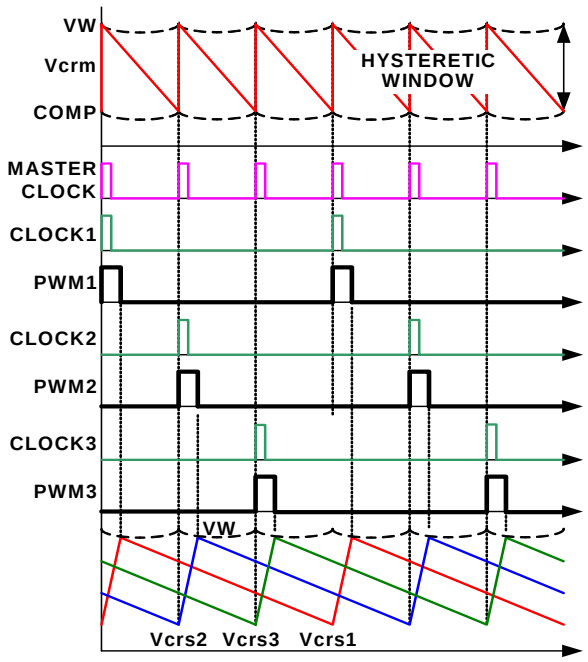



FIGURE 7. R3™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE AT 3-PHASE MODE

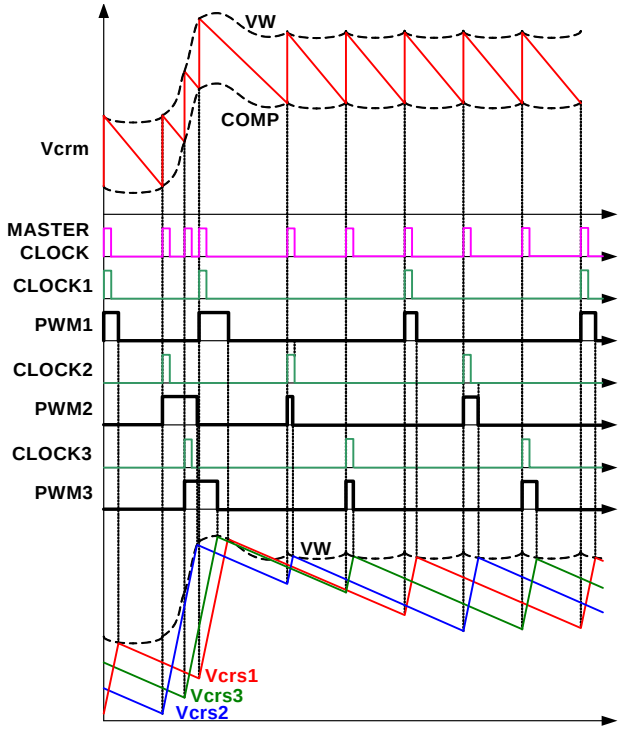



FIGURE 8. R3™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE AT 3-PHASE MODE

Figure 8 illustrates the operational principles during load insertion response. The COMP voltage rises during load insertion (due to the sudden discharge of the output capacitor driving the inverting input of the error amplifier), generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency. This phenomenon allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises with the COMP voltage, making the PWM on-time pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls with the COMP voltage, reducing the current PWM pulse width. The inherent pulse frequency and width increases due to an increasing load transient, and likewise the pulse frequency and width reductions due to a decreasing load transient, produce the excellent load transient response of the R3™ modulator.

Since all phases share the same VW window (master clock frequency generator) and threshold (slave pulse width generator) voltage, dynamic current balance among phases is ensured, inherently, for the duration of any load transient event.

The R3™ modulator intrinsically has input voltage feed-forward control, due to the proportional dependence of the clock generator slave transconductance gains on the input voltage. This dependence decreases the on-time pulse-width of each phase in proportion to an increase in input voltage, making the output voltage insensitive to a fast slew rate input voltage change.

## Diode Emulation and Period Stretching

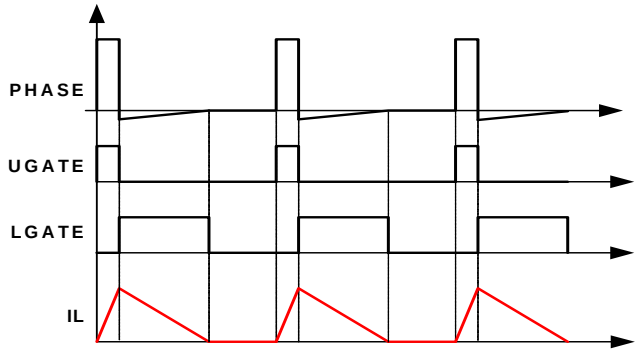



FIGURE 9. DIODE EMULATION

The ISL95820 can operate in diode emulation mode (DEM) to improve light load efficiency. Diode emulation can be optionally enabled in PS2 and PS3, in Phase-1 only operation, by selection of PROG2 pin resistance to ground. In DEM, the low-side MOSFET conducts while the current is flowing from source to drain and blocks reverse current, emulating a diode. As illustrated in Figure 9, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The controller monitors the inductor current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 9 illustrates, the inductor current will reach and stay at zero before the next phase node pulse and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator will appear to operate in continuous conduction mode (CCM), although the controller is nevertheless configured for DEM.

Figure 10 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, making the inductor current triangle the same in the

three cases (only the time between inductor current triangles changes). The controller clamps the ripple capacitor voltage $V_{crs}$ in DEM to make it mimic the inductor current. It takes the COMP voltage longer to hit $V_{crm}$, which produces master clock pulses, naturally stretching the switching period. The inductor current triangles move further apart from each other, such that the inductor current average value is equal to the load current. The reduced switching frequency improves light load efficiency.

Because the next clock pulse occurs when $V_{COMP}$ (which tracks output voltage error) rises above $V_{CRM}$, DEM switching pulse frequency is responsive to load transient events in a manner similar to that of multiphase CCM operation.

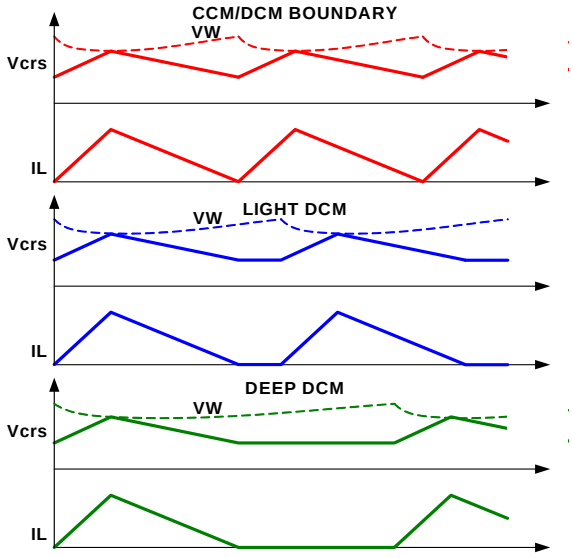



FIGURE 10. PERIOD STRETCHING

## Adaptive Body Diode Conduction Time Reduction

When in DCM, the controller ideally turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative by the product of the (negative) inductor current and the low-side MOSFET $r_{DS(ON)}$, producing a voltage drop that is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero-crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it will flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it will flow through the high-side MOSFET body diode, causing the phase node to have a positive voltage spike (to $V_{IN}$ plus a PN diode voltage drop) until the current decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase comparator threshold voltage accordingly in iterative steps, such that the low-side MOSFET body diode conducts for approximately 40ns (turning off 40ns before the inductor current zero-crossing) to minimize the body diode-related loss.

## Modes of Operation

TABLE 1. VR MODES OF OPERATION

| ISEN4 | ISEN3 | ISEN2 | CONFIG. | PS | MODE | OCP THRESHOLD (µA) |
|---|---|---|---|---|---|---|
| To Power Stage | To Power Stage | To Power Stage | 4-phase CPU VR Config. | 0 | 4-phase CCM | 60 |
| | | | | 1 | 2-phase CCM | 30 |
| | | | | 2 | 1-phase opt: DEM or CCM | 20 |
| | | | | 3 | | |
| Tied to 5V | | | 3-phase CPU VR Config. | 0 | 3-phase CCM | 60 |
| | | | | 1 | 2-phase CCM | 40 |
| | | | | 2 | 1-phase opt: DEM or CCM | 20 |
| | | | | 3 | | |
| | Tied to 5V | | 2-phase CPU VR Config. | 0 | 2-phase CCM | 60 |
| | | | | 1 | 1-phase CCM | 30 |
| | | | | 2 | 1-phase opt: DEM or CCM | |
| | | | | 3 | | |
| | | Tied to 5V | 1-phase CPU VR Config. | 0 | 1-phase CCM | 60 |
| | | | | 1 | | |
| | | | | 2 | 1-phase opt: DEM or CCM | |
| | | | | 3 | | |

VR can be configured for 4-, 3-, 2-, or 1-phase operation. Table 1 shows VR configurations and operational modes, programmed by the ISEN4, ISEN3 and ISEN2 pin status, and the Set PS command. For the 3-phase configuration, tie the ISEN4 pin to 5V. In this configuration, phases 1, 2, and 3 are active. For the 2-phase configuration, tie the ISEN3 and ISEN4 pin to 5V. In this configuration, phases 1 and 2 are active. For the 1-phase configuration, tie the ISEN4, ISEN3, and ISEN2 pin to 5V. In this configuration, only Phase 1 is active.

In the 4-phase configuration, VR operates in 4-phase CCM in PS0. It enters 2-phase CCM mode in PS1 by dropping phases 4 and 3 and reducing the overcurrent protection level to 1/2 of the initial value. It enters 1-phase DEM (optionally CCM) in PS2 and PS3 by dropping phases 4, 3, and 2, and reducing the overcurrent protection levels to 1/4 of the initial value.

In the 3-phase configuration, VR operates in 3-phase CCM in PS0. (Phase 4 is disabled). It enters 2-phase CCM mode in PS1 by dropping phase 3 and reducing the overcurrent protection level to 2/3 of the initial value. It enters 1-phase DEM (optionally CCM) in PS2 and PS3 by dropping phases 3 and 2, and reducing the overcurrent and the protection level to 1/3 of the initial value.

In the 2-phase configuration, VR operates in 2-phase CCM in PS0. (Phases 4 and 3 are disabled.) It enters 1-phase mode in PS1, PS2, and PS3 by dropping phase 2 and reducing the overcurrent

protection level to 1/2 of the initial value. PS1 operates in CCM, and PS2 and PS3 operate in DEM (optionally CCM).

In the 1-phase configuration, VR operates in 1-phase CCM in PS0 and PS1, and enters 1-phase DEM (optionally CCM) in PS2 and PS3. the overcurrent protection level is the same for all power states.

This information is summarized in Table 1.

## Programming Resistors

There are three programming resistors: $R_{PROG1}$, $R_{PROG2}$ and $R_{PROG3}$. Table 2 shows how to select $R_{PROG1}$ based on VR $I_{CC(MAX)}$ register settings. Determine the maximum current VR can support and set the VR $I_{CC(MAX)}$ register value accordingly, by selecting the appropriate $R_{PROG1}$ value. The CPU will read the VR $I_{CC(MAX)}$ register value and ensure that the CPU CORE current doesn't exceed the value specified by VR $I_{CC(MAX)}$.

TABLE 2. PROG1 PROGRAMMING TABLE

| $R_{PROG1}$ (kΩ) EIA E96 1% VALUE | VR $I_{CC(MAX)}$ (A) |
|---|---|
| 3.24 | 15 |
| 5.76 | 20 |
| 9.53 | 25 |
| 13.3 | 30 |
| 16.9 | 35 |
| 21.0 | 40 |
| 24.9 | 45 |
| 28.7 | 50 |
| 34.0 | 55 |
| 42.2 | 60 |
| 49.9 | 65 |
| 57.6 | 70 |
| 64.9 | 75 |
| 73.2 | 80 |
| 80.6 | 90 |
| 88.7 | 100 |
| 100 | 115 |
| 113 | 130 |
| 124 | 145 |
| 137 | 160 |
| 154 | 180 |
| 169 | 200 |
| 187 | 225 |
| 221 | 225 |

$R_{PROG2}$ sets the start-up ($V_{BOOT}$) voltage, and selects whether the Droop (programmable DC loadline) function is enabled on power-up, and whether Diode Emulation is enabled in PS2 and PS3. When the controller works in the targeted application with a CPU, select $R_{PROG2}$, such that VR powers up to $V_{BOOT}$ = 0V, as required by the SVID command. In the absence of a CPU, such as testing of the VR alone, select $R_{PROG2}$ for $V_{BOOT}$ of 1.65V, 1.7V or 1.75V. Table 3 shows how to select $R_{PROG2}$ to enable droop, select $V_{BOOT}$, and select operational mode in PS2 and PS3 (CCM vs DEM). Note that the effective resistance value of the DC loadline, i.e., the output voltage droop due to load current, is determined by components of the output current sense, voltage feedback, and modulator compensation networks.

TABLE 3. PROG2 PROGRAMMING TABLE

| $R_{PROG2}$ (kΩ) EIA E96 1% VALUE | DROOP ENABLED | OPERATIONAL MODE IN PS2 AND PS3 | $V_{BOOT}$ (V) |
|---|---|---|---|
| 3.24 | YES | DEM | 0 |
| 5.76 | YES | DEM | 1.65 |
| 9.53 | YES | DEM | 1.7 |
| 13.3 | YES | DEM | 1.75 |
| 16.9 | YES | CCM | 1.75 |
| 21.0 | YES | CCM | 1.7 |
| 24.9 | YES | CCM | 1.65 |
| 28.7 | YES | CCM | 0 |
| 34.0 | NO | DEM | 0 |
| 42.2 | NO | DEM | 1.65 |
| 49.9 | NO | DEM | 1.7 |
| 57.6 | NO | DEM | 1.75 |
| 64.9 | NO | CCM | 1.75 |
| 73.2 | NO | CCM | 1.7 |
| 80.6 | NO | CCM | 1.65 |
| 88.7 | NO | CCM | 0 |

### SWITCHING FREQUENCY SELECTION

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 17, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in "Output Filter Design" on page 20. Choose the lowest switching frequency that allows the regulator to meet the transient-response and output-voltage ripple requirements.

The resistor from PROG3 to GND selects one of three available switching frequencies, 200kHz, 300kHz, and 450kHz, and sets the modulator slope compensation value. Note that when the ISL95820 is in continuous conduction mode (CCM), the switching frequency is not strictly constant due to the nature of the R3™ modulator. As explained in "Multiphase R3™ Modulator" on page 13, the effective switching frequency will increase during load insertion and will decrease during load release to achieve fast response. However, the switching frequency is nearly constant at constant load. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 15% and doesn't have any significant effect on output voltage ripple magnitude. Table 4 shows how to select $R_{PROG3}$ to obtain the desired modulator slope

compensation and switching frequency. There are many choices of slope compensation for each switching frequency.

TABLE 4. PROG3 PROGRAMMING TABLE

| $R_{PROG3}$ (kΩ) EIA E96 1% VALUE | SLOPE COMPENSATION | SWITCHING FREQUENCY (kHz) |
|---|---|---|
| 3.24 | 0.25x | 200 |
| 5.76 | 0.5x | 200 |
| 9.53 | 0.75x | 200 |
| 13.3 | 1x | 200 |
| 16.9 | 1.25x | 200 |
| 21.0 | 1.5x | 200 |
| 24.9 | 1.75x | 200 |
| 34.0 | 0.25x | 300 |
| 42.2 | 0.5x | 300 |
| 49.9 | 0.75x | 300 |
| 57.6 | 1x | 300 |
| 64.9 | 1.25x | 300 |
| 73.2 | 1.5x | 300 |
| 80.6 | 1.75x | 300 |
| 88.7 | 2x | 300 |
| 100 | 0.25x | 450 |
| 113 | 0.5x | 450 |
| 124 | 0.75x | 450 |
| 137 | 1x | 450 |
| 154 | 1.25x | 450 |
| 169 | 1.5x | 450 |
| 187 | 1.75x | 450 |
| 221 | 2x | 450 |

# General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs, which include schematics, bill of materials, and example board layouts for common microprocessor applications.

## Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily upon the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15A and 25A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

### MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

#### Lower MOSFET Power Calculation

The calculation for heat dissipated in the lower (alternatively called low-side) MOSFET of each phase is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 3, $I_M$ is the maximum continuous output current; $I_{P-P}$ is the peak-to-peak inductor current per phase (see Equation 1 on page 12); d is the duty cycle ($V_{OUT}/V_{IN}$); and L is the per-channel inductance. Equation 3 shows the approximation.

$$P_{LOW,1} = r_{DS(ON)}\left[\frac{I_M}{N}^2 + \frac{I_{P-P}}{12}^2\right] \cdot (1-d) \quad \text{(EQ. 3)}$$

A term can be added to the lower-MOSFET loss equation to account for the loss during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at $I_M$, $V_{D(ON)}$; the switching frequency, $F_{SW}$; and the length of dead times ($t_{d1}$ and $t_{d2}$) at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} F_{SW}\left[\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right) t_{d1} + \left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right) t_{d2}\right] \quad \text{(EQ. 4)}$$

Finally, the power loss of output capacitance of the lower MOSFET is approximated in Equation 5:

$$P_{LOW,3} \approx \frac{2}{3} \cdot V_{IN}^{1.5} \cdot C_{OSS\_LOW} \cdot \sqrt{V_{DS\_LOW}} \cdot F_{SW} \quad \text{(EQ. 5)}$$

where $C_{OSS\_LOW}$ is the output capacitance of lower MOSFET at the test voltage of $V_{DS\_LOW}$. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$, $P_{LOW,2}$ and $P_{LOW,3}$.

#### Upper MOSFET Power Calculation

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage ($V_{IN}$) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge, $Q_{rr}$; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 6, the required time for this commutation is $t_1$ and the approximated associated power loss is $P_{UP(1)}$.

$$P_{UP(1)} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right)\left(\frac{t_1}{2}\right)F_{SW} \quad \text{(EQ. 6)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time ($t_2$). In Equation 7, the approximate power loss is $P_{UP(2)}$.

$$P_{UP(2)} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right)\left(\frac{t_2}{2}\right)F_{SW} \quad \text{(EQ. 7)}$$

A third component involves the lower MOSFET's reverse-recovery charge, $Q_{rr}$. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can draw all of $Q_{rr}$, it is conducted through the upper MOSFET across $V_{IN}$. The power dissipated as a result is $P_{UP(3)}$ and is approximated in Equation 8:

$$P_{UP(3)} = V_{IN}Q_{rr}F_{SW} \quad \text{(EQ. 8)}$$

The resistive part of the upper MOSFET is given in Equation 9 as $P_{UP(4)}$.

$$P_{UP(4)} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{P-P}^2}{12}\right] \cdot d \quad \text{(EQ. 9)}$$

Equation 10 accounts for some power loss due to the drain-source parasitic inductance ($L_{DS}$, including PCB parasitic inductance) of the upper MOSFET, although it is not exact:

$$P_{UP(5)} \approx L_{DS}\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right)^2 \quad \text{(EQ. 10)}$$

Finally, the power loss of output capacitance of the upper MOSFET is approximated in Equation 11:

$$P_{UP(6)} \approx \frac{2}{3} \cdot V_{IN}^{1.5} \cdot C_{OSS\_UP} \cdot \sqrt{V_{DS\_UP}} \cdot F_{SW} \quad \text{(EQ. 11)}$$

where $C_{OSS\_UP}$ is the output capacitance of the lower MOSFET at test voltage of $V_{DS\_UP}$. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 6 through 11. Since the power equations depend on MOSFET parameters, choosing the correct MOSFET can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

## Integrated Driver Operation and Adaptive Shoot-through Protection

The ISL95820 provides three integrated MOSFET drivers, for phases 1 through 3, and a PWM signal to operate a single external driver device, required if a fourth phase is required. Designed for high-speed switching, the internal MOSFET drivers control both high-side and low-side N-Channel FETs from the internal PWM signal

A rising transition on the internal PWM signal (phases 1 through 3) initiates the turn-off of the lower MOSFET. After a short propagation delay [$t_{PDLL}$], the lower gate begins to fall. Following a 25ns blanking period, adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [$t_{PDHU}$] after the LGATE voltage drops below ~1.75V. The upper gate drive then begins to rise [$t_{RU}$] and the upper MOSFET turns on.

A falling transition on the internal PWM signal indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [$t_{PDLU}$] is encountered before the upper gate begins to fall [$t_{FU}$]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time [$t_{PDHL}$] after the upper MOSFET's PHASE voltage drops below +0.8V or 40ns after the upper MOSFET's gate voltage [UGATE-PHASE] drops below ~1.75V. The lower gate then rises [$t_{RL}$], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

The internal drivers are optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.8Ω ON-resistance and 3A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

For VCCP < 7V, Diode Emulation Mode (DEM) **must** be disabled using the PROG2 pin programming resistor.

### INTERNAL BOOTSTRAP DEVICE

The integrated drivers feature an internal bootstrap Schottky diode equivalent circuit implemented by switchers with a typical ON-resistance of 40Ω and without the typical diode forward voltage drop. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces the voltage stress on the BOOT to PHASE pins.

The bootstrap capacitor must have a maximum voltage rating well above the maximum voltage intended for UVCC. Its minimum capacitance value can be estimated using Equation 12:

$$C_{BOOT\_CAP} \geq \frac{Q_{UGATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 12)}$$

$$Q_{UGATE} = \frac{Q_{G1} \bullet UVCC}{V_{GS1}} \bullet N_{Q1}$$

where $Q_{G1}$ is the amount of gate charge per upper MOSFET at $V_{GS1}$ gate-source voltage and $N_{Q1}$ is the number of control MOSFETs. The $\Delta V_{BOOT\_CAP}$ term is defined as the allowable droop in the rail of the upper gate drive. Select results are exemplified in Figure 11.

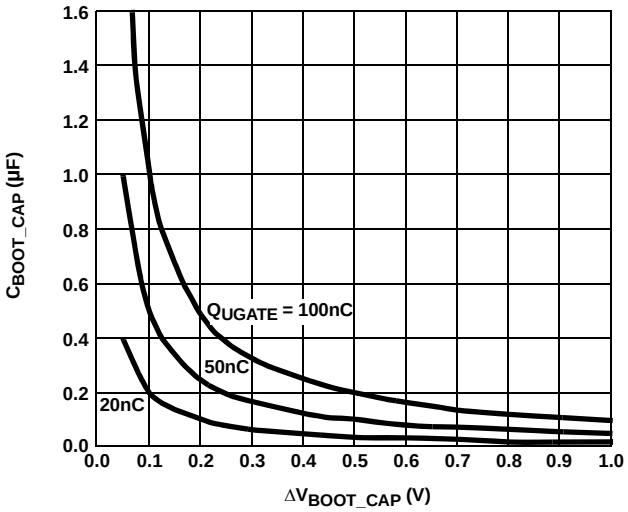



FIGURE 11. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

## POWER DISSIPATION IN THE INTEGRATED DRIVERS

Internal driver power dissipation is mainly a function of the switching frequency ($F_{SW}$), the output drive impedance, the layout resistance, and the selected MOSFET's internal gate resistance and total gate charge ($Q_G$). Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level may push the IC beyond the maximum recommended operating junction temperature. The DFN package is more suitable for high frequency applications. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current, per driver, can be estimated using Equations 13 and 14, respectively:

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCCP$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet UVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet LVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2} \quad \text{(EQ. 13)}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet UVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet LVCC \bullet N_{Q2}}{V_{GS2}}\right) \bullet F_{SW} + I_Q \quad \text{(EQ. 14)}$$

where the gate charge ($Q_{G1}$ and $Q_{G2}$) is defined at a particular gate-to-source voltage ($V_{GS1}$ and $V_{GS2}$) in the corresponding MOSFET datasheet; $I_Q$ is the driver's total quiescent current with no load at both drive outputs; $N_{Q1}$ and $N_{Q2}$ are the number of, and UVCC and LVCC are the drive voltages for, the upper and lower MOSFETs, respectively. The $I_Q * V_{CCP}$ product is the quiescent power of the driver without a load.

The total gate drive power losses are dissipated among the resistive components along the transition path, as outlined in Equation 15. The drive resistance dissipates a portion of the total gate drive power losses; the rest will be dissipated by the external gate resistors ($R_{G1}$ and $R_{G2}$) and the internal gate resistors ($R_{GI1}$ and $R_{GI2}$) of MOSFETs. Figures 12 and 13 show the typical upper and lower gate drives turn-on current paths.

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC \quad \text{(EQ. 15)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

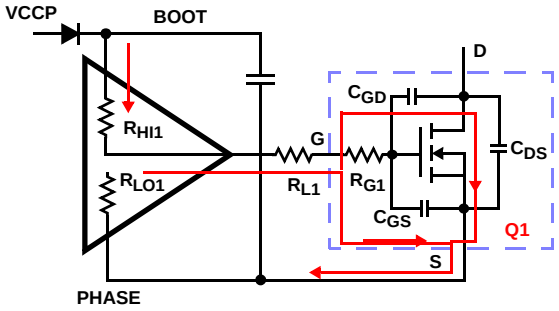



FIGURE 12. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

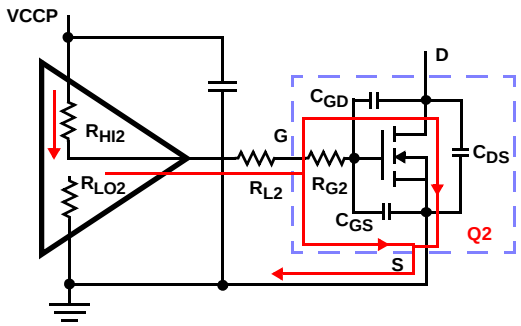



FIGURE 13. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

## UPPER MOSFET SELF TURN-ON EFFECT AT START-UP

Should a driver have insufficient bias voltage applied (at pin VCCP), its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to self-coupling via the internal $C_{GD}$ of the MOSFET, the gate of the upper MOSFET could momentarily rise up to a level greater than the threshold voltage of the device, potentially turning on the upper switch. Therefore, if such a situation could conceivably be encountered, it is a common practice to place a resistor ($R_{UGPH}$)

across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the $C_{GD}/C_{GS}$ ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower $C_{DS}/C_{GS}$ ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ resistor is sufficient, not affecting normal performance and efficiency.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \quad \text{(EQ. 16)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

The coupling effect can be roughly estimated with Equation 16, which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. Figure 6 provides a visual reference for this phenomenon and its potential solution.

### EXTERNAL (PHASE 4) DRIVER SELECTION

When a fourth phase is to be used, it is recommended that the Intersil ISL6625A driver be selected as the external Phase 4 driver device.

## Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output-voltage deviation under transient loading, $\Delta V_{MAX}$. Capacitors are characterized according to their capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount, as shown in Equation 17:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 17)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors, allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors, allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 12 and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C(P-P)}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines a lower limit on the inductance, as shown in Equation 18.

$$L \geq ESR \cdot \frac{V_{OUT} \cdot K_{RCM}}{F_{SW} \cdot V_{IN} \cdot V_{P-P(MAX)}} \quad \text{(EQ. 18)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than $\Delta V_{MAX}$. This places an upper limit on inductance.

Equation 19 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 20 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_{OUT}}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right] \quad \text{(EQ. 19)}$$

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 20)}$$

## Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs, which is related to duty cycle and the number of active phases. The input RMS current can be calculated with Equation 21..

$$I_{IN(RMS)} = \sqrt{K^2_{IN(CM)} \bullet Io^2 + K^2_{RAMP(CM)} \bullet I^2_{Lo(P-P)}} \quad \text{(EQ. 21)}$$

$$K_{IN(CM)} = \sqrt{\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N^2}} \quad \text{(EQ. 22)}$$

$$K_{RAMP(CM)} = \sqrt{\frac{m^2(N \bullet D - m + 1)^3 + (m-1)^2(m - N \bullet D)^3}{12N^2D^2}} \quad \text{(EQ. 23)}$$

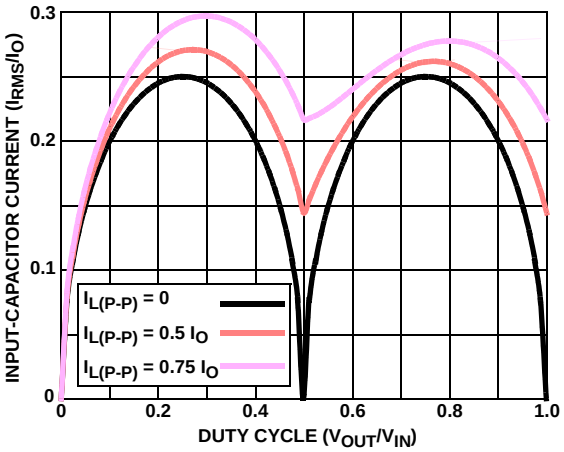



FIGURE 14. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

For a 2-phase design, use Figure 14 to determine the input capacitor RMS current requirement given the duty cycle, maximum sustained output current ($I_O$), and the ratio of the per-phase peak-to-peak inductor current ($I_{L(P-P)}$) to $I_O$. Select a bulk capacitor with a ripple current rating, which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage.

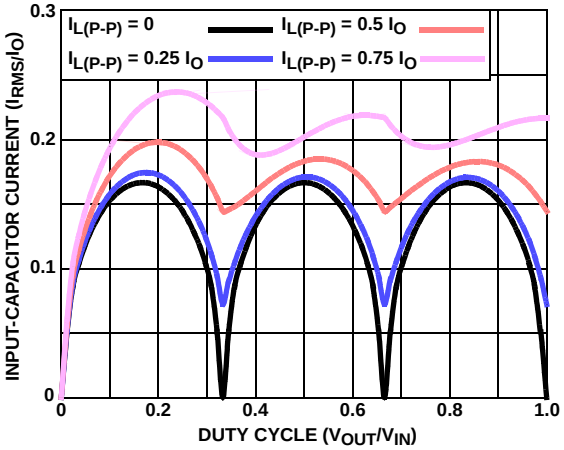



FIGURE 15. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

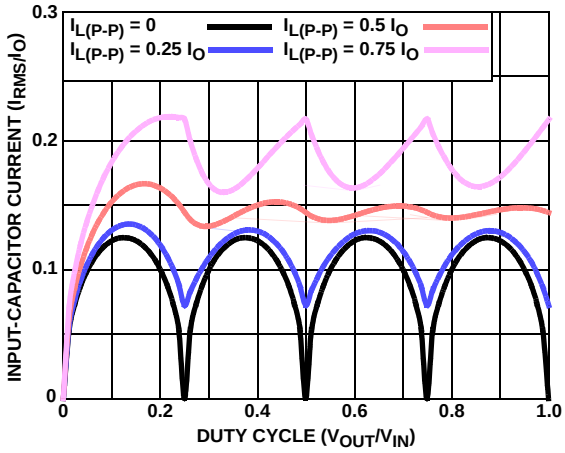



FIGURE 16. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

Figures 15 and 16 provide the same input RMS current information for 3- and 4-phase designs, respectively. Use the same approach to selecting the bulk capacitor type and number, as previously described.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize noise suppression.

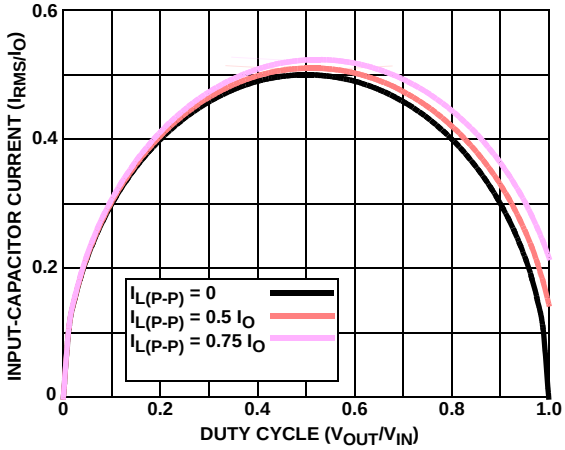



FIGURE 17. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

## MULTIPHASE RMS IMPROVEMENT

Figure 17 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a 2-phase converter versus that of a single-phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{L(P-P)}$ to $I_O$ of 0.5. The single-phase converter would require $17.3A_{RMS}$ current capacity, while the 2-phase converter would only require $10.9A_{RMS}$. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single-phase approach.

## Inductor Current Sensing and Balancing

### INDUCTOR DCR CURRENT-SENSING NETWORK

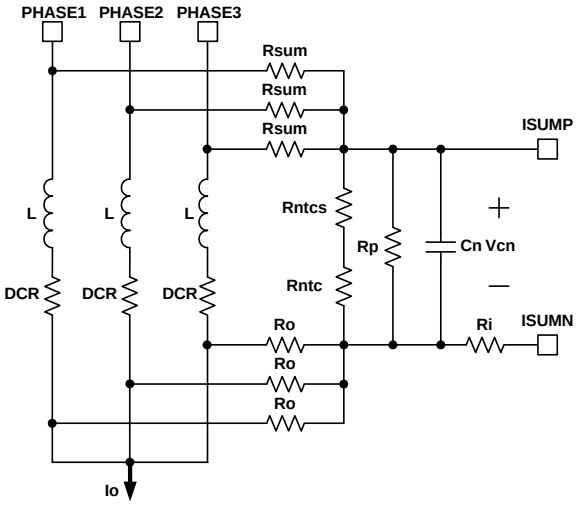



FIGURE 18. DCR CURRENT-SENSING NETWORK

Figure 18 shows the inductor DCR current-sensing network for the example of a 3-phase voltage regulator. An inductor's current flows through the inductor's DCR and creates a voltage drop. Each inductor has two resistors, $R_{sum}$ and $R_o$, connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The $R_{sum}$ and $R_o$ resistors are connected in a summing network as shown, and feed the total current information to the NTC network (consisting of $R_{ntcs}$, $R_{ntc}$ and $R_p$) and capacitor $C_n$. $R_{ntc}$ is a negative temperature coefficient (NTC) thermistor, used to compensate for the change in inductor DCR due to temperature changes.

The inductor output side pads are electrically shorted in the schematic, but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use 1Ω~10Ω $R_o$ to create quality signals. Since the $R_o$ value is much smaller than the rest of the current sensing circuit, the following analysis will ignore it for simplicity.

The summed inductor current information is presented to the capacitor $C_n$. Equations 24 thru 28 describe the frequency-domain relationship between inductor total current $I_o(s)$ and $C_n$ voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left( \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 24)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 25)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 26)}$$

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 27)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 28)}$$

where N is the number of phases.

The inductor DCR value increases as the inductor temperature increases, due to the positive temperature coefficient of the copper windings. If uncompensated, this will cause the estimate of inductor current to increase with temperature. The resistance of the co-located NTC thermistor, $R_{ntc}$, decreases as its temperature increases, compensating for the increase in DCR. Proper selections of $R_{sum}$, $R_{ntcs}$, $R_p$ and $R_{ntc}$ parameters ensure that $V_{Cn}$ represents the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the $R_{sum}$ resistors form a voltage divider, $V_{cn}$ is always a fraction of the inductor DCR voltage. It is recommended to have a high ratio of $V_{cn}$ to the inductor DCR voltage, so the current sense circuit has a higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: $R_{sum}$ = 3.65kΩ, $R_p$ = 11kΩ, $R_{ntcs}$ = 2.61kΩ and $R_{ntc}$ = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current-sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ response must track $I_o(s)$ over a broad range of frequency for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ (Equation 29) has unity gain at DC, a pole $\omega_{sns}$, and a zero $\omega_L$. To obtain unity gain at all frequencies, set $\omega_L$ equal to $\omega_{sns}$ and solve for Cn.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 29)}$$

For example, given N = 3, $R_{sum}$ = 3.65kΩ, $R_p$ = 11kΩ, $R_{ntcs}$ = 2.61kΩ, $R_{ntc}$ = 10kΩ, DCR = 0.9mΩ and L = 0.36µH, Equation 29 gives $C_n$ = 0.397µF.

Assuming the loop compensator design is correct, Figure 26 shows the expected load transient response waveforms for the correctly chosen value of $C_n$. When the load current $I_{core}$ has a step change, the output voltage $V_{core}$ also has a step change, determined by the DC loadline resistance (the output voltage droop value of the regulator, (see "Current Sense Circuit

Adjustments" on page 28).

If the $C_n$ value is too large or too small, $V_{Cn}(s)$ will not accurately represent real-time $I_o(s)$ and will worsen the transient response. Figure 28 shows the load transient response when $C_n$ is too small. $V_{core}$ will droop excessively, briefly, upon abrupt load insertion, before recovering to the intended DC value, which may create a system failure. There will be excessive overshoot during load decreases, which may potentially hurt the CPU reliability.

With the proper selection of $C_n$, assume that $A_{cs}(s) = 1$. With this assumption, Equation 29 can be recast as Equation 30:

$$\frac{V_{Cn}}{I_o} = \left( \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \quad \text{(EQ. 30)}$$

With a properly designed inductor temperature compensation network, we may also assume the room temperature inductor DCR value together with the room temperature value of $R_{ntcnet}$ in subsequent calculations, since any temperature variation in one value will be, ideally, exactly compensated by a variation in the other value. Equation 31 can be evaluated, using room temperature resistance values, to obtain a constant value of the ratio $V_{Cn}/I_o$, in units of resistance, for a given DCR current sense network design. This constant value, designated $\rho_O$, will be required to complete the regulator design.

$$\rho_o = \left( \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \Bigg|_{RoomTemp} \quad \text{(EQ. 31)}$$

This expression applies to the DCR current sense circuit of Figure 18.

Figure 19 shows the resistor current-sensing network for the example of a 3-phase regulator. Each inductor has a series current-sensing resistor $R_{sen}$. $R_{sum}$ and $R_o$ are connected to the $R_{sen}$ pads to accurately capture the inductor current information. The $R_{sum}$ and $R_o$ resistors are connected to capacitor $C_n$. $R_{sum}$ and $C_n$ form a filter for noise attenuation. Equations 32 thru 34 give $V_{Cn}(s)$ expression:

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 32)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{Rsen}}} \quad \text{(EQ. 33)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 34)}$$

## RESISTOR CURRENT-SENSING NETWORK

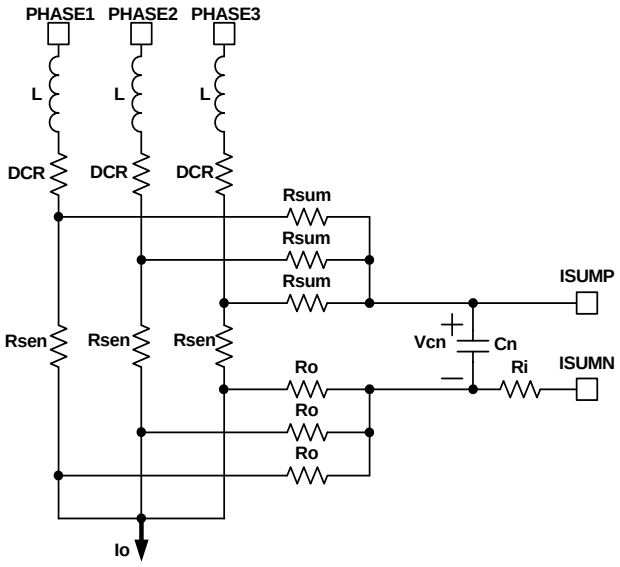



FIGURE 19. RESISTOR CURRENT-SENSING NETWORK

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor $R_{sen}$ value will not have significant variation over-temperature, so there is no need for the NTC network.

The recommended values are $R_{sum}$ = 1kΩ and $C_n$ = 5600pF.

As with the DCR current sense network, Equation 34 can be recast as Equation 35:

$$\frac{V_{Cn}}{I_o} = \frac{R_{sen}}{N} \quad \text{(EQ. 35)}$$

This equation can be evaluated to obtain a constant value of the ratio $V_{Cn}/I_o$, in Ω units, for a given sense-resistor current sense network design. This constant value will be designated $\rho_O$ in

Equation 36.

$$\rho_o = \frac{R_{sen}}{N} \quad \text{(EQ. 36)}$$

As with the DCR-sense design, this constant value will be required to complete the regulator design. This expression applies to the resistor current sense circuit of Figure 19.

## PROGRAMMING OF OUTPUT OVERCURRENT PROTECTION, $I_{DROOP}$, AND IMON

The final step in designing the current sense network is the selection of resistor Ri of Figures 18 or 19. This resistor determines the ratio of the controller's internal representation of output current ($I_{droop}$, also called the "droop current") to the actual output current, that is, to the sum of all the measured inductor currents. This internal representation is itself a current that will be used (a) to compare to the overcurrent protection threshold, (b) to drive the IMON pin external resistor to produce a voltage to represent the output current, which is measured and written to the IOUT register, and (c) to source the $I_{droop}$ current to the FB pin to provide the programmable load-dependent output voltage "droop", or output DC loadline.

Begin by selecting the maximum current that the regulator is designed to provide. This will be the value of VR $I_{CC(MAX)}$ programmed with the PROG1 pin resistance to ground, as per Table 2 on page 16. Select $R_{PROG1}$ to program the lowest available value of $I_{CC(MAX)}$ that exceeds the expected maximum load. The Overcurrent Protection (OCP) threshold $I_{OCP}$ must exceed this value. $I_{OCP}$ is typically chosen to be 20% to 25% greater than $I_{CC(MAX)}$. $I_{OCP}$ will determine the value of Ri.

Refer to Table 1 on page 15. The value of OCP THRESHOLD for any phase configuration (1- through 4-phase regulator) and any powerstate (PS0-PS3) is the value of $I_{droop}$ that will trigger output overcurrent protection. Notice that the OCP THRESHOLD value of the PS0 row of any phase configuration is 60µA. Ri should be chosen, such that $I_{droop}$ will be 60µA when the regulator output current is equal to the chosen value of output $I_{OCP}$.

The mechanism by which Ri determines $I_{droop}$ is illustrated in Figure 20.

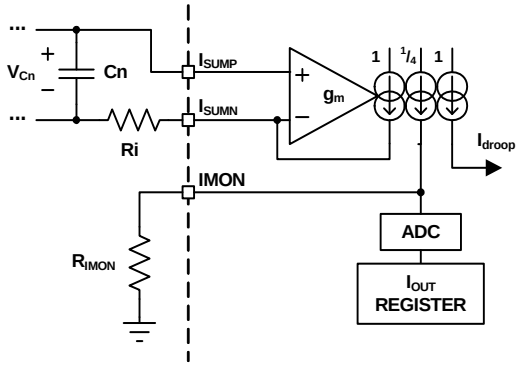



FIGURE 20.

The ISUM transconductance amplifier produces the current that drops the voltage $V_{Cn}$ across Ri, to make $V_{ISUMP} = V_{ISUMN}$. This current is mirrored 1:1 to produce $I_{droop}$, and 4:1 to produce $I_{IMON}$. $I_{droop}$ is compared directly to the OCP THRESHOLD, always 60µA in PS0, so Ri must be chosen to obtain the desired $I_{OCP}$ using Equation 37:

$$Ri = \rho_o \times \frac{I_{OCP}}{60\mu A} \quad \text{(EQ. 37)}$$

where $\rho_o$ is the constant value determined in Equations 31 or 36.

For a given value of output current, $I_o$, $I_{droop}$ will have the value:

$$I_{droop} = \frac{\rho_o}{Ri} \times I_o \quad \text{(EQ. 38)}$$

$I_{droop}$ is also used to program the slope of the output DC loadline. The DC loadline slope is the programmable regulator output resistance.

The IOUT register will contain an 8-bit unsigned number indicative of the IMON pin voltage, scaled such that its value is 00h when $V_{IMON}$ = 0V, and FFh when $V_{IMON}$ = 1.2V. With Ri determined, $R_{IMON}$ is chosen, such that $V_{IMON}$ = 1.2V when the regulator load current is equal to $I_{CC(MAX)}$, the maximum current value programmed by $R_{PROG1}$. Select $R_{IMON}$ using Equation 39:

$$R_{IMON} = 1.2V \times \left(\rho_o \times \frac{I_{CC(MAX)}}{Ri \times 4}\right)^{-1} \quad \text{(EQ. 39)}$$

where again $\rho_o$ is the constant value determined in Equations 31 or 36.

## PROGRAMMING THE DC LOADLINE

The DC loadline is the effective DC series resistance of the voltage regulator output. The output series resistance causes the output voltage to "droop" below the selected regulation voltage by a voltage equal to the load current multiplied by the output resistance. The linear relationship of output voltage drop to load current is called the loadline, and is expressed in units of resistance. It will be designated $R_{LL}$. Figure 21 shows the equivalent circuit of a voltage regulator (VR) with the droop function. An ideal VR is equivalent to a voltage source (V = VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope $R_{LL}$, i.e., constant output impedance independent of frequency, $V_o$ will have step response when $I_o$ has a step change.

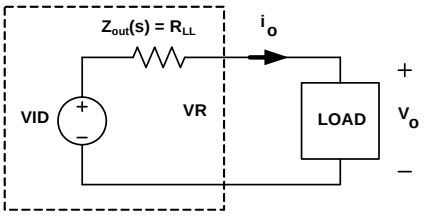



FIGURE 21. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

The ISL95820 provides programmable DC loadline resistance. This feature can be disabled by choice of the programming resistor on pin PROG2, or disabled via the serial bus. A typical desired value of the DC loadline for Intel VR12.5 applications is $R_{LL}$ = 1.5mΩ.

The programmable DC loadline mechanism is integral to the regulator's output voltage feedback compensator. This is illustrated in the feedback circuit and recommended

compensation network shown in Figure 22.

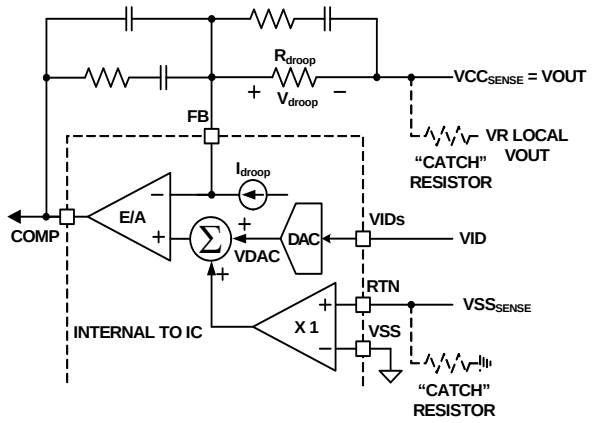



FIGURE 22. DIFFERENTIAL VOLTAGE SENSING AND LOAD LINE IMPLEMENTATION

The ISL95820 implements the DC loadline by injecting a current, $I_{droop}$, which is proportional to the regulator output current $I_{OUT}$, into the voltage feedback node (the FB pin). The scaling of $I_{droop}$ with respect to $I_{OUT}$ was selected in the previous section to obtain the desired output $I_{OCP}$ threshold. The droop voltage is the voltage drop across the resistance, called $R_{droop}$, between the FB pin and the output voltage due to $I_{droop}$. $R_{droop}$ will be selected to implement the desired DC loadline resistance $R_{LL}$. The FB pin voltage is thus raised above $V_{OUT}$ by the droop voltage, requiring the regulator to reduce $V_{OUT}$ to make $V_{FB}$ equal to the voltage regulator reference voltage applied to the Error Amplifier non-inverting input.

$R_{droop}$ is a component of the voltage regulator stability compensation network. Regulator stability and dynamic response are *somewhat* insensitive to the value of $R_{droop}$, since a parallel series-RC will dominate the compensator response at, and well below, the open loop crossover frequency. But $R_{droop}$ plays a singular role in determining the DC loadline, and so will be chosen solely for that purpose.

For a desired $R_{LL}$, the output voltage reduction, $V_{droop}$, due to an output load current, $I_o$, is as shown by Equation 40.

$$V_{droop} = R_{LL} \times I_o \quad \text{(EQ. 4}$$

The value of $V_{droop}$ obtained from the ISL95820 controller is the droop current, $I_{droop}$, multiplied by the droop resistor, $R_{droop}$. Using Equation 41, this value is as shown by Equation 41.

Equate these two expressions for $V_{droop}$ and solve for $R_{droop}$ to obtain the value in Equation 42.

$$R_{droop} = \frac{Ri \times R_{LL}}{\rho_o} \quad \text{(EQ. 42)}$$

$$V_{droop} = I_{droop} \times R_{droop} = \frac{\rho_o}{Ri} \times I_o \times R_{droop} \quad \text{(EQ. 4}$$

## PHASE DUTY CYCLE BALANCING

To equally distribute power dissipation between the phases, the ISL95820 provides a means to reduce the deviation of the duty cycle of each phase from the average of all phases. The controller achieves duty cycle balance by matching the ISEN*n* pin voltages. The connection of these pins to their respective phase nodes is depicted in Figure 23 for the inductor DCR current sense method. The current balancing methods described in this section apply also to current sensing using discrete sense resistors.

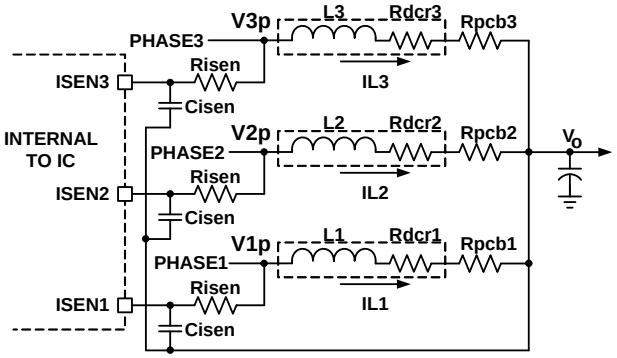



FIGURE 23. CURRENT BALANCING CIRCUIT

The phase nodes have high amplitude square-wave voltage waveforms, for which the comparative duty cycle is indicative of each phase's relative contribution to the output. $R_{isen}$ and $C_{isen}$ form lowpass filters to remove the switching ripple of the phase node voltages, such that the average voltages at the ISEN*n* pins approximately indicate each phase's duty cycle, and thus the relative contribution of each phase. The controller gradually, and continually, trims the R3™ modulator slave circuits, such that the relative duty cycle of each phase, as indicated by each $V_{ISENn}$, is equal to the others. This adjustment occurs slowly compared to the dynamic response of the multi-phase modulator to output voltage commands, load transients, and other system perturbations. It is recommended to use a large $R_{isen}C_{isen}$ time constant, such that the $ISEN_n$ voltages have small ripple and are representative of the average or steady-state contribution of each phase to the output. Recommended values are $R_{isen}$ = 10kΩ and $C_{isen}$ = 0.22µF.

Ideally, balancing the phase duty cycles will also balance the output current provided by each phase, and thus the power dissipated in each phase's components. This will be the case if the current sense elements of each phase are identical (DCR of the inductors, or discrete current sense resistors, and the associated current sense networks), and if parasitic resistances of the circuit board traces from the sense connections to the common output voltage node are identical. Figure 23 includes

the printed circuit trace resistances from each phase to the common output node. If these trace resistances are all equal, then the ideal of phase current balance will be achieved. This balance assumes the inductors and other current sense components are identical, comparing each phase to the others, a true assumption within the published tolerance of component parameters.

Figure 23 includes the trace-resistance from each inductor to a single common output node. Note that each $R_{isen}$ connection (V1p, V2p, and V3p) should be routed to its respective inductor phase-node-side pad in order to eliminate the effect of phase node parasitic PCB resistance from the switching elements to the inductor. Equations 43 thru 45 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} + Vo \quad \text{(EQ. 43)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} + Vo \quad \text{(EQ. 44)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} + Vo \quad \text{(EQ. 45)}$$

where $R_{dcr1}$, $R_{dcr2}$ and $R_{dcr3}$ are the respective inductor DCRs; $R_{pcb1}$, $R_{pcb2}$ and $R_{pcb3}$ are the respective parasitic PCB resistances between the inductor output-side pad and the output voltage rail; and $I_{L1}$, $I_{L2}$ and $I_{L3}$ are inductor average currents.

The controller will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when there are $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Since using the same components for L1, L2 and L3 will typically provide a good match of $R_{dcr1}$, $R_{dcr2}$ and $R_{dcr3}$, board layout will determine $R_{pcb1}$, $R_{pcb2}$ and $R_{pcb3}$, and thus the matching of current per phase. It is recommended to have symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

While careful symmetrical layout of the circuit board can achieve very good matching of these trace resistances, such layout is often difficult to achieve in practice. If trace resistances differ, then exact matching the duty cycles of the phases will result in the *imbalance* of the phase currents. A modification of this circuit (to couple the signals of all the phases in the ISEN*n* networks), can correct the current imbalance due to unequal trace resistances to the output.

For the example case of a 3-phase configuration, Figure 24 shows the current balancing circuit with the recommended trace-resistance imbalance correction. As before, V1p, V2p, and V3p should be routed to their respective inductor phase-node-side pads in order to eliminate the effect of phase node parasitic PCB resistance from the switching elements to each inductor. The sensing traces for V1n, V2n, and V3n should be routed to the $V_{OUT}$ output-side inductor pads so they indicate the voltage due only to the voltage drop across the inductor DCR, and not due to the PCB trace resistance.

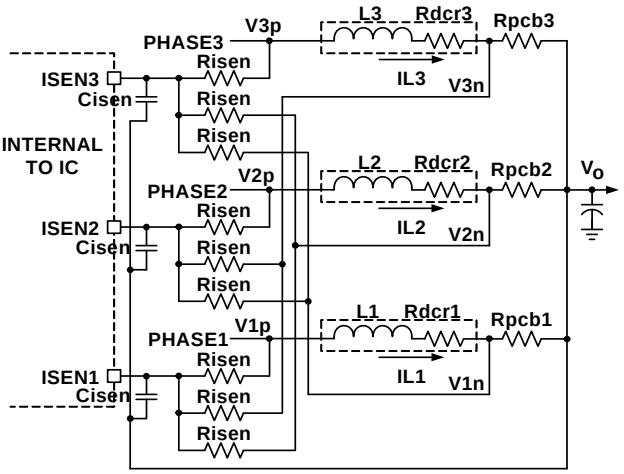



FIGURE 24. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Each ISEN pin sees the average voltage of three sources: its own phase inductor phase-node pad, and the other two phases inductor output-side pads. Equations 46 thru 48 give the ISEN pin voltages:

$$V_{ISEN1} = \frac{(V_{1p} + V_{2n} + V_{3n})}{3} \quad \text{(EQ. 46)}$$

$$V_{ISEN2} = \frac{(V_{1n} + V_{2p} + V_{3n})}{3} \quad \text{(EQ. 47)}$$

$$V_{ISEN3} = \frac{(V_{1n} + V_{2n} + V_{3p})}{3} \quad \text{(EQ. 48)}$$

The controller will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, resulting in the equalities shown in Equations 49 and 50:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 49)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 50)}$$

Simplifying Equation 49 gives Equation 51:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 51)}$$

and simplifying Equation 50 gives Equation 52:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 52)}$$

Combining Equations 51 and 52 gives Equation 53:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 53)}$$

Which produces the desired result in Equation 54:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 54)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) will be achieved independently of any mismatch of $R_{pcb1}$, $R_{pcb2}$, and $R_{pcb3}$, to within the tolerance of the resistance of the current sense elements. Note that with the crosscoupling of Figure 25, the phase balancing circuit no longer seeks to equalize the duty cycles of the phases, but rather to equalize the DC components of the voltage drops across the current sense elements.

Small absolute differences in PCB trace resistance from the inductors to the common output node, can result in significant phase current imbalance. It is strongly recommended that the resistor pads and connections for the current balancing method be included in any PCB layout. The decision to include the additional Nx(N-1) trace-resistance-correcting resistors can then be deferred until the extent of the current imbalance can be measured on a functioning circuit. Considerations for making this decision are described in “Current Sense OFFSET Error” on page 28.

With the ISEN*n* phase balancing mechanism (with cross coupling resistors if needed, or without if not needed), the R3™ modulator achieves excellent current balancing during both steady state and transient operation. Figure 25 shows current balancing performance of an evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at low rep rate, but cannot track the load when the rep rate gets into the hundred-kHz range, which is outside of the control loop bandwidth. Regardless, the controller achieves excellent current *balancing* in all cases.

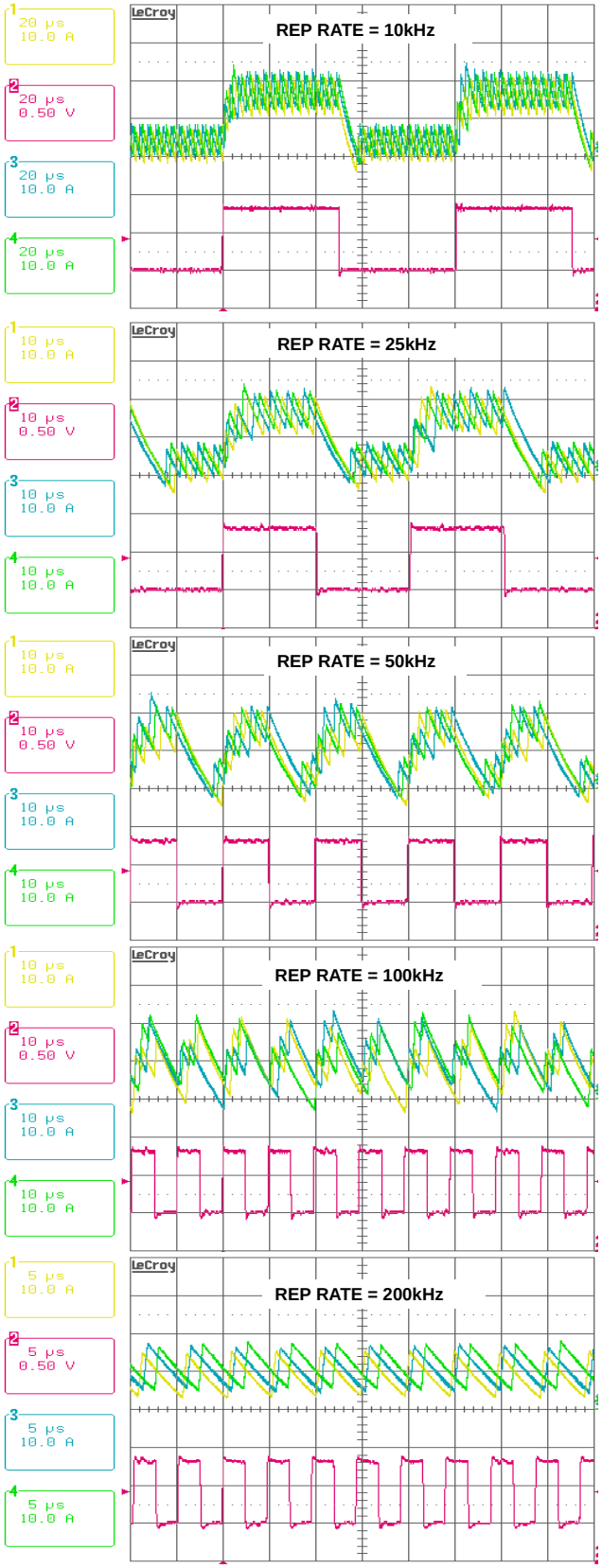



FIGURE 25. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: IL1, CH2: $I_{LOAD}$, CH3: IL2, CH4: IL3

## Current Sense Circuit Adjustments

Once the voltage regulator is designed and a functional prototype has been assembled, adjustments may be necessary to correct for non-ideal components, or assembly and printed circuit board parasitic effects. These are effects that are usually not known until the design has been realized. The following adjustments should be considered when refining a product design.

### VERIFICATION OF INDUCTOR-DCR CURRENT-SENSE POLE-ZERO MATCHING

Recall that if the inductor DCR is used as the phase current sense-element, it is necessary to select the capacitor $C_n$ such that the current sense transfer function pole at $\omega_{sns}$, matches the zero at $\omega_L$. The ideal response to a load step, with DC Loadline (i.e., "droop") enabled, is shown in Figure 26.

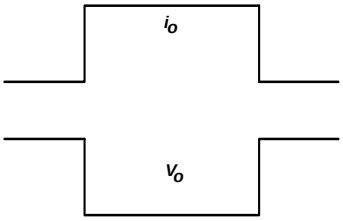



FIGURE 26. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

Figure 27 shows the load step transient response when $C_n$ is too large. $V_{core}$ droop response (rising or falling) lags in settling to its final value.

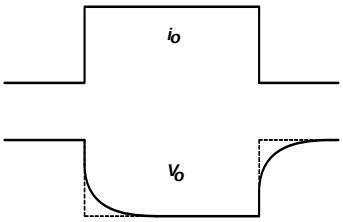



FIGURE 27. LOAD TRANSIENT RESPONSE WHEN $C_n$ IS TOO LARGE

Figure 28 shows the load step response when Cn is too small. $V_{core}$ response is underdamped, and overshoots before settling to its final voltage.

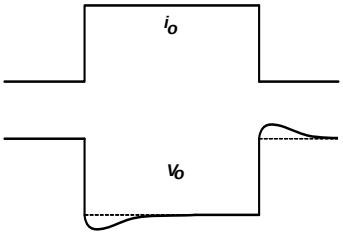



FIGURE 28. LOAD TRANSIENT RESPONSE WHEN $C_n$ IS TOO SMALL

Once the regulator design is complete, the measured load step response can be compared to Figures 26 through 28. $C_n$ should be adjusted if necessary to obtain the behavior of Figure 26.

### CURRENT SENSE SENSITIVITY ERROR

The current sense, IMON, and DC Loadline (droop) network component values should be designed according to the instructions in "Current Sense Circuit Adjustments" on page 28. This will ensure the correct *ratio* of $V_{IMON}$ to $I_{droop}$ (which determines $R_{LL}$) for the chosen system design parameters, for which no adjustment should be required. However, testing of the resulting circuit may reveal a measurement *sensitivity* error factor, which should effect $V_{IMON}$ and $I_{droop}$ equally. This error may be seen as a too-large $R_{LL}$ value (droop voltage per load current), and as a too-large IMON voltage for a given load current. A single component modification will correct both errors.

The current sense resistance value per phase (either a discrete sense resistor, or the inductor DCR) is typically very small, on the order of 1m$\Omega$. The solder connections used in the assembly of such sense elements may contribute significant resistance to these sense elements, resulting in a larger load-dependent voltage drop than due to the sense element alone. Thus, the sensed output current value will be greater than intended for a given load current. If this is the case, then the value of Ri (the ISUMN pin resistor) should be increased by the factor of the sensitivity error. For example, if the current sense value is 3% larger than intended, then Ri should be increased by 3%. Changing Ri will change the sensitivity, with respect to $I_{OUT}$, of $V_{IMON}$ and $I_{droop}$ by the same factor, thus simultaneously correcting the IMON voltage error and the loadline resistance, while preserving the intended ratio between the two parameters.

Note that the assembly procedure for installing the current sense elements (sense resistors or inductors) can have a significant impact on the effective total resistance of each sense element. It is important that any adjustments to Ri be performed on circuits that have been assembled with the same procedures that will be used in mass production. The current measurement sensitivity error should be determined on a sufficient number of samples to avoid adjusting sensitivity to correct what may be a component-tolerance outlier.

### CURRENT SENSE OFFSET ERROR

Nonlinearity of the $R_{SUM}$ resistors can induce a small positive offset in the ISUMP voltage, and thus in the IMON pin current (viewed as a positive offset in the ICC register value), and also in the droop current (viewed as an output voltage negative offset). The offset error occurs as follows: for each inductor, the instantaneous voltage across its $R_{SUM}$ resistor is approximately $V_{RSUM} = V_{PHASE} - V_{VOUT}$. During that phase's on time, $V_{PHASE} = V_{VIN}$, giving $V_{RSUM-ON} = V_{VIN} - V_{VOUT}$. During the off time, $V_{PHASE} = 0V$, and so $V_{RSUM-OFF} = -V_{VOUT}$. For the example of $V_{VOUT} = 1.8V$ and $V_{VIN} = 12V$, $V_{RSUM-ON} = 10.2V$ and $V_{RSUM-OFF} = -1.8V$, a sign-dependent magnitude difference exceeding 8V. Inexpensive thick film resistors can have a voltage nonlinearity of 25ppm/volt or more, with the device resistance decreasing with increasing voltage. Because of this $R_{SUM}$ resistor nonlinearity, each $R_{SUM}$'s (positive) current into the common ISUMP node (during its on-time) will be biased slightly greater than the nominal V/R value expected. Each $R_{SUM}$'s (negative) current (during its off-time) will also be biased negatively due to the resistor nonlinearity, but less so because the $R_{SUM}$ voltage magnitude is always much less during the off-time than during the on-time. This nonlinearity-bias-current polarity mismatch causes a small positive offset error in $V_{ISUMP}$.

The exact magnitude of this offset error is difficult to predict. It depends on an attribute of the sense resistors that is typically not specified or controlled, and so not reliably quantified. It also varies with the input voltage and the output voltage. If battery powered, the input voltage can vary significantly. The output voltage is subject to the VID setting, and to a lesser extent on the droop voltage. A further complication is that the nonlinearity offset changes with the number of active phases. For a 4-phase configuration in PS0, four $R_{SUM}$ resistors are subjected to the high difference in on-time compared to off-time voltage magnitudes. But in PS1, two phases are disabled with the respective PHASE nodes approximately following the output. So $V_{RSUM}$ for the disabled phases is approximately zero for the entire switching cycle, reducing the offset error by half. In PS2, three phases are disabled, leaving only a fourth of the PS0 offset error.

The most direct solution to the phenomenon of current sense offset due to resistor nonlinearity is to use highly linear summing resistors, such as thin film resistors. But the magnitude of the offset error typically does not warrant the considerably greater expense of doing so. Instead, a correcting fixed offset can be introduced to the current sense network.

For the example case described, with each thick film $R_{SUM}$ = 3.65kΩ, and an $I_{CC(MAX)}$ setting of 100A, the current sense offset error in PS0 typically represents less than 1% of full scale, and is always positive. It has been found empirically that a 10MΩ pulldown resistor, from the ISUMP node to ground, provides a good correcting offset compromise, slightly under-correcting in PS0, and slightly over-correcting in PS2, but meeting processor vendor specification tolerances with adequate margin in all cases. For other applications, a suitable compromise pull-down resistor can be determined empirically by testing over the full range of expected operating conditions and power states. It is recommended that this resistor be included in any VR design layout to allow population of the pull-down resistor if required. Because of the high value of resistance, two smaller valued resistors in series may be preferred, to reduce the environmental sensitivity of high resistance value devices.

## PHASE CURRENT BALANCING

Phase current imbalance should be measured on a functioning circuit. First determine the correct assembly of the current balancing mechanism by measuring, on a stable operating regulator, the voltage difference between the ISEN1 pin and the remaining ISEN*n* pins (of all the operational phases) with various static loads applied. Whether using the simplest circuit of Figure 1 on page 1, or the PCB trace resistance compensating circuit of Figure 2 on page 7, the voltage difference between any pair of the ISEN*n* pins should be very small, usually less than 1mV. If not, there may be an assembly error.

Then, again with various static loads applied, measure the voltage directly across each active sense element (sense resistor or inductor). Any discrepancy in the phase sense element voltages beyond what can be attributed to the sense element resistance tolerance must be due to PCB trace resistance deviations. Install the cross-coupling resistors of Figure 29, and again compare the sense element voltages. Now the sense element voltages should be the same among the phases in all cases (to within the tolerance of the cross-coupling resistors), and the phase current balance will be within the parametric tolerance of the sense element resistance, independently of the PCB trace resistance differences.

The decision to populate the cross-coupling phase sense resistors will depend upon the magnitude of, and system tolerance of, the uncorrected imbalance current.

## LOAD STEP RING BACK

Figure 29 shows the output voltage ring back problem during load transient response with DC Loadline (i.e., “droop”) enabled. The load current $i_o$ has a fast step change, but the inductor current $i_L$ cannot accurately follow. Instead, $i_L$ responds in first order system fashion due to the nature of current loop. The ESR and ESL effect of the output capacitors makes the output voltage $V_o$ dip quickly upon load current change. However, the controller regulates $V_o$ according to the droop current $i_{droop}$, which is a real-time representation of $i_L$; therefore it pulls $V_o$ back to the level dictated by $i_L$, causing the ring back problem. This phenomenon is not observed when the output capacitor bank has very low ESR and ESL, such as if using only ceramic capacitors.

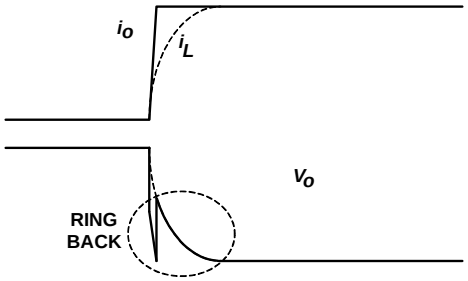



FIGURE 29. OUTPUT VOLTAGE RING BACK PROBLEM

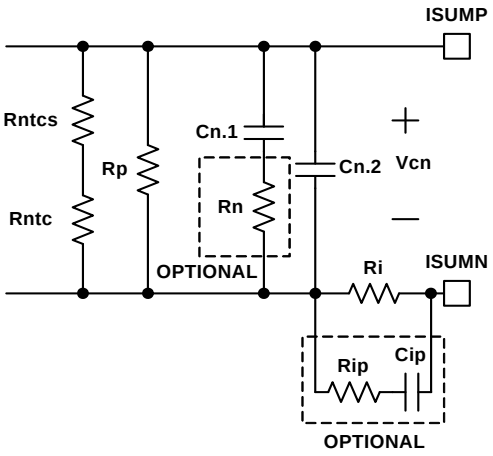



FIGURE 30. OPTIONAL CIRCUITS FOR RING BACK REDUCTION

Figure 30 shows two optional circuits for reduction of the ring back.

$C_n$ is the capacitor used to match the inductor time constant. It often takes the paralleling of multiple capacitors to get the desired value. Figure 30 shows that two capacitors $C_{n.1}$ and $C_{n.2}$ are in parallel. Resistor $R_n$ is an optional component to reduce the $V_o$ ring back. At steady state, $C_{n.1} + C_{n.2}$ provides the desired $C_n$ capacitance. At the beginning of $i_o$ change, the effective

capacitance is less because $R_n$ increases the impedance of the $C_{n.1}$ branch. As Figure 28 shows, $V_o$ tends to dip when $C_n$ is too small, and this effect will reduce the $V_o$ ring back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when $R_n$ is bigger. However, the presence of $R_n$ increases the ripple of the $V_n$ signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. $R_n$ value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and $R_n$ values should be determined through tuning the load transient response waveforms directly on the target system circuit board.

$R_{ip}$ and $C_{ip}$ form an R-C branch in parallel with $R_i$, providing a lower impedance path than $R_i$ at the beginning of $I_{OUT}$ change. $R_{ip}$ and $C_{ip}$ do not have any effect at steady state. Through proper selection of $R_{ip}$ and $C_{ip}$ values, $I_{droop}$ can resemble $I_{OUT}$ rather than $i_L$, and $V_o$ will not ring back. The recommended value for $R_{ip}$ is 100Ω. $C_{ip}$ should be determined by observing the load transient response waveforms in a physical circuit. The recommended range for $C_{ip}$ is 100pF~2000pF. However, it should be noted that the $R_{ip}$ -$C_{ip}$ branch may distort the $I_{droop}$ waveform. Instead of being triangular as the real inductor current, $I_{droop}$ may have sharp spikes, which may adversely affect $I_{droop}$ average value detection and therefore may affect OCP accuracy.

## Voltage Regulation

### COMPENSATOR

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network, so the VR achieves constant output impedance as a stable system. Please go to www.intersil.com/design/ to request spreadsheet.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop, which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 31 conceptually shows T1(s) measurement set-up and Figure 32 conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. T(1) is measured after the summing node, and T2(s) is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can be actually measured on an ISL95820 regulator.

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s) and has more meaning of system stability.

T2(s) is the voltage loop gain with closed droop loop. It has more meaning of output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin, and output impedance equal or smaller than the load line slope.

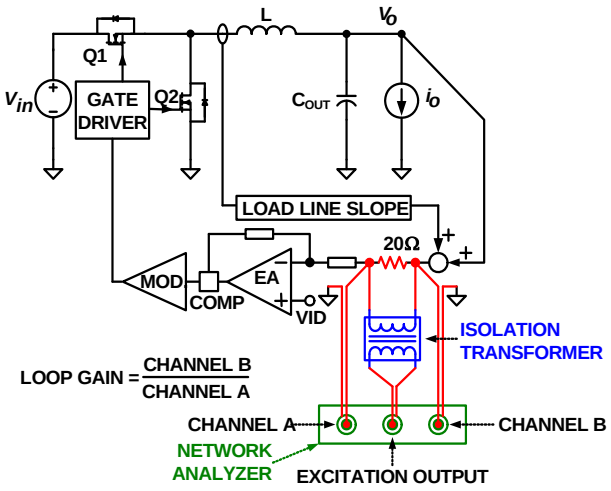



FIGURE 31. LOOP GAIN T1(s) MEASUREMENT SET-UP

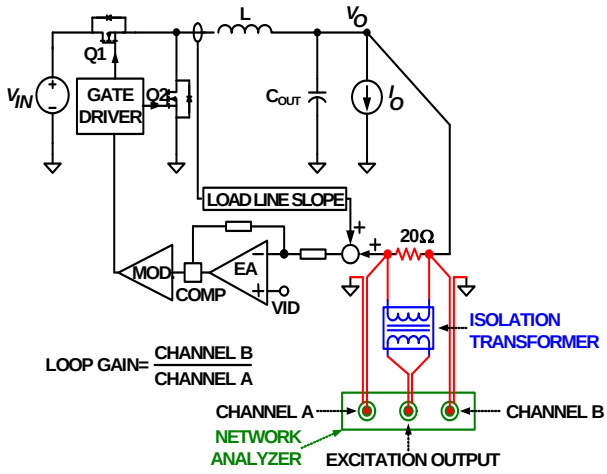



FIGURE 32. LOOP GAIN T2(s) MEASUREMENT SET-UP

### FB2 Function

The FB2 function allows modification of the compensator when operating in 1-phase. Figure 33 shows the FB2 function.

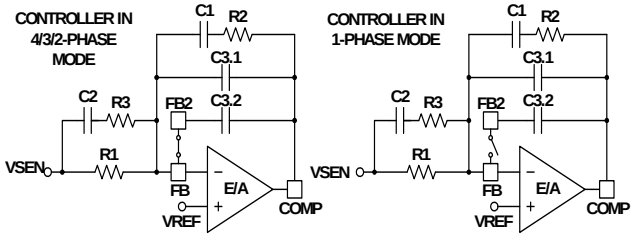



FIGURE 33. FB2 FUNCTION

A switch (called FB2 switch) turns on (closes) to short, internally, the FB and the FB2 pins when the controller is in 4-phase, 3-phase or 2-phase mode. When FB2 is closed, capacitors C3.1 and C3.2 are in parallel, serving as part of the compensator. When the controller enters 1-phase mode, the FB2 switch opens, removing

C3.2 and leaving only C3.1 in the compensator. The compensator gain will increase with the removal of C3.2. By properly sizing C3.1 and C3.2, the compensator can be optimized separately for 4-, 3-, 2-phase modes and for 1-phase mode.

While the FB2 switch is open and C3.2 is disconnected from the FB pin, the controller actively drives the FB2 pin voltage to track the FB pin voltage, such that the C3.2 voltage remains equal to the C3.1 voltage. When the controller closes the FB2 switch, C3.2 will be reconnected to the compensator smoothly with no capacitor voltage discontinuities.

The FB2 function ensures excellent transient response in 4-, 3-, 2-phase modes and in 1-phase mode. If one decides not to use the FB2 function, simply populate C3.1 only.

### FB3 Function

The FB3 function allows for changing the compensator loop gain depending on whether the $V_{OUT}$ droop function is enabled. Figure 34 shows the FB3 pin function.

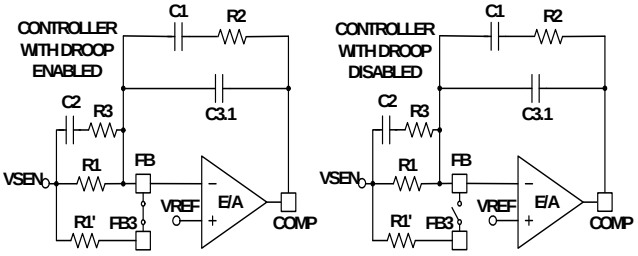



FIGURE 34. FB3 FUNCTION

A switch (called the FB3 switch) turns on to short ( internally) the FB and the FB3 pins, whenever the droop function is enabled. Resistors R1 and R1' are in parallel when droop is enabled, together setting the droop loadline resistance, and serving as part of the compensator. When droop is disabled, the FB3 switch turns off (opens), removing R1' and leaving only R1 in the compensator. The compensator gain will decrease with the removal of R1'. By properly sizing R1 and R1', the compensator can be optimized separately for both droop enabled and disabled.

To use the FB3 function, the droop resistor ($R_{droop}$ in Equation 56) is the parallel combination of R1 and R1'. The compensator will use R1 only while droop is disabled, and R1 in parallel with R1' when droop is enabled. If one decides not to use the FB3 function, simply populate R1 only.

## START-UP TIMING

With the controller's $V_{DD}$ voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the logic high threshold. Figure 35 shows the typical start-up timing. The controller uses digital soft-start to ramp-up DAC to the voltage programmed by the SetVID command. PGOOD is asserted high and ALERT# is asserted low at the end of the ramp up. Similar behavior occurs if VR_ON is tied to $V_{DD}$, with the soft-start sequence starting 2.3ms after $V_{DD}$ crosses the POR threshold.

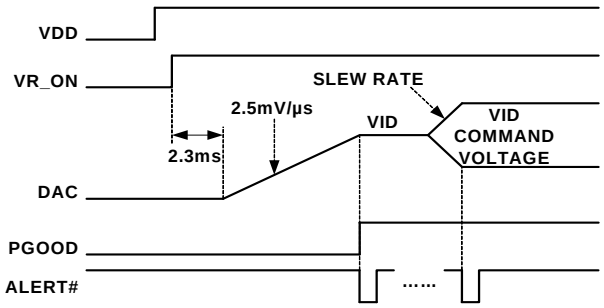



FIGURE 35. VR SOFT-START WAVEFORMS

## VOLTAGE REGULATION

After the start sequence, the controller regulates the output voltage to the value set by the VID information per Table 5. The controller will control the no-load output voltage to an accuracy of ±0.5% over the VID range. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die. This mechanism is illustrated in Figure 22. $VCC_{SENSE}$ and $VSS_{SENSE}$ are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the $VSS_{SENSE}$ voltage and adds it to the DAC output. Note how the illustrated DC Loadline mechanism (the "droop" mechanism, described in "Programming the DC Loadline" on page 24), introduces a load-dependent reduction in the output voltage, (denoted $VCC_{SENSE}$), below the VID value output by the DAC. The error amplifier regulates the inverting and the non-inverting input voltages to be equal, as shown in Equation 55:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 55)}$$

Rewriting Equation 55 and substitution of Equation 5 gives Equation 56:

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 56)}$$

Equation 56 is the exact equation required for load line implementation.

The $VCC_{SENSE}$ and $VSS_{SENSE}$ signals come from the processor die. The feedback will be open circuit in the absence of the processor. As Figure 22 shows, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without a processor installed.

The maximum VID (output voltage command) value supported is 2.3V. Any VID command (or sum of VID command and VID offset) above 2.3V will be ignored.

TABLE 5. VID TABLE

| VID | | | | | | | | HEX | | $V_O$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | VR12.5 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.00000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.50000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2 | 0.51000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 3 | 0.52000 |

TABLE 5. VID TABLE (Continued)

| VID | | | | | | | | HEX | | $V_O$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | VR12.5 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4 | 0.53000 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 5 | 0.54000 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 6 | 0.55000 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 7 | 0.56000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8 | 0.57000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 9 | 0.58000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | A | 0.59000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | B | 0.60000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | C | 0.61000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | D | 0.62000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | E | 0.63000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | F | 0.64000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0.65000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0.66000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 2 | 0.67000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 3 | 0.68000 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 4 | 0.69000 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 5 | 0.70000 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 6 | 0.71000 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 7 | 0.72000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 8 | 0.73000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 9 | 0.74000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | A | 0.75000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B | 0.76000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | C | 0.77000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | D | 0.78000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | E | 0.79000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | F | 0.80000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 2 | 0 | 0.81000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 2 | 1 | 0.82000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 2 | 2 | 0.83000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 2 | 3 | 0.84000 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 2 | 4 | 0.85000 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 2 | 5 | 0.86000 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 2 | 6 | 0.87000 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 2 | 7 | 0.88000 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 2 | 8 | 0.89000 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 2 | 9 | 0.90000 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2 | A | 0.91000 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2 | B | 0.92000 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2 | C | 0.93000 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2 | D | 0.94000 |

TABLE 5. VID TABLE (Continued)

| VID | | | | | | | | HEX | | $V_O$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | VR12.5 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2 | E | 0.95000 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 2 | F | 0.96000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 3 | 0 | 0.97000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 3 | 1 | 0.98000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 3 | 2 | 0.99000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 3 | 3 | 1.00000 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 3 | 4 | 1.01000 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 3 | 5 | 1.02000 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 3 | 6 | 1.03000 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 3 | 7 | 1.04000 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 3 | 8 | 1.05000 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 3 | 9 | 1.06000 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3 | A | 1.07000 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3 | B | 1.08000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3 | C | 1.09000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 3 | D | 1.10000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3 | E | 1.11000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 3 | F | 1.12000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 | 1.13000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 4 | 1 | 1.14000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 4 | 2 | 1.15000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 4 | 3 | 1.16000 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | 4 | 1.17000 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 4 | 5 | 1.18000 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 4 | 6 | 1.19000 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 4 | 7 | 1.20000 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 4 | 8 | 1.21000 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 4 | 9 | 1.22000 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 4 | A | 1.23000 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 4 | B | 1.24000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4 | C | 1.25000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 4 | D | 1.26000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 4 | E | 1.27000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4 | F | 1.28000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 5 | 0 | 1.29000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 5 | 1 | 1.30000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 5 | 2 | 1.31000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 5 | 3 | 1.32000 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 5 | 4 | 1.33000 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 5 | 5 | 1.34000 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 5 | 6 | 1.35000 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 5 | 7 | 1.36000 |

TABLE 5. VID TABLE (Continued)

| VID | | | | | | | | HEX | | $V_O$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | VR12.5 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 5 | 8 | 1.37000 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 5 | 9 | 1.38000 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5 | A | 1.39000 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 | B | 1.40000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5 | C | 1.41000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5 | D | 1.42000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5 | E | 1.43000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5 | F | 1.44000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 6 | 0 | 1.45000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 6 | 1 | 1.46000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 6 | 2 | 1.47000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 6 | 3 | 1.48000 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 6 | 4 | 1.49000 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 6 | 5 | 1.50000 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 6 | 6 | 1.51000 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 6 | 7 | 1.52000 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 6 | 8 | 1.53000 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 6 | 9 | 1.54000 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 6 | A | 1.55000 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 6 | B | 1.56000 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6 | C | 1.57000 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 6 | D | 1.58000 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 6 | E | 1.59000 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 6 | F | 1.60000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 | 0 | 1.61000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 7 | 1 | 1.62000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 7 | 2 | 1.63000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 7 | 3 | 1.64000 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 7 | 4 | 1.65000 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 7 | 5 | 1.66000 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 7 | 6 | 1.67000 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 7 | 7 | 1.68000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 7 | 8 | 1.69000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 7 | 9 | 1.70000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7 | A | 1.71000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 7 | B | 1.72000 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7 | C | 1.73000 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 7 | D | 1.74000 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7 | E | 1.75000 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7 | F | 1.76000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 | 1.77000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 8 | 1 | 1.78000 |

TABLE 5. VID TABLE (Continued)

| VID | | | | | | | | HEX | | $V_O$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | VR12.5 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 8 | 2 | 1.79000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 8 | 3 | 1.80000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8 | 4 | 1.81000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 8 | 5 | 1.82000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 8 | 6 | 1.83000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 8 | 7 | 1.84000 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 | 8 | 1.85000 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 8 | 9 | 1.86000 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 8 | A | 1.87000 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8 | B | 1.88000 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 8 | C | 1.89000 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 8 | D | 1.90000 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 8 | E | 1.91000 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8 | F | 1.92000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 9 | 0 | 1.93000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 9 | 1 | 1.94000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 9 | 2 | 1.95000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 9 | 3 | 1.96000 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 9 | 4 | 1.97000 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 9 | 5 | 1.98000 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 9 | 6 | 1.99000 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 9 | 7 | 2.00000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 9 | 8 | 2.01000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 9 | 9 | 2.02000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 9 | A | 2.03000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 9 | B | 2.04000 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 9 | C | 2.05000 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 9 | D | 2.06000 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 9 | E | 2.07000 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 9 | F | 2.08000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A | 0 | 2.09000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A | 1 | 2.10000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A | 2 | 2.11000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | A | 3 | 2.12000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A | 4 | 2.13000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A | 5 | 2.14000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | A | 6 | 2.15000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | A | 7 | 2.16000 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A | 8 | 2.17000 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | A | 9 | 2.18000 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | A | A | 2.19000 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | A | B | 2.20000 |

TABLE 5. VID TABLE (Continued)

| VID | | | | | | | | HEX | | $V_O$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | VR12.5 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | A | C | 2.21000 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | A | D | 2.22000 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | A | E | 2.23000 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | A | F | 2.24000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B | 0 | 2.25000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B | 1 | 2.26000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B | 2 | 2.27000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B | 3 | 2.28000 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B | 4 | 2.29000 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B | 5 | 2.30000 |

## DYNAMIC VID OPERATION

The controller receives VID commands via either the Serial VID (SVID) port or the serial $I^2C$/SMBus/PMBus port. It responds to VID changes by slewing to the new voltage at a slew rate indicated in the SetVID command. There are three SetVID slew rates: SetVID_fast, SetVID_slow, and SetVID_decay.

SetVID_fast command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a slew rate up to but not to exceed 10mV/µs.

SetVID_slow command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a slew rate up to but not to exceed 2.5mV/µs.

SetVID_decay command prompts the controller to enter DEM. The output voltage will decay down to the new VID value at a slew rate determined by the load. If the voltage decay rate is too fast, the controller will limit the voltage slew rate to the fast slew rate of 10mV/µs. If DEM is disabled by the PROG2 programming resistor, the SVID command "SetVID_decay" executes as single-phase (Phase 1 only) “SetVID_slow” except that ALERT# signaling mimics that of the “SetVID_decay” command.

ALERT# is asserted (low) upon completion of all non-zero VID transitions.

Figure 36 shows SetVID Decay Pre-Emptive response, which occurs whenever a new VID command is received before completion of a previous SetVID Decay command.

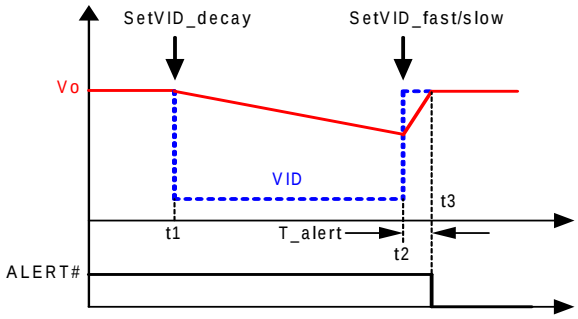



FIGURE 36. SETVID DECAY PRE-EMPTIVE BEHAVIOR

In the example scenario of Figure 36, the controller receives a SetVID_decay command at t1. The VR enters DEM and the output voltage Vo decays down slowly. At t2, before Vo reaches the intended VID target of the SetVID_decay command, the controller receives a SetVID_fast (or SetVID_slow) command to go to a voltage higher than the actual Vo. The controller will preempt the decay to the lower voltage and slew Vo to the new target voltage at the slew rate specified by the SetVID command. At t3, Vo reaches the new target voltage and the controller asserts the ALERT# signal.

## SLEW RATE COMPENSATION CIRCUIT FOR VID TRANSITION

During a large VID transition, the DAC steps through the VID table at proscribed step rate. For example, the DAC may change 1 tick (10mV) per $1^+$µs, controlling output voltage $V_{core}$ slew rate at less than 10mV/µs, or 1 tick per $4^+$µs, controlling output voltage $V_{core}$ slew rate at less than 2.5mV/µs.

Figure 37 shows the waveforms of VID transition.

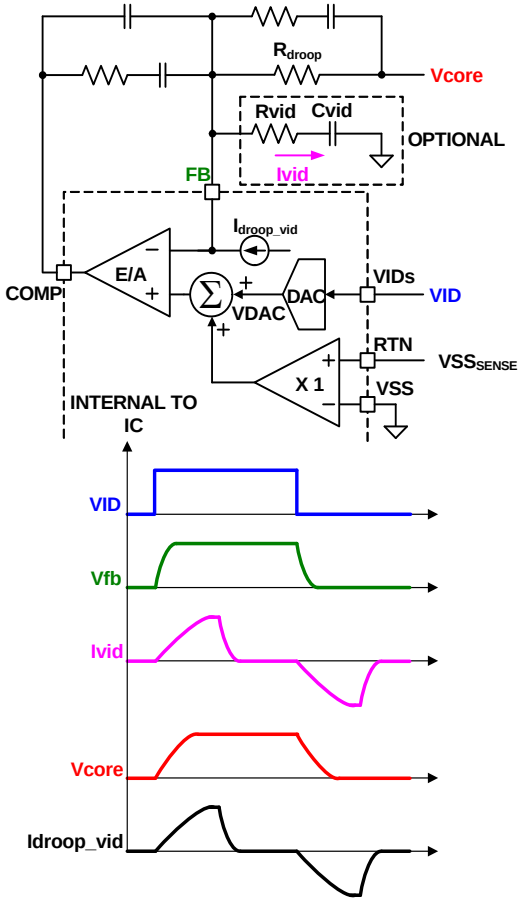



FIGURE 37. SLEW RATE COMPENSATION CIRCUIT FOR VID TRANSITION

During VID transition, the output capacitor is being charged and discharged, causing $C_{out}$ x $dV_{core}/dt$ current on the inductor. The controller senses the inductor current increase during the up transition (as the $I_{droop\_vid}$ waveform shows) and will droop the output voltage $V_{core}$ accordingly, making $V_{core}$ slew rate slow. Similar behavior occurs during the down transition. To get the correct $V_{core}$ slew rate during VID transition, one can add the $R_{vid}$-$C_{vid}$ branch, whose current $I_{vid}$ compensates for $I_{droop\_vid}$.

Choose the R, C values from the reference design as a starting point, then tweak the actual values on the board to get the best performance.

During normal transient response, the FB pin voltage is held constant, therefore is virtual ground in small signal sense. The $R_{vid}$ - $C_{vid}$ network is between the virtual ground and the real ground, and hence has no effect on transient response.

### EXTENDED $V_{OUT}$ RANGE

If a higher (than max supported VID) output voltage is required, such as for overclocking applications, the feedback voltage can be divided down to the FB pin such that $V_{FB}$ = VID for $V_{VOUT}$ > VID. Figure 38 shows the addition of resistor Rg (and optional 2N7002 switch), which adds the feedback voltage division to the schematic of Figure 22 on page 25.

With the 2N7002 off, $V_{VOUT}$ = VID – Vdroop = VID – Rdroop*Idroop, the same as in the normal configuration. But with the 2N7002 switch closed, $V_{OUT}$ = VID -(Idroop - VID/Rg)*Rdroop = VID (1 + Rdroop/Rg) – Idroop*Rdroop.

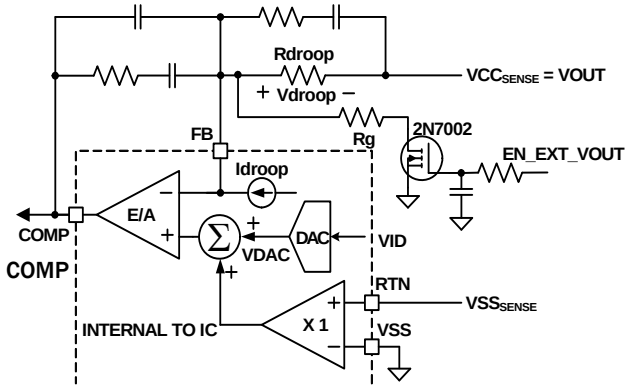



FIGURE 38. EXTENDING THE RANGE OF VOUT WITH A FEEDBACK RESISTOR DIVIDER

The unloaded output voltage is then $V_{VOUT\ (unloaded)}$ = VID (1 + Rdroop/Rg), and the droop voltage Vdroop = Idroop*Rdroop. Notice that the droop voltage is determined by the droop resistor, and is independent of whether the feedback voltage is divided or not. Then Rg is selected to obtain the desired divider ratio. The programmed loadline resistance is not affected by the addition of Rg.

To avoid false OVP faults, the OVP threshold may have to be changed to 3.3V fixed, rather than at the relative value of 300mV above VID, via the PMBus interface (see “Fault Protection” on page 35 for details). The OVP threshold must be changed prior to turning on the EN_EXT_VOUT switch. Because of OVP, a practical upper limit for $V_{VOUT}$ is 3.04V, which is also the maximum *defined* VID value. The maximum *supported* VID value in the ISL95820 is 2.3V, so the inverse divider ratio (1 + Rdroop/Rg) should not exceed 1.32.

Because the higher output voltage requires a higher switching duty cycle, a higher slope compensation value may be required for stability.

The abrupt inclusion of Rg to the feedback network will create a step in the selected output voltage, which may result in high overshoot or ringing in the output. The RC network on the gate of the 2N7002 may slow the transition from normal range to extended range.

Note that with extended range enabled, the VID step size will increase by the inverse divider ratio. Consequently, the DVID slew rates will also increase by the same ratio.

# Fault Protection

The ISL95820 provides overcurrent, current-balance and overvoltage fault protections. The controller also provides over-temperature protection.

The controller determines overcurrent protection (OCP) by comparing the average value of the droop current $I_{droop}$ with an internal current source threshold as Table 4 shows. It declares OCP when $I_{droop}$ is above the threshold for 120µs.

The controller monitors the ISEN pin voltages to determine current-balance protection. If the difference of one ISEN pin voltage and the average ISENs pin voltage is greater than 9mV (for at most 4ms), the controller will declare a fault and latch off.

The controller takes the same actions for all of the above fault protections: de-assertion of PGOOD and turn-off of all the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes.

The controller will declare an overvoltage protection (OVP) fault and de-assert PGOOD if the voltage of the ISUMN pin (approximately the output voltage) exceeds the VID set value by +300mV. Optionally, the overvoltage threshold can be set, via the PMBus interface, to 3.3V fixed. The controller will immediately declare an OV fault, de-assert PGOOD, and turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value when all power MOSFETs are turned off. If the output voltage rises above the VID set value again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground.

The default overvoltage fault threshold is 2.6V when output voltage ramps up from 0V. The overvoltage fault threshold reverts to VID + 300mV after the output voltage settles. Optionally, via the PMBus interface, the overvoltage threshold can be fixed at 3.3V prior to increasing VID from 0V.

All the above fault conditions can be reset by bringing VR_ON low or by bringing $V_{DD}$ below the POR threshold. When VR_ON and $V_{DD}$ return to their high operating levels, a soft-start will occur.

Table 6 summarizes the fault protections.

TABLE 6. FAULT PROTECTION SUMMARY

| FAULT TYPE | FAULT DURATION BEFORE PROTECTION | PROTECTION ACTION | FAULT RESET |
|---|---|---|---|
| Overcurrent | 120µs | PWM4/Phase tri-state, PGOOD latched low | VR_ON toggle or VDD toggle |
| Phase Current Imbalance | 4ms | | |
| Overvoltage: $V_{OUT}$ > VID + 300mV (optionally 3.3V fixed) | Immediate | PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-states the phase switches (Phases 1, 2, 3) and PWM4. | |
| Overvoltage: $V_{OUT}$ > 2.6V = VIDmax + 300mV (optionally 3.3V fixed) during output voltage ramp up from 0V | | | |

## VR_HOT#/ALERT# Behavior

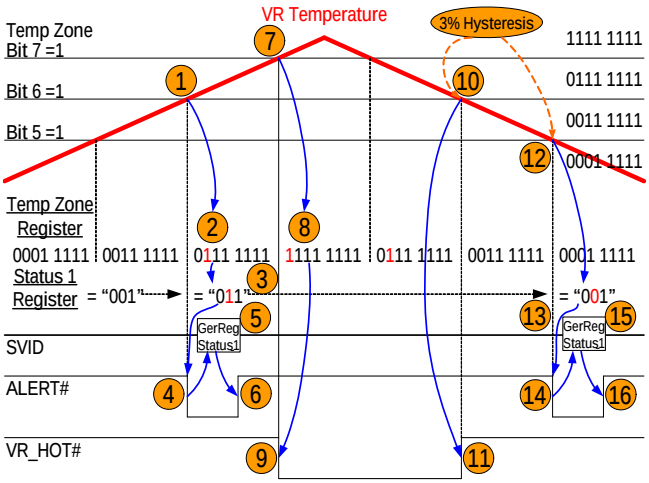



FIGURE 39. VR_HOT#/ALERT# BEHAVIOR

The controller drives 60µA current source out of the NTC pin. The current source flows through the respective NTC resistor networks on the pins and creates voltages that are monitored by the controller through an A/D converter (ADC) to generate the Tzone value. Table 7 shows the programming table for Tzone. The user needs to scale the NTC network resistance, such that it generates the NTC pin voltage that corresponds to the left-most column. Do not use any capacitor to filter the voltage.

TABLE 7. TZONE TABLE

| VNTC (V) | TMAX (%) | TZONE |
|---|---|---|
| 0.84 | >100 | FFh |
| 0.88 | 100 | FFh |
| 0.92 | 97 | 7Fh |
| 0.96 | 94 | 3Fh |
| 1.00 | 91 | 1Fh |

TABLE 7. TZONE TABLE

| VNTC (V) | TMAX (%) | TZONE |
|---|---|---|
| 1.04 | 88 | 0Fh |
| 1.08 | 85 | 07h |
| 1.12 | 82 | 03h |
| 1.16 | 79 | 01h |
| 1.2 | 76 | 01h |
| >1.2 | <76 | 00h |

Figure 39 shows how the NTC network should be designed to get correct VR_HOT#/ALERT# behavior when the system temperature rises and falls, manifested as the NTC pin voltage falls and rises. The series of events are:

1. The temperature rises so the NTC pin voltage drops. Tzone value changes accordingly.
2. The temperature crosses the threshold where Tzone register Bit 6 changes from 0 to 1.
3. The controller changes Status_1 register bit 1 from 0 to 1.
4. The controller asserts ALERT#.
5. The CPU reads Status_1 register value to know that the alert assertion is due to Tzone register Bit 6 flipping.
6. The controller clears ALERT#.
7. The temperature continues rising.
8. The temperature crosses the threshold where Tzone register Bit 7 changes from 0 to 1.
9. The controller asserts VR_HOT# signal. The CPU reduces power consumption, and the system temperature eventually drops.
10. The temperature crosses the threshold where Tzone register Bit 6 changes from 1 to 0. This threshold is 1 ADC step lower than the one when VR_HOT# gets asserted, to provide 3% hysteresis.
11. The controllers de-asserts VR_HOT# signal.
12. The temperature crosses the threshold where Tzone register Bit 5 changes from 1 to 0. This threshold is 1 ADC step lower than the one when ALERT# gets asserted during the temperature rise to provide 3% hysteresis.
13. The controller changes Status_1 register bit 1 from 1 to 0.
14. The controller asserts ALERT#.
15. The CPU reads Status_1 register value to know that the alert assertion is due to Tzone register Bit 5 flipping.
16. The controller clears ALERT#.

To disable the NTC function, connect the NTC pin to VDD using a pullup resistor.

# Serial Interfaces

## Serial VID (SVID) Supported Data and Configuration Registers

The controller supports the following data and configuration registers, accessible via the SVID interface.

The device is compliant with Intel VR12.5/VR12/IMVP7 SVID protocol. To ensure proper CPU operation, refer to this document for SVID bus design and layout guidelines; each platform requires

different pull-up impedance on the SVID bus, while impedance matching and spacing among DATA, CLK, and ALERT# signals must be followed. Common mistakes are insufficient spacing among signals and improper pull-up impedance.

**TABLE 8. SUPPORTED DATA AND CONFIGURATION REGISTERS**

| INDEX | REGISTER NAME | DESCRIPTION | DEFAULT VALUE |
|---|---|---|---|
| 00h | Vendor ID | Uniquely identifies the VR vendor. Assigned by Intel. | 12h |
| 01h | Product ID | Uniquely identifies the VR product. Intersil assigns this number. | 10h |
| 02h | Product Revision | Uniquely identifies the revision of the VR control IC. Intersil assigns this data. | |
| 05h | Protocol ID | Identifies what revision of SVID protocol the controller supports. | 03h |
| 06h | Capability | Identifies the SVID VR capabilities and which of the optional telemetry registers are supported. | 81h |
| 10h | Status_1 | Data register read after ALERT# signal. Indicating if a VR rail has settled, has reached VRHOT condition or has reached ICC max. | 00h |
| 11h | Status_2 | Data register showing status_2 communication. | 00h |
| 12h | Temperature Zone | Data register showing temperature zones that have been entered. | 00h |
| 15h | ICC | Read output current, range 00h to FFh | |
| 1Ch | Status_2_ LastRead | This register contains a copy of the Status_2 data that was last read with the GetReg (Status_2) command. | 00h |
| 21h | $I_{CC(MAX)}$ | Data register containing the ICC max the platform supports, set at start-up by resistors Rprog1 and Rprog2. The platform design engineer programs this value during the design process. Binary format in amps, i.e., 100A = 64h | Refer to Table 2 |
| 22h | Temp max | Not supported | 00h |
| 24h | SR-fast | Slew Rate Normal. The fastest slew rate the platform VR can sustain. Binary format in mV/µs. i.e., 0Ah = 10mV/µs. | 0Ah |
| 25h | SR-slow | Is 4x slower than normal. Binary format in mV/µs. i.e., 02h = 2.5mV/µs | 02h |
| 26h | $V_{BOOT}$ | If programmed by the platform, the VR supports $V_{BOOT}$ voltage during start-up ramp. The VR will ramp to $V_{BOOT}$ and hold at $V_{BOOT}$ until it receives a new SetVID command to move to a different voltage. | 00h |
| 30h | $V_{OUT}$ max | This register is programmed by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR will respond with “not supported” acknowledge. | B5h |
| 31h | VID Setting | Data register containing currently programmed VID voltage. See Table 5 beginning on page 31. | |
| 32h | Power State | Register containing the current programmed power state. | 00h |
| 33h | Voltage Offset | Sets offset in VID steps added to the VID setting for voltage margining, expressed as an 8-bit 2's-complement offset value. For example:<br>...<br>FEh = -2 VID steps<br>FFh = -1 VID step<br>00h = zero offset, no margin<br>01h = +1 VID step<br>02h = +2 VID steps<br>... | 00h |
| 34h | Multi VR Config | Data register that configures multiple VRs behavior on the same SVID bus. | 00h |

The SVID alertB is asserted for the following conditions:

1. When VRsettled is asserted for non-zero volt commandedVID. If the commandedVID is changed, the alertB will de-assert while the DAC is moving to the new target.
2. Therm alert changing from 0 to 1 or from 1 to 0. (Read Status1 required to clear this alert flag.)
3. $I_{CC(MAX)}$ alert changing from 0 to 1 or from 1 to 0. (Read Status1 required to clear this alert flag.)

## Serial PMBus ($I^2C$/SMBus/PMBus) Supported Data and Configuration Registers

The ISL95820 features SMBus, PMBus, and $I^2C$ with fixed write address 80h and fixed read address 81h. (The least significant bit of the 8-bit address is for write (0h) and read (1h).) SMBus/PMBus includes an Alert# line and Packet Error Check (PEC) to ensure data properly transmitted. In addition, the output voltage and offset, droop enable, overvoltage setpoint, and the priority of SVID and SMBus/PMBus/$I^2C$ can be written and read via this bus, as summarized in Table 9. Output current and voltage setting can be read as summarized in Table 10. For proper operation, users should follow the SMBus, PMBus, and $I^2C$ protocol, as shown in Figure 42. Note that STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of register, as shown in Figure 42.

SMBus/PMBus/I$^2$C allows programming the registers of Table 9, 11ms after VCC above POR, and after VR_ON input is high.

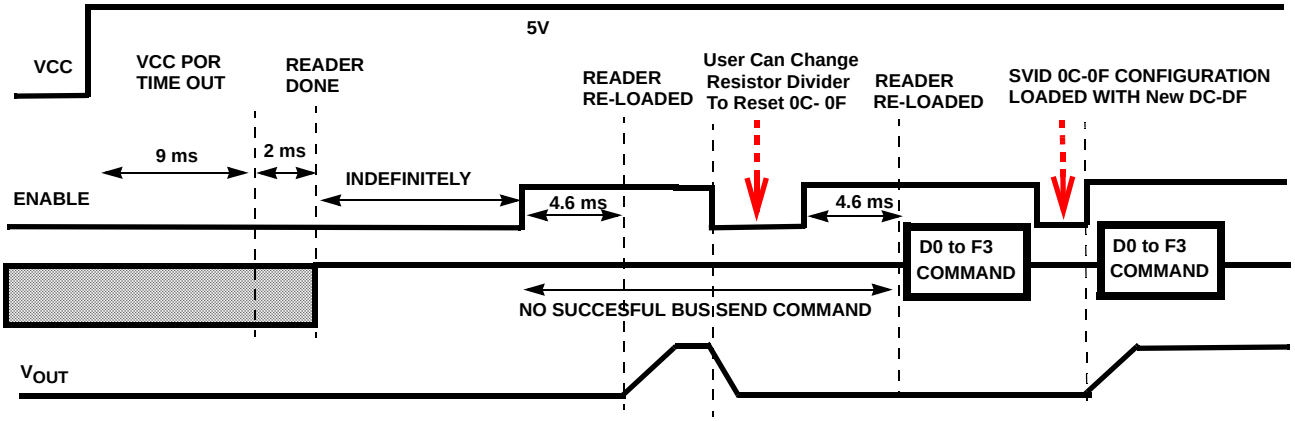



FIGURE 40. SIMPLIFIED SMBus/PMBus/I$^2$C INITIALIZATION TIMING DIAGRAM WHEN NO BUS WRITE COMMAND RECEIVED

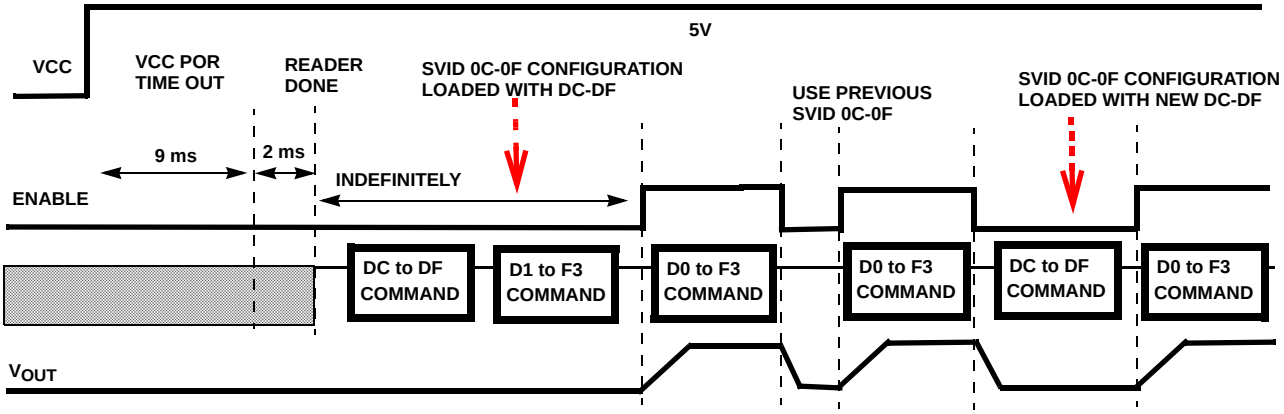



FIGURE 41. SIMPLIFIED SMBus/PMBus/I$^2$C INITIALIZATION TIMING DIAGRAM WHEN BUS WRITE COMMAND SUCESSFULLY RECEIVED


Example command: DAh SET_VID (one word, High Data Byte and ACK are not used)

S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition

Acknowledge or DATA from Slave, ISL95820 Controller

FIGURE 42. SMBus/PMBus/I$^2$C PROTOCOL

TABLE 9. SMBus, PMBus, AND $I^2C$ WRITE AND READ REGISTERS

| COMMAND CODE | ACCESS | DEFAULT | COMMAND NAME | DESCRIPTION |
|---|---|---|---|---|
| D4h[0] | R/W | | DROOP_EN | 0h=Droop Disabled; 1h = Droop Enabled; default determined by PROG2 pin resistance to ground. See Table 3. When the controller is reset by the VR_ON pin transitioning from low to high, the PROG2 resistance is measured and this register is stored accordingly. |
| D6h[1:0] | R/W | 00h | LOCK_SVID | set SVID and SMBus/PMBus/$I^2C$ Priority (See Table 11 for details) |
| D8h[0] | R/W | 00h | SET_0V | 0h = VID+300mV, 1h = 3.3V fixed. |
| DAh[7:0] | R/W | | SET_VID | SVID Bus VID Code. See Table 5 beginning on page 31. Default to $V_{BOOT}$ value on start-up, determined by PROG2 pin resistance to ground. |
| DBh[7:0] | R/W | 00h | SET_OFFSET | SVID Bus VID offset code, expressed as an 8-bit 2's-complement offset value. For example:<br>...<br>FEh = -2 VID steps<br>FFh = -1 VID step<br>00h = zero offset, no margin<br>01h = +1 VID step<br>02h = +2 VID steps<br>... |

TABLE 10. SMBus, PMBus, AND $I^2C$ TELEMETRIES

| CODE | WORD LENGTH (BYTE) | COMMAND NAME | DESCRIPTION | TYPICAL RESOLUTION |
|---|---|---|---|---|
| 8Bh | TWO | READ_VOUT | Output Voltage (VID+OFFSET, see Table 5 | 8-BIT, 10mV |
| 8Ch | TWO | READ_IOUT | Output Current (FF = $I_{CC(MAX)}$ | 8-BIT, $I_{CC(MAX)}/255$ |

TABLE 11. LOCK_SVID

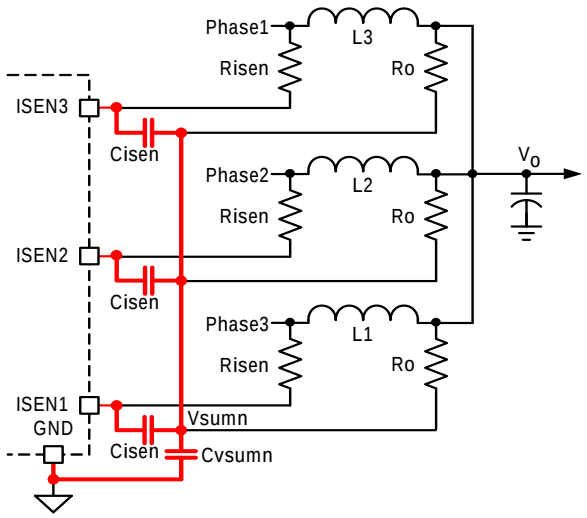
| D6h | SVID | | | SMBus, PMBus or $I^2C$ | | FINAL DAC | TARGETED APPLICATIONS |
|---|---|---|---|---|---|---|---|
| | SETVID | SETPS (1/2/3) AND SETDECAY | SET OFFSET | SETVID | SET OFFSET | | |
| 00h | Yes | Yes | Yes | Not | Not | SV_VID + SV_OFFSET | Not Overclocking |
| 01h | Yes | Yes | Yes | Not | Yes | SV_VID + PM_OFFSET | Not Overclocking |
| 02h | Yes | ACK ONLY | ACK ONLY | Not | Yes | SV_VID + PM_OFFSET | Overclocking |
| 03h | ACK ONLY | ACK ONLY | ACK ONLY | Yes | Yes | PM_VID + PM_OFFSET | Overclocking |

NOTE:

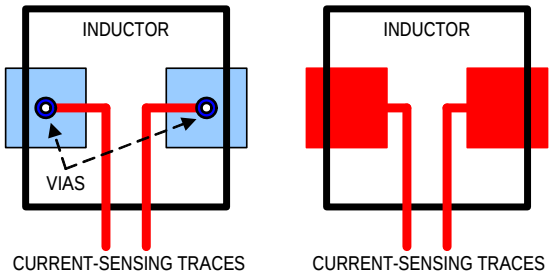
8. The ISL95820 controller is designed such that all SVID commands are acknowledged as if the SMBus, PMBus or $I^2C$ does not exist. To avoid conflict between SMBus/PMBus/$I^2C$ and SVID bus during operation, execute this command prior to writing the VID setting or offset commands. With 01h option, SMBus/PMBus/$I^2C$'s OFFSET should only adjust slightly higher or lower (say ±20mV) than SVID OFFSET for margining purpose or PCB loss compensation so that CPU will not draw significantly more power in PSI1/2/3/Decay mode. To program full range of PM_OFFSET for overclocking applications, select 02h or 03h options. 03h option gives full control of the output voltage (VID+OFFSET) via SMBus/PMBus/$I^2C$, commonly used in overclocking applications. Prior to a successful written PMBus VID or OFFSET, the controller will continue executing SVID VID or OFFSET command.

# Layout Guidelines

| ISL95820 PIN NUMBER | SYMBOL | LAYOUT GUIDELINES |
|---|---|---|
| BOTTOM PAD | GND | Connect this ground pad to the ground plane through low impedance path. Recommend use of at least 5 vias to connect to ground planes in PCB internal layers. This is also the primary conduction path for heat removal. |
| 1 | VR_ON | No special consideration. |
| 2 | PGOOD | No special consideration. |
| 3 | IMON | No special consideration. |
| 4 | VR_HOT# | No special consideration. |
| 5 | NTC | The NTC thermistor needs to be placed close to the thermal source that is monitored to determine CPU $V_{core}$ thermal throttling. Recommend placing it at the hottest spot of the CPU $V_{core}$ VR. |
| 6 | COMP | Place the compensator components in general proximity of the controller. |
| 7 | FB | |
| 8 | FB2 | |
| 9 | FB3 | |
| 10 | ISEN4 | Each ISEN pin has a capacitor (Cisen) decoupling it to VSUMN, then through another capacitor (Cvsumn) to GND. Place Cisen capacitors as close as possible to the controller and keep the following loops small:<br>1. Any ISEN pin to another ISEN pin<br>2. Any ISEN pin to GND<br>The red traces in the following drawing show the loops that need to minimized. |
| 11 | ISEN3 | |
| 12 | ISEN2 | |
| 13 | ISEN1 | |
| 14 | RTN | Place the RTN filter in close proximity of the controller for good decoupling. |



## Layout Guidelines (Continued)

| ISL95820 PIN NUMBER | SYMBOL | LAYOUT GUIDELINES |
|---|---|---|
| 15 | ISUMN | Place the current sensing circuit in general proximity of the controller.<br>Place capacitor $C_n$ very close to the controller.<br>Place the inductor temperature sensing NTC thermistor next to phase-1 inductor (L1) so it senses the inductor temperature correctly.<br>Each phase of the power stage sends a pair of VSUMP and VSUMN signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil).<br>IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. Route the ISUMPn and ISENn resistor traces to the phase-side pad of each inductor. The ISUMNn network Ro resistor traces should be routed to the VOUT-side pad of each inductor. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces.<br>  <br> |
| 16 | ISUMP | |
| 17 | VDD | A capacitor decouples it to GND. Place it in close proximity of the controller. |
| 18 | BOOT1 | Place the Phase1 bootstrap capacitor between BOOT1 and PHASE1, near the controller. |
| 19 | PHASE1 | No special consideration. |
| 20 | UGATE1 | No special consideration. |
| 21 | LGATE1 | No special consideration. |
| 22 | BOOT2 | Place the Phase2 bootstrap capacitor between BOOT2 and PHASE2, near the controller. |
| 23 | PHASE2 | No special consideration. |
| 24 | UGATE2 | No special consideration. |
| 25 | VCCP | A capacitor decouples it to GND. Place it in close proximity of the controller. |
| 26 | LGATE2 | No special consideration. |
| 27 | LGATE3 | No special consideration. |
| 28 | PHASE3 | No special consideration. |
| 29 | UGATE3 | No special consideration. |
| 30 | BOOT3 | Place the Phase3 bootstrap capacitor between BOOT3 and PHASE3, near the controller. |
| 31 | PWM4 | No special consideration. |
| 32 | VIN | A capacitor decouples it to GND. Place it in close proximity of the controller. |
| 33 | PROG3 | No special consideration. |
| 34 | PROG2 | No special consideration. |
| 35 | PROG1 | No special consideration. |
| 36, 37, 38, 39, 40 | I2DATA, I2CLK, SDA, ALERT#, SCLK | Follow Intel recommendation. |

## Typical Performance

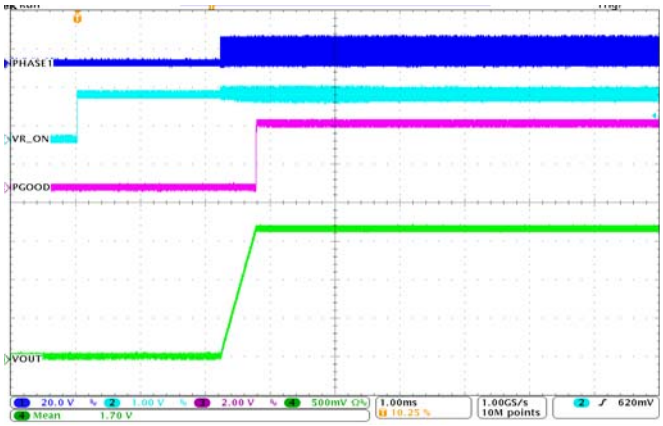



FIGURE 43. SOFT-START, $V_{IN}$ = 12V, $I_O$ = 5A, VID = 1.7V, Ch1: PHASE1, Ch2: VR_ON, Ch3: PGOOD, Ch4: $V_{OUT}$

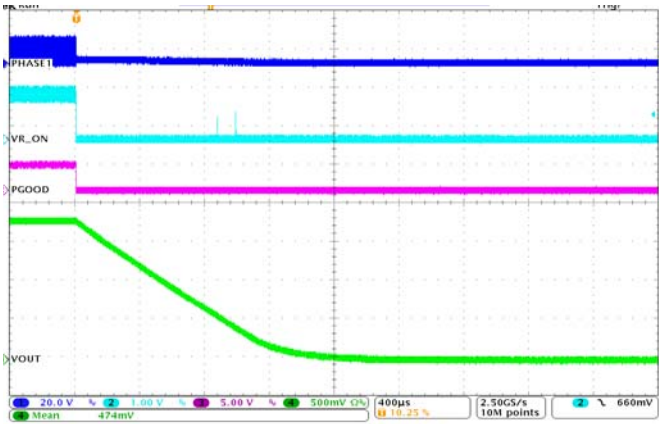



FIGURE 44. SHUT DOWN, $V_{IN}$ = 12V, $I_O$ = 5A, VID = 1.7V, Ch1: PHASE1, Ch2: VR_ON, Ch3: PGOOD, Ch4: $V_{OUT}$

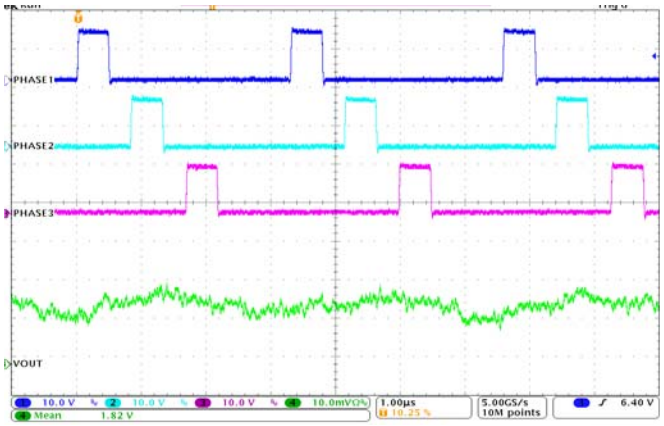



FIGURE 45. STEADY STATE, PS0, $V_{IN}$ = 12V, $I_O$ = 5A, VID = 1.8V Ch1: PHASE1, Ch2: PHASE2, Ch3: PHASE3, Ch4: $V_{OUT}$, PHASE4 NOT SHOWN

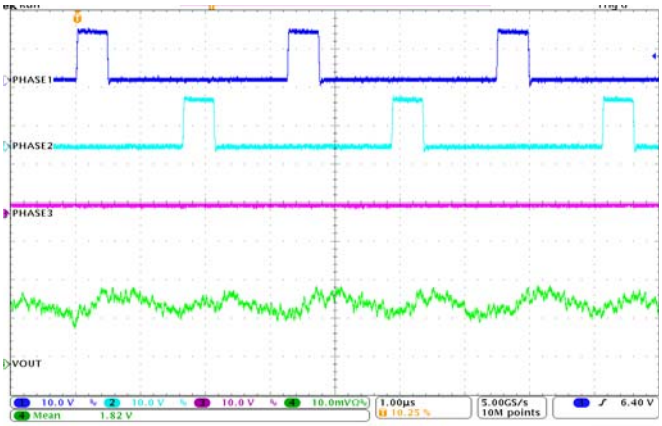



FIGURE 46. STEADY STATE, PS1, $V_{IN}$ = 12V, $I_O$ = 5A, VID = 1.8V Ch1: PHASE1, Ch2: PHASE2, Ch3: PHASE3, Ch4: $V_{OUT}$, PHASE4 NOT SHOWN

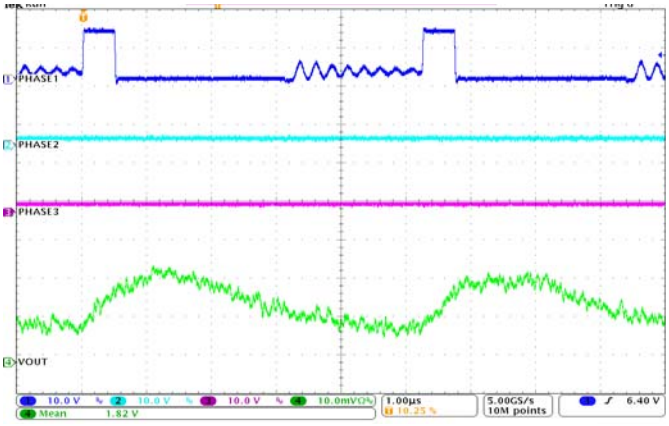



FIGURE 47. STEADY STATE, PS2, $V_{IN}$ = 12V, $I_O$ = 5A, VID = 1.8V Ch1: PHASE1, Ch2: PHASE2, Ch3: PHASE3, Ch4: $V_{OUT}$, PHASE4 NOT SHOWN

## Typical Performance (Continued)

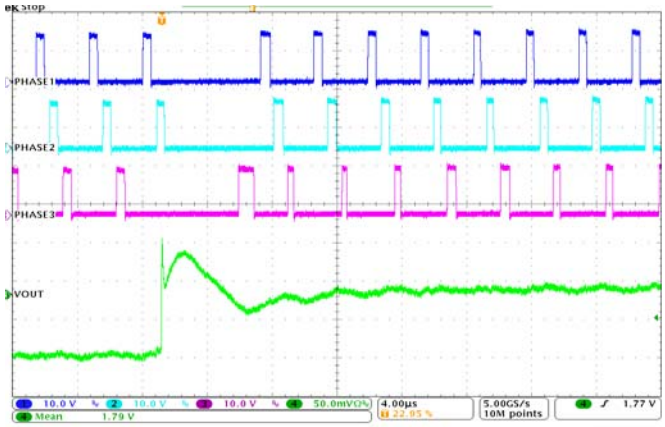



FIGURE 48. VR1 LOAD RELEASE RESPONSE, $V_{IN}$ = 12V, VID = 1.8V, $I_O$ = 61A/1A, SLEW TIME = 50ns, LL = 1.5mΩ, Ch1: PHASE1, Ch2: PHASE2, Ch3: PHASE3, Ch4: $V_{OUT}$, PHASE4 NOT SHOWN

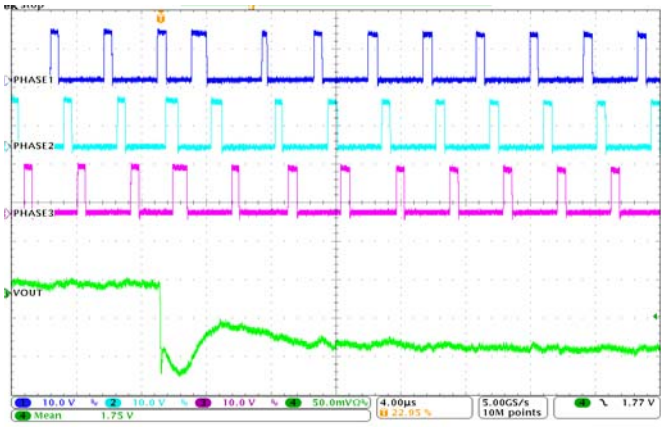



FIGURE 49. VR1 LOAD INSERTION RESPONSE, $V_{IN}$ = 12V, VID = 1.8V, $I_O$ = 1A/61A, SLEW TIME = 50ns, LL = 1.5mΩ, Ch1: PHASE1, Ch2: PHASE2, Ch3: PHASE3, Ch4: $V_{OUT}$, PHASE4 NOT SHOWN

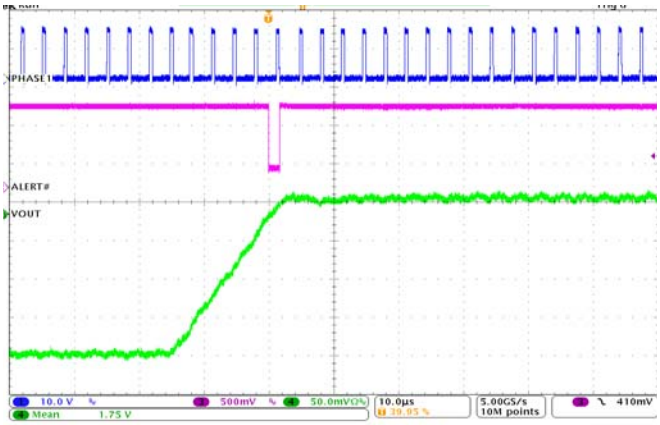



FIGURE 50. SETVID-FAST RESPONSE, $I_O$ = 5A, VID = 1.6V - 1.8V, Ch1: PHASE1, Ch3: ALERT#, Ch4: $V_{OUT}$

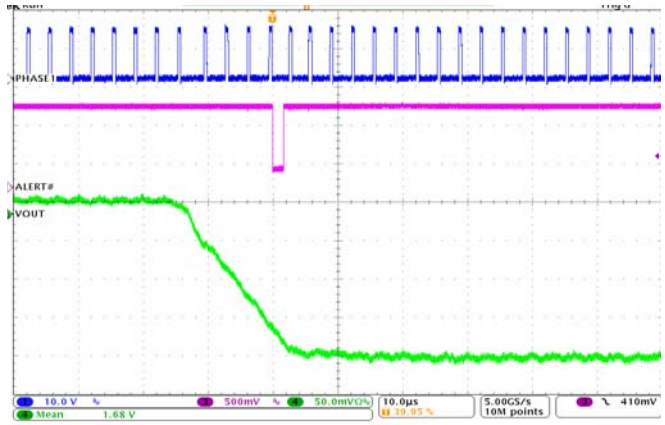



FIGURE 51. SETVID-FAST RESPONSE, $I_O$ = 5A, VID = 1.8V - 1.6V, Ch1: PHASE1, Ch3: ALERT#, Ch4: $V_{OUT}$

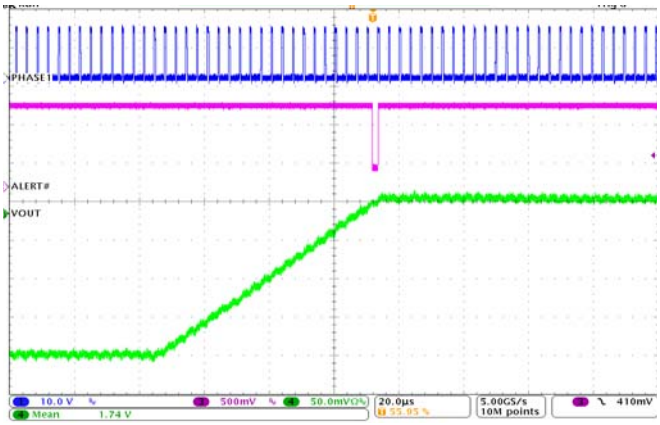



FIGURE 52. SETVID-SLOW RESPONSE, $I_O$ = 5A, VID = 1.6V - 1.8V, Ch1: PHASE1, Ch3: ALERT#, Ch4: $V_{OUT}$

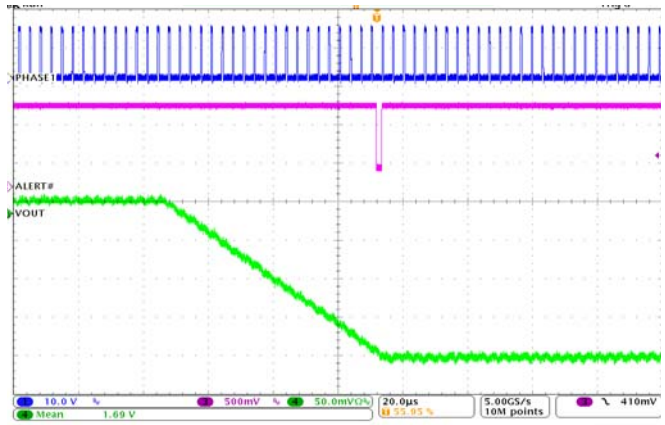



FIGURE 53. SETVID-SLOW RESPONSE, $I_O$ = 5A, VID = 1.8V - 1.6V, Ch1: PHASE1, Ch3: ALERT#, Ch4: $V_{OUT}$

## Typical Performance (Continued)

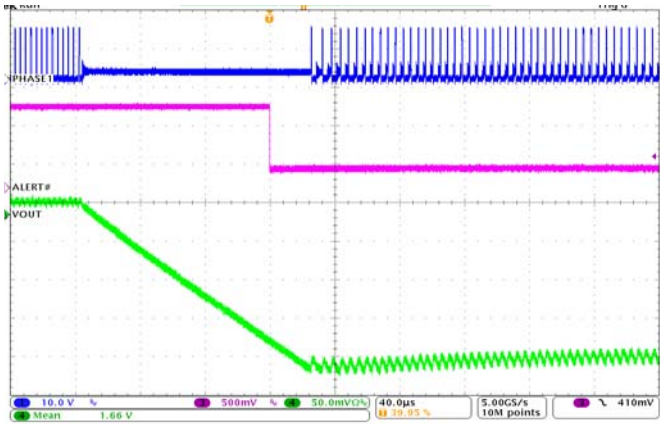



FIGURE 54. SETVID DECAY RESPONSE, $I_O$ = 5A, VID = 1.8V - 1.6V, Ch1: PHASE1, Ch3: ALERT#, Ch4: $V_{OUT}$

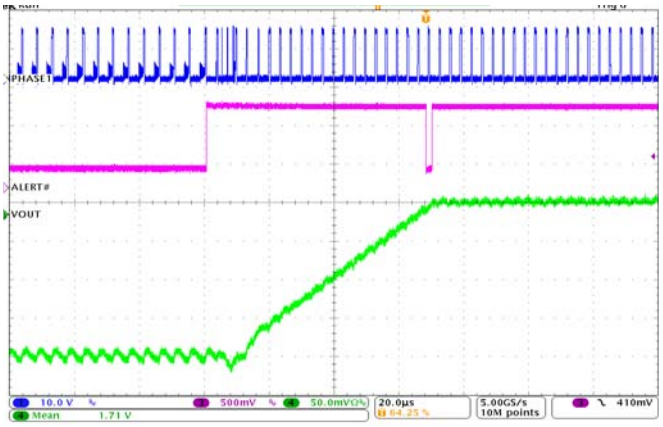



FIGURE 55. SETVID SLOW RESPONSE FOLLOWING SETVID DECAY, $I_O$ = 5A, VID = 1.6V - 1.8V, Ch1: PHASE1, Ch3: ALERT#, Ch4: $V_{OUT}$

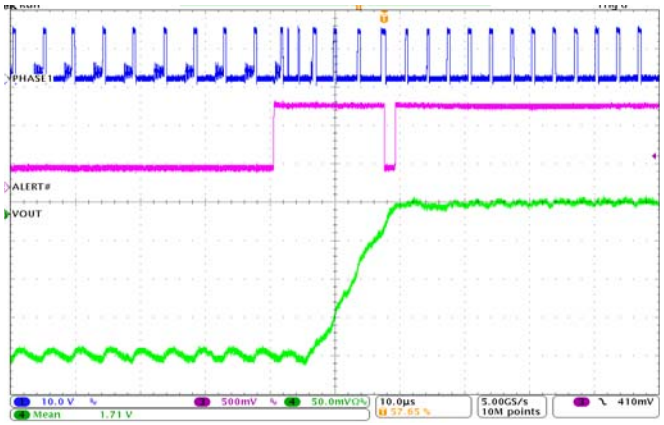



FIGURE 56. SETVID FAST RESPONSE FOLLOWING SETVID DECAY, $I_O$ = 5A, VID = 1.6V - 1.8V, Ch1: PHASE1, Ch3: ALERT#, Ch4: $V_{OUT}$

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web for the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| February 4, 2013 | FN8318.0 | Initial Release. |

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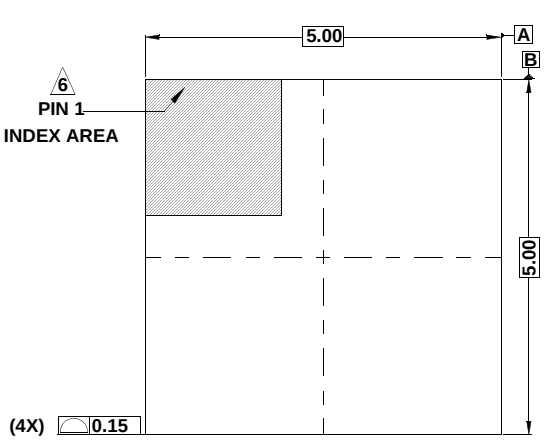
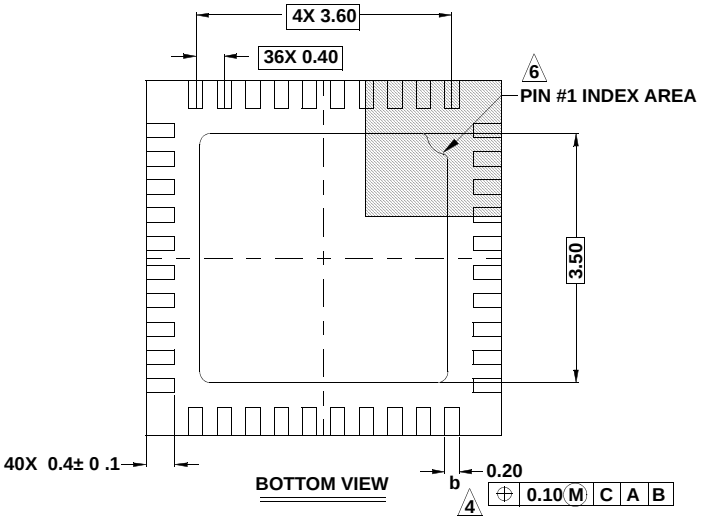
# Package Outline Drawing

## L40.5x5

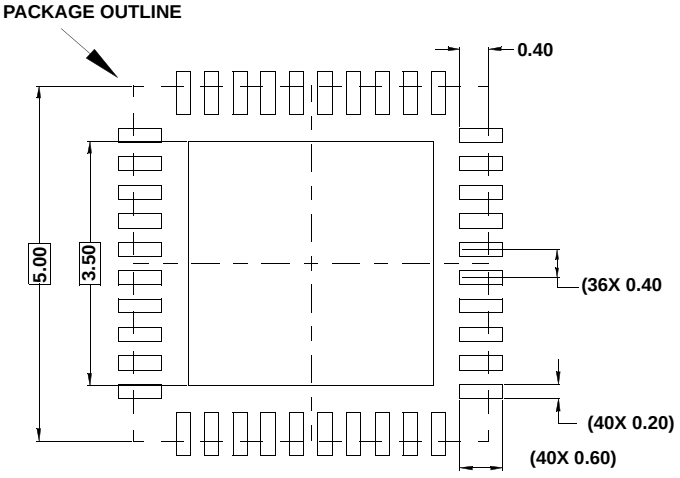
**40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 1, 9/10**



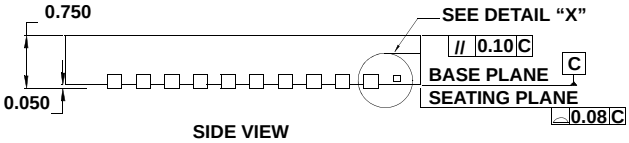

TOP VIEW



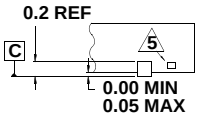

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1

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