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CY7C1441KV33
CY7C1443KV33
CY7C1441KVE33

36-Mbit (1M × 36/2M × 18) Flow-Through SRAM (With ECC)

Features

- Supports 133-MHz bus operations
- 1M × 36/2M × 18 common I/O
- 3.3 V core power supply
- 2.5 V or 3.3 V I/O power supply
- Fast clock-to-output times
 - 6.5 ns (133 MHz version)
- Provide high-performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- CY7C1441KV33, CY7C1443KV33, and CY7C1441KVE33 are available in JEDEC-standard 100-pin TQFP and 165-ball FBGA Pb-free packages.
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- “ZZ” Sleep Mode option
- On-chip error correction code (ECC) to reduce soft error rate (SER)

Functional Description

The CY7C1441KV33/CY7C1443KV33/CY7C1441KVE33 are 3.3 V, 1M × 36/2M × 18/1M × 36 synchronous flow-through SRAMs, respectively designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock (CLK) input. The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable (\overline{CE}_1), depth-expansion Chip Enables (\overline{CE}_2 and \overline{CE}_3), Burst Control inputs (\overline{ADSC} , \overline{ADSP} , and \overline{ADV}), Write Enables (\overline{BW}_x , and \overline{BWE}), and Global Write (\overline{GW}). Asynchronous inputs include the Output Enable (\overline{OE}) and the ZZ pin.

The CY7C1441KV33/CY7C1443KV33/CY7C1441KVE33 allow either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe (\overline{ADSP}) or the cache Controller Address Strobe (\overline{ADSC}) inputs. Address advancement is controlled by the Address Advancement (\overline{ADV}) input.

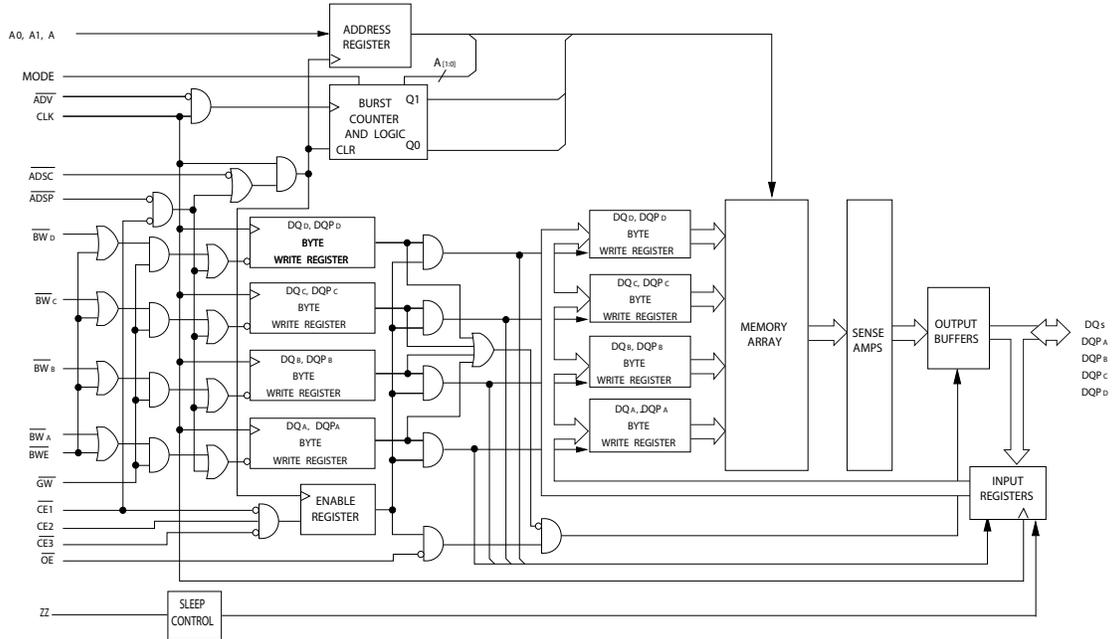
Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor (\overline{ADSP}) or Address Strobe Controller (\overline{ADSC}) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (\overline{ADV}).

The CY7C1441KV33/CY7C1443KV33/CY7C1441KVE33 operate from a +3.3 V core power supply while all outputs may operate with either a +2.5 V or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

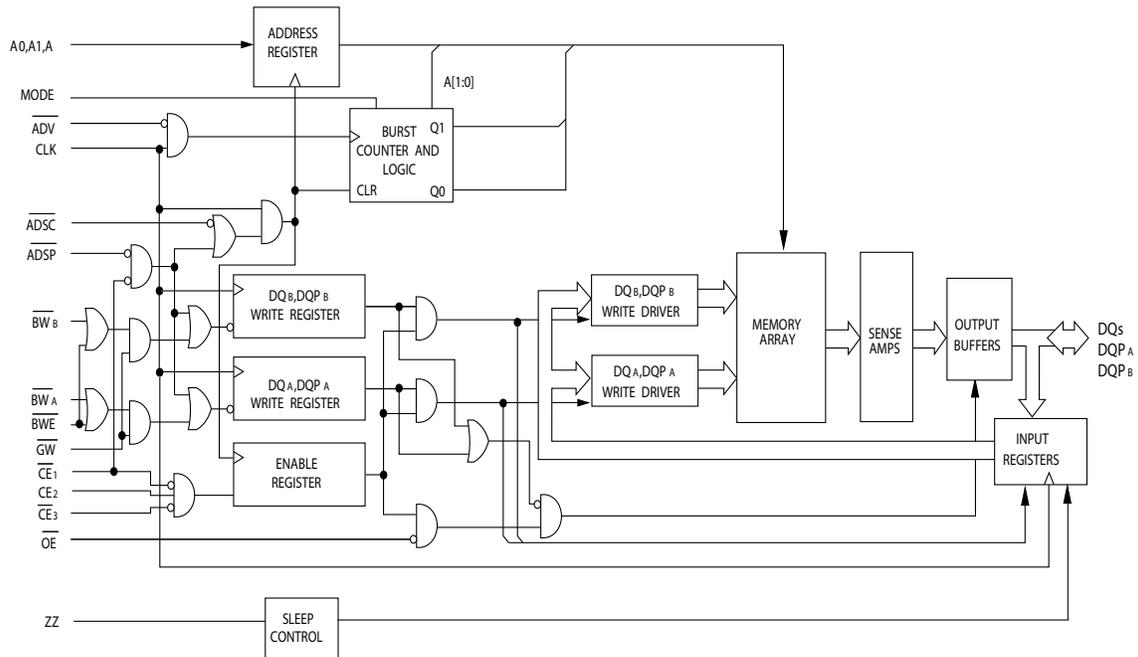
Selection Guide

Description	133 MHz	Unit
Maximum access time	6.5	ns
Maximum operating current	× 18	150
	× 36	170

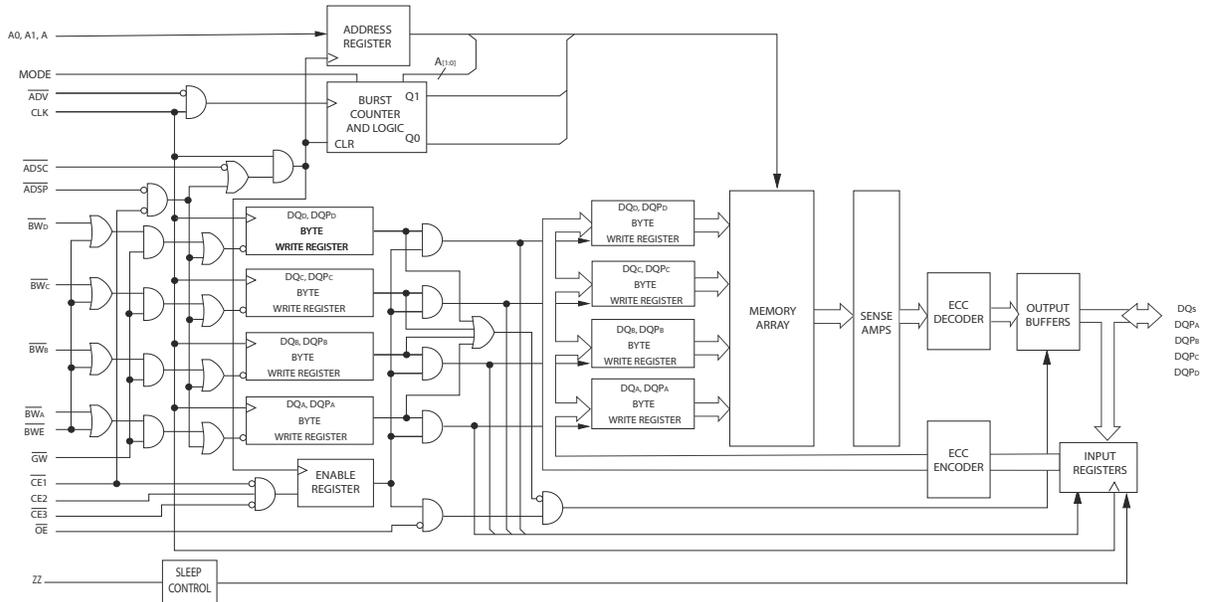
Logic Block Diagram – CY7C1441KV33



Logic Block Diagram – CY7C1443KV33



Logic Block Diagram – CY7C1441KVE33

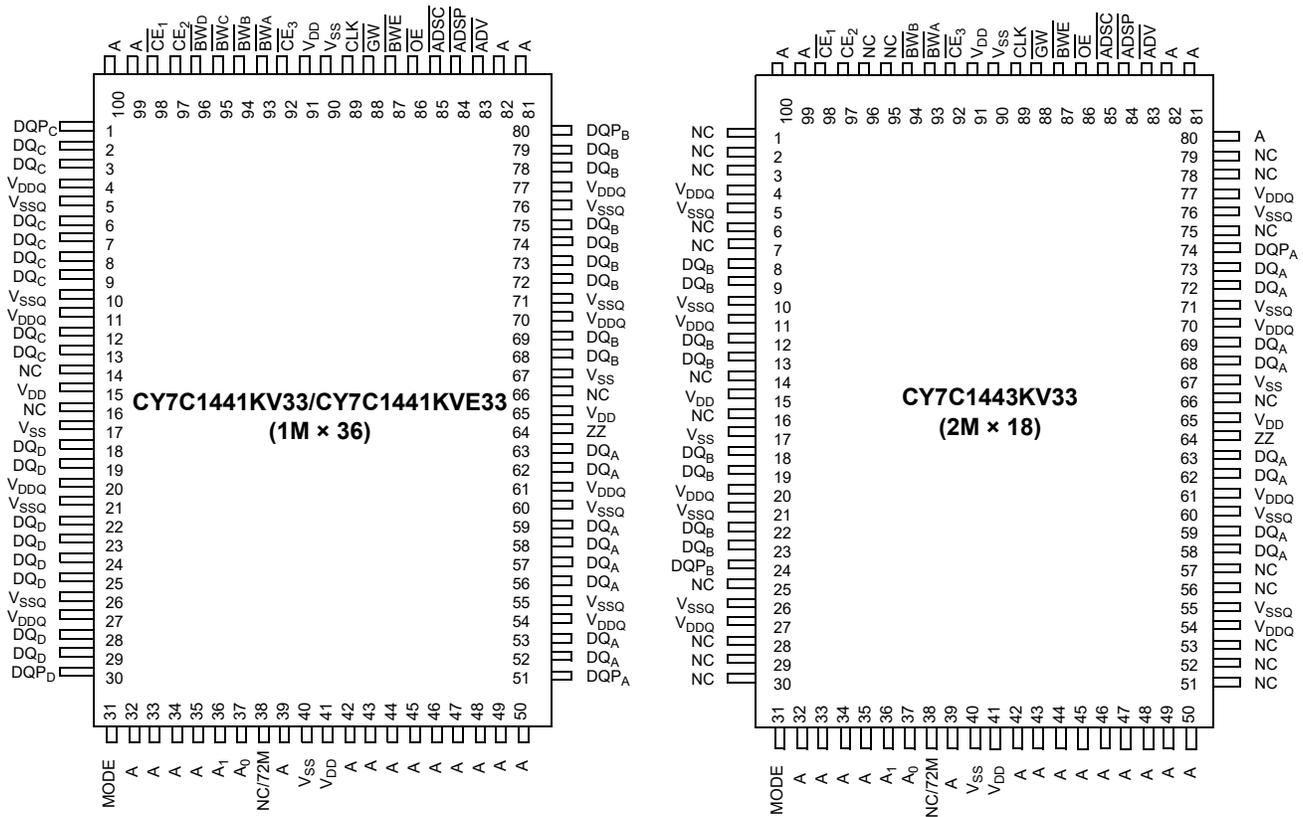


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Pin Configurations

Figure 1. 100-pin TQFP Pinout



Pin Configurations (continued)

Figure 2. 165-ball FBGA Pinout
CY7C1441KV33 (1M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	\overline{CE}_1	\overline{BW}_C	\overline{BW}_B	\overline{CE}_3	\overline{BWE}	\overline{ADSC}	\overline{ADV}	A	NC
B	NC/144M	A	CE_2	\overline{BW}_D	\overline{BW}_A	CLK	\overline{GW}	\overline{OE}	\overline{ADSP}	A	NC/576M
C	DQP _C	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC/1G	DQP _B
D	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
E	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
F	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
G	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
H	NC	NC	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	NC	ZZ
J	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
K	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
L	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
M	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
N	DQP _D	NC	V _{DDQ}	V _{SS}	NC	A	NC	V _{SS}	V _{DDQ}	NC	DQP _A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	Address Inputs Used to Select One of the Address Locations. Sampled at the rising edge of the CLK if \overline{ADSP} or \overline{ADSC} is active LOW, and $\overline{CE}_1, \overline{CE}_2,$ and \overline{CE}_3 are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A, \overline{BW}_B, \overline{BW}_C, \overline{BW}_D$	Input-Synchronous	Byte Write Select Inputs, Active LOW. Qualified with \overline{BWE} to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
\overline{GW}	Input-Synchronous	Global Write Enable Input, Active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on \overline{BW}_X and \overline{BWE}).
CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
\overline{CE}_1	Input-Synchronous	Chip Enable 1 Input, Active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 and \overline{CE}_3 to select/deselect the device. ADSP is ignored if \overline{CE}_1 is HIGH. \overline{CE}_1 is sampled only when a new external address is loaded.
\overline{CE}_2	Input-Synchronous	Chip Enable 2 Input, Active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select/deselect the device. \overline{CE}_2 is sampled only when a new external address is loaded.
\overline{CE}_3	Input-Synchronous	Chip Enable 3 Input, Active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select/deselect the device. \overline{CE}_3 is assumed active throughout this document for BGA. \overline{CE}_3 is sampled only when a new external address is loaded.
\overline{OE}	Input-Asynchronous	Output Enable, Asynchronous Input, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. \overline{OE} is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	Advance Input Signal, Sampled on the Rising Edge of CLK. When asserted, it automatically increments the address in a burst cycle.
\overline{ADSP}	Input-Synchronous	Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When \overline{ADSP} and \overline{ADSC} are both asserted, only \overline{ADSP} is recognized. \overline{ADSP} is ignored when \overline{CE}_1 is deasserted HIGH.
\overline{ADSC}	Input-Synchronous	Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When \overline{ADSP} and \overline{ADSC} are both asserted, only \overline{ADSP} is recognized.
\overline{BWE}	Input-Synchronous	Byte Write Enable Input, Active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-Asynchronous	ZZ “sleep” Input, Active HIGH. When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the read cycle. The direction of the pins is controlled by \overline{OE} . When \overline{OE} is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of \overline{OE} .

Pin Definitions (continued)

Name	I/O	Description
DQP _x	I/O-Synchronous	Bidirectional Data Parity I/O Lines. Functionally, these signals are identical to DQ _s . During write sequences, DQP _x is controlled by BW _[A:H] correspondingly.
MODE	Input-Static	Selects Burst Order. When tied to GND selects linear burst sequence. When tied to V _{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull up.
V _{DD}	Power Supply	Power Supply Inputs to the Core of the Device.
V _{DDQ}	I/O Power Supply	Power Supply for the I/O Circuitry.
V _{SS}	Ground	Ground for the Core of the Device.
V _{SSQ}	I/O Ground	Ground for the I/O Circuitry.
TDO	JTAG serial output Synchronous	Serial Data-Out to the JTAG Circuit. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	Serial Data-In to the JTAG Circuit. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be left floating or connected to V _{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	Serial Data-In to the JTAG Circuit. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V _{DD} . This pin is not available on TQFP packages.
TCK	JTAG-Clock	Clock Input to the JTAG Circuitry. If the JTAG feature is not being utilized, this pin must be connected to V _{SS} . This pin is not available on TQFP packages.
NC	–	No Connects. Not internally connected to the die. 72M, 144M and 288M are address expansion pins are not internally connected to the die.
NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	No Connects. Not internally connected to the die. NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

The CY7C1441KV33/CY7C1443KV33/CY7C1441KVE33 support secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium processors. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (\overline{ADSP}) or the Controller Address Strobe (\overline{ADSC}). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (\overline{BWE}) and Byte Write Select (\overline{BW}_x) inputs. A Global Write Enable (\overline{GW}) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) and an asynchronous Output Enable (\overline{OE}) provide for easy bank selection and output tristate control. \overline{ADSP} is ignored if \overline{CE}_1 is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are all asserted active, and (2) \overline{ADSP} or \overline{ADSC} is asserted LOW (if the access is initiated by \overline{ADSC} , the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the \overline{OE} input is asserted LOW, the requested data is available at the data outputs a maximum to t_{CDV} after clock rise. \overline{ADSP} is ignored if \overline{CE}_1 is HIGH.

Single Write Accesses Initiated by \overline{ADSP}

This access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3 are all asserted active, and (2) \overline{ADSP} is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (\overline{GW} , \overline{BWE} , and \overline{BW}_x) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous \overline{OE} input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data

lines are tristated once a write cycle is detected, regardless of the state of \overline{OE} .

Single Write Accesses Initiated by \overline{ADSC}

This write access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are all asserted active, (2) \overline{ADSC} is asserted LOW, (3) \overline{ADSP} is deasserted HIGH, and (4) the write input signals (\overline{GW} , \overline{BWE} , and \overline{BW}_X) indicate a write access. \overline{ADSC} is ignored if \overline{ADSP} is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ_S is written into the specified address location. Byte writes are allowed. All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous \overline{OE} input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQ_S . As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of \overline{OE} .

Burst Sequences

The CY7C1441KV33/CY7C1443KV33/CY7C1441KVE33 provide an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. \overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3 , \overline{ADSP} , and \overline{ADSC} must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	75	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

On-Chip ECC

CY7C1441KVE33 SRAMs include an on-chip ECC algorithm that detects and corrects all single-bit memory errors, including Soft Error Upset (SEU) events induced by cosmic rays, alpha particles etc. The resulting Soft Error Rate (SER) of these devices is anticipated to be <0.01 FITs/Mb a 4-order-of-magnitude improvement over comparable SRAMs with no On-Chip ECC, which typically have an SER of 200 FITs/Mb or more. To protect the internal data, ECC parity bits (invisible to the user) are used.

The ECC algorithm does not correct multi-bit errors. However, Cypress SRAMs are designed in such a way that a single SER event has a very low probability of causing a multi-bit error across any data word. The extreme rarity of multi-bit errors results in a SER of <0.01 FITs/Mb.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Truth Table

The truth table for CY7C1441KV33/CY7C1443KV33/CY7C1441KVE33 is as follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	\overline{CE}_1	CE_2	\overline{CE}_3	ZZ	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WRITE}	\overline{OE}	CLK	DQ
Deselected Cycle, Power down	None	H	X	X	L	X	L	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	L	L	X	L	L	X	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	L	X	H	L	L	X	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	L	L	X	L	H	L	X	X	X	L-H	Tristate
Deselected Cycle, Power down	None	X	X	H	L	H	L	X	X	X	L-H	Tristate
Sleep Mode, Power down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tristate
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tristate
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tristate
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tristate
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes

1. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
2. \overline{WRITE} = L when any one or more Byte Write enable signals and \overline{BWE} = L or \overline{GW} = L. \overline{WRITE} = H when all Byte write enable signals, \overline{BWE} , \overline{GW} = H.
3. The DQ pins are controlled by the current cycle and the \overline{OE} signal. \overline{OE} is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when \overline{ADSP} is asserted, regardless of the state of \overline{GW} , \overline{BWE} , or \overline{BW}_x . Writes may occur only on subsequent clocks after the \overline{ADSP} or with the assertion of \overline{ADSC} . As a result, \overline{OE} must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate. \overline{OE} is a don't care for the remainder of the write cycle.
5. \overline{OE} is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when \overline{OE} is inactive or when the device is deselected, and all data bits behave as output when \overline{OE} is active (LOW).

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1441KV33/CY7C1441KVE33 is as follows. [6, 7, 8]

Function (CY7C1441KV33/CY7C1441KVE33)	\overline{GW}	\overline{BWE}	\overline{BW}_D	\overline{BW}_C	\overline{BW}_B	\overline{BW}_A
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A (DQ _A , DQP _A)	H	L	H	H	H	L
Write Byte B (DQ _B , DQP _B)	H	L	H	H	L	H
Write Bytes A, B (DQ _A , DQ _B , DQP _A , DQP _B)	H	L	H	H	L	L
Write Byte C (DQ _C , DQP _C)	H	L	H	L	H	H
Write Bytes C, A (DQ _C , DQ _A , DQP _C , DQP _A)	H	L	H	L	H	L
Write Bytes C, B (DQ _C , DQ _B , DQP _C , DQP _B)	H	L	H	L	L	H
Write Bytes C, B, A (DQ _C , DQ _B , DQ _A , DQP _C , DQP _B , DQP _A)	H	L	H	L	L	L
Write Byte D (DQ _D , DQP _D)	H	L	L	H	H	H
Write Bytes D, A (DQ _D , DQ _A , DQP _D , DQP _A)	H	L	L	H	H	L
Write Bytes D, B (DQ _D , DQ _B , DQP _D , DQP _B)	H	L	L	H	L	H
Write Bytes D, B, A (DQ _D , DQ _B , DQ _A , DQP _D , DQP _B , DQP _A)	H	L	L	H	L	L
Write Bytes D, B (DQ _D , DQ _B , DQP _D , DQP _B)	H	L	L	L	H	H
Write Bytes D, B, A (DQ _D , DQ _C , DQ _A , DQP _D , DQP _C , DQP _A)	H	L	L	L	H	L
Write Bytes D, C, A (DQ _D , DQ _B , DQ _A , DQP _D , DQP _B , DQP _A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1443KV33 is as follows. [6, 7, 8]

Function (CY7C1443KV33)	\overline{GW}	\overline{BWE}	\overline{BW}_B	\overline{BW}_A
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ _A and DQP _A)	H	L	H	L
Write Byte B – (DQ _B and DQP _B)	H	L	L	H
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

Notes

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- Table only lists a partial listing of the byte write combinations. Any Combination of \overline{BW}_X is valid. Appropriate write is done based on which byte write is active.
- \overline{BW}_X represents any byte write signal $\overline{BW}_{[A..H]}$. To enable any byte write \overline{BW}_X , a Logic LOW signal should be applied at clock rise. Any number of byte writes can be enabled at the same time for any given write.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1441KV33 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1441KV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO should be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register (see [TAP Controller Block Diagram on page 14](#)).

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see [TAP Controller State Diagram on page 14](#)).

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and scan data into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the [TAP Controller Block Diagram on page 14](#). Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This shifts data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The [Boundary Scan Order on page 18](#) show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the [Identification Register Definitions on page 17](#).

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO balls and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is given during the "Update IR" state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock

during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the clock captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the shift-DR controller state.

EXTEST OUTPUT BUS TRISTATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

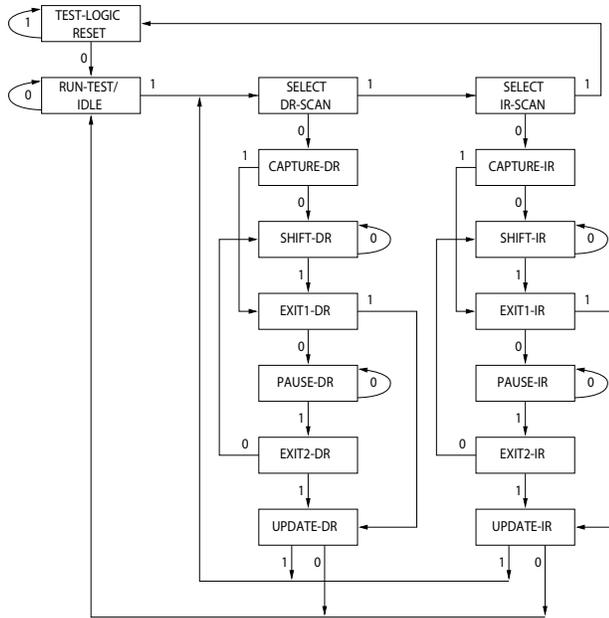
The boundary scan register has a special bit located at bit #89 (for 165-FBGA package). When this scan cell, called the "extest output bus tristate", is latched into the preload register during the "Update-DR" state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the "Shift-DR" state. During "Update-DR", the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the "Test-Logic-Reset" state.

Reserved

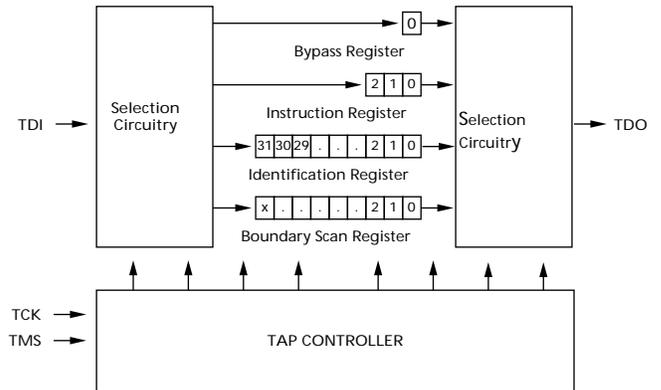
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

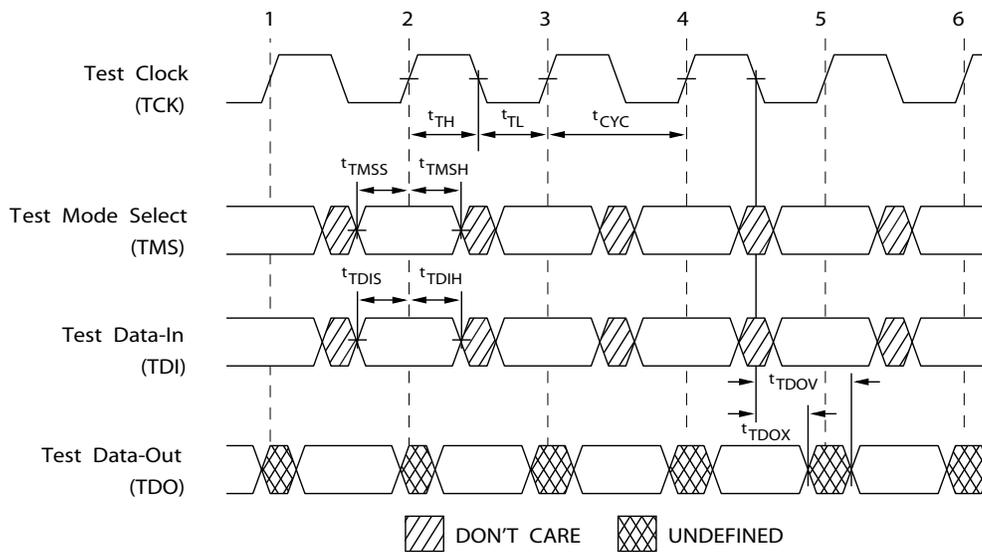


The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing



TAP AC Switching Characteristics

Over the Operating Range

Parameter [9, 10]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH time	20	–	ns
t_{TL}	TCK Clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns

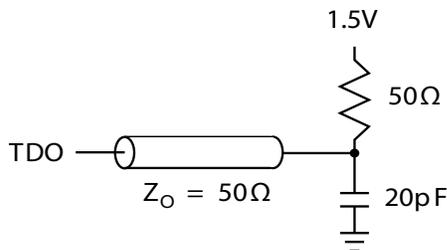
3.3 V TAP AC Test Conditions

Input pulse levels V_{SS} to 3.3 V
 Input rise and fall times (Slew Rate) 2 V/ns
 Input timing reference levels 1.5 V
 Output reference levels 1.5 V
 Test load termination supply voltage 1.5 V

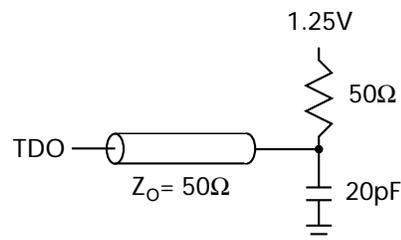
2.5 V TAP AC Test Conditions

Input pulse levels V_{SS} to 2.5 V
 Input rise and fall times (Slew Rate) 2 V/ns
 Input timing reference levels 1.25 V
 Output reference levels 1.25 V
 Test load termination supply voltage 1.25 V

3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Output Load Equivalent



Notes

9. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
10. Test conditions are specified using the load in TAP AC test Conditions. $t_R/t_F = 2$ V/ns (Slew Rate).

TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.135 V to 3.6 V unless otherwise noted)

Parameter ^[11]	Description	Description	Conditions	Min	Max	Unit
V _{OH1}	Output HIGH Voltage	I _{OH} = -4.0 mA	V _{DDQ} = 3.3 V	2.4	-	V
		I _{OH} = -1.0 mA	V _{DDQ} = 2.5 V	2.0	-	V
V _{OH2}	Output HIGH Voltage	I _{OH} = -100 μA	V _{DDQ} = 3.3 V	2.9	-	V
			V _{DDQ} = 2.5 V	2.1	-	V
V _{OL1}	Output LOW Voltage	I _{OL} = 8.0 mA	V _{DDQ} = 3.3 V	-	0.4	V
		I _{OL} = 1.0 mA	V _{DDQ} = 2.5 V	-	0.4	V
V _{OL2}	Output LOW Voltage	I _{OL} = 100 μA	V _{DDQ} = 3.3 V	-	0.2	V
			V _{DDQ} = 2.5 V	-	0.2	V
V _{IH}	Input HIGH Voltage		V _{DDQ} = 3.3 V	2.0	V _{DD} + 0.3	V
			V _{DDQ} = 2.5 V	1.7	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage		V _{DDQ} = 3.3 V	-0.3	0.8	V
			V _{DDQ} = 2.5 V	-0.3	0.7	V
I _X	Input Load Current	GND ≤ V _{IN} ≤ V _{DDQ}		-5	5	μA

Note

11. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1441KV33 (1M × 36)	Description
Revision Number (31:29)	000	Describes the version number.
Device Depth (28:24)	01011	Reserved for Internal Use
Architecture/Memory Type(23:18) ^[12]	000001	Defines memory type and architecture
Bus Width/Density(17:12)	100111	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction Bypass	3
Bypass	1
ID	32
Boundary Scan Order (165-ball FBGA package)	89

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note

12. Bit #24 is "1" in the ID Register Definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Order

165-ball FBGA [13, 14]

CY7C1441KV33 (1M × 36)

Bit #	Ball ID
1	N6
2	N7
3	N10
4	P11
5	P8
6	R8
7	R9
8	P9
9	P10
10	R10
11	R11
12	H11
13	N11
14	M11
15	L11
16	K11
17	J11
18	M10
19	L10
20	K10
21	J10
22	H9
23	H10
24	G11
25	F11

Bit #	Ball ID
26	E11
27	D11
28	G10
29	F10
30	E10
31	D10
32	C11
33	A11
34	B11
35	A10
36	B10
37	A9
38	B9
39	C10
40	A8
41	B8
42	A7
43	B7
44	B6
45	A6
46	B5
47	A5
48	A4
49	B4
50	B3

Bit #	Ball ID
51	A3
52	A2
53	B2
54	C2
55	B1
56	A1
57	C1
58	D1
59	E1
60	F1
61	G1
62	D2
63	E2
64	F2
65	G2
66	H1
67	H3
68	J1
69	K1
70	L1
71	M1
72	J2
73	K2
74	L2
75	M2

Bit #	Ball ID
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

Notes

- 13. Balls which are NC (No Connect) are preset LOW.
- 14. Bit# 89 is preset HIGH.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage on V _{DD} Relative to GND	-0.3 V to +4.6 V
Supply Voltage on V _{DDQ} Relative to GND	-0.3 V to +V _{DD}
DC Voltage Applied to Outputs in Tristate	-0.5 V to V _{DDQ} + 0.5 V
DC Input Voltage	-0.5 V to V _{DD} + 0.5 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001 V
Latch-up Current	> 200 mA
DC Input Voltage	-0.5 V to V _{DD} + 0.5 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001 V
Latch-up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{DD}	V _{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V _{DD}
Industrial	-40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU (Device without ECC)	Logical Single-Bit Upsets	25 °C	<5	5	FIT/Mb
			0	0.01	FIT/Mb
LSBU (Device with ECC)					
LMBU (All Devices)	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/Mb
SEL (All Devices)	Single Event Latch up	85 °C	0	0.1	FIT/Dev

* No LMBU or SEL events occurred during testing; this column represents a statistical χ^2 , 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

Electrical Characteristics

Over the Operating Range

DC Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Max	Units
V _{DD}	Power supply voltage	–	3.135	3.6	V
V _{DDQ}	I/O supply voltage	for 3.3 V I/O	3.135	V _{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V _{OH}	Output HIGH voltage	for 3.3 V I/O, I _{OH} = -4.0 mA	2.4	–	V
		for 2.5 V I/O, I _{OH} = -1.0 mA	2.0	–	V
V _{OL}	Output LOW voltage	for 3.3 V I/O, I _{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I _{OL} = 1.0 mA	–	0.4	V
V _{IH}	Input HIGH voltage ^[15]	for 3.3 V I/O	2.0	V _{DD} + 0.3 V	V
		for 2.5 V I/O	1.7	V _{DD} + 0.3 V	V
V _{IL}	Input LOW voltage ^[15]	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V

Notes

15. Overshoot: V_{IH}(AC) < V_{DD} + 1.5V (Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > -2V (Pulse width less than t_{CYC}/2).
 16. T_{Power-up}: Assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics (continued)

Over the Operating Range

DC Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Max	Units	
I_X	Input leakage current except ZZ and MODE	$GND \leq V_I \leq V_{DDQ}$	-5	5	μA	
	Input current of MODE	Input = V_{SS}	-30	-	μA	
		Input = V_{DD}	-	5	μA	
	Input current of ZZ	Input = V_{SS}	-5	-	μA	
Input = V_{DD}		-	30	μA		
I_{OZ}	Output leakage current	$GND \leq V_I \leq V_{DDQ}$, Output Disabled	-5	5		
I_{DD}	V_{DD} operating supply current	$V_{DD} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{CYC}$	7.5-ns cycle, 133 MHz	-	150	mA
			$\times 18$	-	170	
I_{SB1}	Automatic CE power down current – TTL inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$, inputs switching	7.5-ns cycle, 133 MHz	-	85	mA
			$\times 18$	-	90	
I_{SB2}	Automatic CE power down current – CMOS inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{DD} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$, inputs static	7.5-ns cycle, 133 MHz	-	75	mA
			$\times 18$	-	80	
I_{SB3}	Automatic CE power down current – CMOS inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{DDQ} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$, $f = f_{MAX}$, inputs switching	7.5-ns cycle, 133 MHz	-	85	mA
			$\times 18$	-	90	
I_{SB4}	Automatic CE power down current – TTL inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{DD} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$, inputs static	7.5-ns cycle, 133 MHz	-	75	mA
			$\times 18$	-	80	

Capacitance

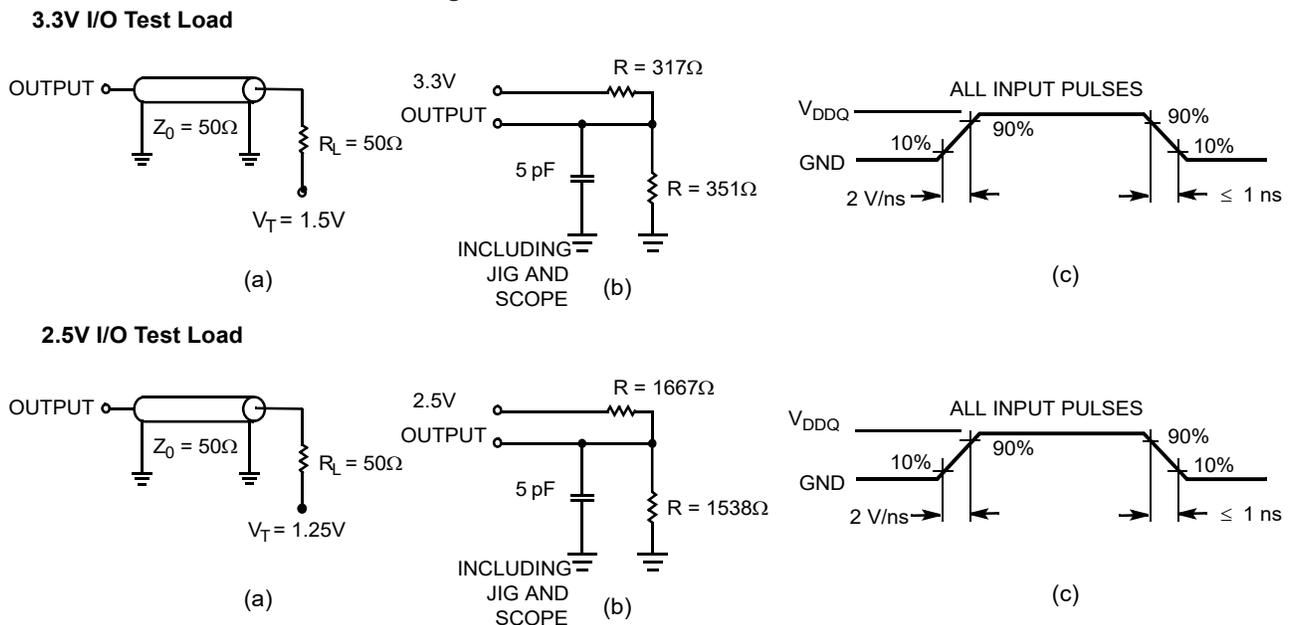
Parameter ^[17]	Description	Test Conditions	100-pin TQFP Max.	165-ball FBGA Max.	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{DDQ} = 2.5\text{V}$	5	5	pF
C_{CLK}	Clock input capacitance		5	5	pF
C_{IO}	Input/output capacitance		5	5	pF

Thermal Resistance

Parameter ^[17]	Description	Test Conditions	100-pin TQFP Package	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	With Still Air (0 m/s)	35.36	14.24	$^\circ\text{C/W}$
		With Air Flow (1 m/s)	31.30	12.47	$^\circ\text{C/W}$
		With Air Flow (3 m/s)	28.86	11.40	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)	—	7.52	3.92	$^\circ\text{C/W}$
Θ_{JB}	Thermal resistance (junction to board)		28.89	7.19	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Note

17. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter [18, 19]	Description	-133		Unit
		Min	Max	
t _{POWER}	V _{DD} (Typical) to the first Access ^[20]	1	–	ms
Clock				
t _{CYC}	Clock cycle time	7.5	–	ns
t _{CH}	Clock HIGH	2.5	–	ns
t _{CL}	Clock LOW	2.5	–	ns
Output Times				
t _{CDV}	Data Output Valid after CLK Rise	–	6.5	ns
t _{DOH}	Data Output Hold after CLK Rise	2.5	–	ns
t _{CLZ}	Clock to Low Z ^[21, 22, 23]	2.5	–	ns
t _{CHZ}	Clock to High Z ^[21, 22, 23]	–	3.8	ns
t _{OE_V}	$\overline{\text{OE}}$ LOW to Output Valid	–	3.0	ns
t _{OE_{LZ}}	$\overline{\text{OE}}$ LOW to Output Low Z ^[21, 22, 23]	0	–	ns
t _{OE_{HZ}}	$\overline{\text{OE}}$ HIGH to Output High Z ^[21, 22, 23]	–	3.0	ns
Setup Times				
t _{AS}	Address setup before CLK Rise	1.5	–	ns
t _{ADS}	ADSP, ADSC setup before CLK Rise	1.5	–	ns
t _{ADVS}	$\overline{\text{ADV}}$ setup before CLK Rise	1.5	–	ns
t _{WES}	$\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_X$ setup before CLK Rise	1.5	–	ns
t _{DS}	Data input setup before CLK Rise	1.5	–	ns
t _{CES}	Chip Enable setup	1.5	–	ns
Hold Times				
t _{AH}	Address Hold after CLK Rise	0.5	–	ns
t _{ADH}	ADSP, ADSC Hold after CLK Rise	0.5	–	ns
t _{WEH}	$\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_X$ Hold after CLK Rise	0.5	–	ns
t _{ADVH}	$\overline{\text{ADV}}$ Hold after CLK Rise	0.5	–	ns
t _{DH}	Data Input Hold after CLK Rise	0.5	–	ns
t _{CEH}	Chip Enable Hold after CLK Rise	0.5	–	ns

Notes

18. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V.

19. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

20. This part has a voltage regulator internally; t_{POWER} is the time that the power must be supplied above V_{DD}(minimum) initially, before a read or write operation can be initiated.

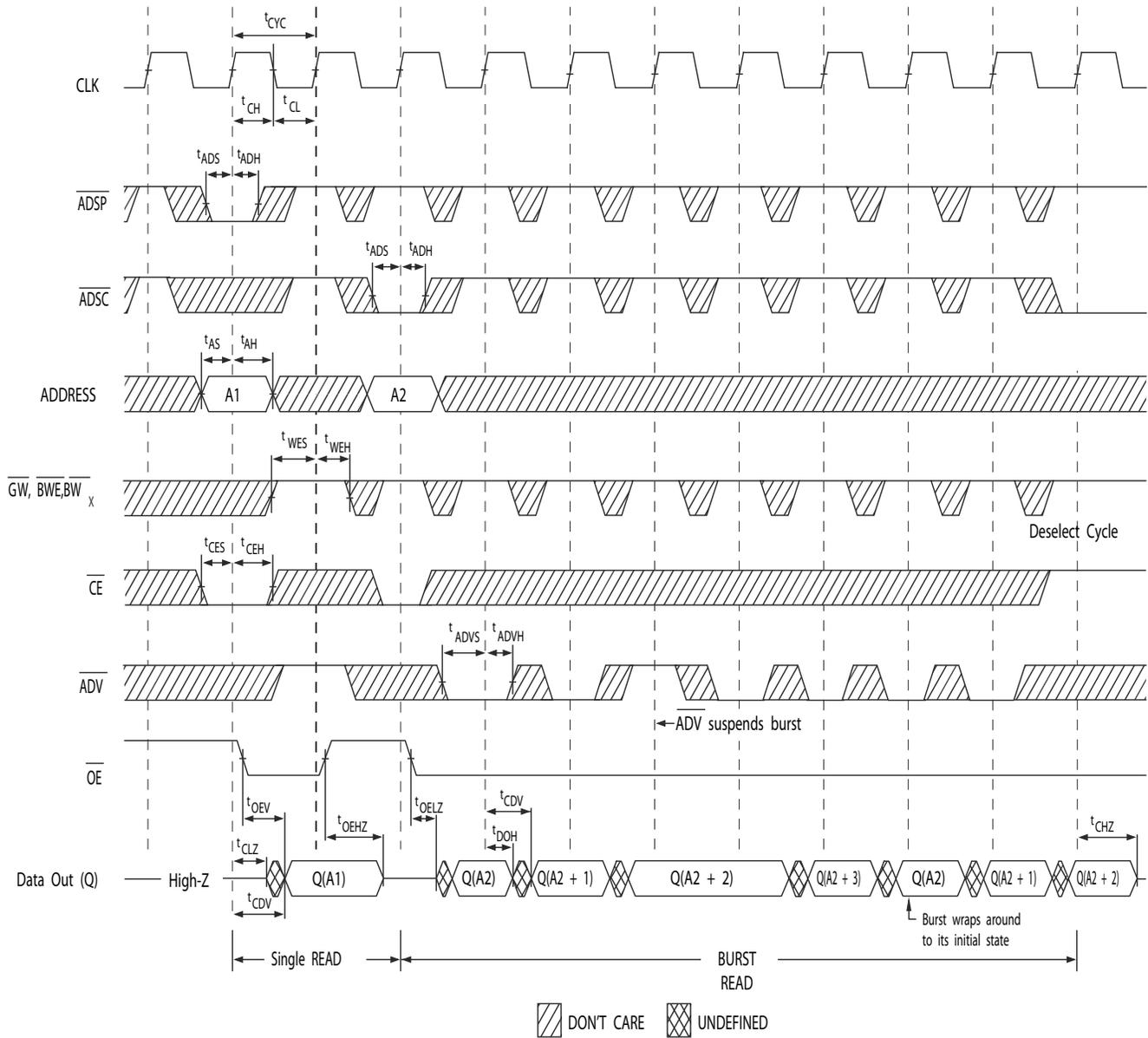
21. t_{CHZ}, t_{CLZ}, t_{OE_{LZ}}, and t_{OE_{HZ}} are specified with AC test conditions shown in part (b) of Figure 3 on page 21. Transition is measured ± 200 mV from steady-state voltage.

22. At any given voltage and temperature, t_{OE_{HZ}} is less than t_{OE_{LZ}} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.

23. This parameter is sampled and not 100% tested.

Timing Diagrams

Figure 4. Read Cycle Timing [24]

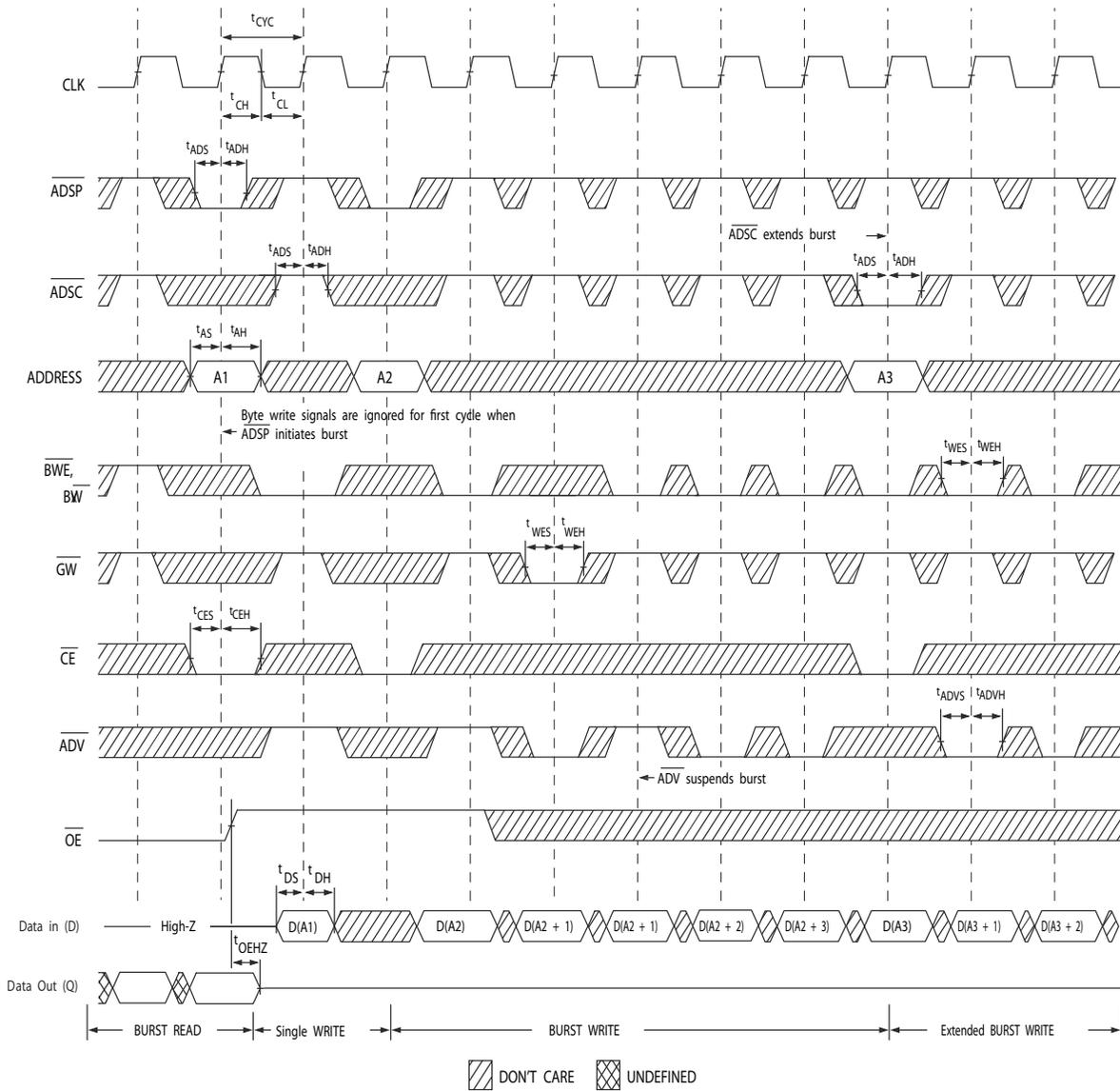


Note

24. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW or \overline{CE}_3 is HIGH.

Timing Diagrams (continued)

Figure 5. Write Cycle Timing [25, 26]

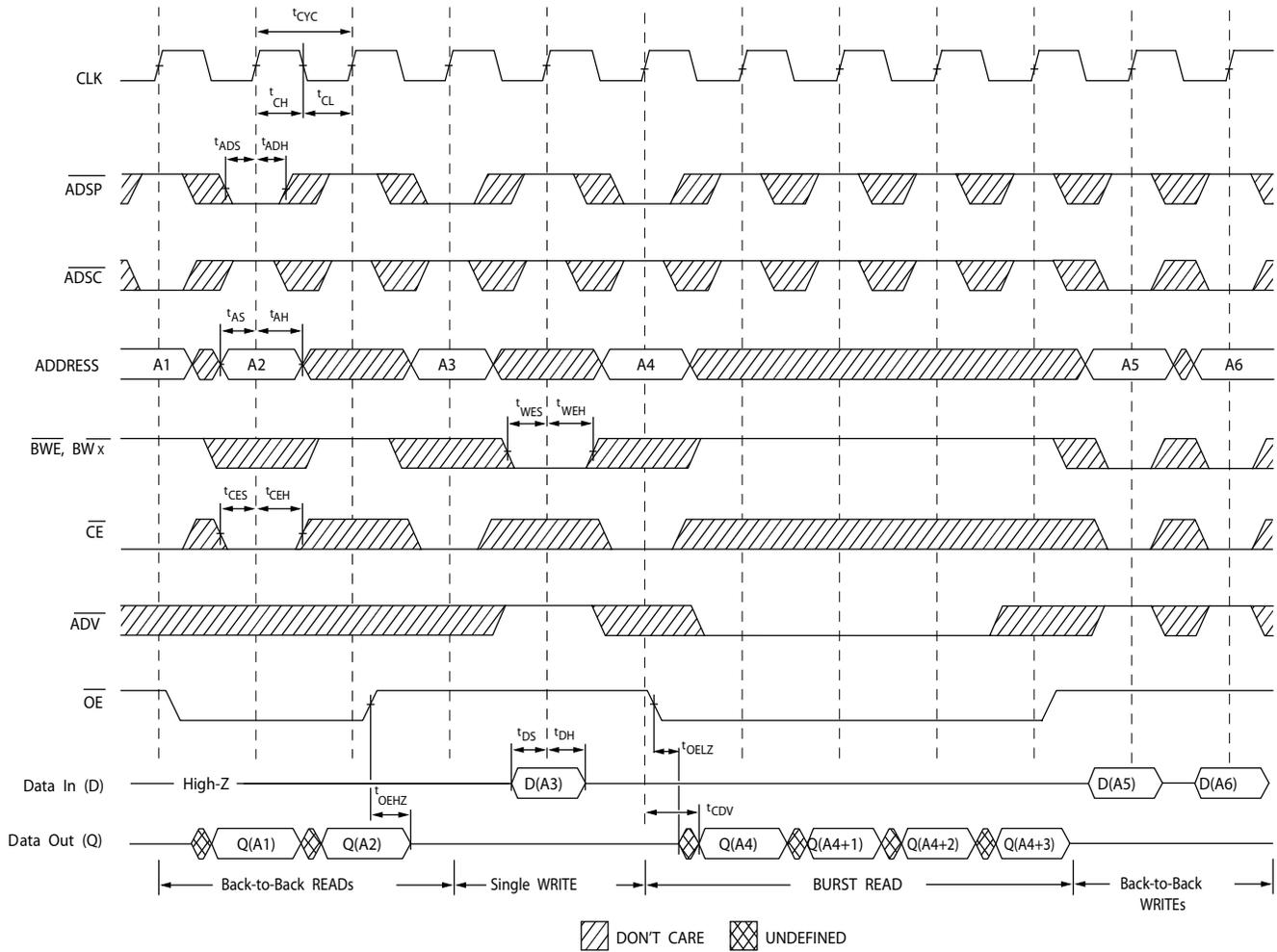


Notes

25. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, CE_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH or CE_2 is LOW or \overline{CE}_3 is HIGH.
 26. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW and BW_x LOW.

Timing Diagrams (continued)

Figure 6. Read/Write Cycle Timing [27, 28, 29]

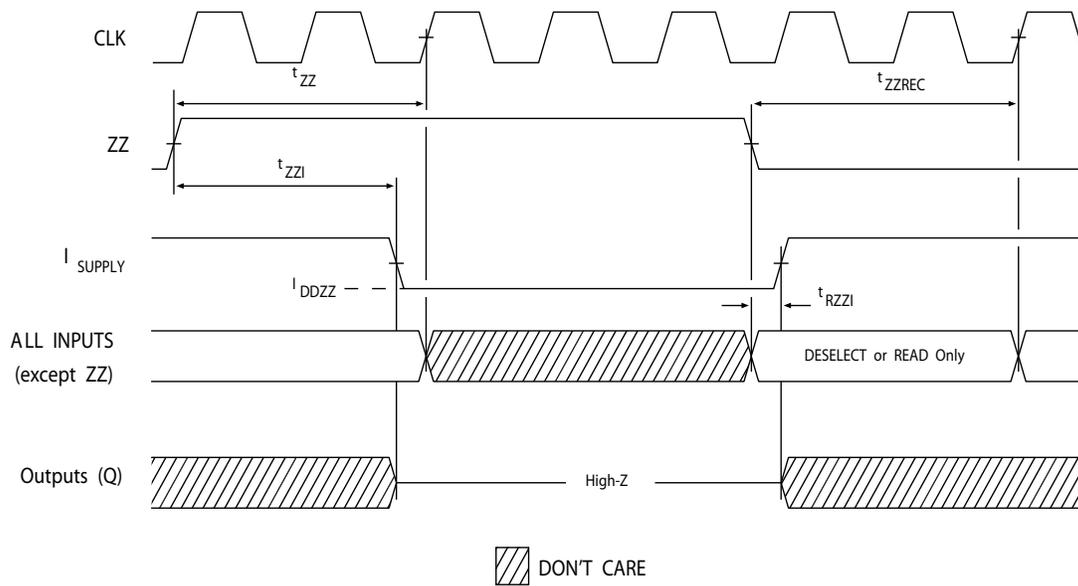


Notes

- 27. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, CE_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH or CE_2 is LOW or \overline{CE}_3 is HIGH.
- 28. The data bus (Q) remains in high Z following a Write cycle, unless a new read access is initiated by ADSP or ADSC.
- 29. GW is HIGH.

Timing Diagrams (continued)

Figure 7. ZZ Mode Timing [30, 31]



Notes

- 30. Device must be deselected when entering ZZ mode. See the Cycle Descriptions table for all possible signal conditions to deselect the device.
- 31. DQs are in high Z when exiting ZZ sleep mode.

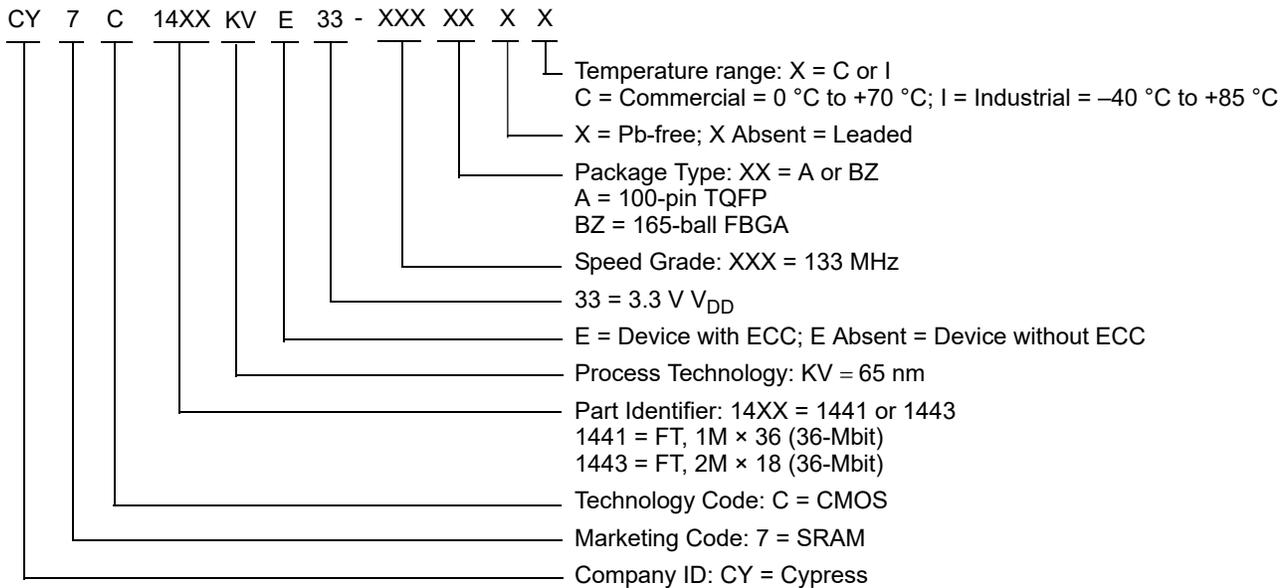
Ordering Information

Table 1 lists the ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>.

Table 1. Ordering Information

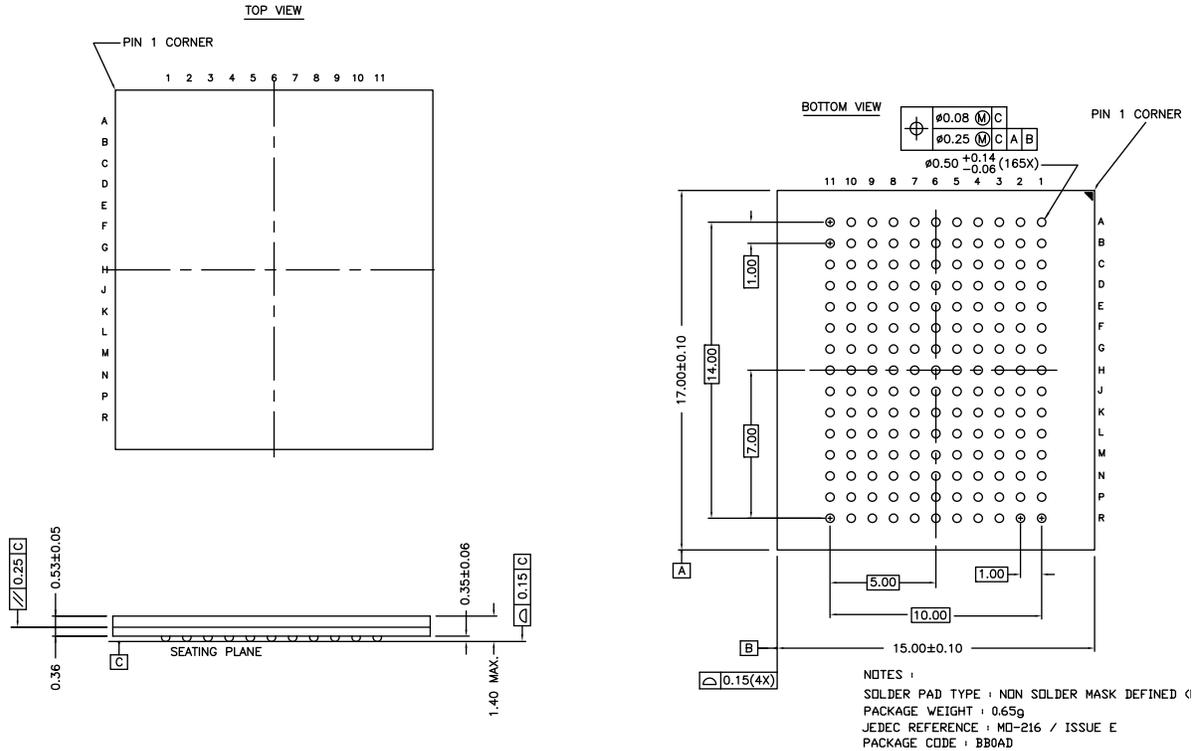
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1441KV33-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1441KVE33-133AXC			
	CY7C1441KV33-133AXI			
	CY7C1441KVE33-133AXI			
	CY7C1443KV33-133AXI			
	CY7C1441KV33-133BZXI	51-85195	165-ball FBGA (15 × 17 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagrams (continued)

Figure 9. 165-ball FBGA (15 × 17 × 1.4 mm (0.5 Ball Diameter)) Package Outline, 51-85195



51-85195 *D

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
NoBL	No Bus Latency
OE	Output Enable
SRAM	Static Random Access Memory
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select
TQFP	Thin Quad Flat Pack
WE	Write Enable
ECC	Error Correcting Code

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mm	millimeter
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1441KV33/CY7C1443KV33/CY7C1441KVE33, 36-Mbit (1M × 36/2M × 18) Flow-Through SRAM (With ECC)			
Document Number: 001-66677			
Revision	ECN	Submission Date	Description of Change
*E	4680535	04/10/2015	Changed status from Preliminary to Final.
*F	4757974	05/07/2015	Added Logic Block Diagram – CY7C1441KVE33 . Updated Functional Overview : Updated ZZ Mode Electrical Characteristics : Changed maximum value of I _{DDZZ} parameter from 89 mA to 75 mA.
*G	4965199	10/15/2015	Updated Selection Guide : Updated value of “Maximum Operating Current”.
*H	5338013	07/05/2016	Updated Truth Table : Updated details in “CE ₃ ” column corresponding to fifth row of “Deselected Cycle, Power Down”. Updated Neutron Soft Error Immunity : Updated values in “Typ” and “Max” columns corresponding to LSBU (Device without ECC) parameter. Updated to new template.
*I	6072311	02/15/2018	Updated Package Diagrams : spec 51-85050 – Changed revision from *E to *G. Updated to new template.
*J	6745577	12/05/2019	Updated Ordering Information : Updated part numbers. Updated to new template.

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