

ADM709

FEATURES

Precision Supply Voltage Monitor
 +5 V, +3.3 V, +3 V Power Supply Monitor
 35 μ A Quiescent Current
 140 ms (min) Power-On Reset Pulse
 Low Cost
 8-Pin DIP/SO Packages
 Upgrade for MAX709

APPLICATIONS

Microprocessor Systems
 Computers
 Controllers
 Intelligent Instruments
 Critical μ P Monitoring
 Automotive Systems
 Critical μ P Power Monitoring

GENERAL DESCRIPTION

The ADM709 contains a power supply monitor which generates a system reset during power-up, power-down and brownout conditions. When V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$ goes low and holds the μ P in reset. On power-up the $\overline{\text{RESET}}$ output is held low for 140 ms after V_{CC} rises above the threshold. The RESET output remains operational with V_{CC} as low as 1 V.

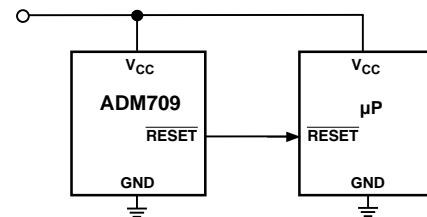
Three supply-voltage threshold levels are available suitable for +5 V, +3.3 V and for +3 V supply monitoring. The actual reset voltage threshold is given below.

The ADM709 is available in 8-pin DIP and SOIC packages.

Table I. Reset Threshold

| Suffix | Voltage (V) |
|--------|-------------|
| L | 4.65 |
| M | 4.40 |
| T | 3.08 |
| S | 2.93 |
| R | 2.63 |

FUNCTIONAL BLOCK DIAGRAM



Typical Operating Circuit

ORDERING GUIDE

| Model | Reset Threshold | Temperature Range | Package Option* |
|-----------|-----------------|-------------------|-----------------|
| ADM709LAN | 4.65 V | -40°C to +85°C | N-8 |
| ADM709LAR | 4.65 V | -40°C to +85°C | SO-8 |
| ADM709MAN | 4.40 V | -40°C to +85°C | N-8 |
| ADM709MAR | 4.40 V | -40°C to +85°C | SO-8 |
| ADM709TAN | 3.08 V | -40°C to +85°C | N-8 |
| ADM709TAR | 3.08 V | -40°C to +85°C | SO-8 |
| ADM709SAN | 2.93 V | -40°C to +85°C | N-8 |
| ADM709SAR | 2.93 V | -40°C to +85°C | SO-8 |
| ADM709RAN | 2.63 V | -40°C to +85°C | N-8 |
| ADM709RAR | 2.63 V | -40°C to +85°C | SO-8 |

*N = Plastic DIP; SO = SOIC.

REV. 0

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ADM709—SPECIFICATIONS (V_{CC} = Full Operating Range, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions/Comments |
|--|-----------------------|------|------|---------------|--|
| V_{CC} Operating Voltage Range | 1.0 | | 5.5 | V | $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ |
| Supply Current | 1.2 | 35 | 85 | μA | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} < 3.6\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ |
| | | 35 | 110 | μA | $V_{CC} < 3.6\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ |
| | | 65 | 150 | μA | $V_{CC} < 5.5\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ |
| | | 65 | 200 | μA | $V_{CC} < 5.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ |
| Reset Threshold | 4.5 | 4.65 | 4.75 | V | ADM709L |
| | 4.25 | 4.40 | 4.50 | V | ADM709M |
| | 3.00 | 3.08 | 3.15 | V | ADM709T |
| | 2.85 | 2.93 | 3.00 | V | ADM709S |
| | 2.55 | 2.63 | 2.70 | V | ADM709R |
| V_{CC} to $\overline{\text{RESET}}$ Delay | | 20 | | μs | V_{CC} = Reset Threshold max–min |
| $\overline{\text{RESET}}$ Active Time-Out Period | 140 | 280 | 380 | ms | V_{CC} = Reset Threshold max, V_{CC} Rising |
| $\overline{\text{RESET}}$ Output Voltage | | | 0.3 | V | ADM709R/S/T, $I_{\text{SINK}} = 1.2\text{ mA}$. V_{CC} = Reset Threshold min |
| | | | 0.4 | V | ADM709L/M, $I_{\text{SINK}} = 3.2\text{ mA}$. V_{CC} = Reset Threshold min |
| | | | 0.3 | V | $I_{\text{SINK}} = 50\ \mu\text{A}$. $V_{CC} \geq 1.0\text{ V}$ |
| | | | 0.4 | V | $I_{\text{SINK}} = 100\ \mu\text{A}$. $V_{CC} \geq 1.2\text{ V}$ |
| | $0.8 \times V_{CC}$ | | | V | ADM709R/S/T, $I_{\text{SOURCE}} = 500\ \mu\text{A}$, $V_{CC} \geq$ Reset Threshold max |
| | $V_{CC}-1.5\text{ V}$ | | | V | ADM709L/M, $I_{\text{SOURCE}} = 800\ \mu\text{A}$, $V_{CC} \geq$ Reset Threshold max |

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

($T_A = +25^\circ\text{C}$ unless otherwise noted)

| | |
|--|-----------------------------------|
| V_{CC} | –0.3 V to +6 V |
| $\overline{\text{RESET}}$ Output | –0.3 V to $V_{CC} + 0.3\text{ V}$ |
| V_{CC} Input Current | 20 mA |
| $\overline{\text{RESET}}$ Output Current | 20 mA |
| Power Dissipation, N-8 DIP | 727 mW |
| θ_{JA} Thermal Impedance | 135°C/W |
| Power Dissipation, SO-8 SOIC | 470 mW |
| θ_{JA} Thermal Impedance | 110°C/W |
| Operating Temperature Range | |
| Industrial (A Version) | –40°C to +85°C |
| Lead Temperature (Soldering, 10 secs) | +300°C |
| Vapor Phase (60 secs) | +215°C |
| Infrared (15 secs) | +220°C |
| Storage Temperature Range | –65°C to +150°C |
| ESD Rating | >5 kV |

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

PIN FUNCTION DESCRIPTION

| Mnemonic | Pin No. | Function |
|---------------------------|---------------|---|
| NC | 1, 4, 5, 6, 8 | No Connect Pins. |
| V_{CC} | 2 | +5 V, +3.3 V, +3 V Power Supply Input. |
| $\overline{\text{RESET}}$ | 7 | Logic Output. It remains low while V_{CC} is below the reset threshold voltage and for 280 ms (typ) after V_{CC} rises above the threshold. |
| GND | 3 | Ground, 0 V. |

PIN CONFIGURATION





Figure 1. Functional Block Diagram



Figure 2. Typical Operating Circuit

CIRCUIT INFORMATION

RESET Output

$\overline{\text{RESET}}$ is an active low output which provides a reset signal to the microprocessor whenever the V_{CC} supply voltage is below the reset threshold. An internal timer holds $\overline{\text{RESET}}$ low for 140 ms after the voltage on V_{CC} rises above the threshold. This is intended as a power-on reset signal for the processor. It allows time for the power supply and microprocessor to stabilize after power up. Similarly a power supply brownout will initiate a processor reset. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply drops.



Figure 3. Power Off/On $\overline{\text{RESET}}$ Timing

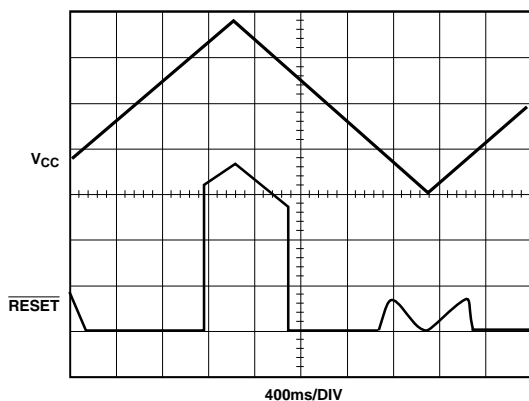


Figure 4. $\overline{\text{RESET}}$ Output vs. V_{CC}

RESET at Voltages < 1 V

The ADM709 $\overline{\text{RESET}}$ output is guaranteed to operate with supply voltages as low as 1 V. If it is desired that the $\overline{\text{RESET}}$ output remains low below 1 V, then a pull-down resistor should be connected between the $\overline{\text{RESET}}$ output and GND. A resistor of 100 k Ω is suitable. This is illustrated in Figure 5.



Figure 5. $\overline{\text{RESET}}$ Valid @ $V_{CC} < 1 \text{ V}$

Glitch Immunity

The ADM709 is immune to short transients which may occur on the V_{CC} line. This is important so that spurious resets are not generated as a result of minor glitches on the power supply.

Additional glitch immunity may be obtained by connecting a capacitor (0.1 μF or greater) as close as possible to the V_{CC} pin on the device.

Microprocessors with Bidirectional I-O

Some microprocessors or microcontrollers such as the MC68HC11 have bidirectional reset lines. In order to avoid signal contention, a resistor of 4.7 k Ω should be connected between the ADM709 $\overline{\text{RESET}}$ output and the microcontroller $\overline{\text{RESET}}$ line. This arrangement is shown in Figure 6.



Figure 6. Interfacing to Microprocessors with Bidirectional $\overline{\text{RESET}}$

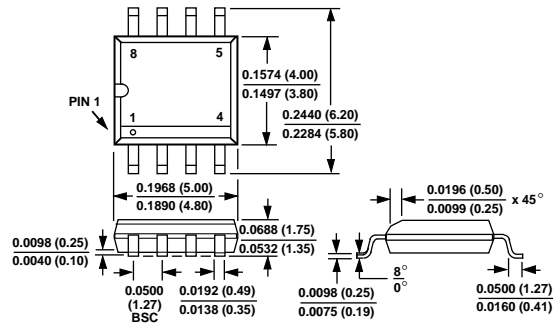
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**8-Lead Plastic DIP
(N-8)**



**8-Lead SOIC
(SO-8)**





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