TMS320C54CST Client Side Telephony DSP

Data Manual

Literature Number: SPRS187C
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REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPRS187B device-specific data sheet to make it an SPRS187C revision.

Scope: This document has been reviewed for technical accuracy; the technical content is up-to-date as of the specified release date with the following changes.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
21	Table 2−3, Signal Descriptions: − Updated DESCRIPTION of $\overline{\text{TRST}}$ − Added footnote about $\overline{\text{TRST}}$
113	Figure 3−63, TMS320C54CST Hardware Reference Design: − Changed “R47 NI” to “R47”
115	Table 3−52, Bill of Materials: − Added separate row (now row 38) for R47 [R47 was in the same row as R32 (row 37) in SPRS187B] − Updated rows 37 and 38 − renumbered subsequent rows
169	Section 6, Mechanical Data: − Moved “Si3016 Mechanical Data” section (was Section 6.3 in SPRS187B) to Section 6.1 − Moved “Package Thermal Resistance Characteristics” section (Section 5.4 in SPRS187B) to Section 6.2 − Added Section 6.3, Packaging Information − Mechanical drawings will be appended to this document via an automated process

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1 TMS320C54CST Client Side Telephony DSP Features

- On-Chip ROM
  - 128K × 16-Bit Configured for Program Memory
  - Contains 14 TMS320™ DSP Algorithm Standard Compliant Telephony Algorithms
- 40K x 16-Bit On-Chip RAM Composed of Five Blocks of 8K × 16-Bit On-Chip Dual-Access Program/Data RAM
- CST Software in ROM:
  - Data Transfer (Modem up to V.32BIS 14400 bps)
  - Telephony Signals Processing (DTMF, CPTD, Caller ID)
  - Voice Processing (Echo Canceller, G726, VAD, CNG, AGC)
- Configurable in Either:
  - Chipset Mode: Stand-Alone Telephony/Data Modem (ROM-Only Code Execution)
  - Flex Mode: Code Execution From RAM, ROM, or External.
- Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus
- 40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators
- 17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation
- Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle
- Data Bus With a Bus Holder Feature
- Extended Addressing Mode for 8M × 16-Bit Maximum Addressable External Program Space
- Enhanced External Parallel Interface (XIO2)
- Single-Instruction-Repeat and Block-Repeat Operations for Program Code
- Block-Memory-Move Instructions for Better Program and Data Management
- Instructions With a 32-Bit Long Word Operand
- Instructions With Two- or Three-Operand Reads
- Arithmetic Instructions With Parallel Store and Parallel Load
- Conditional Store Instructions
- Fast Return From Interrupt
- On-Chip Peripherals
  - Software-Programmable Wait-State Generator and Programmable Bank-Switching
  - On-Chip Programmable Phase-Locked Loop (PLL) Clock Generator With External Clock Source
  - Two 16-Bit Timers
  - Six-Channel Direct Memory Access (DMA) Controller
  - Two Multichannel Buffered Serial Ports (McBSPs)
  - 8/16-Bit Enhanced Parallel Host-Port Interface (HPI8/16)
  - Universal Asynchronous Receiver/ Transmitter (UART) With Integrated Baud Rate Generator
  - Integrated Direct Access Arrangement (DAA) Module
- Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes
- CLKOUT Off Control to Disable CLKOUT
- On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic
- 144-Pin Ball Grid Array (BGA) (GGU Suffix)
- 144-Pin Low-Profile Quad Flatpack (LQFP) (PGE Suffix)
- 8.33-ns Single-Cycle Fixed-Point Instruction Execution Time (120 MIPS)
- 3.3-V I/O Supply Voltage
- 1.5-V Core Supply Voltage

Note: Human Body Model ESD test performance for this product was demonstrated to be ±1.5 kV during product qualification. Industry standard test method used was EIA/JESD22-A114. Adherence to ESD handling precautionary procedures is advised at all times.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

2 Introduction

This data manual discusses features and specifications of the TMS320C54CST Client Side Telephony DSP (hereafter referred to as the 54CST unless otherwise specified) digital signal processors (DSPs).

This section lists the pin assignments and describes the function of each pin. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

NOTE: This data manual is designed to be used in conjunction with the *TMS320C54x™ DSP Functional Overview* (literature number SPRU307).

2.1 Description

The 54CST are based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. These processors provide an arithmetic logic unit (ALU) with a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The basis of the operational flexibility and speed of these DSPs is a highly specialized instruction set.

Separate program and data spaces allow simultaneous access to program instructions and data, providing a high degree of parallelism. Two read operations and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. These DSPs also include the control mechanisms to manage interrupts, repeated operations, and function calls.

2.2 Pin Assignments

Figure 2−1 illustrates the ball locations for the 144-pin ball grid array (BGA) package and is used in conjunction with Table 2−1 to locate signal names and ball grid numbers. Figure 2−2 provides the pin assignments for the 144-pin low-profile quad flatpack (LQFP) package. Figure 2−3 provides the pin assignments for the Si3016 line-side device.

TMS320C54x is a trademark of Texas Instruments.

2.2.1 Terminal Assignments for the GGU Package

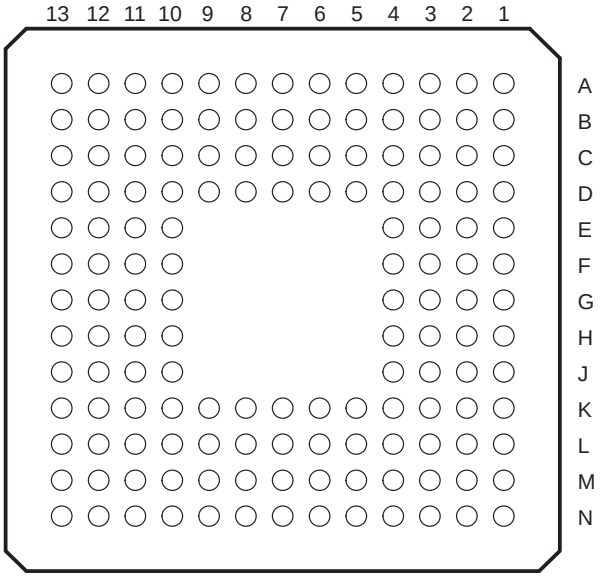


Figure 2−1. 144-Ball GGU MicroStar BGA™ (Bottom View)

Table 2−1 lists each signal name and BGA ball number for the 144-pin TMS320C54CSTGGU package. Table 2−3 lists each terminal name, terminal function, and operating modes for the TMS320C54CST.

MicroStar BGA is a trademark of Texas Instruments.

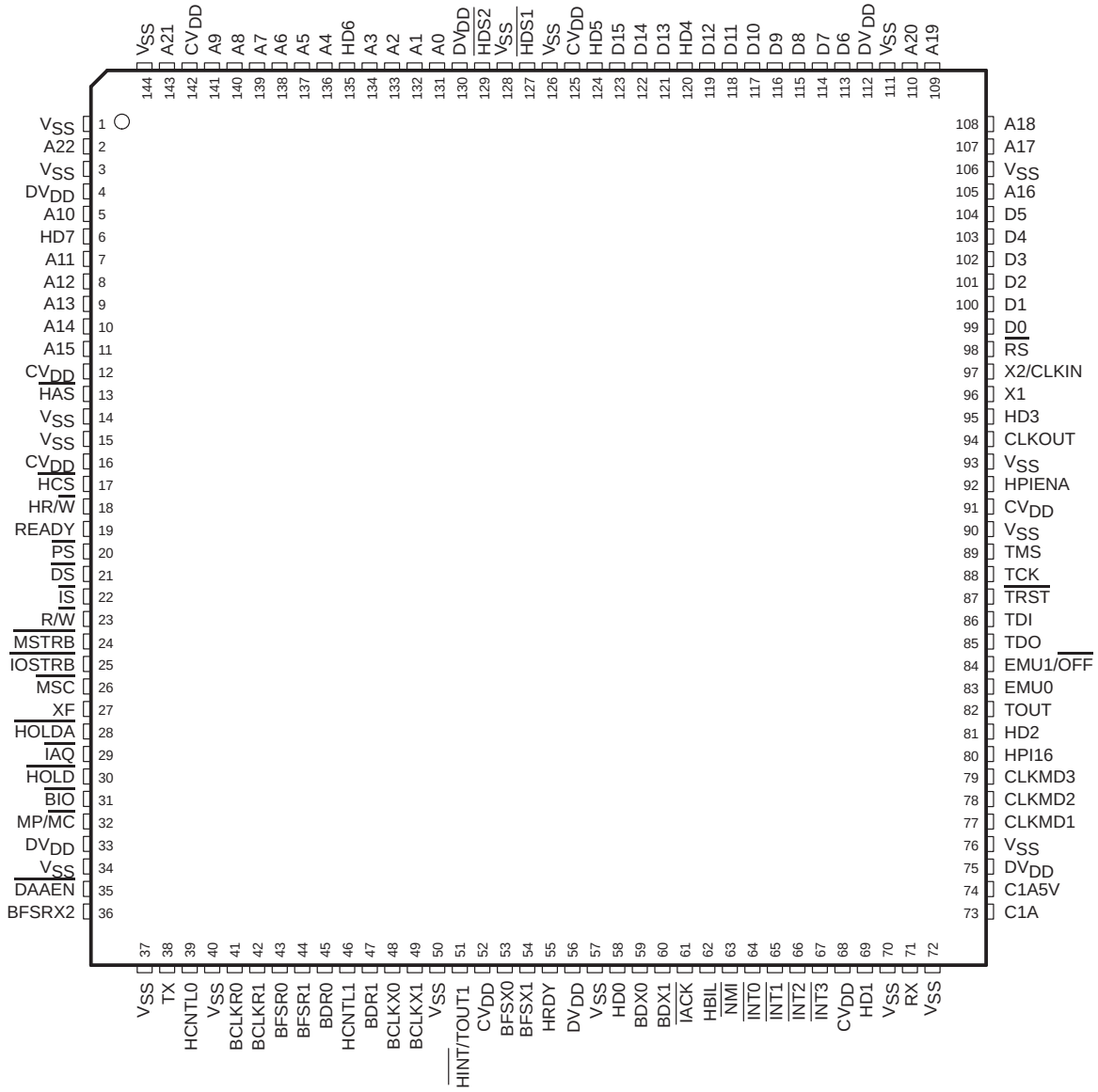
Table 2−1. Terminal Assignments for the 144-Pin BGA Package†

SIGNAL QUADRANT 1	BGA BALL #	SIGNAL QUADRANT 2	BGA BALL #	SIGNAL QUADRANT 3	BGA BALL #	SIGNAL QUADRANT 4	BGA BALL #
V_{SS}	A1	C1A	N13	V_{SS}	N1	A19	A13
A22	B1	C1A5V	M13	TX	N2	A20	A12
V_{SS}	C2	DV_{DD}	L12	HCNTL0	M3	V_{SS}	B11
DV_{DD}	C1	V_{SS}	L13	V_{SS}	N3	DV_{DD}	A11
A10	D4	CLKMD1	K10	BCLKR0	K4	D6	D10
HD7	D3	CLKMD2	K11	BCLKR1	L4	D7	C10
A11	D2	CLKMD3	K12	BFSR0	M4	D8	B10
A12	D1	HPI16	K13	BFSR1	N4	D9	A10
A13	E4	HD2	J10	BDR0	K5	D10	D9
A14	E3	TOUT	J11	HCNTL1	L5	D11	C9
A15	E2	EMU0	J12	BDR1	M5	D12	B9
CV_{DD}	E1	EMU1/$\overline{OFF}$	J13	BCLKX0	N5	HD4	A9
$\overline{HAS}$	F4	TDO	H10	BCLKX1	K6	D13	D8
V_{SS}	F3	TDI	H11	V_{SS}	L6	D14	C8
V_{SS}	F2	$\overline{TRST}$	H12	$\overline{HINT}$/TOUT1	M6	D15	B8
CV_{DD}	F1	TCK	H13	CVDD	N6	HD5	A8
$\overline{HCS}$	G2	TMS	G12	BFSX0	M7	CV_{DD}	B7
HR/$\overline{W}$	G1	V_{SS}	G13	BFSX1	N7	V_{SS}	A7
READY	G3	CV_{DD}	G11	HRDY	L7	$\overline{HDS1}$	C7
$\overline{PS}$	G4	HPIENA	G10	DV_{DD}	K7	V_{SS}	D7
$\overline{DS}$	H1	V_{SS}	F13	V_{SS}	N8	$\overline{HDS2}$	A6
$\overline{IS}$	H2	CLKOUT	F12	HD0	M8	DV_{DD}	B6
R/$\overline{W}$	H3	HD3	F11	BDX0	L8	A0	C6
$\overline{MSTRB}$	H4	X1	F10	BDX1	K8	A1	D6
$\overline{IOSTRB}$	J1	X2/CLKIN	E13	$\overline{IACK}$	N9	A2	A5
$\overline{MSC}$	J2	$\overline{RS}$	E12	HBIL	M9	A3	B5
XF	J3	D0	E11	$\overline{NMI}$	L9	HD6	C5
$\overline{HOLDA}$	J4	D1	E10	$\overline{INT0}$	K9	A4	D5
$\overline{IAQ}$	K1	D2	D13	$\overline{INT1}$	N10	A5	A4
$\overline{HOLD}$	K2	D3	D12	$\overline{INT2}$	M10	A6	B4
$\overline{BIO}$	K3	D4	D11	$\overline{INT3}$	L10	A7	C4
MP/$\overline{MC}$	L1	D5	C13	CV_{DD}	N11	A8	A3
DV_{DD}	L2	A16	C12	HD1	M11	A9	B3
V_{SS}	L3	V_{SS}	C11	V_{SS}	L11	CV_{DD}	C3
$\overline{DAAEN}$	M1	A17	B13	RX	N12	A21	A2
BFSRX2	M2	A18	B12	V_{SS}	M12	V_{SS}	B2

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

2.2.2 Pin Assignments for the PGE Package

The TMS320C54CSTPGE 144-pin low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2−2.



NOTE A: DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

Figure 2−2. 144-Pin PGE Low-Profile Quad Flatpack (Top View)

2.2.3 Pin Assignments for the Si3016

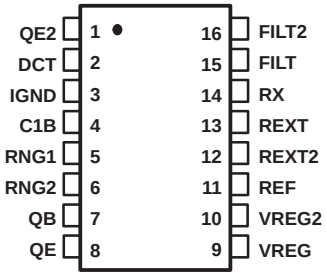


Figure 2−3. Si3016 Pin Assignments

Table 2−2. Si3016 Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	QE2	**TRANSISTOR EMITTER 2.** Connects to the emitter of Q4.
2	DCT	**DC TERMINATION.** Provides DC termination to the telephone network.
3	IGND	**ISOLATED GROUND.** Connects to ground on the line-side interface. Also connects to capacitor C2.
4	C1B	**ISOLATION CAPACITOR 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side module.
5	RNG1	**RING 1.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si3016.
6	RNG2	**RING 2.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si3016.
7	QB	**TRANSISTOR BASE.** Connects to the base of transistor Q3. Used to go on/off-hook.
8	QE	**TRANSISTOR EMITTER.** Connects to the emitter of transistor Q3. Used to go on/off-hook.
9	VREG	**VOLTAGE REGULATOR.** Connects to an external capacitor to provide bypassing for an internal power supply.
10	VREG2	**VOLTAGE REGULATOR 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	REF	**REFERENCE.** Connects to an external resistor to provide a high accuracy reference current.
12	REXT2	**EXTERNAL RESISTOR 2.** Sets the complex AC termination impedance.
13	REXT	**EXTERNAL RESISTOR.** Sets the real AC termination impedance.
14	RX	**RECEIVE INPUT.** Serves as the receive side input from the telephone network.
15	FILT	**FILTER.** Provides filtering for the DC termination circuits.
16	FILT2	**FILTER 2.** Provides filtering for the bias circuits.

2.3 Signal Descriptions

Table 2−3 lists each signal, function, and operating mode(s) grouped by function. See Section 2.2 for exact pin locations based on package type.

Table 2−3. Signal Descriptions

TERMINAL NAME	I/O†	DESCRIPTION		
EXTERNAL MEMORY INTERFACE PINS				
A22(MSB) A21 A20 A19 A18 A17 A16	O/Z	Parallel address bus A22 (MSB) through A0 (LSB). The lower sixteen address pins—A0 to A15—are multiplexed to address all external memory (program, data) or I/O, while the upper seven address pins—A22 to A16—are only used to address external program space. These pins are placed in the high-impedance state when the hold mode is enabled, or when $\overline{OFF}$ is low.		
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0(LSB)		A15(MSB) A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0(LSB)	I	These pins can be used to address internal memory via the HPI when the HPI16 pin is high.
D15(MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0(LSB)	I/O/Z	D15(MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0(LSB)	I/O	Parallel data bus D15 (MSB) through D0 (LSB). The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when $\overline{RS}$ or $\overline{HOLD}$ is asserted. The data bus also goes into the high-impedance state when $\overline{OFF}$ is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

Table 2−3. Signal Descriptions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
INITIALIZATION, INTERRUPT, AND RESET PINS		
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge signal. $\overline{\text{IACK}}$ Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. $\overline{\text{IACK}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$	I	External user interrupt inputs. $\overline{\text{INT0-3}}$ are prioritized and maskable via the interrupt mask register and interrupt mode bit. The status of these pins can be polled by way of the interrupt flag register.
$\overline{\text{NMI}}$	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is an external interrupt that cannot be masked by way of the INTM or the IMR. When $\overline{\text{NMI}}$ is activated, the processor traps to the appropriate vector location.
$\overline{\text{RS}}$	I	Reset input. $\overline{\text{RS}}$ causes the DSP to terminate execution and causes a re-initialization of the CPU and peripherals. When $\overline{\text{RS}}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{\text{RS}}$ affects various registers and status bits.
MP/$\overline{\text{MC}}$	I	Microprocessor/microcomputer mode select pin. If active low at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 16K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/$\overline{\text{MC}}$ bit of the PMST register can override the mode that is selected at reset.
MULTIPROCESSING AND GENERAL PURPOSE PINS		
$\overline{\text{BIO}}$	I	Branch control input. A branch can be conditionally executed when $\overline{\text{BIO}}$ is active. If low, the processor executes the conditional instruction. The $\overline{\text{BIO}}$ condition is sampled during the decode phase of the pipeline for XC instruction, and all other instructions sample $\overline{\text{BIO}}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when $\overline{\text{OFF}}$ is low, and is set high at reset.
MEMORY CONTROL PINS		
$\overline{\text{DS}}$ $\overline{\text{PS}}$ $\overline{\text{IS}}$	O/Z	Data, program, and I/O space select signals. $\overline{\text{DS}}$, $\overline{\text{PS}}$, and $\overline{\text{IS}}$ are always high unless driven low for accessing a particular external memory space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. $\overline{\text{DS}}$, $\overline{\text{PS}}$, and $\overline{\text{IS}}$ also go into the high-impedance state when $\overline{\text{OFF}}$ is low.
MSTRB	O/Z	Memory strobe signal. MSTRB is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. MSTRB also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
READY	I	Data ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{\text{W}}$	O/Z	Read/write signal. R/$\overline{\text{W}}$ indicates transfer direction during communication to an external device. Normally in read mode (high), unless asserted low when the DSP performs a write operation. Placed in high-impedance state in hold mode. R/$\overline{\text{W}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{IOSTRB}}$	O/Z	I/O strobe signal. $\overline{\text{IOSTRB}}$ is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. $\overline{\text{IOSTRB}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{HOLD}}$	I	Hold input. $\overline{\text{HOLD}}$ is asserted to request control of the address, data, and control lines. When acknowledged by the C54x™ DSP, these lines go into high-impedance state.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

C54x is a trademark of Texas Instruments.

Table 2−3. Signal Descriptions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
MEMORY CONTROL PINS (CONTINUED)		
$\overline{\text{HOLDA}}$	O/Z	Hold acknowledge signal. $\overline{\text{HOLDA}}$ indicates that the DSP is in a hold state and that the address, data, and control lines are in a high-impedance state, allowing the external memory interface to be accessed by other devices. $\overline{\text{HOLDA}}$ also goes into the high-impedance state when is $\overline{\text{OFF}}$ low.
$\overline{\text{MSC}}$	O/Z	Microstate complete. $\overline{\text{MSC}}$ indicates completion of all software wait states. When two or more software wait states are enabled, the $\overline{\text{MSC}}$ pin goes active at the beginning of the first software wait state, and goes inactive (high) at the beginning of the last software wait state. If connected to the ready input, $\overline{\text{MSC}}$ forces one external wait state after the last internal wait state is completed. $\overline{\text{MSC}}$ also goes into the high impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{IAQ}}$	O/Z	Instruction acquisition signal. $\overline{\text{IAQ}}$ is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
OSCILLATOR/TIMER PINS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. CLKOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. CLKMD1−CLKMD3 allows you to select and configure different clock modes such as crystal, external clock, various PLL factors.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal oscillator is not being used, an external clock source can be applied to this pin. The internal machine cycle time is determined by the clock operating mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when $\overline{\text{OFF}}$ is low.
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT cycle wide. TOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
TOUT1	I/O/Z	Timer1 output. TOUT1 signals a pulse when the on-chip timer1 counts down past zero. The pulse is a CLKOUT cycle wide. The TOUT1 output is multiplexed with the $\overline{\text{HINT}}$ pin of the HPI, and TOUT1 is only available when the HPI is disabled.
MULTI-CHANNEL BUFFERED SERIAL PORT PINS		
BCLKR0 BCLKR1	I/O/Z	Receive clock input. BCLKR serves as the serial shift clock for the buffered serial port receiver.
BDR0 BDR1	I	Serial data receive input.
BFSR0 BFSR1 BFSRX2	I/O/Z	Frame synchronization pulse for receive input. The BFSR pulse initiates the receive data process over BDR. BFSRX2 is McBSP2 transmit AND receive frame sync.
BCLKX0 BCLKX1	I/O/Z	Transmit clock. BCLKX serves as the serial shift clock for the buffered serial port transmitter. The BCLKX pins are configured as inputs after reset. BCLKX goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
BDX0 BDX1	O/Z	Serial data transmit output. BDX is placed in the high-impedance state when not transmitting, when $\overline{\text{RS}}$ is asserted or when $\overline{\text{OFF}}$ is low.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit output. The BFSX pulse initiates the transmit data process over $\overline{\text{BDX}}$. The BFSX pins are configured as inputs after reset. BFSX goes into the high-impedance state when $\overline{\text{OFF}}$ is low.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

Table 2−3. Signal Descriptions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
INTEGRATED DAA		
C1A	I/O	DAA I/O connection.
C1A5V	S	Dedicated 5.0V power supply for I/O pin C1A.
$\overline{\text{DAAEN}}$	I	DAA Enable Input. Enables the DAA when low.
UART		
TX	O	UART asynchronous serial transmit data output.
RX	I	UART asynchronous serial receive data input.
HOST PORT INTERFACE PINS		
A0−A15	I	These pins can be used to address internal memory via the HPI when the HPI16 pin is HIGH.
D0−D15	I/O	These pins can be used to read/write internal memory via the HPI when the HPI16 pin is high. The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when $\overline{\text{RS}}$ or $\overline{\text{HOLD}}$ is asserted. The data bus also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.
HD0−HD7	I/O/Z	Parallel bi-directional data bus. These pins can also be used as general-purpose I/O pins when the HPI16 pin is high. HD0−HD7 is placed in the high-impedance state when not outputting data or when $\overline{\text{OFF}}$ is low. The HPI data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. When the HPI data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The HPI data bus holders are disabled at reset, and can be enabled/disabled via the HBH bit of the BSCR.
HCNTL0 HCNTL1	I	Control inputs. These inputs select a host access to one of the three HPI registers. (Pullup only enabled when HPIENA=0, HPI16=1)
HBIL	I	Byte identification input. Identifies first or second byte of transfer. (Pullup only enabled when HPIENA=0, invalid when HPI16=1)
$\overline{\text{HCS}}$	I	Chip select input. This pin is the select input for the HPI, and must be driven low during accesses. (Pullup only enabled when HPIENA=0, or HPI16=1)
$\overline{\text{HDS1}}$ $\overline{\text{HDS2}}$	I	Data strobe inputs. These pins are driven by the host read and write strobes to control transfers. (Pullup only enabled when HPIENA=0)
$\overline{\text{HAS}}$	I	Address strobe input. Address strobe input. Hosts with multiplexed address and data pins require this input, to latch the address in the HPIA register. (Pull-up only enabled when HPIENA=0)
HR/$\overline{\text{W}}$	I	Read/write input. This input controls the direction of an HPI transfer. (Pullup only enabled when HPIENA=0)
HRDY	O/Z	Ready output. The ready output informs the host when the HPI is ready for the next transfer. HRDY goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{HINT}}$	O/Z	Interrupt output. This output is used to interrupt the host. When the DSP is in reset, this signal is driven high. $\overline{\text{HINT}}$ can also be used for timer 1 output (TOUT1), when the HPI is disabled. The signal goes into the high-impedance state when $\overline{\text{OFF}}$ is low. (invalid when HPI16=1)

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

Table 2−3. Signal Descriptions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
HOST PORT INTERFACE PINS (CONTINUED)		
HPIENA	I	HPI enable input. This pin must be driven high during reset to enable the HPI. An internal pulldown resistor is always active and the HPIENA pin is sampled on the rising edge of $\overline{RS}$. If HPIENA is left open or driven low during reset, the HPI module is disabled. Once the HPI is disabled, the HPIENA pin has no effect until the DSP is reset.
HPI16	I	HPI 16-bit Select Pin. HPI16=1 selects the non-multiplexed mode. The non-multiplexed mode allows hosts with separate address/data buses to access the HPI address range via the 16 address pins A0−A15. 16-bit Data is also accessible through pins D0−D15. HOST-to-DSP and DSP-to-HOST interrupts are not supported. There are no HPIC and HPIA registers in the non-multiplexed mode since there are HCNTRL0,1 signals available. Internally pulled low.
SUPPLY PINS		
CV_{DD}	S	$+V_{DD}$. Dedicated 1.5V power supply for the core CPU.
DV_{DD}	S	$+V_{DD}$. Dedicated 3.3V power supply for I/O pins.
V_{SS}	S	Ground.
TCK	I	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input, pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO also goes into the high-impedance state when $\overline{OFF}$ is low.
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{TRST}$‡	I	IEEE standard 1149.1 test reset. $\overline{TRST}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{TRST}$ is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator 0 pin. When $\overline{TRST}$ is driven low, EMU0 must be high for activation of the $\overline{OFF}$ condition. When $\overline{TRST}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system. Should be pulled up to DV_{DD} with a separate 4.7-kΩ resistor.
EMU1/$\overline{OFF}$	I/O/Z	Emulator 1 pin/disable all outputs. When $\overline{TRST}$ is driven high, EMU1/$\overline{OFF}$ is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system. When $\overline{TRST}$ is driven low, EMU1/$\overline{OFF}$ is configured as $\overline{OFF}$. The EMU1/$\overline{OFF}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{OFF}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Thus, for the $\overline{OFF}$ feature, the following conditions apply: $\overline{TRST}$=low, EMU0=high, EMU1/$\overline{OFF}$ = low. Should be pulled up to DV_{DD} with a separate 4.7-kΩ resistor.

† I = Input, O = Output, Z = High-impedance, S = Supply

‡ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

3 Functional Overview

The following functional overview is based on the block diagram in Figure 3−1.

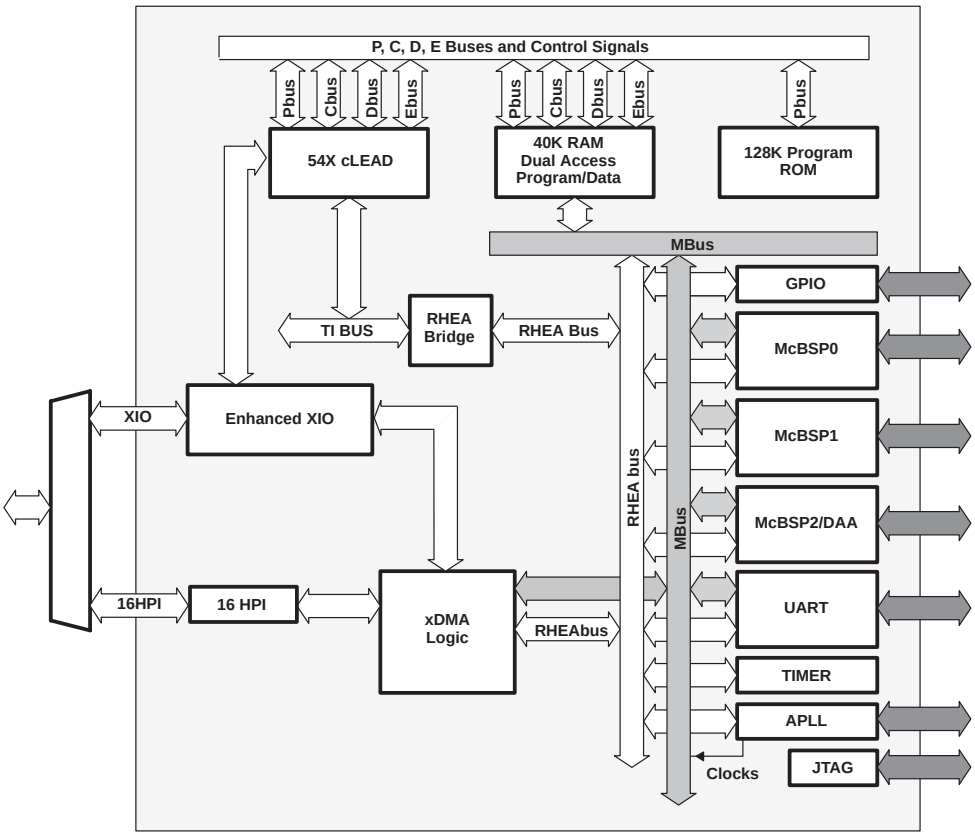


Figure 3−1. TMS320C54CST Functional Block Diagram

3.1 Memory

The 54CST device provides both on-chip ROM and RAM memories to aid in system performance and integration.

3.1.1 Data Memory

The data memory space addresses up to 64K of 16-bit words. The device automatically accesses the on-chip RAM when addressing within its bounds. When an address is generated outside the RAM bounds, the device automatically generates an external access.

The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Higher performance because of better flow within the pipeline of the central arithmetic logic unit (CALU)
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

3.1.2 Program Memory

Software can configure their memory cells to reside inside or outside of the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the program-address generation (PAGEN) logic generates an address outside its bounds, the device automatically generates an external access. The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

3.1.3 Extended Program Memory

The 54CST uses a paged extended memory scheme in program space to allow access of up to 8192K of program memory. In order to implement this scheme, the 54CST includes several features which are also present on C548/549/5410:

- Twenty-three address lines, instead of sixteen
- An extra memory-mapped register, the XPC
- Six extra instructions for addressing extended program space

Program memory in the 54CST is organized into 128 pages that are each 64K in length.

The value of the XPC register defines the page selection. This register is memory-mapped into data space to address 001Eh. At a hardware reset, the XPC is initialized to 0.

3.2 On-Chip ROM With Bootloader and Client Side Telephony Algorithms

The 54CST features a 128K-word $\times$ 16-bit on-chip maskable ROM that is mapped into program memory space.

The 54CST on-chip ROM contains a flexible bootloader program, 14 eXpressDSP-compliant telephony alogrithms, and an eXpressDSP-compliant telephony framework.

The bootloader can be used to automatically transfer user code from an external source to anywhere in the program memory at power up. If MP/$\overline{\text{MC}}$ of the device is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the bootloader program.

The standard 54CST devices provide different ways to download the code to accommodate various system requirements:

- Parallel from 8-bit or 16-bit-wide EPROM
- Parallel from I/O space, 8-bit or 16-bit mode
- Serial boot from serial ports, 8-bit or 16-bit mode
- UART boot mode
- Host-port interface boot
- Client side telephony chipset boot
- Warm boot

For additional information about the 54CST bootloader, see *TMS320C54CST Bootloader Technical Reference* (literature number SPRA853).

The eXpressDSP-compliant telephony algorithms in the on-chip ROM can be used in either chipset mode (initiated through the bootloader), where the implemented functions are controlled through external user commands, or in flex mode, where these algorithms can be called from user code residing anywhere in memory. For complete information regarding the use of these algorithms, see the *Client Side Telephony (CST) Chip Software User's Guide* (literature number SPRU029).

The telephony algorithms included in the ROM are the following:

- **Modem Algorithms**
  - V.32bis/V.22bis (up to 14.4 kbps)
  - V.42 error correction
    - Embedded V.42bis compression
  - Modem Integrator
    - Embedded V.14 async-to-sync conversion
- **Telephony Algorithms**
  - UMTG/UMTD (Universal multifrequency tone generator/detector)
    - DTMF generation/detection
    - Call Progress Tone generation/detection
  - Caller ID types 1 and 2
- **Voice Algorithms**
  - G.168 line echo cancellation
  - G.726 ACPCM compression (16−40 kbps)
    - Embedded G.711 PCM
  - Automatic Gain Control (AGC)
  - Voice Activity Detection (VAD)
  - Comfort Noise Generation (CNG)

3.3 On-Chip RAM

The 54CST device contains 40K-words x 16-bit of DARAM.

The DARAM is composed of five blocks of 8K words each. Each block in the DARAM can support two reads in one cycle, or a read and a write in one cycle. The five blocks of DARAM on the 54CST are located in the address range 0080h−9FFFh in data space and can be mapped in program/data space by setting the OVLY bit to one.

3.4 On-Chip Memory Security

The 54CST device provides maskable options to protect the contents of on-chip memories. When the ROM protect option is selected, no externally originating instruction can access the on-chip ROM; when the RAM protect option is selected, HPI RAM is protected; HPI writes are not restricted, but HPI reads are restricted to 2000h − 3FFFh.

3.5 Memory Map

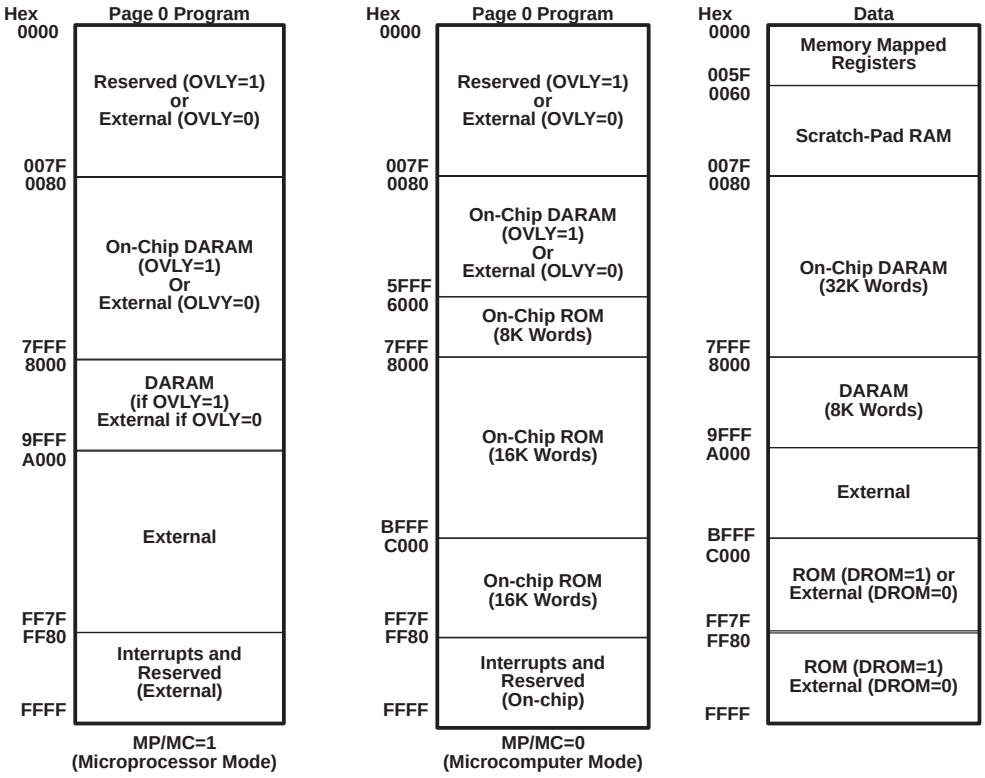
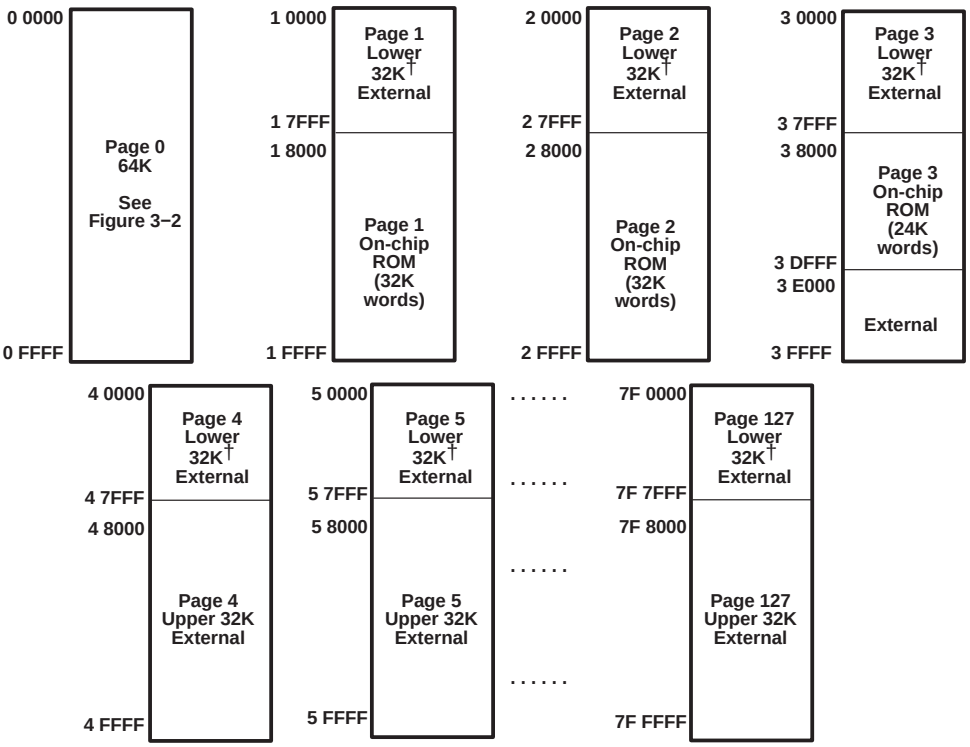


Figure 3−2. Program and Data Memory Map



† The lower 32 K words of pages 1 through 127 are only available when the OVLY bit is cleared to 0. If the OVLY bit is set to 1, the on-chip memory is mapped to the lower 32 K words of all program space pages.

Figure 3−3. Extended Program Memory Map

3.5.1 Relocatable Interrupt Vector Table

The reset, interrupt, and trap vectors are addressed in program space. These vectors are soft — meaning that the processor, when taking the trap, loads the program counter (PC) with the trap address and executes the code at the vector location. Four words, either two 1-word instructions or one 2-word instruction, are reserved at each vector location to accommodate a delayed branch instruction which allows branching to the appropriate interrupt service routine without the overhead.

At device reset, the reset, interrupt, and trap vectors are mapped to address FF80h in program space. However, these vectors can be remapped to the beginning of any 128-word page in program space after device reset. This is done by loading the interrupt vector pointer (IPTR) bits in the PMST register with the appropriate 128-word page boundary address. After loading IPTR, any user interrupt or trap vector is mapped to the new 128-word page.

NOTE: The hardware reset ($\overline{RS}$) vector cannot be remapped because the hardware reset loads the IPTR with 1s. Therefore, the reset vector is always fetched at location FF80h in program space.

15							8
IPTR							
R/W-1FF							

7	6	5	4	3	2	1	0
IPTR	MP/$\overline{MC}$	OVLY	AVIS	DROM	CLKOFF	SMUL	SST
R	MP/$\overline{MC}$ Pin	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read, W = Write

Figure 3−4. Processor Mode Status (PMST) Register

Table 3−1. Processor Mode Status (PMST) Register Bit Fields

BIT NO.	BIT NAME	RESET VALUE	DESCRIPTION
15−7	IPTR	1FFh	Interrupt vector pointer. The 9-bit IPTR field points to the 128-word program page where the interrupt vectors reside. The interrupt vectors can be remapped to RAM for boot-loaded operations. At reset, these bits are all set to 1; the reset vector always resides at address FF80h in program memory space. The RESET instruction does not affect this field.
6	MP/$\overline{MC}$	MP/$\overline{MC}$ pin	Microprocessor/microcomputer mode. MP/$\overline{MC}$ enables/disables the on-chip ROM to be addressable in program memory space. ❑ MP/$\overline{MC}$ = 0: The on-chip ROM is enabled and addressable. ❑ MP/$\overline{MC}$ = 1: The on-chip ROM is not available. MP/$\overline{MC}$ is set to the value corresponding to the logic level on the MP/$\overline{MC}$ pin when sampled at reset. This pin is not sampled again until the next reset. The RESET instruction does not affect this bit. This bit can also be set or cleared by software.
5	OVLY	0	RAM overlay. OVLY enables on-chip dual-access data RAM blocks to be mapped into program space. The values for the OVLY bit are: ❑ OVLY = 0: The on-chip RAM is addressable in data space but not in program space. ❑ OVLY = 1: The on-chip RAM is mapped into program space and data space. Data page 0 (addresses 0h to 7Fh), however, is not mapped into program space.
4	AVIS	0	Address visibility mode. AVIS enables/disables the internal program address to be visible at the address pins. ❑ AVIS = 0: The external address lines do not change with the internal program address. Control and data lines are not affected and the address bus is driven with the last address on the bus. ❑ AVIS = 1: This mode allows the internal program address to appear at the pins of the 54CST so that the internal program address can be traced. Also, it allows the interrupt vector to be decoded in conjunction with $\overline{IACK}$ when the interrupt vectors reside on on-chip memory.
3	DROM	0	Data ROM. DROM enables on-chip ROM to be mapped into data space. The DROM bit values are: ❑ DROM = 0: The on-chip ROM is not mapped into data space. ❑ DROM = 1: A portion of the on-chip ROM is not mapped into data space. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
2	CLKOFF	0	CLOCKOUT off. When the CLKOFF bit is 1, the output of CLKOUT is disabled and remains at a high level.

Table 3−1. Processor Mode Status (PMST) Register Bit Fields (Continued)

BIT NO.	BIT NAME	RESET VALUE	DESCRIPTION
1	SMUL	N/A	Saturation on multiplication. When SMUL = 1, saturation of a multiplication result occurs before performing the accumulation in a MAC of MAS instruction. The SMUL bit applies only when OVM = 1 and FRCT = 1.
0	SST	N/A	Saturation on store. When SST = 1, saturation of the data from the accumulator is enabled before storing in memory. The saturation is performed after the shift operation.

3.6 On-Chip Peripherals

The 54CST device has the following peripherals:

- Software-programmable wait-state generator
- Programmable bank-switching
- A host-port interface (HPI8/16)
- Three multichannel buffered serial ports (McBSPs)
- Two hardware timers
- A clock generator with a multiple phase-locked loop (PLL)
- Enhanced external parallel interface (XIO2)
- A DMA controller (DMA)
- A UART with an integrated baud rate generator
- An integrated DAA module

3.6.1 Software-Programmable Wait-State Generator

The software wait-state generator of the 54CST can extend external bus cycles by up to fourteen machine cycles. Devices that require more than fourteen wait states can be interfaced using the hardware READY line. When all external accesses are configured for zero wait states, the internal clocks to the wait-state generator are automatically disabled. Disabling the wait-state generator clocks reduces the power consumption of the 54CST.

The software wait-state register (SWWSR) controls the operation of the wait-state generator. The 14 LSBs of the SWWSR specify the number of wait states (0 to 7) to be inserted for external memory accesses to five separate address ranges. This allows a different number of wait states for each of the five address ranges. Additionally, the software wait-state multiplier (SWSM) bit of the software wait-state control register (SWCR) defines a multiplication factor of 1 or 2 for the number of wait states. At reset, the wait-state generator is initialized to provide seven wait states on all external memory accesses. The SWWSR bit fields are shown in Figure 3−5 and described in Table 3−2.

15	14	12	11	9	8
XPA	I/O		DATA		DATA
R/W-0	R/W-111		R/W-111		

6	5	3	2	0
DATA	PROGRAM		PROGRAM	
R/W-111	R/W-111		R/W-111	

LEGEND: R = Read, W = Write, 0 = Value after reset

Figure 3−5. Software Wait-State Register (SWWSR) [Memory-Mapped Register (MMR) Address 0028h]

Table 3−2. Software Wait-State Register (SWWSR) Bit Descriptions

BIT NO.	BIT NAME	RESET VALUE	DESCRIPTION
15	XPA	0	Extended program address control bit. XPA is used in conjunction with the program space fields (bits 0 through 5) to select the address range for program space wait states.
14−12	I/O	111	I/O space. The field value (0−7) corresponds to the base number of wait states for I/O space accesses within addresses 0000−FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
11−9	Data	111	Upper data space. The field value (0−7) corresponds to the base number of wait states for external data space accesses within addresses 8000−FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
8−6	Data	111	Lower data space. The field value (0−7) corresponds to the base number of wait states for external data space accesses within addresses 0000−7FFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
5−3	Program	111	Upper program space. The field value (0−7) corresponds to the base number of wait states for external program space accesses within the following addresses: ❑ XPA = 0: xx8000 − xxFFFFh ❑ XPA = 1: 400000h − 7FFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
2−0	Program	111	Lower program space. The field value (0−7) corresponds to the base number of wait states for external program space accesses within the following addresses: ❑ XPA = 0: xx0000 − xx7FFFh ❑ XPA = 1: 000000 − 3FFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.

The software wait-state multiplier bit of the software wait-state control register (SWCR) is used to extend the base number of wait states selected by the SWWSR. The SWCR bit fields are shown in Figure 3−6 and described in Table 3−3.

15	8
Reserved	
R/W-0	

7	1	0
Reserved		SWSM
R/W-0		R/W-0

LEGEND: R = Read, W = Write, 0 = Value after reset

Figure 3−6. Software Wait-State Control Register (SWCR) [MMR Address 002Bh]

Table 3−3. Software Wait-State Control Register (SWCR) Bit Descriptions

PIN NO.	PIN NAME	RESET VALUE	DESCRIPTION
15−1	Reserved	0	These bits are reserved and are unaffected by writes.
0	SWSM	0	Software wait-state multiplier. Used to multiply the number of wait states defined in the SWWSR by a factor of 1 or 2. ❑ SWSM = 0: wait-state base values are unchanged (multiplied by 1). ❑ SWSM = 1: wait-state base values are multiplied by 2 for a maximum of 14 wait states.

3.6.2 Programmable Bank-Switching

Programmable bank-switching logic allows the 54CST to switch between external memory banks without requiring external wait states for memories that need additional time to turn off. The bank-switching logic automatically inserts one cycle when accesses cross a 32K-word memory-bank boundary inside program or data space.

Bank-switching is defined by the bank-switching control register (BSCR), which is memory-mapped at address 0029h. The bit fields of the BSCR are shown in Figure 3−7 and are described in Table 3−4.

15	14	13	12	11	8
$\overline{\text{CONSEC}}$	DIVFCT		IACKOFF	Reserved	
R/W-1	R/W-11		R/W-1	R	

7	5	4	3	2	1	0
Reserved		$\overline{\text{DAARST}}$	DAACLKDV	HBH	BH	Reserved
R		R/W-0	R/W-0	R/W-0	R/W-0	R

LEGEND: R = Read, W = Write

Figure 3−7. Bank-Switching Control Register (BSCR) [MMR Address 0029h]

Table 3−4. Bank-Switching Control Register (BSCR) Bit Descriptions

BIT	NAME	RESET VALUE	DESCRIPTION
15	$\overline{\text{CONSEC}}$†	1	Consecutive bank-switching**.** Specifies the bank-switching mode. $\overline{\text{CONSEC}}$ = 0: Bank-switching on 32K bank boundaries only. This bit is cleared if fast access is desired for continuous memory reads (i.e., no starting and trailing cycles between read cycles). $\overline{\text{CONSEC}}$ = 1: Consecutive bank switches on external memory reads. Each read cycle consists of 3 cycles: starting cycle, read cycle, and trailing cycle.
13−14	DIVFCT	11	CLKOUT output divide factor**.** The CLKOUT output is driven by an on-chip source having a frequency equal to 1/(DIVFCT+1) of the DSP clock. DIVFCT = 00: CLKOUT is not divided. DIVFCT = 01: CLKOUT is divided by 2 from the DSP clock. DIVFCT = 10: CLKOUT is divided by 3 from the DSP clock. DIVFCT = 11: CLKOUT is divided by 4 from the DSP clock (default value following reset).
12	IACKOFF	1	$\overline{\text{IACK}}$ signal output off**.** Controls the output of the $\overline{\text{IACK}}$ signal. IACKOFF is set to 1 at reset. IACKOFF = 0: The $\overline{\text{IACK}}$ signal output off function is disabled. IACKOFF = 1: The $\overline{\text{IACK}}$ signal output off function is enabled.
11−5	Rsvd	−	Reserved
4	$\overline{\text{DAARST}}$	0	DAA reset (low true). When low, resets DAA.
3	DAACLKDV	0	DAA clock divide ratio control bit. Selects divide ratio of clock sent to DAA. DAACLKDV = 0: the DAA is clocked at the same rate as the CPU DAACLKDV = 1: the DAA is clocked at half the rate of the CPU
2	HBH	0	HPI bus holder. Controls the HPI bus holder. HBH is cleared to 0 at reset**.** HBH = 0: The bus holder is disabled except when HPI16=1. HBH = 1: The bus holder is enabled. When not driven, the HPI data bus, HD[7:0] is held in the previous logic level.
1	BH	0	Bus holder. Controls the bus holder. BH is cleared to 0 at reset. BH = 0: The bus holder is disabled. BH = 1: The bus holder is enabled. When not driven, the data bus, D[15:0] is held in the previous logic level.
0	Rsvd	−	Reserved

† For additional information, see Section 3.11 of this document.

The 54CST has an internal register that holds the MSB of the last address used for a read or write operation in program or data space. In the non-consecutive bank switches ($\overline{\text{CONSEC}}$ = 0), if the MSB of the address used for the current read does not match that contained in this internal register, the $\overline{\text{MSTRB}}$ (memory strobe) signal is not asserted for one CLKOUT cycle. During this extra cycle, the address bus switches to the new address. The contents of the internal register are replaced with the MSB for the read of the current address. If the MSB of the address used for the current read matches the bits in the register, a normal read cycle occurs.

In non-consecutive bank switches ($\overline{\text{CONSEC}}$ = 0), if repeated reads are performed from the same memory bank, no extra cycles are inserted. When a read is performed from a different memory bank, memory conflicts are avoided by inserting an extra cycle. For more information, see Section 3.11 of this document.

The bank-switching mechanism automatically inserts one extra cycle in the following cases:

- A memory read followed by another memory read from a different memory bank.
- A program-memory read followed by a data-memory read.
- A data-memory read followed by a program-memory read.
- A program-memory read followed by another program-memory read from a different page.

3.6.3 Bus Holders

The 54CST has two bus holder control bits, BH (BSCR[1]) and HBH (BSCR[2]), to control the bus keepers of the address bus (A[17−0]), data bus (D[15−0]), and the HPI data bus (HD[7−0]). Bus keeper enabling/disabling is described in Table 3−4.

Table 3−5. Bus Holder Control Bits

HPI16 PIN	BH	HBH	D[15−0]	A[17−0]	HD[7−0]
0	0	0	OFF	OFF	OFF
0	0	1	OFF	OFF	ON
0	1	0	ON	OFF	OFF
0	1	1	ON	OFF	ON
1	0	0	OFF	OFF	ON
1	0	1	OFF	ON	ON
1	1	0	ON	OFF	ON
1	1	1	ON	ON	ON

3.7 Parallel I/O Ports

The 54CST has a total of 64K I/O ports. These ports can be addressed by the PORTR instruction or the PORTW instruction. The $\overline{IS}$ signal indicates a read/write operation through an I/O port. The 54CST can interface easily with external devices through the I/O ports while requiring minimal off-chip address-decoding circuits.

3.7.1 Enhanced 8-/16-Bit Host-Port Interface (HPI8/16)

The 54CST host-port interface, also referred to as the HPI8/16, is an enhanced version of the standard 8-bit HPI found on earlier TMS320C54x™ DSPs (542, 545, 548, and 549). The 54CST HPI can be used to interface to an 8-bit or 16-bit host. When the address and data buses for external I/O is not used (to interface to external devices in program/data/IO spaces), the 54CST HPI can be configured as an HPI16 to interface to a 16-bit host. This configuration can be accomplished by connecting the HPI16 pin to logic “1”.

When the HPI16 pin is connected to a logic “0”, the 54CST HPI is configured as an HPI8. The HPI8 is an 8-bit parallel port for interprocessor communication. The features of the HPI8 include:

Standard features:

- Sequential transfers (with autoincrement) or random-access transfers
- Host interrupt and C54x™ interrupt capability
- Multiple data strobes and control pins for interface flexibility

The HPI8 interface consists of an 8-bit bidirectional data bus and various control signals. Sixteen-bit transfers are accomplished in two parts with the HBIL input designating high or low byte. The host communicates with the HPI8 through three dedicated registers — the HPI address register (HPIA), the HPI data register (HPID), and the HPI control register (HPIC). The HPIA and HPID registers are only accessible by the host, and the HPIC register is accessible by both the host and the 54CST.

Enhanced features:

- Access to entire on-chip RAM through DMA bus
- Capability to continue transferring during emulation stop

The HPI16 is an enhanced 16-bit version of the TMS320C54x™ DSP 8-bit host-port interface (HPI8). The HPI16 is designed to allow a 16-bit host to access the DSP on-chip memory, with the host acting as the master of the interface. Some of the features of the HPI16 include:

- 16-bit bidirectional data bus
- Multiple data strobes and control signals to allow glueless interfacing to a variety of hosts
- Only nonmultiplexed address/data modes are supported
- 18-bit address bus used in nonmultiplexed mode to allow access to all internal memory (including internal extended address pages)
- HRDY signal to hold off host accesses due to DMA latency
- The HPI16 acts as a slave to a 16-bit host processor and allows access to the on-chip memory of the DSP.

  NOTE: Only the nonmultiplexed mode is supported when the 54CST HPI is configured as a HPI16 (see Figure 3−8).

The 54CST HPI functions as a slave and enables the host processor to access the on-chip memory. A major enhancement to the 54CST HPI over previous versions is that it allows host access to the entire on-chip memory range of the DSP. The host and the DSP both have access to the on-chip RAM at all times and host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one cycle. Note that since host accesses are always synchronized to the 54CST clock, an active input clock (CLKIN) is required for HPI accesses during IDLE states, and host accesses are not allowed while the 54CST reset pin is asserted.

3.7.2 HPI Nonmultiplexed Mode

In *nonmultiplexed* mode, a host with separate address/data buses can access the HPI16 data register (HPID) via the HD 16-bit bidirectional data bus, and the address register (HPIA) via the 23-bit HA address bus. The host initiates the access with the strobe signals ($\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, $\overline{\text{HCS}}$) and controls the direction of the access with the HR/$\overline{\text{W}}$ signal. The HPI16 can stall host accesses via the HRDY signal. Note that the HPIC register is not available in *nonmultiplexed* mode since there are no HCNTL signals available. All host accesses initiate a DMA read or write access. Figure 3−8 shows a block diagram of the HPI16 in *nonmultiplexed* mode.

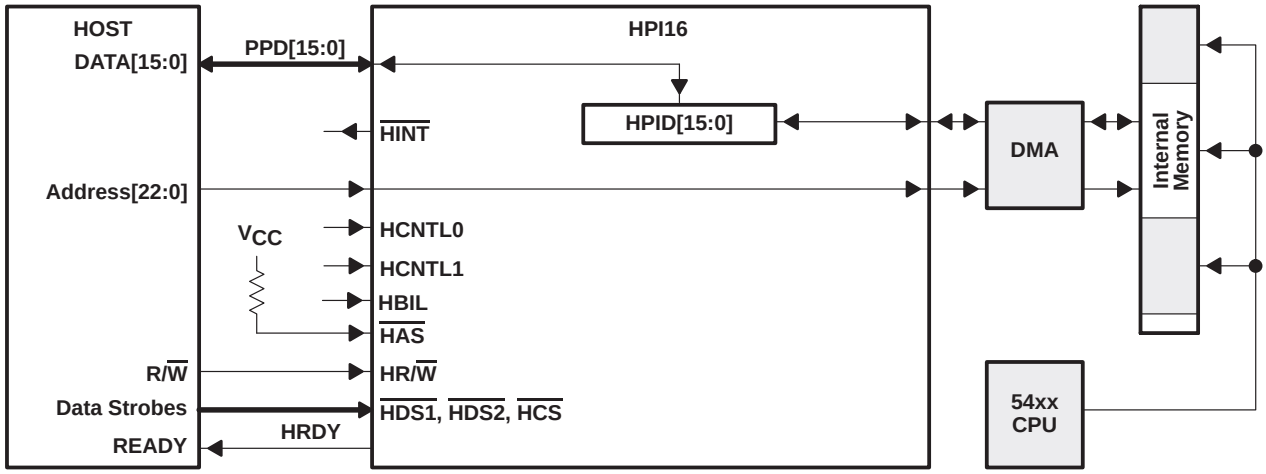


Figure 3−8. Host-Port Interface — Nonmultiplexed Mode

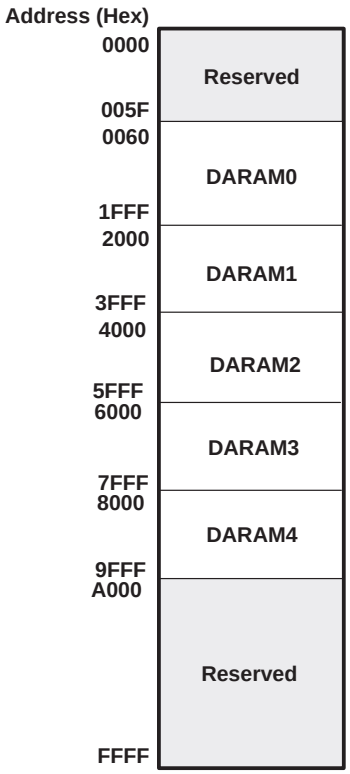


Figure 3−9. HPI Memory Map

3.8 Multichannel Buffered Serial Ports (McBSPs)

The 54CST device provides three high-speed, full-duplex, multichannel buffered serial ports that allow direct interface to other C54x/LC54x devices, codecs, and other devices in a system. The McBSPs are based on the standard serial-port interface found on other 54x devices. Like their predecessors, the McBSPs provide:

- Full-duplex communication
- Double-buffer data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSPs have the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching compatible and ST-BUS compliant devices
  - IOM-2 compliant devices
  - AC97-compliant devices
  - IIS-compliant devices
  - Serial peripheral interface
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes, including 8, 12, 16, 20, 24, or 32 bits
- μ-law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

The McBSP consists of a data path and control path. The six pins, BDX, BDR, BFSX, BFSR, BCLKX, and BCLKR, connect the control and data paths to external devices. The implemented pins can be programmed as general-purpose I/O pins if they are not used for serial communication. Note that on McBSP2, the transmit and receive clocks and the transmit and recieve frame sync have been combined. Also, McBSP2 is dedicated to the DAA module and is not available externally with the exception of the BFSRX2 pin.

The data is communicated to devices interfacing to the McBSP by way of the data transmit (BDX) pin for transmit and the data receive (BDR) pin for receive. The CPU or DMA reads the received data from the data receive register (DRR) and writes the data to be transmitted to the data transmit register (DXR). Data written to the DXR is shifted out to BDX by way of the transmit shift register (XSR). Similarly, receive data on the BDR pin is shifted into the receive shift register (RSR) and copied into the receive buffer register (RBR). RBR is then copied to DRR, which can be read by the CPU or DMA. This allows internal data movement and external data communications simultaneously.

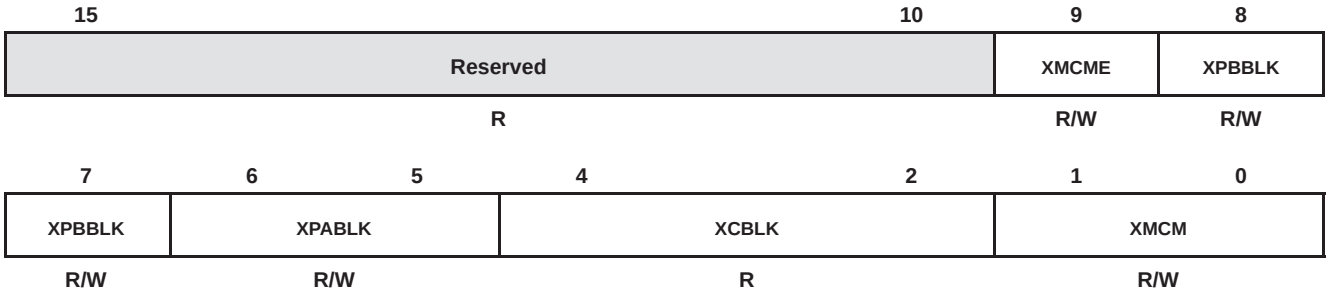
Control information in the form of clocking and frame synchronization is communicated by way of BCLKX, BCLKR, BFSX, and BFSR. The device communicates to the McBSP by way of 16-bit-wide control registers accessible via the internal peripheral bus.

The control block consists of internal clock generation, frame synchronization signal generation, and their control, and multichannel selection. This control block sends notification of important events to the CPU and DMA by way of two interrupt signals, XINT and RINT, and two event signals, XEVT and REVT.

The on-chip companding hardware allows compression and expansion of data in either μ-law or A-law format. When companding is used, transmitted data is encoded according to the specified companding law and received data is decoded to 2s complement format.

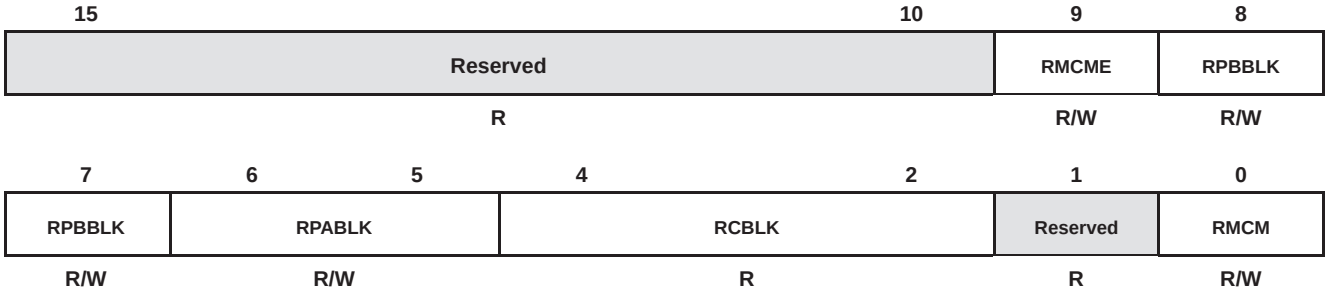
The sample rate generator provides the McBSP with several means of selecting clocking and framing for both the receiver and transmitter. Both the receiver and transmitter can select clocking and framing independently.

The McBSP allows the multiple channels to be independently selected for the transmitter and receiver. When multiple channels are selected, each frame represents a time-division multiplexed (TDM) data stream. In using time-division multiplexed data streams, the CPU may only need to process a few of them. Thus, to save memory and bus bandwidth, multichannel selection allows independent enabling of particular channels for transmission and reception. All 128 channels in a bit stream consisting of a maximum of 128 channels can be enabled.



LEGEND: R = Read, W = Write, 0 = Value after reset

Figure 3−10. Multichannel Control Register (MCR1)



LEGEND: R = Read, W = Write, 0 = Value after reset

Figure 3−11. Multichannel Control Register (MCR2)

The 54CST McBSP has two working modes:

- In the first mode, when (R/X)MCME = 0, it is comparable with the McBSPs used in the 5410 where the normal 32-channel selection is enabled (default).
- In the second mode, when (R/X)MCME = 1, it has 128-channel selection capability. Multichannel control register Bit 9, (R/X)MCME, is used as the 128-channel selection enable bit. Once (R/X)MCME = 1, twelve new registers ((R/X)CERC − (R/X)CERH) are used to enable the 128-channel selection.

The clock stop mode (CLKSTP) in the McBSP provides compatibility with the serial port interface protocol. Clock stop mode works with only single-phase frames and one word per frame. The word sizes supported by the McBSP are programmable for 8-, 12-, 16-, 20-, 24-, or 32-bit operation. When the McBSP is configured to operate in SPI mode, both the transmitter and the receiver operate together as a master or as a slave.

Although the BCLKS pin is not available on the 54CST PGE and GGU packages, the 54CST is capable of synchronization to external clock sources. BCLKX or BCLKR can be used by the sample rate generator for external synchronization. The sample rate clock mode extended (SCLKME) bit field is located in the PCR to accommodate this option.

15	14	13	12	11	10	9	8
Reserved		XIOEN	RIOEN	FSXM	FSRM	CLKXM	CLKRM
RW		RW	RW	RW	RW	RW	RW

7	6	5	4	3	2	1	0
SCLKME	CLKS STAT	DX STAT	DR STAT	FSXP	FSRP	CLKXP	CLKRP
RW	RW	RW	RW	RW	RW	RW	RW

Legend: R = Read, W = Write

Figure 3−12. Pin Control Register (PCR)

The selection of sample rate input clock is made by the combination of the CLKSM (bit 13 in SRGR2) bit value and the SCLKME bit value as shown in Table 3−6.

Table 3−6. Sample Rate Input Clock Selection

SCLKME	CLKSM	SAMPLE RATE CLOCK MODE
0	0	Reserved (CLKS pin unavailable)
0	1	CPU clock
1	0	BCLKR
1	1	BCLKX

When the SCLKME bit is cleared to 0, the CLKSM bit is used, as before, to select either the CPU clock or the CLKS pin (not bonded out on the 54CST device package) as the sample rate input clock. Setting the SCLKME bit to 1 enables the CLKSM bit to select between the BCLKR pin or BCLKX pin for the sample rate input clock.

When either the BCLKR or CLKX is configured this way, the output buffer for the selected pin is automatically disabled. For example, with SCLKME = 1 and CLKSM = 0, the BCLKR pin is configured as the input of the sample rate generator. Both the transmitter and receiver circuits can be synchronized to the sample rate generator output by setting the CLKXM and CLKRM bits of the pin configuration register (PCR) to 1. Note that the sample rate generator output will only be driven on the BCLKX pin since the BCLKR output buffer is automatically disabled.

The McBSP is fully static and operates at arbitrary low clock frequencies. For maximum operating frequency, see Section 5.12.

3.9 Hardware Timers

The 54CST device features two 16-bit timing circuits with 4-bit prescalers. The timer counters are decremented by one every CLKOUT cycle. Each time the counter decrements to 0, a timer interrupt is generated. The timer can be stopped, restarted, reset, or disabled by specific status bits.

Both timers can be use to generate interrupts to the CPU, however, the second timer (Timer1) has its interrupt combined with external interrupt 3 ($\overline{\text{INT3}}$) in the interrupt flag register. Therefore, to use the Timer1 interrupt, the $\overline{\text{INT3}}$ input should be disabled (tied high), and to use the $\overline{\text{INT3}}$ input, the timer should be disabled (placed in reset).

3.10 Clock Generator

The clock generator provides clocks to the 54CST device, and consists of a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided from an external clock source. The reference clock input is then divided by two (DIV mode) to generate clocks for the 54CST device, or the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU. The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. Then, other internal clock circuitry allows the synthesis of new clock frequencies for use as master clock for the 54CST device.

This clock generator allows system designers to select the clock source. The external clock source is directly connected to the X2/CLKIN pin, and X1 is left unconnected.

The software-programmable PLL features a high level of flexibility, and includes a clock scaler that provides various clock multiplier ratios, capability to directly enable and disable the PLL, and a PLL lock timer that can be used to delay switching to PLL clocking mode of the device until lock is achieved. Devices that have a built-in software-programmable PLL can be configured in one of two clock modes:

- PLL mode. The input clock (X2/CLKIN) is multiplied by 1 of 31 possible ratios.
- DIV (divider) mode. The input clock is divided by 2 or 4. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

The software-programmable PLL is controlled using the 16-bit memory-mapped (address 0058h) clock mode register (CLKMD). The CLKMD register is used to define the clock configuration of the PLL clock module. Note that upon reset, the CLKMD register is initialized with a predetermined value dependent only upon the state of the CLKMD1 − CLKMD3 pins. For more programming information, see the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131). The CLKMD pin configured clock options are shown in Table 3−7.

Table 3−7. Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE†
0	0	0	0000h	1/2 (PLL and oscillator disabled)
0	0	1	9007h	PLL x 10
0	1	0	4007h	PLL x 5
1	0	0	1007h	PLL x 2
1	1	0	F007h	PLL x 1
1	0	1	F000h	1/4 (PLL disabled)
1	1	1	0000h	1/2 (PLL disabled)
0	1	1	—	Reserved

† The external CLKMD1−CLKMD3 pins are sampled to determine the desired clock generation mode while $\overline{RS}$ is low. Following reset, the clock generation mode can be reconfigured by writing to the internal clock mode register in software.

3.11 Enhanced External Parallel Interface (XIO2)

The 54CST external interface has been redesigned to include several improvements, including: simplification of the bus sequence, more immunity to bus contention when transitioning between read and write operations, the ability for external memory access to the DMA controller, and optimization of the power-down modes.

The bus sequence on the 54CST still maintains all of the same interface signals as on previous 54x devices, but the signal sequence has been simplified. Most external accesses now require 3 cycles composed of a leading cycle, an active (read or write) cycle, and a trailing cycle. The leading and trailing cycles provide additional immunity against bus contention when switching between read operations and write operations. To maintain high-speed read access, a consecutive read mode that performs single-cycle reads as on previous 54x devices is available.

Figure 3−13 shows the bus sequence for three cases: all I/O reads, memory reads in nonconsecutive mode, or single memory reads in consecutive mode. The accesses shown in Figure 3−13 always require 3 CLKOUT cycles to complete.

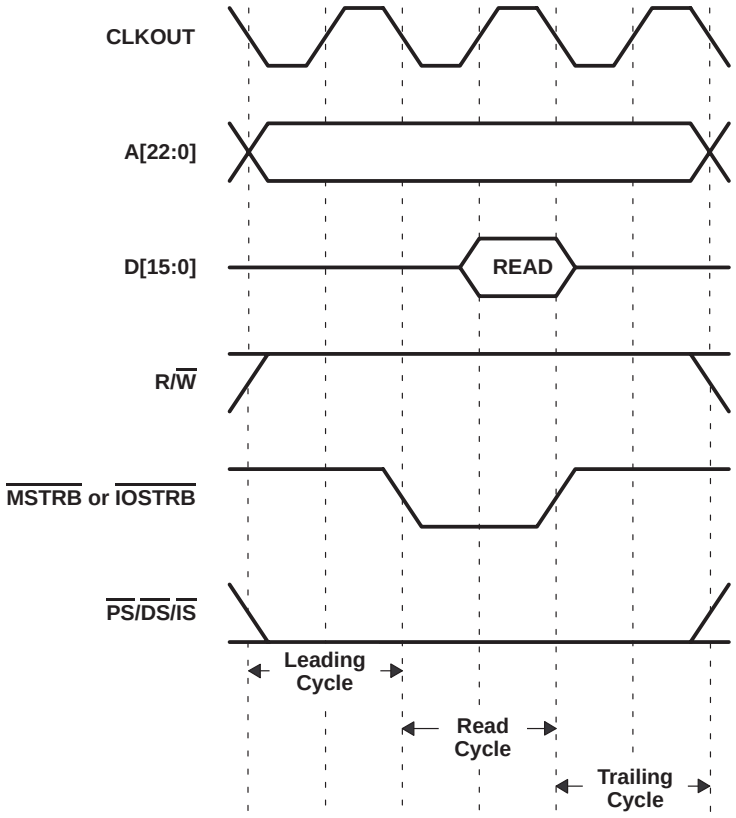


Figure 3−13. Nonconsecutive Memory Read and I/O Read Bus Sequence

Figure 3−14 shows the bus sequence for repeated memory reads in consecutive mode. The accesses shown in Figure 3−14 require (2+n) CLKOUT cycles to complete, where n is the number of consecutive reads performed.

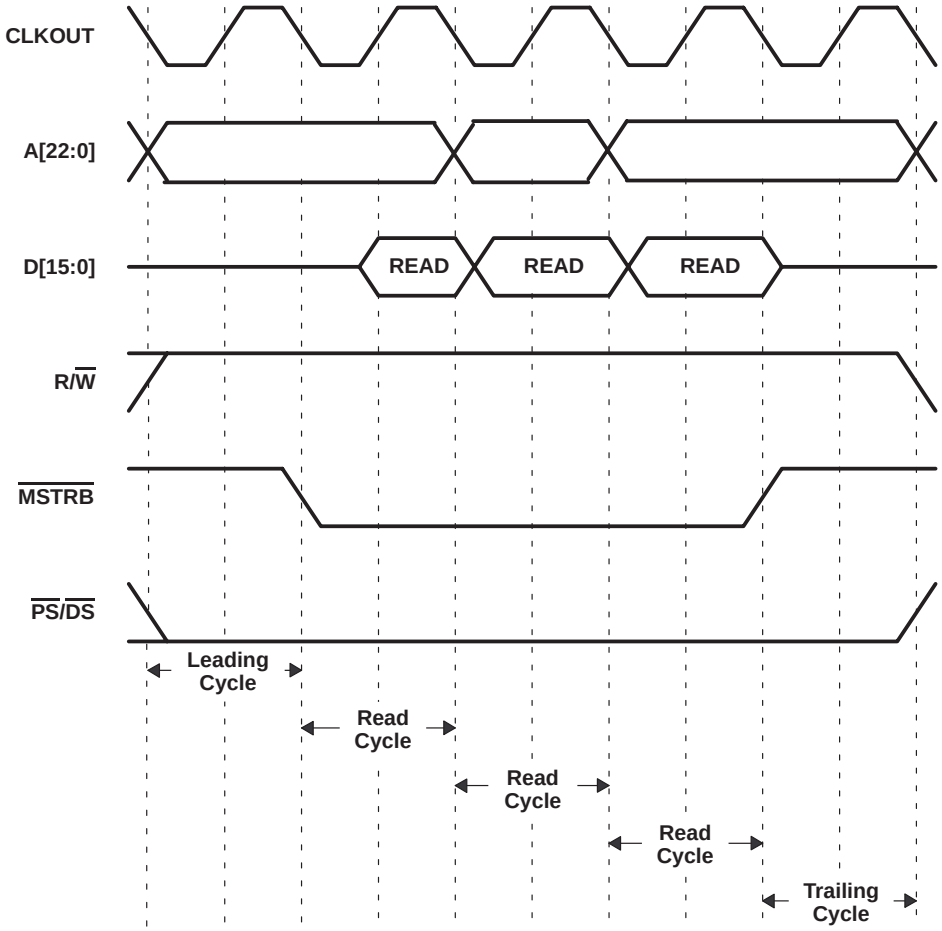


Figure 3−14. Consecutive Memory Read Bus Sequence (n = 3 reads)

Figure 3−15 shows the bus sequence for all memory writes and I/O writes. The accesses shown in Figure 3−15 always require 3 CLKOUT cycles to complete.

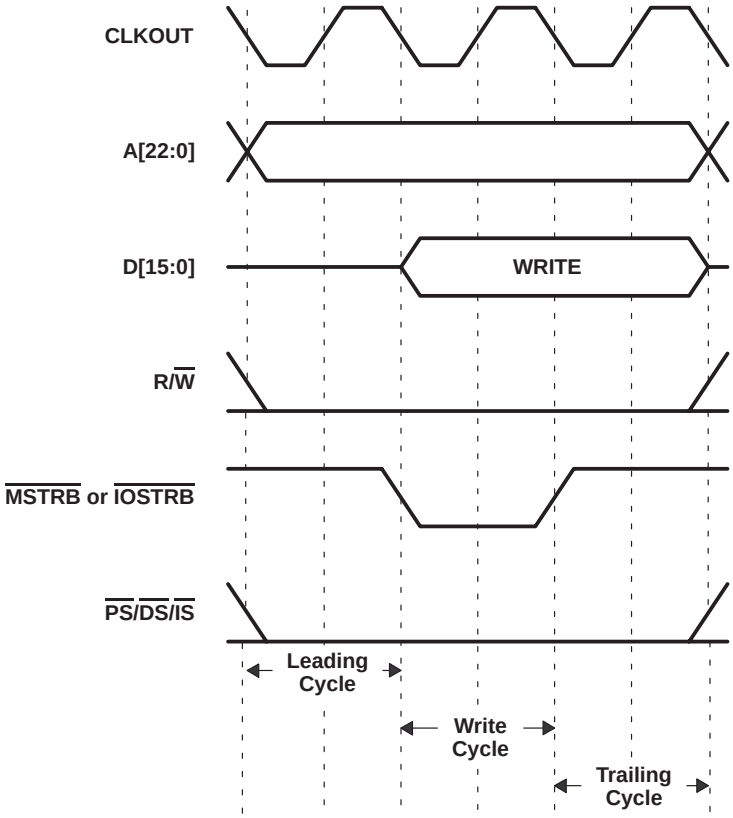


Figure 3−15. Memory Write and I/O Write Bus Sequence

The enhanced interface also provides the ability for DMA transfers to extend to external memory. For more information on DMA capability, see the DMA sections that follow.

The enhanced interface improves the low-power performance already present on the TMS320C5000™ DSP platform by switching off the internal clocks to the interface when it is not being used. This power-saving feature is automatic, requires no software setup, and causes no latency in the operation of the interface.

Additional features integrated in the enhanced interface are the ability to automatically insert bank-switching cycles when crossing 32K memory boundaries (see Section 3.6.2), the ability to program up to 14 wait states through software (see Section 3.6.1), and the ability to divide down CLKOUT by a factor of 1, 2, 3, or 4. Dividing down CLKOUT provides an alternative to wait states when interfacing to slower external memory or peripheral devices. While inserting wait states extends the bus sequence during read or write accesses, it does not slow down the bus signal sequences at the beginning and the end of the access. Dividing down CLKOUT provides a method of slowing the entire bus sequence when necessary. The CLKOUT divide-down factor is controlled through the DIVFCT field in the bank-switching control register (BSCR) (see Table 3−4).

3.12 DMA Controller

The 54CST direct memory access (DMA) controller transfers data between points in the memory map without intervention by the CPU. The DMA allows movements of data to and from internal program/data memory, internal peripherals (such as the McBSPs), or external memory devices to occur in the background of CPU operation. The DMA has six independent programmable channels, allowing six different contexts for DMA operation.

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3.12.1 Features

The DMA has the following features:

- The DMA operates independently of the CPU.
- The DMA has six channels. The DMA can keep track of the contexts of six independent block transfers.
- The DMA has higher priority than the CPU for both internal and external accesses.
- Each channel has independently programmable priorities.
- Each channel's source and destination address registers can have configurable indexes through memory on each read and write transfer, respectively. The address may remain constant, be post-incremented, be post-decremented, or be adjusted by a programmable value.
- Each read or write internal transfer may be initialized by selected events.
- On completion of a half- or entire-block transfer, each DMA channel may send an interrupt to the CPU.
- The DMA can perform double-word internal transfers (a 32-bit transfer of two 16-bit words).

3.12.2 DMA External Access

The 54CST DMA supports external accesses to extended program memory. A maximum of two DMA channels can be used for external memory accesses. The DMA external accesses require a minimum of 8 cycles for external writes and a minimum of 11 cycles for external reads assuming the XIO02 is in consecutive mode ($\overline{\text{CONSEC}}$ = 1), wait state is set to two, and CLKOUT is not divided (DIVFCT = 00).

The control of the bus is arbitrated between the CPU and the DMA. While the DMA or CPU is in control of the external bus, the other will be held-off via wait states until the current transfer is complete. The DMA takes precedence over XIO requests.

- Only two channels are available for external accesses. (One for external reads and one for external writes.)
- Single-word (16-bit) transfers are supported for external accesses.
- The DMA does not support transfers from the peripherals to external memory.
- The DMA does not support transfers from external memory to the peripherals.
- The DMA does not support external-to-external transfers.

15	14	13	12	11	10 … 8
AUTOINIT	DINM	IMOD	CTMOD	SLAXS	SIND

7	6	5	4 … 2	1	0
DMS		DLAXS	DIND		DMD

Figure 3−16. DMA Transfer Mode Control Register (DMMCRn)

These new bit fields were created to allow the user to define the space-select for the DMA (internal/external). Also, a new extended destination data page (XDSTDP[6:0], subaddress 029h) and extended source data page (XSRCDP[6:0], subaddress 028h) have been created. The functions of the DLAXS and SLAXS bits are as follows:

DLAXS(DMMCRn[5]) Destination 0 = No external access (default internal)
1 = External access

SLAXS(DMMCRn[11]) Source 0 = No external access (default internal)
1 = External access

Table 3−8 lists the DMD bit values and their corresponding destination space.

Table 3−8. DMD Section of the DMMCRn Register

DMD	DESTINATION SPACE
00	PS
01	DS
10	I/O
11	Reserved

For the CPU external access, software can configure the memory cells to reside inside or outside the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the address generation logic generates an address outside its bounds, the device automatically generates an external access.

Two new registers are added to the 54CST DMA to support DMA accesses to/from DMA extended data memory, page 1 to page 127.

- The DMA extended source data page register (XSRCDP[6:0]) is located at subbank address 028h.
- The DMA extended destination data page register (XDSTDP[6:0]) is located at subbank address 029h.

3.12.3 DMA Memory Map

The DMA memory map, shown in Figure 3−17, allows the DMA transfer to be unaffected by the status of the MP/$\overline{MC}$, DROM, and OVLY bits.

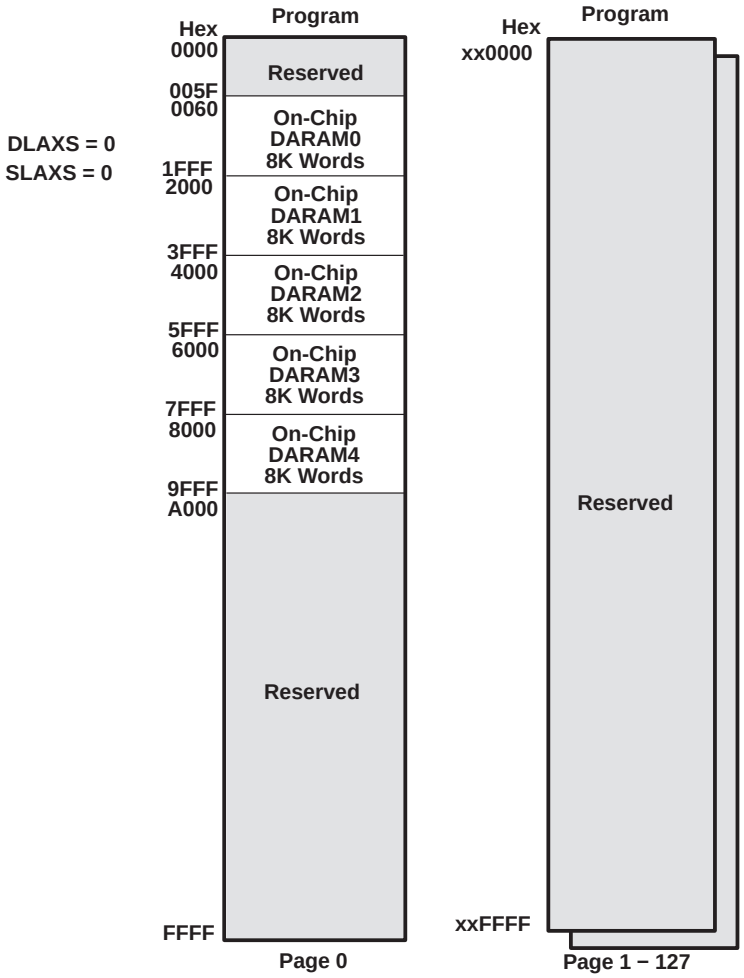


Figure 3−17. On-Chip DMA Memory Map for Program Space (DLAXS = 0 and SLAXS = 0)

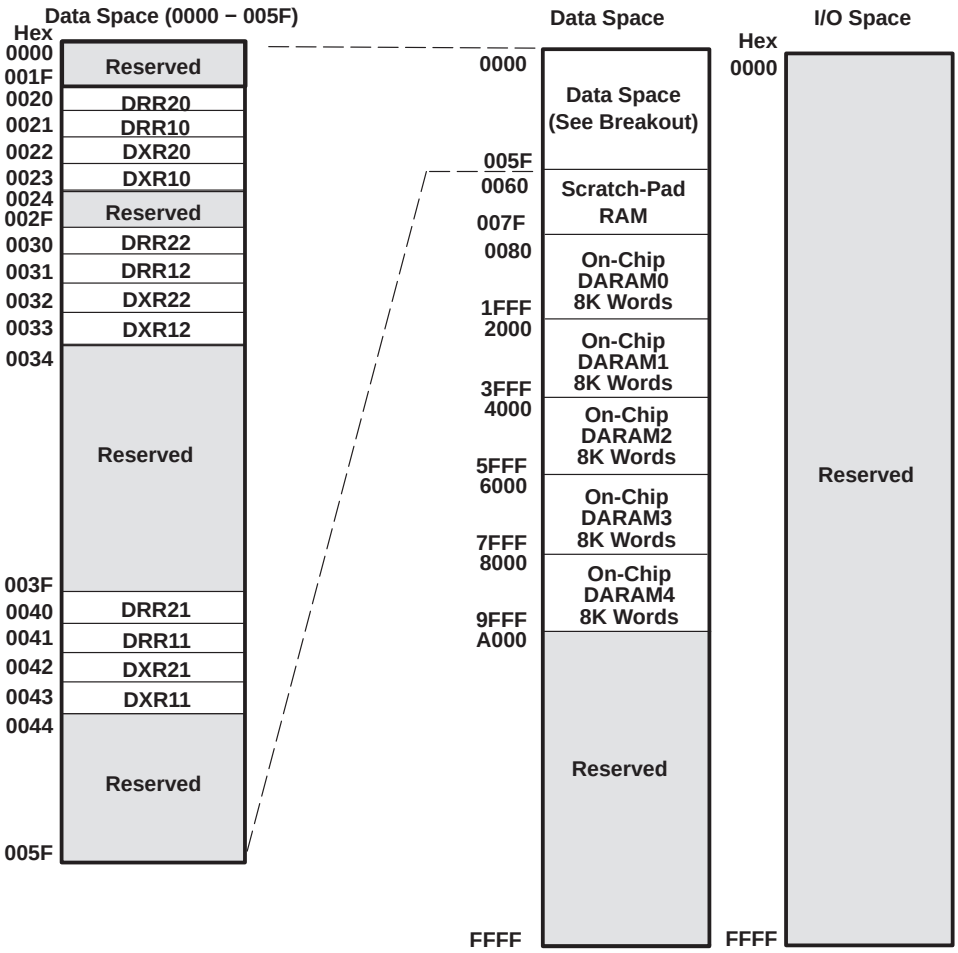


Figure 3−18. On-Chip DMA Memory Map for Data and IO Space (DLAXS = 0 and SLAXS = 0)

3.12.4 DMA Priority Level

Each DMA channel can be independently assigned high- or low-priority relative to each other. Multiple DMA channels that are assigned to the same priority level are handled in a round-robin manner.

3.12.5 DMA Source/Destination Address Modification

The DMA provides flexible address-indexing modes for easy implementation of data management schemes such as autobuffering and circular buffers. Source and destination addresses can be indexed separately and can be post-incremented, post-decremented, or post-incremented with a specified index offset.

3.12.6 DMA in Autoinitialization Mode

The DMA can automatically reinitialize itself after completion of a block transfer. Some of the DMA registers can be preloaded for the next block transfer through the DMA reload registers (DMGSA, DMGDA, DMGCR, and DMGFR). Autoinitialization allows:

- Continuous operation: Normally, the CPU would have to reinitialize the DMA immediately after the completion of the current block transfers, but with the reload registers, it can reinitialize these values for the next block transfer any time after the current block transfer begins.
- Repetitive operation: The CPU does not preload the reload register with new values for each block transfer but only loads them on the first block transfer.

The 54CST DMA has been enhanced to expand the DMA reload register sets. Each DMA channel now has its own DMA reload register set. For example, the DMA reload register set for channel 0 has DMGSA0, DMGDA0, DMGCR0, and DMGFR0 while DMA channel 1 has DMGSA1, DMGDA1, DMGCR1, and DMGFR1, etc.

To utilize the additional DMA reload registers, the AUTOIX bit is added to the DMPREC register as shown in Figure 3−19.

15	14	13	8
FREE	AUTOIX	DPRC[5:0]	
	R/W-0		

7	6	5	0
INT0SEL		DE[5:0]	

LEGEND: R = Read, W = Write

Figure 3−19. DMPREC Register

Table 3−9. DMA Reload Register Selection

AUTOIX	DMA RELOAD REGISTER USAGE IN AUTO INIT MODE
0 (default)	All DMA channels use DMGSA0, DMGDA0, DMGCR0 and DMGFR0
1	Each DMA channel uses its own set of reload registers

3.12.7 DMA Transfer Counting

The DMA channel element count register (DMCTRx) and the frame count register (DMFRCx) contain bit fields that represent the number of frames and the number of elements per frame to be transferred.

- Frame count. This 8-bit value defines the total number of frames in the block transfer. The maximum number of frames per block transfer is 128 (FRAME COUNT= 0FFh). The counter is decremented upon the last read transfer in a frame transfer. Once the last frame is transferred, the selected 8-bit counter is reloaded with the DMA global frame reload register (DMGFR) if the AUTOINIT bit is set to 1. A frame count of 0 (default value) means the block transfer contains a single frame.
- Element count. This 16-bit value defines the number of elements per frame. This counter is decremented after the read transfer of each element. The maximum number of elements per frame is 65536 (DMCTRn = 0FFFFh). In autoinitialization mode, once the last frame is transferred, the counter is reloaded with the DMA global count reload register (DMGCR).

3.12.8 DMA Transfer in Doubleword Mode

Doubleword mode allows the DMA to transfer 32-bit words in any index mode. In doubleword mode, two consecutive 16-bit transfers are initiated and the source and destination addresses are automatically updated following each transfer. In this mode, each 32-bit word is considered to be one element.

3.12.9 DMA Channel Index Registers

The particular DMA channel index register is selected by way of the SIND and DIND fields in the DMA transfer mode control register (DMMCRn). Unlike basic address adjustment, in conjunction with the frame index DMFRI0 and DMFRI1, the DMA allows different adjustment amounts depending on whether or not the element transfer is the last in the current frame. The normal adjustment value (element index) is contained in the element index registers DMIDX0 and DMIDX1. The adjustment value (frame index) for the end of the frame, is determined by the selected DMA frame index register, either DMFRI0 or DMFRI1.

The element index and the frame index affect address adjustment as follows:

- Element index: For all except the last transfer in the frame, the element index determines the amount to be added to the DMA channel for the source/destination address register (DMSRCx/DMDSTx) as selected by the SIND/DIND bits.
- Frame index: If the transfer is the last in a frame, frame index is used for address adjustment as selected by the SIND/DIND bits. This occurs in both single-frame and multiframe transfers.

3.12.10 DMA Interrupts

The ability of the DMA to interrupt the CPU based on the status of the data transfer is configurable and is determined by the IMOD and DINM bits in the DMA transfer mode control register (DMMCRn). The available modes are shown in Table 3−10.

Table 3−10. DMA Interrupts

MODE	DINM	IMOD	INTERRUPT
ABU (non-decrement)	1	0	At full buffer only
ABU (non-decrement)	1	1	At half buffer and full buffer
Multiframe	1	0	At block transfer complete (DMCTRn = DMSEFCn[7:0] = 0)
Multiframe	1	1	At end of frame and end of block (DMCTRn = 0)
Either	0	X	No interrupt generated
Either	0	X	No interrupt generated

3.12.11 DMA Controller Synchronization Events

The transfers associated with each DMA channel can be synchronized to one of several events. The DSYN bit field of the DMSEFCn register selects the synchronization event for a channel. The list of possible events and the DSYN values are shown in Table 3−11.

Table 3−11. DMA Synchronization Events

DSYN VALUE	DMA SYNCHRONIZATION EVENT
0000b	No synchronization used
0001b	McBSP0 receive event
0010b	McBSP0 transmit event
0011b	McBSP2 receive event
0100b	McBSP2 transmit event
0101b	McBSP1 receive event
0110b	McBSP1 transmit event
0111b	UART
1000b	Reserved
1001b	Reserved
1010b	Reserved
1011b	Reserved
1100b	Reserved
1101b	Timer 0 interrupt event
1110b	External interrupt 3
1111b	Timer 1 interrupt event

The DMA controller can generate a CPU interrupt for each of the six channels. However, due to a limit on the number of internal CPU interrupt inputs, channels 0, 1, 2, and 3 are multiplexed with other interrupt sources. DMA channels 0, 1, 2, and 3 share an interrupt line with the receive and transmit portions of the McBSP. When the 54CST is reset, the interrupts from these three DMA channels are deselected. The INT0SEL bit field in the DMPREC register can be used to select these interrupts, as shown in Table 3−12.

Table 3−12. DMA/CPU Channel Interrupt Selection

INT0SEL VALUE	IMR/IFR[6]	IMR/IFR[7]	IMR/IFR[10]	IMR/IFR[11]
00b (reset)	BRINT2	BXINT2	BRINT1	BXINT1
01b	BRINT2	BXINT2	DMAC2	DMAC3
10b	DMAC0	DMAC1	DMAC2	DMAC3
11b	Reserved			

3.13 Universal Asynchronous Receiver/Transmitter (UART)

The UART peripheral is based on the industry-standard TL16C550B asynchronous communications element, which in turn is a functional upgrade of the TL16C450. Functionally similar to the TL16C450 on power up (character or TL16C450 mode), the UART can be placed in an alternate FIFO (TL16C550) mode. This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO.

The UART performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from the CPU. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The UART includes a programmable baud rate generator capable of dividing the CPU clock by divisors from 1 to 65535 and producing a 16× reference clock for the internal transmitter and receiver logic. See Section 5.14 for detailed timing specifications for the UART.

The TMS320C54CST chip has two dedicated pins for UART — RX and TX data, the rest of the UART control and status lines are emulated by CST software and use Host Port Interface (HPI) pins. For more information, see *Client Side Telephony (CST) Chip Software User's Guide* (literature number SPRU029).

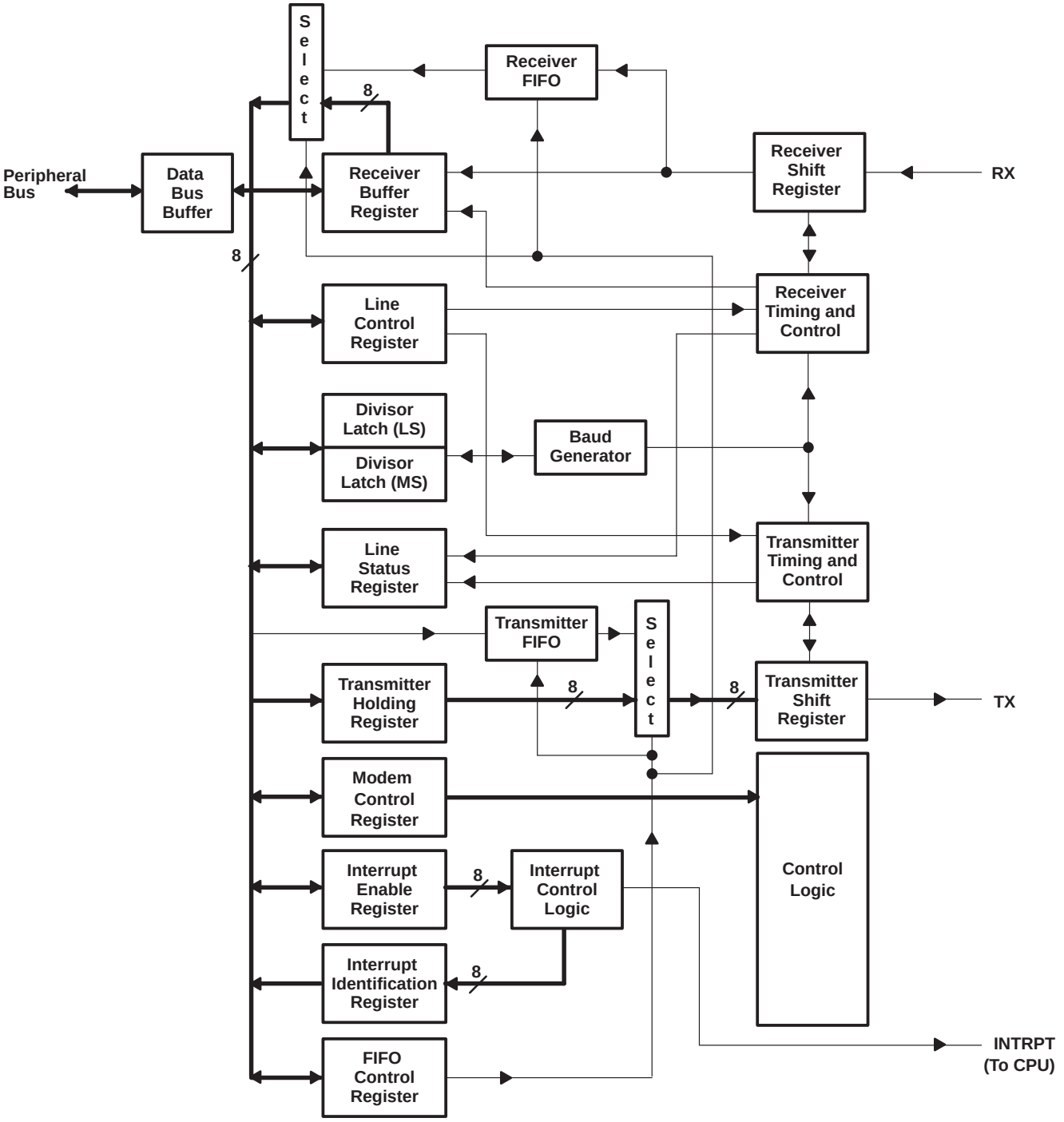


Figure 3−20. UART Functional Block Diagram

Table 3−13. UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Master reset	All bits cleared (0−3 forced and 4−7 permanent)
Interrupt identification register	Master reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4−5 are permanently cleared
FIFO control register	Master reset	All bits cleared
Line control register	Master reset	All bits cleared
Modem control register	Master reset	All bits cleared (6−7 permanent)
Line status register	Master reset	Bits 5 and 6 are set; all other bits are cleared
Reserved register	Master reset	Indeterminate
SOUT	Master reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/write THR/MR	Low
Scratch register	Master reset	No effect
Divisor latch (LSB and MSB) registers	Master reset	No effect
Receiver buffer register	Master reset	No effect
Transmitter holding register	Master reset	No effect
RCVR FIFO	MR/FCR1−FCR0/ΔFCR0	All bits cleared
XMIT FIFO	MR/FCR2−FCR0/ΔFCR0	All bits cleared

3.13.1 UART Accessible Registers

The system programmer has access to and control over any of the UART registers that are summarized in Table 3−13. These registers control UART operations, receive data, and transmit data. Descriptions of these registers follow Table 3−14. See Table 3−23 for more information on peripheral memory mapped registers.

Table 3−14. Summary of Accessible Registers

BIT NO.	UART SUBBANK ADDRESS											
	0 (DLAB = 0)	0 (DLAB = 0)	0 (DLAB = 1) or 8	1 (DLAB = 0)	1 (DLAB = 1) or 9	2	2	3	4	5	6	7
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Divisor Latch (LSB)	Interrupt Enable Register	Divisor Latch (MSB)	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Reserved Register	Scratch Register
	RBR	THR	DLL	IER	DLM	IIR	FCR	LCR	MCR	LSR	RSV	SCR
0	Data Bit 0†	Data Bit 0	Bit 0	Enable Received Data Available Interrupt (ERBI)	Bit 8	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	X	Data Ready (DR)	X	Bit 0
1	Data Bit 1	Data Bit 1	Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Bit 9	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	X	Overrun Error (OE)	X	Bit 1
2	Data Bit 2	Data Bit 2	Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Bit 10	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	X	Parity Error (PE)	X	Bit 2
3	Data Bit 3	Data Bit 3	Bit 3	0‡	Bit 11	Interrut ID Bit 3§	0‡	Parity Enable (PEN)	X	Framing Error (FE)	X	Bit 3
4	Data Bit 4	Data Bit 4	Bit 4	0	Bit 12	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	X	Bit 4
5	Data Bit 5	Data Bit 5	Bit 5	0	Bit 13	0	Reserved	Stick Parity	0‡	Transmitter Holding Register (THRE)	X	Bit 5
6	Data Bit 6	Data Bit 6	Bit 6	0	Bit 14	FIFOs Enabled§	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	X	Bit 6
7	Data Bit 7	Data Bit 7	Bit 7	0	Bit 15	FIFOs Enabled§	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO§	X	Bit 7
8 − 15	0	0	0	0	0	0	0	0	0	0	0	0

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
‡ Must always be written as zero.
§ These bits are always 0 in the TL16C450 mode.
NOTE: X = Don't care for write, indeterminate on read.

3.13.2 FIFO Control Register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables and clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit, when set, enables the transmitter and receiver FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit, when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 2: This bit, when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bits 3, 4, and 5: These three bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt (see Table 4).

Table 3−15. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

3.13.3 FIFO Interrupt Mode Operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), a receiver interrupt occurs as follows:

1. The received data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06) has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled:

1. FIFO time-out interrupt occurs if the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO has occurred more than four continuous character times before. This causes a maximum character received command to interrupt an issued delay of 160 ms at a 300 baud rate with a 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (makes the delay proportional to the baud rate).

3. When a time-out interrupt has occurred, it is cleared and the timer is cleared when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register empty interrupt [IIR (3−0) = 2] occurs when the transmit FIFO is empty. It is cleared [IIR (3−0) = 1] when the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter holding register empty interrupt is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time that the FIFO was empty. The first transmitter interrupt after changing FCR0 is immediate if it is enabled.

3.13.4 FIFO Polled Mode Operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four to 0 puts the UART in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR. As stated previously:

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 − LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the THR is empty.
- LSR6 indicates that both the THR and TSR are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

3.13.5 Interrupt Enable Register (IER)

The IER enables each of the five types of interrupts (refer to Table 5) and enables INTRPT in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bullets.

- Bit 0: When set, this bit enables the received data available interrupt.
- Bit 1: When set, this bit enables the THRE interrupt.
- Bit 2: When set, this bit enables the receiver line status interrupt.
- Bits 3 through 7: These bits are not used

3.13.6 Interrupt Identification Register (IIR)

The UART has an on-chip interrupt generation and prioritization capability that permits flexible communication with the CPU.

The UART provides three prioritized levels of interrupts:

- Priority 1 − Receiver line status (highest priority)
- Priority 2 − Receiver data ready or receiver character time-out
- Priority 3 − Transmitter holding register empty

When an interrupt is generated, the IIR indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 5. Detail on each bit is as follows:

- Bit 0: This bit is used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending If bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 3
- Bit 3: This bit is always cleared in TL16C450 mode. In FIFO mode, bit 3 is set with bit 2 to indicate that a time-out interrupt is pending.
- Bits 4 and 5: These two bits are not used (always cleared).
- Bits 6 and 7: These bits are always cleared in TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

Table 3−16. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Read the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Read the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Read the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Read the interrupt identification register (if source of interrupt) or writing into the transmitter holding register

3.13.7 Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 3−17.

Table 3−17. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit 2 are shown in Table 3−18.

Table 3−18. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This bit is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where SOUT is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only effects SOUT.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

3.13.8 Line Status Register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

- Bit 2‡: This bit is the parity error (PE) indicator. When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The UART samples this start bit twice and then accepts the input data.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state for at least two RCLK samples and then receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. THRE is set when the THR is empty, indicating that the UART is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550C mode, this bit is always cleared. In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

3.13.9 Modem Control Register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device. On the UART peripheral, only one bit is active in this register

- Bit 4: This bit (LOOP) provides a local loop back feature for diagnostic testing of the UART. When LOOP is set, the following occurs:
  - The transmitter SOUT is set high.
  - The receiver SIN is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.

3.13.10 Programmable Baud Generator

The UART contains a programmable baud generator that takes the DSP clock as input and divides it by a divisor in the range between 1 and ($2^{16}-1$). The DSP clock frequency is 58.9824 MHz or 117.9648 MHz. The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

divisor = DSP clock frequency / (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the UART in order to ensure desired operation of the baud rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Table 3−19 and Table 3−20 illustrate the use of the baud generator with clock frequencies of 58.9824 MHz and 117.9648 MHz, respectively.

‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

Table 3−19. Baud Rates Using a 58.9824-MHz Clock

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 × CLOCK
150	24576
300	12288
1200	3072
2400	1536
4800	768
9600	384
19200	192
38400	96
57600	64
115200	32

Table 3−20. Baud Rates Using a 117.9648-MHz Clock

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 × CLOCK
150	49152
300	24576
1200	6144
2400	3072
4800	1536
9600	768
19200	384
38400	192
57600	128
115200	64

3.13.10.1 Receiver Buffer Register (RBR)

The UART receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock. Receiver section control is a function of the UART line control register.

The UART RSR receives serial data from SIN. The RSR then concatenates the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled (IER0 = 1), an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

3.13.10.2 Scratch Register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

3.13.10.3 Transmitter Holding Register (THR)

The UART transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Transmitter section control is a function of the UART line control register.

The UART THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at SOUT. In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER1 = 1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

3.14 General-Purpose I/O Pins

In addition to the standard $\overline{\text{BIO}}$ and XF pins, the 54CST has pins that can be configured for general-purpose I/O. These pins are:

- 13 McBSP pins — BCLKX0/1, BCLKR0/1, BDR0/1, BFSX0/1, BFSR0/1, BDX0/1, BFSRX2
- 8 HPI data pins—HD0−HD7

The general-purpose I/O function of these pins is only available when the primary pin function is not required.

3.14.1 McBSP Pins as General-Purpose I/O

When the receive or transmit portion of a McBSP is in reset, its pins can be configured as general-purpose inputs or outputs. For more details on this feature, see Section 3.8.

3.14.2 HPI Data Pins as General-Purpose I/O

The 8-bit bidirectional data bus of the HPI can be used as general-purpose input/output (GPIO) pins when the HPI is disabled (HPIENA = 0) or when the HPI is used in HPI16 mode (HPI16 = 1). By default, CST software UART driver uses the HPI GPIO pins HD0−HD5 for UART hardware flow control as described in Table 3−21. The CST SDK provides a flex example which shows how to disable this behavior in order to use the HD0−HD5 pins as GPIOs or to enable the HPI. Two memory-mapped registers are used to control the GPIO function of the HPI data pins—the general-purpose I/O control register (GPIOCR) and the general-purpose I/O status register (GPIOSR). The GPIOCR is shown in Figure 3−21. The direction bits (DIRx) are used to configure HD0−HD7 as inputs or outputs.

15							8
Reserved							
0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read, W = Write

Figure 3−21. General-Purpose I/O Control Register (GPIOCR) [MMR Address 003Ch]

The status of the GPIO pins can be monitored using the bits of the GPIOSR. The GPIOSR is shown in Figure 3−22.

15							8
Reserved							
0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read, W = Write

Figure 3−22. General-Purpose I/O Status Register (GPIOSR) [MMR Address 003Dh]

Table 3−21. HPI Pins Used For UART Flow Control

SIGNAL NAME	UART DRIVER FUNCTION	DIRECTION
HD0	UART Data Terminal Ready (DTR)	Input
HD1	UART Request to Send (RTS)	Input
HD2	UART Clear to Send (CTS)	Output
HD3	UART Data Set Reade (DSR)	Output
HD4	UART Data Carrier Detect (DCD)	Output
HD5	UART Ring Indication (RI)	Output
HD6	Available as GPIO	Output
HD7	Available as GPIO	Output

NOTE: For more information about the HPI pins used by the UART driver, see Section 3.4 in the *Client SIde Telephony (CST) Chip Software User's Guide* (literature number SPRU029)

3.15 Device ID Register

A read-only memory-mapped register has been added to the 54CST to allow user application software to identify on which device the program is being executed.

15							8
CHIP ID							
R							
7			**4**	**3**			**0**
CHIP REVISION				SUBSYSID			
R				R			

LEGEND: R = Read, W = Write

NOTE: Bits 15:8 − Chip-ID (hex code of 06),
Bits 7:4 − Chip-Revision ID,
Bits 3:0 − Subsystem-ID (0000b for single core device)

Figure 3−23. Device ID Register (CSIDR) [MMR Address 003Eh]

3.16 Memory-Mapped Registers

The 54CST has 27 memory-mapped CPU registers, which are mapped in data memory space address 0h to 1Fh. Each 54CST device also has a set of memory-mapped registers associated with peripherals. Table 3−22 gives a list of CPU memory-mapped registers (MMRs) available on 54CST. Table 3−23 shows additional peripheral MMRs associated with the 54CST.

Table 3−22. CPU Memory-Mapped Registers

NAME	ADDRESS		DESCRIPTION
	DEC	HEX	
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
—	2−5	2−5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15−0)
AH	9	9	Accumulator A high word (31−16)
AG	10	A	Accumulator A guard bits (39−32)
BL	11	B	Accumulator B low word (15−0)
BH	12	C	Accumulator B high word (31−16)
BG	13	D	Accumulator B guard bits (39−32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block repeat counter
RSA	27	1B	Block repeat start address
REA	28	1C	Block repeat end address
PMST	29	1D	Processor mode status (PMST) register
XPC	30	1E	Extended program page register
—	31	1F	Reserved

Table 3−23. Peripheral Memory-Mapped Registers for Each DSP Subsystem

NAME	ADDRESS DEC	ADDRESS HEX	DESCRIPTION
DRR20	32	20	McBSP 0 Data Receive Register 2
DRR10	33	21	McBSP 0 Data Receive Register 1
DXR20	34	22	McBSP 0 Data Transmit Register 2
DXR10	35	23	McBSP 0 Data Transmit Register 1
TIM	36	24	Timer 0 Register
PRD	37	25	Timer 0 Period Register
TCR	38	26	Timer 0 Control Register
—	39	27	Reserved
SWWSR	40	28	Software Wait-State Register
BSCR	41	29	Bank-Switching Control Register
—	42	2A	Reserved
SWCR	43	2B	Software Wait-State Control Register
HPIC	44	2C	HPI Control Register (HMODE = 0 only)
—	45−47	2D−2F	Reserved
DRR22	48	30	McBSP 2 Data Receive Register 2
DRR12	49	31	McBSP 2 Data Receive Register 1
DXR22	50	32	McBSP 2 Data Transmit Register 2
DXR12	51	33	McBSP 2 Data Transmit Register 1
SPSA2	52	34	McBSP 2 Subbank Address Register†
SPSD2	53	35	McBSP 2 Subbank Data Register†
—	54−55	36−37	Reserved
SPSA0	56	38	McBSP 0 Subbank Address Register†
SPSD0	57	39	McBSP 0 Subbank Data Register†
—	58−59	3A−3B	Reserved
GPIOCR	60	3C	General-Purpose I/O Control Register
GPIOSR	61	3D	General-Purpose I/O Status Register
CSIDR	62	3E	Device ID Register
—	63	3F	Reserved
DRR21	64	40	McBSP 1 Data Receive Register 2
DRR11	65	41	McBSP 1 Data Receive Register 1
DXR21	66	42	McBSP 1 Data Transmit Register 2
DXR11	67	43	McBSP 1 Data Transmit Register 1
USAR	68	44	UART Subbank Address Register
USDR	69	45	UART Subbank Data Register
—	70−71	46−47	Reserved
SPSA1	72	48	McBSP 1 Subbank Address Register†
SPSD1	73	49	McBSP 1 Subbank Data Register†
—	74−75	4A−4B	Reserved
TIM1	76	4C	Timer 1 Register
PRD1	77	4D	Timer 1 Period Register
TCR1	78	4E	Timer 1 Control Register
—	79−83	4F−53	Reserved
DMPREC	84	54	DMA Priority and Enable Control Register
DMSA	85	55	DMA Subbank Address Register‡
DMSDI	86	56	DMA Subbank Data Register with Autoincrement‡
DMSDN	87	57	DMA Subbank Data Register‡
CLKMD	88	58	Clock Mode Register (CLKMD)
—	89−95	59−5F	Reserved

† See Table 3−24 for a detailed description of the McBSP control registers and their subaddresses.
‡ See Table 3−25 for a detailed description of the DMA subbank addressed registers.

3.17 McBSP Control Registers and Subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The McBSP subbank address register (SPSA) is used as a pointer to select a particular register within the subbank. The McBSP data register (SPSDx) is used to access (read or write) the selected register. Table 3−24 shows the McBSP control registers and their corresponding subaddresses.

Table 3−24. McBSP Control Registers and Subaddresses

McBSP0		McBSP1		McBSP2		SUB-ADDRESS	DESCRIPTION
NAME	ADDRESS	NAME	ADDRESS	NAME	ADDRESS		
SPCR10	39h	SPCR11	49h	SPCR12	35h	00h	Serial port control register 1
SPCR20	39h	SPCR21	49h	SPCR22	35h	01h	Serial port control register 2
RCR10	39h	RCR11	49h	RCR12	35h	02h	Receive control register 1
RCR20	39h	RCR21	49h	RCR22	35h	03h	Receive control register 2
XCR10	39h	XCR11	49h	XCR12	35h	04h	Transmit control register 1
XCR20	39h	XCR21	49h	XCR22	35h	05h	Transmit control register 2
SRGR10	39h	SRGR11	49h	SRGR12	35h	06h	Sample rate generator register 1
SRGR20	39h	SRGR21	49h	SRGR22	35h	07h	Sample rate generator register 2
MCR10	39h	MCR11	49h	MCR12	35h	08h	Multichannel control register 1
MCR20	39h	MCR21	49h	MCR22	35h	09h	Multichannel control register 2
RCERA0	39h	RCERA1	49h	RCERA2	35h	0Ah	Receive channel enable register partition A
RCERB0	39h	RCERB1	49h	RCERA2	35h	0Bh	Receive channel enable register partition B
XCERA0	39h	XCERA1	49h	XCERA2	35h	0Ch	Transmit channel enable register partition A
XCERB0	39h	XCERB1	49h	XCERA2	35h	0Dh	Transmit channel enable register partition B
PCR0	39h	PCR1	49h	PCR2	35h	0Eh	Pin control register
RCERC0	39h	RCERC1	49h	RCERC2	35h	010h	Additional channel enable register for 128-channel selection
RCERD0	39h	RCERD1	49h	RCERD2	35h	011h	Additional channel enable register for 128-channel selection
XCERC0	39h	XCERC1	49h	XCERC2	35h	012h	Additional channel enable register for 128-channel selection
XCERD0	39h	XCERD1	49h	XCERD2	35h	013h	Additional channel enable register for 128-channel selection
RCERE0	39h	RCERE1	49h	RCERE2	35h	014h	Additional channel enable register for 128-channel selection
RCERF0	39h	RCERF1	49h	RCERF2	35h	015h	Additional channel enable register for 128-channel selection
XCERE0	39h	XCERE1	49h	XCERE2	35h	016h	Additional channel enable register for 128-channel selection
XCERF0	39h	XCERF1	49h	XCERF2	35h	017h	Additional channel enable register for 128-channel selection
RCERG0	39h	RCERG1	49h	RCERG2	35h	018h	Additional channel enable register for 128-channel selection
RCERH0	39h	RCERH1	49h	RCERH2	35h	019h	Additional channel enable register for 128-channel selection
XCERG0	39h	XCERG1	49h	XCERG2	35h	01Ah	Additional channel enable register for 128-channel selection
XCERH0	39h	XCERH1	49h	XCERH2	35h	01Bh	Additional channel enable register for 128-channel selection

3.18 DMA Subbank Addressed Registers

The direct memory access (DMA) controller has several control registers associated with it. The main control register (DMPREC) is a standard memory-mapped register. However, the other registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The DMA subbank address (DMSA) register is used as a pointer to select a particular register within the subbank, while the DMA subbank data (DMSD) register or the DMA subbank data register with autoincrement (DMSDI) is used to access (read or write) the selected register.

When the DMSDI register is used to access the subbank, the subbank address is automatically postincremented so that a subsequent access affects the next register within the subbank. This autoincrement feature is intended for efficient, successive accesses to several control registers. If the autoincrement feature is not required, the DMSDN register should be used to access the subbank. Table 3−25 shows the DMA controller subbank addressed registers and their corresponding subaddresses.

Table 3−25. DMA Subbank Addressed Registers

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMSRC0	56h/57h	00h	DMA channel 0 source address register
DMDST0	56h/57h	01h	DMA channel 0 destination address register
DMCTR0	56h/57h	02h	DMA channel 0 element count register
DMSFC0	56h/57h	03h	DMA channel 0 sync select and frame count register
DMMCR0	56h/57h	04h	DMA channel 0 transfer mode control register
DMSRC1	56h/57h	05h	DMA channel 1 source address register
DMDST1	56h/57h	06h	DMA channel 1 destination address register
DMCTR1	56h/57h	07h	DMA channel 1 element count register
DMSFC1	56h/57h	08h	DMA channel 1 sync select and frame count register
DMMCR1	56h/57h	09h	DMA channel 1 transfer mode control register
DMSRC2	56h/57h	0Ah	DMA channel 2 source address register
DMDST2	56h/57h	0Bh	DMA channel 2 destination address register
DMCTR2	56h/57h	0Ch	DMA channel 2 element count register
DMSFC2	56h/57h	0Dh	DMA channel 2 sync select and frame count register
DMMCR2	56h/57h	0Eh	DMA channel 2 transfer mode control register
DMSRC3	56h/57h	0Fh	DMA channel 3 source address register
DMDST3	56h/57h	10h	DMA channel 3 destination address register
DMCTR3	56h/57h	11h	DMA channel 3 element count register
DMSFC3	56h/57h	12h	DMA channel 3 sync select and frame count register
DMMCR3	56h/57h	13h	DMA channel 3 transfer mode control register
DMSRC4	56h/57h	14h	DMA channel 4 source address register
DMDST4	56h/57h	15h	DMA channel 4 destination address register
DMCTR4	56h/57h	16h	DMA channel 4 element count register
DMSFC4	56h/57h	17h	DMA channel 4 sync select and frame count register
DMMCR4	56h/57h	18h	DMA channel 4 transfer mode control register
DMSRC5	56h/57h	19h	DMA channel 5 source address register
DMDST5	56h/57h	1Ah	DMA channel 5 destination address register
DMCTR5	56h/57h	1Bh	DMA channel 5 element count register
DMSFC5	56h/57h	1Ch	DMA channel 5 sync select and frame count register
DMMCR5	56h/57h	1Dh	DMA channel 5 transfer mode control register
DMSRCP	56h/57h	1Eh	DMA source program page address (common channel)
DMDSTP	56h/57h	1Fh	DMA destination program page address (common channel)

Table 3−25. DMA Subbank Addressed Registers (Continued)

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMIDX0	56h/57h	20h	DMA element index address register 0
DMIDX1	56h/57h	21h	DMA element index address register 1
DMFRI0	56h/57h	22h	DMA frame index register 0
DMFRI1	56h/57h	23h	DMA frame index register 1
DMGSA0	56h/57h	24h	DMA global source address reload register, channel 0
DMGDA0	56h/57h	25h	DMA global destination address reload register, channel 0
DMGCR0	56h/57h	26h	DMA global count reload register, channel 0
DMGFR0	56h/57h	27h	DMA global frame count reload register, channel 0
XSRCDP	56h/57h	28h	DMA extended source data page
XDSTDP	56h/57h	29h	DMA extended destination data page
DMGSA1	56h/57h	2Ah	DMA global source address reload register, channel 1
DMGDA1	56h/57h	2Bh	DMA global destination address reload register, channel 1
DMGCR1	56h/57h	2Ch	DMA global count reload register, channel 1
DMGFR1	56h/57h	2Dh	DMA global frame count reload register, channel 1
DMGSA2	56h/57h	2Eh	DMA global source address reload register, channel 2
DMGDA2	56h/57h	2Fh	DMA global destination address reload register, channel 2
DMGCR2	56h/57h	30h	DMA global count reload register, channel 2
DMGFR2	56h/57h	31h	DMA global frame count reload register, channel 2
DMGSA3	56h/57h	32h	DMA global source address reload register, channel 3
DMGDA3	56h/57h	33h	DMA global destination address reload register, channel 3
DMGCR3	56h/57h	34h	DMA global count reload register, channel 3
DMGFR3	56h/57h	35h	DMA global frame count reload register, channel 3
DMGSA4	56h/57h	36h	DMA global source address reload register, channel 4
DMGDA4	56h/57h	37h	DMA global destination address reload register, channel 4
DMGCR4	56h/57h	38h	DMA global count reload register, channel 4
DMGFR4	56h/57h	39h	DMA global frame count reload register, channel 4
DMGSA5	56h/57h	3Ah	DMA global source address reload register, channel 5
DMGDA5	56h/57h	3Bh	DMA global destination address reload register, channel 5
DMGCR5	56h/57h	3Ch	DMA global count reload register, channel 5
DMGFR5	56h/57h	3Dh	DMA global frame count reload register, channel 5

3.19 Direct Access Arrangement (DAA)

The DAA (direct access arrangement) peripheral is an integrated module that is used to provide a programmable interface circuit which meets global telephone line interface requirements.

The complete DAA telephone line interface is composed of two separate sections; the on-chip integrated DAA module, and an external companion DAA chip. These two sections provide the complete DAA telephone line interface circuit. The distinction between these two separate sections of the circuit is transparent to the user, and the DAA should be considered to be implemented in one single functional block of circuitry.

Of these two separate sections, the integrated DAA module is referred to as the system side module and the external companion DAA chip is referred to as the line-side chip. The line-side chip contains much of the analog circuitry required for the telephone line interface. The line-side chip which must be used with this DSP is the Si3016 from Silicon Laboratories. For additional information and electrical specifications for this device, see the device specific documentation supplied by the manufacturer.

The DAA circuit performs the functions of an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid, and eliminates the need for these functions to be implemented discretely. This dramatically reduces the number of components and cost required to achieve compliance with global regulatory requirements.

This DAA provides a rich feature-set of telephone line interface and telephony functions. These include the following:

- Programmable AC/DC phone line interface characteristics.
- Telephone line status monitoring functions.
- Ring characteristics and detection.
- Transient and overload protection.
- Support for caller ID.

This DAA circuit facilitates efficient and cost effective implementation of numerous telephony-type applications such as modem and FAX functions, set top boxes, and internet-based products.

The integrated DAA peripheral module interfaces with the DSP CPU through the McBSP. Across this McBSP interface, the DAA and CPU communicate data, control and configuration information. Figure 3−24 shows a block diagram of the DAA and its interface with the CPU through the McBSP.

Within the DAA module, the McBSP has access to a bank of registers that contain bits which perform control and configuration functions in the DAA, and report status information.

The function of the DAA control register bits and operation of the McBSP interface with the DAA is discussed in more detail in the following subsections.

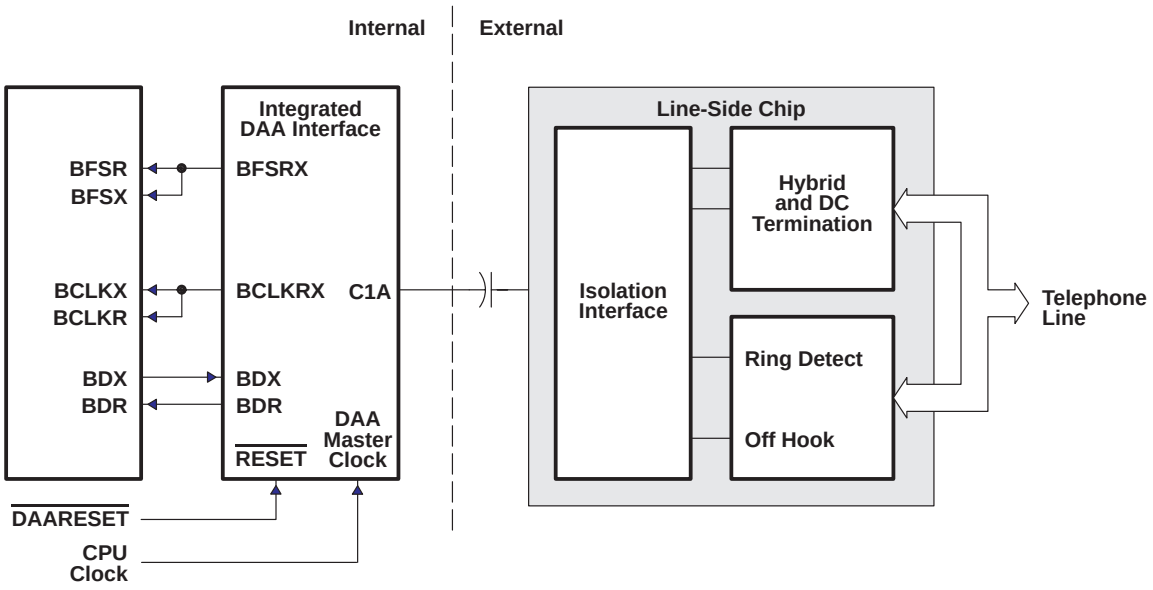


Figure 3−24. Functional Block Diagram

3.19.1 DAA Control Registers

This subsection describes the DAA control registers accessible through the McBSP and the functions of the individual bits in the registers (a later subsection describes how these registers are accessed through the McBSP). Table 3−26 shows each of the control registers, along with its address, and all of the active bits within the register. The Table 3−27 through Table 3−45 describe the function of each of the control register bits in detail. Note that the description of each of the register bits function is included here for reference, however, these functions are more meaningful when described within the context of their use in DAA operation, which is described in the later subsections. It is recommended, therefore, that this section be considered for familiarity, and used for reference after referring to the remaining subsections of the DAA documentation.

Table 3−26. DAA Register Summary

REGISTER	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	Control 1	SR						DL	SB
2	Control 2					AL		HBE	RXE
3:4	Reserved								
5	DAA Control 1		RDTN	RDTP		ONHM	RDT		OH
6	DAA Control 2				PDL	PDN			
7:8	Reserved								
9	Sample Rate Control						SRC[2:0]		
10	Reserved								
11	Chip A Revision					REVA[3:0]			
12	Line Side Status	CLE	FDT			LCS[3:0]			
13	Chip B Revision		CBID	REVB[3:0]				ARXB	ATXB
14	Line Side Validation						CHK	CIP	SAFE
15	TX/RX Gain Control	TXM	ATX[2:0]			RXM	ARX[2:0]		
16	International Control 1	OFF/SQL2	OHS	ACT		DCT[1:0]		RZ	RT
17	International Control 2		MCAL	CALD	LIM	OPE	BTE	ROV	BTD
18	International Control 3	FULL	DIAL	FJM	VOL	FLVM	MODE	RFWE	SQLH
19	International Control 4	LVCS[4:0]					OVL	DOD	OPD

NOTE: Any register not listed here is reserved and must not be written.

3.19.1.1 DAA Register 1

7	6	2	1	0
SR	Reserved		DL	SB
R/W			R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−25. Register 1 − Control 1 Register Layout

Table 3−27. Register 1 − Control 1 Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	SR	Software Reset. 0 = Enables chip for normal operation. 1 = Sets all registers to their reset value. Bit will automatically clear after being set.
6:2	Reserved	Read returns zero.
1	DL	Isolation Digital Loopback. 0 = Digital loopback across isolation barrier disabled. 1 = Enables digital loopback mode across isolation barrier. The line side must be enabled prior to setting this mode.
0	SB	Serial Digital Interface Mode. 0 = Operation is in 15-bit mode, and the LSB of the data field indicates whether a secondary frame is required. 1 = The serial port is operating in 16-bit mode, and no secondary frames can be requested. This bit should be left cleared. Once set, it can only be cleared by a reset.

3.19.1.2 DAA Register 2

7	4	3	2	1	0
Reserved		AL	Reserved	HBE	RXE
		R/W		R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = 0000_0011

Figure 3−26. Register 2 − Control 2 Register Layout

Table 3−28. Register 2 − Control 2 Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:4	Reserved	Read returns zero.
3	AL	Analog Loopback. 0 = Analog loopback mode disabled. 1 = Enables external analog loopback mode.
2	Reserved	Read returns zero.
1	HBE	Hybrid Enable. 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	Receive Enable. 0 = Receive path disabled. 1 = Enables receive path.

3.19.1.3 DAA Register 3

7							0
Reserved							

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−27. Register 3 − Reserved Register Layout

Table 3−29. Register 3 − Reserved Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:0	Reserved	Read returns zero.

3.19.1.4 DAA Register 4

7							0
Reserved							

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−28. Register 4 − Reserved Register Layout

Table 3−30. Register 4 − Reserved

BIT NO.	BIT NAME	DESCRIPTION
7:0	Reserved	Read returns zero.

3.19.1.5 DAA Register 5

7	6	5	4	3	2	1	0
Reserved	RDTN	RDTP	Reserved	ONHM	RDT	Reserved	OH
	R	R		R/W	R		R/W

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−29. Register 5 − DAA Control 1 Register Layout

Table 3−31. Register 5 − DAA Control 1 Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	Reserved	Read returns zero.
6	RDTN	Ring Detect Signal Negative. 0 = No negative ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	Ring Detect Signal Positive. 0 = No positive ring signal is occurring. 1 = A positive ring signal is occurring.
4	Reserved	Read returns zero.
3	ONHM	On-Hook Line Monitor. 0 = Normal on-hook mode. 1 = Enables low-power monitoring mode allowing the DSP to receive line activity without going off-hook. This mode is used for caller-ID detection. When MODE bit = 1 (Register 18, bit 2), the device consumes ~7 mA from the phone line when in on-hook line monitor mode. When MODE = 0, the device consumes ~450 mA from the phone line when in on-hook line monitor mode. Note: This bit should be cleared before setting the OH bit.
2	RDT	Ring Detect. 0 = Reset either 4.5–9 seconds after last positive ring is detected or when the system executes an off-hook. 1 = Indicates a ring is occurring.
1	Reserved	Read returns zero.
0	OH	Off-Hook. 0 = Line-side device on-hook. 1 = Causes the line-side chip to go off-hook. This bit operates independently of the OHE bit and is a logic OR with the off-hook pin when enabled. When the MODE bit (Register 12, bit 2) is set to 1, the device will go on-hook without enabling the off-hook counter, thus allowing the device to go immediately (i.e., no timeout required on the counter) back off-hook when the MODE bit is cleared. This is useful in supporting Type II caller ID. Note: The ONHM bit should be cleared before setting this bit.

3.19.1.6 DAA Register 6

7	6	5	4	3	2	1	0
Reserved	ATM[1]	ARM[1]	PDL	PDN	Reserved	ATM[0]	ARM[0]
	R/W	R/W	R/W	R/W		R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = 0111_0000

Figure 3−30. Register 6 − DAA Control 2 Register Layout

Table 3−32. Register 6 − DAA Control 2

BIT NO.	BIT NAME	DESCRIPTION
7	Reserved	Read returns zero.
6,1	ATM[1:0]	AOUT Transmit Path Level Control. 00 = –20 dB transmit path attenuation for call progress AOUT pin only. 01 = –32 dB transmit path attenuation for call progress AOUT pin only. 10 = Mutes transmit path for call progress AOUT pin only. 11 = –26 dB transmit path attenuation for call progress AOUT pin only.
5,0	ARM[1:0]	AOUT Receive Path Level Control. 00 = 0 dB receive path attenuation for call progress AOUT pin only. 01 = –12 dB receive path attenuation for call progress AOUT pin only. 10 = Mutes receive path for call progress AOUT pin only. 11 = –6 dB receive path attenuation for call progress AOUT pin only.
4	PDL	Power Down Line-Side Chip. 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Places the line-side chip in lower power mode.
3	PDN	Power Down. 0 = Normal operation. 1 = Powers down the system-side module. An internal $\overline{\text{RESET}}$ to the system-side module is required to restore normal operation.
2	Reserved	Read returns zero.

3.19.1.7 DAA Register 7

7							0
Reserved							

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−31. Register 7 − Reserved Register Layout

Table 3−33. Register 7 − Reserved Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:0	Reserved	Read returns zero.

3.19.1.8 DAA Register 8

7							0
Reserved							

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−32. Register 8 Layout (Reserved)

Table 3−34. Register 8 − Reserved Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:0	Reserved	Read returns zero.

3.19.1.9 DAA Register 9

7	3	2	0
Reserved		SRC[2:0]	
			R/W

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−33. Register 9 − Sample Rate Control Register Layout

Table 3−35. Register 9 − Sample Rate Control Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:3	Reserved	Read returns zero.
2:0	SRC[2:0]	Sample Rate Control. This 3-bit value controls the sampling rate of the DAA. 000 = 7200 Hz 001 = 8000 Hz 010 = 8229 Hz 011 = 8400 Hz 100 = 9000 Hz 101 = 9600 Hz 110 = 10286 Hz 111 = Reserved

3.19.1.10 DAA Register 10

7	0
Reserved	

LEGEND: R = Read, W = Write, Reset settings = 0000_0000

Figure 3−34. Register 10 − Reserved Register Layout

Table 3−36. Register 10 − Reserved Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:0	Reserved	Read returns zero.

3.19.1.11 DAA Register 11

7	4	3	0
Reserved		REVA[3:0]	
		R	

LEGEND: R = Read, W = Write, Reset settings = N/A

Figure 3−35. Register 11 − Chip A Revision Register Layout

Table 3−37. Register 11 − Chip A Revision Register Layout Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:4	Reserved	Read returns zero.
3:0	REVA[3:0]	Chip A Revision. Four-bit value indicating the revision of the integrated system-side module.

3.19.1.12 DAA Register 12

7	6	5	4	3	0
CLE	FDT	Reserved		LCS[3:0]	
R/W	R			R	

LEGEND: R = Read, W = Write, Reset settings = N/A

Figure 3−36. Register 12 − Line-Side Status Register Layout

Table 3−38. Register 12 − Line-Side Status Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	CLE	Communications Error. 0 = communication link between the integrated system-side module and line-side chip is operating correctly. 1 = Indicates a communication problem between the integrated system-side module and the line-side chip. When it goes high, it remains high until a logic 0 is written to it.
6	FDT	Frame Detect. 0 = Indicates link has not established frame lock. 1 = Indicates link frame lock has been established.
5:4	Reserved	Read returns zero.
3:0	LCS[3:0]	Loop Current Sense. Four-bit value returning the loop current. It is decoded from the LVCS bits. See LVCS bits for line voltage and current monitoring. When off-hook, these bits are decoded as follows from LVCS[4:0]: LCS[3:0] = LVCS[4:1] except when LVCS[4:0] = 11110, LCS[3:0] = 1110 or when LVCS[4:0] = 00001, LCS[3:0] = 0001. When on-hook, LCS[3:0] = LVCS[4:1].

3.19.1.13 DAA Register 13

7	6	5	2	1	0
Reserved	CBID	REVB[3:0]		ARXB	ATXB
	R	R		R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = N/A

Figure 3−37. Register 13 − Chip B Revision Register Layout

Table 3−39. Register 13 − Chip B Revision Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	Reserved	Read returns zero.
6	CBID	Chip B ID. 0 = Indicates the line side is domestic only. 1 = Indicates the line side has international support.
5:2	REVB[3:0]	Chip B Revision. Four-bit value indicating the revision of the DAA (line-side) chip.
1	ARXB	Receive Gain. 0 = 0 dB gain is applied. 1 = A 6 dB gain is applied to the receive path. Note: This bit should not be used. The DAA has the additional receive gain settings ARX[2:0]. ARXB should be set to 0 and the ARX bits should be used.
0	ATXB	Transmit Attenuation. 0 = 0 dB gain is applied. 1 = A 3 dB attenuation is applied to the transmit path. This bit should not be used. The DAA has the additional transmit gain settings ATX[2:0]. ATXB should be set to 0 and the ATX bits should be used.

3.19.1.14 DAA Register 14

7	3	2	1	0
Reserved		CHK	CIP	SAFE
		R	R	R

LEGEND: R = Read, W = Write, Reset settings = 0000-0100

Figure 3−38. Register 14 − Line-Side Validation Register Layout

Table 3−40. Register 14 − Line Side Validation Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:3	Reserved	Read returns zero.
2	CHK	Line-Side Chip Verification Performed. When the line-side device is first enabled, an automatic safety check is performed internally to ensure that it is the correct device. 0 = A check has been performed on the line-side chip to ensure that it is the proper device. 1 = A check has not yet been performed on the line-side device to ensure that it is the proper device.
1	CIP	Line-Side Chip Verification In Progress 0 = The line-side device check is not in progress. 1 = The line-side device check is currently in progress.
0	SAFE	Line-Side Chip Verification Result. This bit is only valid after a line side verification check has been performed. Thus, the CHK and CIP bits should be clear when this bit is read. 0 = A correct line-side device was detected. Chip operation is normal. 1 = An incorrect line-side device was detected. The integrated system-side module will not function properly. Register accesses can still be performed, but data transfer will not occur.

3.19.1.15 DAA Register 15

7	6 4	3	2 0
TXM	ATX[2:0]	RXM	ARX[2:0]
R/W	R/W	R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = 0000-0000

Figure 3−39. Register 15 − TX/RX Gain Control Register Layout

Table 3−41. Register 15 − TX/RX Gain Control Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	TXM	Transmit Mute. 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	Analog Transmit Attenuation. 000 = 0 dB attenuation. 001 = 3 dB attenuation. 010 = 6 dB attenuation. 011 = 9 dB attenuation. 1xx = 12 dB attenuation. Note: The ATXB bit must be 0 if these bits are used.
3	RXM	Receive Mute. 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	Analog Receive Gain/On-Hook Line Monitor Receive Attenuation. This register functions as both a gain setting for the regular DAA receive path and an attenuation setting for the new low-power on-hook line monitor ADC receive path. **Receive Gain** / **On-Hook Line Monitor Attenuation** 000 = 0 dB gain. / 000 = 0 dB attenuation. 001 = 3 dB gain. / 001 = 1 dB attenuation. 010 = 6 dB gain. / 010 = 2.2 dB attenuation. 011 = 9 dB gain. / 011 = 3.5 dB attenuation. 1xx = 12 dB gain. / 1xx = 5 dB attenuation. Note: The ARXB bit must be 0 if these bits are used.

3.19.1.16 DAA Register 16

7	6	5	4	3	2	1	0
OFF/SQL2	OHS	ACT	Reserved	DCT[1:0]		RZ	RT
R/W	R/W	R/W		R/W		R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = 0000-1000

Figure 3−40. Register 16 − International Control 1 Register Layout

Table 3−42. Register 16 − International Control 1 Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	OFF/SQL2	DC Termination Off (DAA is off-hook). When the DAA is off-hook, this bit functions as the DC Termination Off bit. When the DAA is on-hook, this bit functions as the Enhanced Ring Detect Network Squelch bit. 0 = Normal operation. 1 = DC termination disabled and the device presents an 800 W DC impedance to the line which is used to enhance operation with a parallel phone. The DCT pin voltage is also reduced for improved low line voltage performance. Enhanced Ring Detect Network Squelch (DAA is on-hook). To properly receive caller ID data, this bit must be set following a polarity reversal or ring signal detection and must be left enabled during the reception of caller ID data. It should be disabled before the start of the next ring signal. It is used to recover the offset on the RNG1/2 pins after a polarity reversal or ring signal. 0 = Normal operation. 1 = Enhanced squelch function is enabled.
6	OHS	On-Hook Speed. 0 = The DAA will execute a fast on-hook. (Off-hook counter = 1024/Fs seconds.) 1 = The DAA will execute a slow, controlled on-hook. (Off-hook counter = 4096/Fs seconds.)
5	ACT	AC Termination Select. 0 = Selects the real impedance. 1 = Selects the complex impedance.
4	Reserved	Read returns zero.
3:2	DCT[1:0]	DC Termination Select. 00 = Low Voltage Mode. (Transmit level = –5 dBm). 01 = Japan Mode. Lower voltage mode. (Transmit level = –3 dBm). 10 = FCC Mode. Standard voltage mode. (Transmit level = –1 dBm). 11 = CTR21 Mode. Current limiting mode. (Transmit level = –1 dBm).
1	RZ	Ringer Impedance. 0 = Maximum (high) ringer impedance. 1 = Synthesized ringer impedance. C15, R14, Z2, and Z3 must not be installed when setting this bit. See Section 3.19.2.15, Ringer Impedance.
0	RT	Ringer Threshold Select. Used to satisfy country requirements on ring detection. Signals below the lower level will not generate a ring detection; signals above the upper level are ensured to generate a ring detection. 0 = 11 to 22 V_{RMS} 1 = 17 to 33 V_{RMS}

3.19.1.17 DAA Register 17

7	6	5	4	3	2	1	0
Reserved	MCAL	CALD	LIM	OPE	BTE	ROV	BTD
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = 0000-0000

Figure 3−41. Register 17 − International Control 2 Register Layout

Table 3−43. Register 17 − International Control 2 Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	Reserved	Must be zero.
6	MCAL	Manual Calibration. 0 = No calibration. 1 = Initiate calibration.
5	CALD	Auto-Calibration Disable. 0 = Enable auto-calibration. 1 = Disable auto-calibration.
4	LIM	Current Limit This bit only affects chip operation when the CTR21 DC termination mode is selected. 0 = No current limiting in CTR21 mode. 1 = Enables current limiting in CTR21 mode. The DC termination will current limit before 60 mA.
3	OPE	Overload Protect Enable. 0 = Disable overload protection. 1 = Enable overload protection. The overload protection feature prevents damage to the DAA when going off-hook with excessive line current or voltage. When off-hook, if OPE is set and LVCS = 11111, the DC termination is disabled (800 W presented to the line), the hookswitch current is reduced, and the OPD bit is set. The OPE bit should be written ~25 ms after going off-hook; it should be written to 0 to reset.
2	BTE	Billing Tone Protect Enable. 0 = Disabled. 1 = Enabled. When set, the DAA will automatically respond to a collapse of the line-derived power supply during a billing tone event. When off-hook, if BTE = 1 and BTD goes high, the DC termination is changed to present 800 W to the line, and the DCT pin stops tracking the receive input pin. During normal operation, the DCT pin tracks the receive input.
1	ROV	Receive Overload. This bit is set when the receive input has an excessive input level (i.e., receive pin goes below ground). This bit is cleared by writing a zero to this location. 0 = Normal receive input level. 1 = Excessive receive input level.
0	BTD	Billing Tone Detected. This bit will be set if a billing tone is detected. This bit is cleared by writing a zero to this location. 0 = No billing tone detected. 1 = Billing tone detected.

3.19.1.18 DAA Register 18

7	6	5	4	3	2	1	0
FULL	DIAL	FJM	VOL	FLVM	MODE	RFWE	SQLH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read, W = Write, Reset settings = 0000-0000

Figure 3−42. Register 18 − International Control 3 Register Layout

Table 3−44. Register 18 − International Control 3 Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7	FULL	Full Scale. 0 = Default. 1 = Transmit/receive full scale = +3.2 dBm. This bit changes the full scale of the ADC and DAC from –1 dBm min to +3.2 dBm min. When this bit is set, R2 must be changed from 402 W to 243 W. This mode, which can be useful for certain voice applications, should only be used in the FCC/600 W AC Termination mode.
6	DIAL	DTMF Dialing Mode. This bit should be set during DTMF dialing in CTR21 mode if LCS[3:0] < 6 or LVCS[4:0] < 12 decimal. 0 = Normal operation. 1 = Increase headroom for DTMF dialing.
5	FJM	Force Japan DC Termination Mode. 0 = Normal Gain 1 = When the DCT[1:0] bits are set to 10b (FCC mode), setting this bit will force the Japan DC termination mode while allowing for a transmit level of –1 dBm. DTMF dialing are also supported. See Section 3.19.2.16, DTMF Dialing.
4	VOL	Line Voltage Adjust. When set, this bit will adjust the TIP-RING line voltage. Lowering this voltage will improve margin in low voltage countries. Raising this voltage may improve large signal distortion performance. 0 = Normal operation. 1 = Lower DCT voltage. **Description / DCT / OFF / VOL / VDCT / DELTA** CTR21/FCC / 1x / 0 / 0 / 4.00 / CTR21/FCC+VOL / 1 / 0 / 1 / 3.51 / 0.49 V JAPAN / 01 / 0 / 0 / 3.15 / JAPAN+VOL / 01 / 0 / 1 / 2.87 / 0.28 V LVMode / 00 / 0 / 0 / 2.65 / LVMode+VOL / 00 / 0 / 1 / 2.47 / 0.18 V CTR21/FCC+OFF / 1x / 1 / 0 / 2.33 / CTR21/FCC+VOL+OFF / 1x / 1 / 1 / 2.21 / 0.12 V JAPAN+OFF / 01 / 1 / 0 / 2.10 / JAPAN+VOL+OFF / 01 / 1 / 1 / 2.01 / 0.09 V LVMode+OFF / 00 / 1 / 0 / 1.94 / LVMode+VOL+OFF / 00 / 1 / 1 / 1.87 / 0.07 V
3	FLVM	Force Low Voltage DC Termination Mode. 0 = Normal gain. 1 = When the DCT[1:0] bits are set to 10b (FCC mode), setting this bit will force the Low Voltage DC termination mode while allowing for a transmit level of –1 dBm. DTMF dialing are also supported. See Section 3.19.2.16, DTMF Dialing.

Table 3−44. Register 18 − International Control 3 Bit Descriptions (Continued)

<table>
<tr><th colspan="2">BIT</th><th>DESCRIPTION</th></tr>
<tr><th>NO.</th><th>NAME</th><th></th></tr>
<tr><td>2</td><td>MODE</td><td>
MODE Control.
This bit is used to enable the on-hook line monitor ADC and the line voltage monitor.
<table>
<tr><th>MODE</th><th>OH</th><th>ONHM</th><th>Line Function</th><th>SDO</th><th>LVCS[4:0]</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>on-hook</td><td>ring data</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>on-hook</td><td>line data using the higher current line monitor</td><td>11111 if a line voltage exists, or 00000 if no line voltage exists</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>off-hook</td><td>line data</td><td>loop current</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>off-hook/Fast DCT mode</td><td>line data</td><td>loop current</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>on-hook</td><td>ring data</td><td>line voltage</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>on-hook</td><td>line data using the low current line monitor</td><td>line voltage</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>force on-hook</td><td>no data is transmitted on SDO in this mode</td><td>line voltage</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>force on-hook</td><td>line data using the low current line monitor</td><td>line voltage</td></tr>
</table>
Notes:
1) If RZ = 1, LVCS[4:0] = either 11111 or 00000 during a ring event. All ones are shown if a line voltage exists; all zeroes are shown if no line voltage exists.
2) Force on-hook mode puts the DAA into an on-hook state without restarting the off-hook counter. This is used to support Type II caller ID.
3) The MODE bit is in a different register than the OH and ONHM bits. The user should write the registers in a sequence so as not to pass through an undesired state.
4) Fast DCT mode puts the DAA into an off-hook state that is intended to quickly settle the line voltage just after going off-hook. While in this mode, data transmission is not recommended. This is used to support Type II caller ID.
5) The ONHM bit should be cleared before setting the OH bit. If both bits need to be set, the OH bit should be set first, and then the ONHM bit should be set in a separate register access.
</td></tr>
<tr><td>1</td><td>RFWE</td><td>Ring Detector Full Wave Rectifier Enable.
When set, the ring detection circuitry provides full-wave rectification. This will affect the $\overline{\text{RGDT}}$ pin as well as the data stream presented on SDO during ring detection.
0 = Half Wave.
1 = Full Wave.</td></tr>
<tr><td>0</td><td>SQLH</td><td>Ring Detect Network Squelch.
This bit must be set, then cleared after at least 1 ms, following a polarity reversal or ring signal detection. It is used to quickly recover the offset on the RNG1/2 pins after a polarity reversal or ring signal. If the SQL2 bit is enabled during CID data reception, this bit should not be used.
0 = Normal operation.
1 = Squelch function is enabled.</td></tr>
</table>

3.19.1.19 DAA Register 19

7	3	2	1	0
LVCS[4:0]		OVL	DOD	OPD
R		R	R	R

LEGEND: R = Read, W = Write, Reset settings = 0000-0000

Figure 3−43. Register 19 − International Control 4 Register Layout

Table 3−45. Register 19 − International Control 4 Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
7:3	LVCS[4:0]	Line Voltage/Current Sense. Represents either the line voltage, loop current, or on-hook line monitor depending on the state of the MODE, OH, and ONHM bits. On-Hook Voltage Monitor (2.75 V/bit). 00000 = No line connected. 00001 = Minimum line voltage (V_{MIN} = 3 V ± 0.5 V). 11111 = Maximum line voltage (87 V ± 20%). The line voltage monitor full scale may be modified by changing R5 as follows: $V_{MAX} = V_{MIN} + 4.2 (10M + R5 + 1.6k)/[(R5 +1.6k)*5]$ Off-Hook Loop Current Monitor (3 mA/bit). 00000 = Loop current is less than required for normal operation. 00001 = Minimum normal loop current. 11110 = Maximum normal loop current. 11111 = Loop current is excessive (overload). Overload > 140 mA in all modes except CTR21. Overload > 54 mA in CTR21 mode.
2	OVL	Overload Detected. This bit has the same function as ROV in Register 17, but will clear itself after the overload has been removed. See Section 3.19.2.18, Billing Tone Detection. This bit is only masked by the off-hook counter and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
1	DOD	Recal/Dropout Detect. When the line-side device is off-hook, it is powered from the line itself. If this line-derived power supply collapses, such as when the line is disconnected, this bit is set to 1. Sixteen frames (16/Fs) after the line-derived power supply returns, this bit is set to 0. When on-hook, this bit is set to 0. 0 = Normal operation. 1 = Line supply dropout detected when on-hook.
0	OPD	Overload Protect Detected. 0 = Inactive. 1 = Overload protection active. Note: See description of overload protect operation (OPE bit).

3.19.2 Operation of the DSP Interface to the DAA

The DAA is connected to the DSP through the McBSP. All data, control, and configuration information is communicated across this interface. Note that the McBSP CPU-to-DAA connection is internal and some or all of the McBSP signals may not be available externally. See the device pinout and McBSP description for further information.

The CPU clock is used as the master clock for the DAA, and from this master clock, the DAA derives the serial port clock, transmit and receive frame sync signals, and receive data (from the DAA). Transmit data is driven from the processor side of the McBSP.

Note that while the DAA master clock must be operated at a rate of 58.9824 MHz, the DAA master clock from the CPU can be programmed to run at either the CPU clock rate or half of the CPU clock rate. This is selected through the DAACLKDV bit in the memory mapped bank switching control register (BSCR) located at data memory address 0029h. See Section 3.6.2 for more information on this memory mapped register.

The capability to operate the DAA master clock at these two different clock rates allows the CPU to run at either the DAA frequency of 58.9824 MHz, or at 117.9648 MHz. Operating the CPU at the lower frequency saves power, while operating at the higher frequency allows use of the much faster processing rate.

Before the DSP attempts to interact with the DAA in any fashion, the DAA should be held in its reset state, and the McBSP should be initialized to its proper operating configuration. Note that the McBSP initialization should be completed before the DAA is released from its reset state.

The DAA is reset using the dedicated DAA reset signal generated from the DSP. This signal comes from a bit in the memory mapped bank switching control register (BSCR), which is located at data memory address 0029h. Refer to Section 3.6.2 for more information on this memory mapped register.

The DAA reset signal is initialized to an active (resetting) state when the DSP is reset, therefore, following a DSP reset, initialization of the McBSP can begin.

For proper communication with the DAA, several aspects of McBSP configuration are critical. FSXM and FSRM should be cleared to zero, since BFSR and BFSX are inputs. FSRP and FSXP should be set to one, since the frame pulses from the DAA are low-true. Transmit and receive data delay (XDATDLY, RDATDLY) should be set to zero.

Note that there may be additional system-dependent serial port configurations that may be required. Refer to the serial port description section and the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for further information.

Once the McBSP is properly initialized, the DAA can be taken out of reset. To take the DAA out of reset, the DSP software must deactivate the DAA reset signal by setting it to a 1 (the DAA reset signal is low-true). After the DAA is taken out of reset, serial communications with the DAA can begin.

The master clock frequency and the value of the sample rate control register (DAA register 9) determine the sample rate (Fs). The serial port clock runs at 256 bits per frame, where the frame rate is equivalent to the sample rate.

Serial port communications with the DAA are conducted in two types of frames or timeslots. These timeslots are designated primary and secondary timeslots.

The DAA transfers 15-bit telephony data in the primary timeslot and 16-bit control data in the secondary timeslot. Figure 3−44 shows the relative timing of the serial frames. Primary frames occur at the frame rate and are always present. To minimize CPU overhead, secondary frames are present only when requested.

Secondary frames are requested using the LSB of the 16-bit transmit data word as a flag to request a secondary transfer. Only 15-bit TX data is transferred, resulting in a slight loss of SNR, but allowing software control of the secondary frames. Therefore, transmitted data should always have a zero LSB unless a secondary time is being requested.

Figure 3−45 and Figure 3−46 illustrate the secondary frame read cycle and write cycle, respectively. During a read cycle, the R/$\overline{W}$ bit is set high and the 5-bit address field contains the address of the register to be read. The contents of the 8-bit control register are placed in the serial data sent to the CPU. During a write cycle, the R/$\overline{W}$ bit is low and the 5-bit address field contains the address of the register to be written. The 8-bit data to be written immediately follows the address on the serial data transmitted from the CPU. Only one register can be read or written during each secondary frame. See Section 3.19.1, DAA Control Registers, for definition of the register addresses and functions.

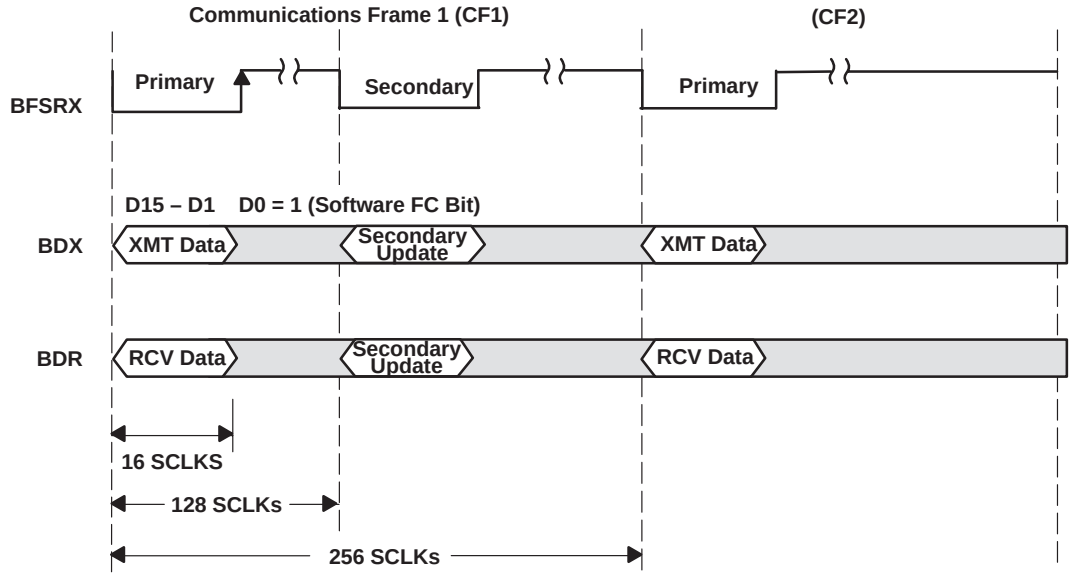


Figure 3−44. Software FC/$\overline{RGDT}$ Secondary Request

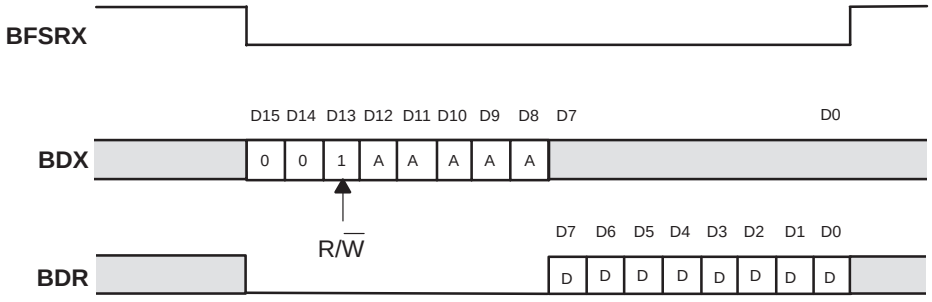


Figure 3−45. Secondary Communication Data Format—Read Cycle

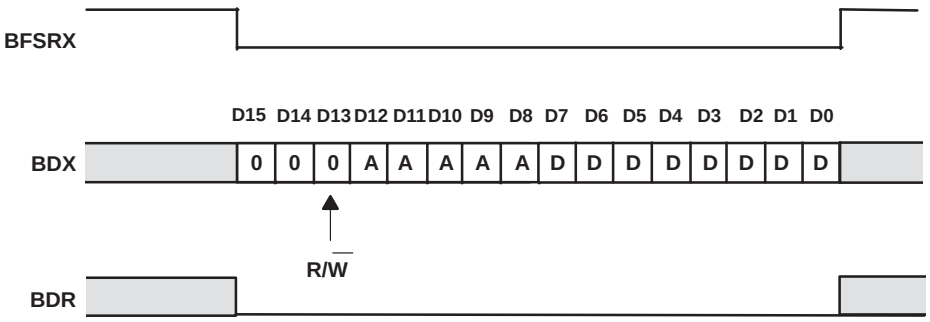


Figure 3−46. Secondary Communication Data Format—Write Cycle

3.19.2.1 DAA Initialization

When the integrated system-side module and the line-side chip are initially powered up, the DAA registers will have default values that ensure the line-side chip is powered down with no possibility of loading the line (i.e., off-hook). An example initialization procedure is outlined below:

1. Program the desired sample rate with the Sample Rate Control Register.
2. Wait until the DAA PLL is locked. This time is between 100 ms and 1 ms.
3. Write a 00H into the DAA Control 2 Register. This powers up the line-side chip.
4. Set the desired line interface parameters (i.e., DCT[1:0], ACT, OHS, RT, LIM[1:0], and VOL) as shown in Table 3−49.

After this procedure is complete, the DAA is ready for ring detection and off-hook.

3.19.2.2 Power Supply

When on-hook, the DAA draws power across the isolation link from the system-side module. When off-hook, power is drawn from the 2-wire line. Thus, no power supply connections are needed for the DAA.

3.19.2.3 Isolation Barrier

The DAA achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with proprietary signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. The high voltage capacitors isolate the system-side from the line-side chip. All transmit, receive, control, ring detect, and caller ID data are communicated through this barrier.

The communications link is disabled by default. To enable it, the PDL bit must be cleared. No communication between the system-side module and the line-side chip can occur until this bit is cleared. When the PDL bit is cleared, a check is performed to ensure the line-side device is of the correct type. If it is not, the system-side module will not function.

3.19.2.4 Transmit/Receive Full Scale Level

The DAA supports programmable maximum transmit and receive levels. The full scale TX/RX level is established by writing the FULL bit in Register 18. With FULL = 1, the full scale TX/RX level is increased to 3.2 dBm to support certain FCC voice applications which require higher TX/RX levels. When FULL = 1, R2 must be changed from 402 W to 243 W. The default full scale value is –1 dBm (FULL = 0). Note that this higher TX/RX full scale mode must be used in FCC/600 W termination mode.

3.19.2.5 Filter Responses

Figure 3−47 through Figure 3−50 show the frequency response of the receive and transmit low-pass filters. The overall filter responses along with details of the stopband response are shown.

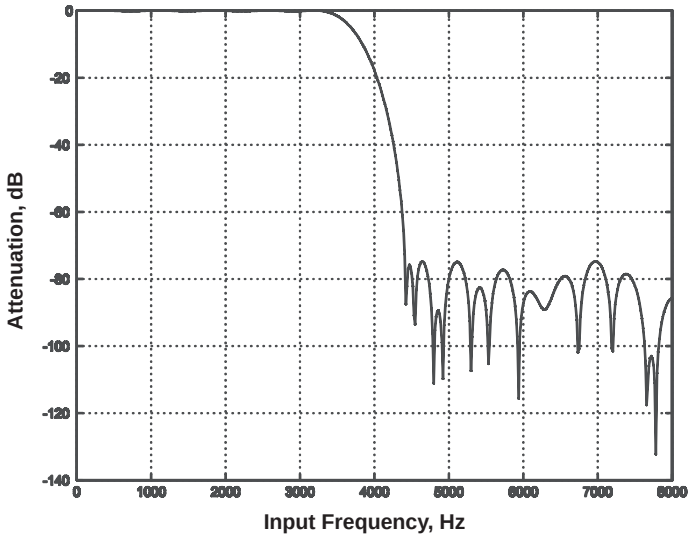


Figure 3−47. FIR Receive Filter Response

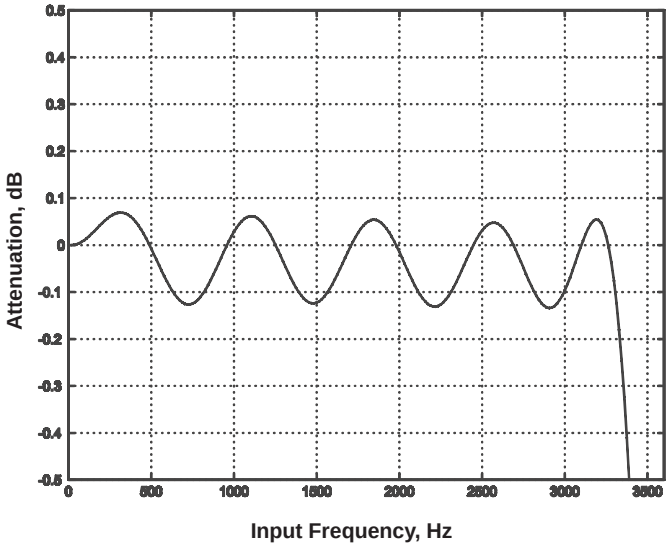


Figure 3−48. FIR Receive Filter Passband Ripple

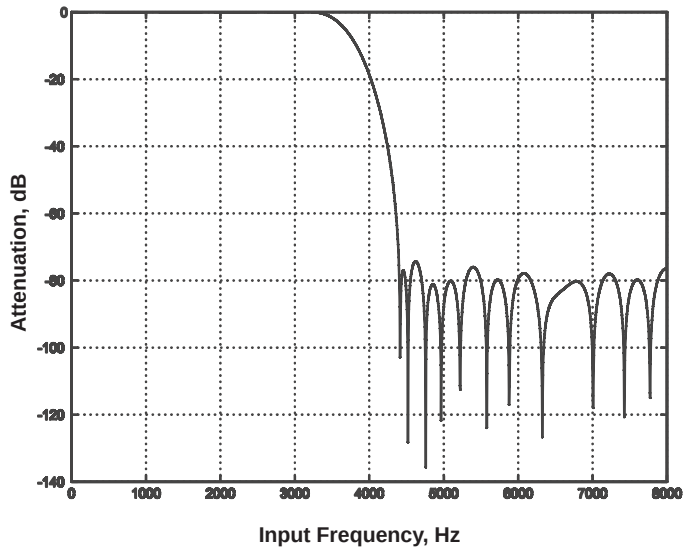


Figure 3−49. FIR Transmit Filter Response

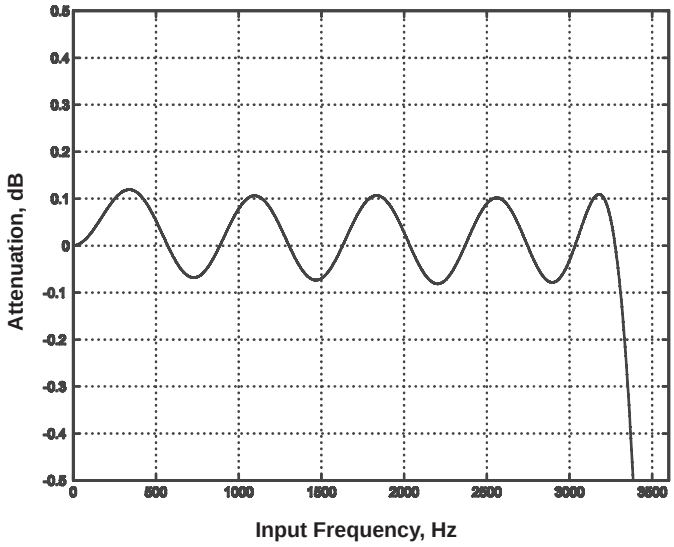


Figure 3−50. FIR Transmit Filter Passband Ripple

For Figure 3−47 through Figure 3−50, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(0.1\ dB)} = 0.4125\ Fs$

$F_{(-3\ dB)} = 0.45\ Fs$

where Fs is the sample frequency.

3.19.2.6 Parallel Handset Detection

The DAA is capable of detecting a parallel handset going off-hook. When the DAA is off-hook, the loop current can be monitored via the LVCS bits. A significant drop in loop current can signal a parallel handset going off-hook. If a parallel handset causes the LVCS bits to read all 0's, the Drop-Out Detect (DOD) bit may be checked to verify a valid line still exists.

When on-hook, the LVCS bits may also be read to determine the line voltage. Significant drops in line voltage may also be used to detect a parallel handset. For the DAA to operate in parallel with another handset, the parallel handset must have a sufficiently high DC termination to support two off-hook DAAs on the same line. The OFF bit in Register 16 is designed to improve parallel handset operation by changing the DC impedance from 50 W to 800 W and reducing the DCT pin voltage.

3.19.2.7 Line Voltage/Loop Current Sensing

The DAA has the ability to measure both line voltage and loop current. The five bit LVCS register reports line voltage measurements when on-hook, loop current measurements when off-hook, or on-hook line monitor data depending on the state of the MODE, OH, and ONHM bits. Using the LVCS bits, the user can determine the following:

- When on-hook, detect if a line is connected.
- When on-hook, detect if a parallel phone is off-hook.
- When off-hook, detect if a parallel phone goes on or off-hook.
- Detect if enough loop current is available to operate.
- Detect if there is an overload condition which could damage the DAA (see overload protection feature).

3.19.2.8 Line Voltage Measurement

The DAA reports the line voltage with the LVCS bits in Register 19. LVCS has a full scale of 87 V with an LSB of 2.75 V. The first code ($0 \rightarrow 1$) is skewed such that a 0 indicates that the line voltage is < 3 V. The accuracy of the LVCS bits is ±20%. The user can read these bits directly through the LVCS register when on-hook and the MODE bit is set to 1. A typical transfer function is shown in Figure 3−51.

3.19.2.9 Loop Current Measurement

When the DAA is off-hook, the LVCS bits measure loop current in 3 mA/bit resolution. These bits enable the user to detect another phone going off-hook by monitoring the DC loop current. The line voltage current sense transfer function is shown in Figure 3−52 and is detailed in Table 3−46.

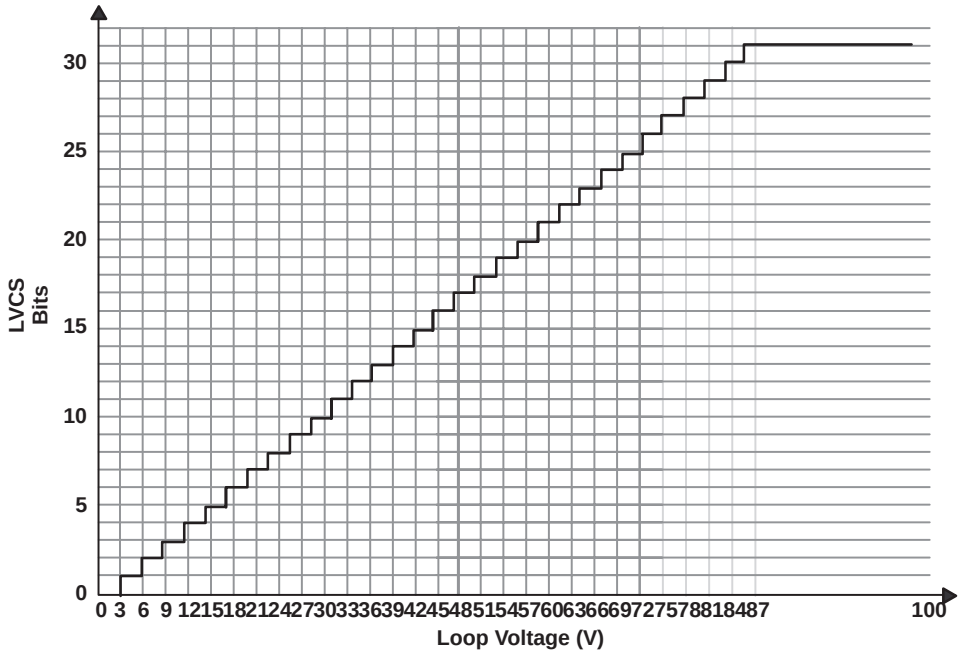


Figure 3−51. Typical Loop Voltage LVCS Transfer Function

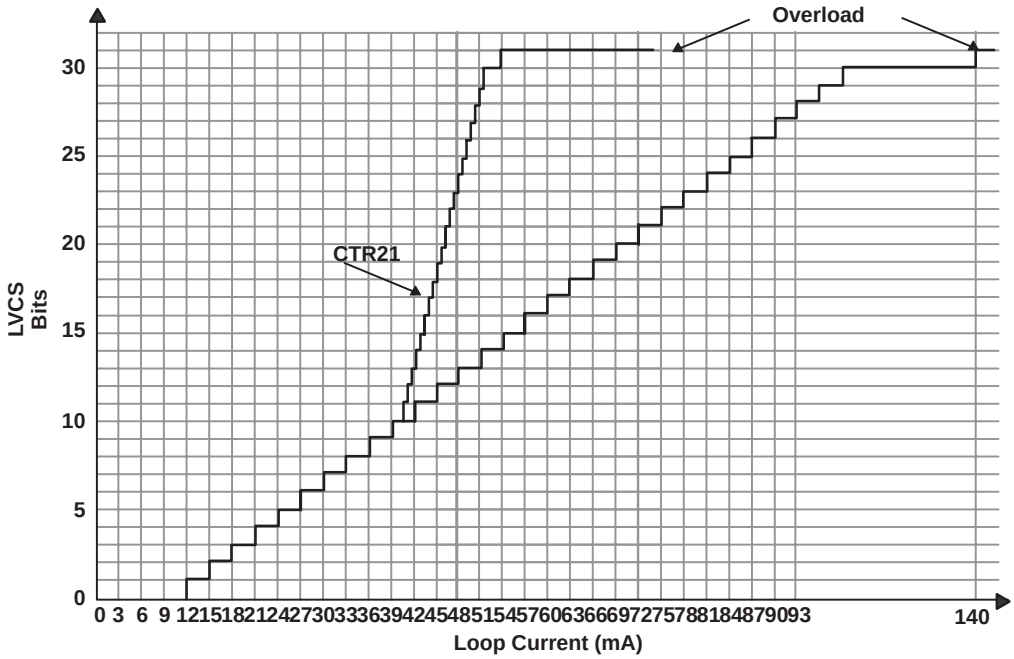


Figure 3−52. Typical Loop Current LVCS Transfer Function

Table 3−46. Loop Current Transfer Function

LVCS[4:0]	CONDITION
00000	Insufficient line current for normal operation. Use the DOD bit to determine if a line is still connected.
00001	Minimum line current for normal operation.
11111	Loop current is excessive (overload). Overload > 140 mA in all modes except CTR21. Overload > 54 mA in CTR21 mode.

3.19.2.10 Off-Hook

The communication system generates an off-hook command by setting the OH bit. With the $\overline{OH}$ bit set, the system is in an off-hook state.

The off-hook state is used to seize the line for incoming/outgoing calls and can also be used for pulse dialing. When the DAA is on-hook, negligible DC current flows through the hookswitch. When the DAA is placed in the off-hook state, the hookswitch transistor pair, Q1 and Q2, turn on. This applies a termination impedance across TIP and RING and causes DC loop current to flow. The termination impedance has both an AC and DC component.

When executing an off-hook sequence, the DAA requires 1548/Fs seconds to complete the off-hook and provide phone-line data on the serial link. This includes the 12/Fs filter group delay. If necessary, for the shortest delay, a higher Fs may be established prior to executing the off-hook, such as an Fs of 10.286 kHz. The delay allows for line transients to settle prior to normal use.

3.19.2.11 DC Termination

The DAA has four programmable DC termination modes which are selected with the DCT[1:0] bits in Register 16.

FCC mode (DCT[1:0] = 10 b), shown in Figure 3−53, is the default DC termination mode and supports a transmit full scale level of –1 dBm at TIP and RING. This mode meets FCC requirements in addition to the requirements of many other countries.

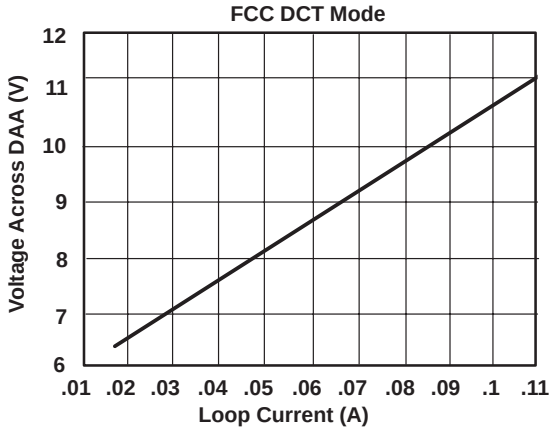


Figure 3−53. FCC Mode I/V Characteristics

CTR21 mode (DCT[1:0] = 11 b), shown in Figure 3−54, provides current limiting while maintaining a transmit full scale level of –1 dBm at TIP and RING. In this mode, the DC termination will current limit before reaching 60 mA if the LIM bit is set.

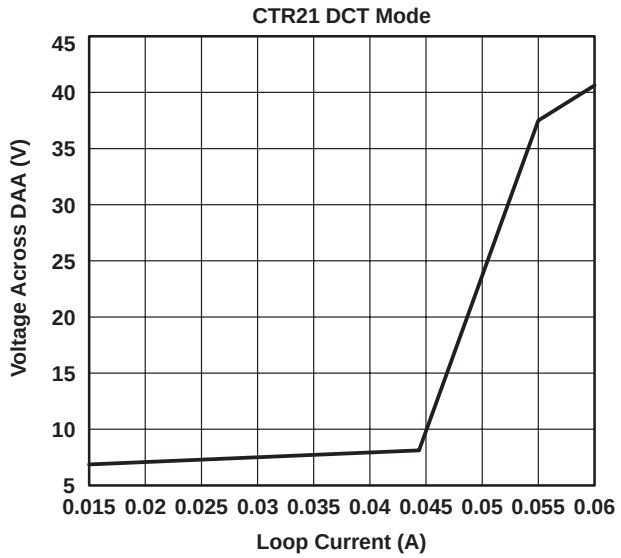


Figure 3−54. CTR21 Mode I/V Characteristics

Japan mode (DCT[1:0] = 01 b), shown in Figure 3−55, is a lower voltage mode and supports a transmit full scale level of –2.71 dBm. Higher transmit levels for DTMF dialing are also supported. See Section 3.19.2.16, DTMF Dialing. The low voltage requirement is dictated by countries such as Japan and Malaysia.

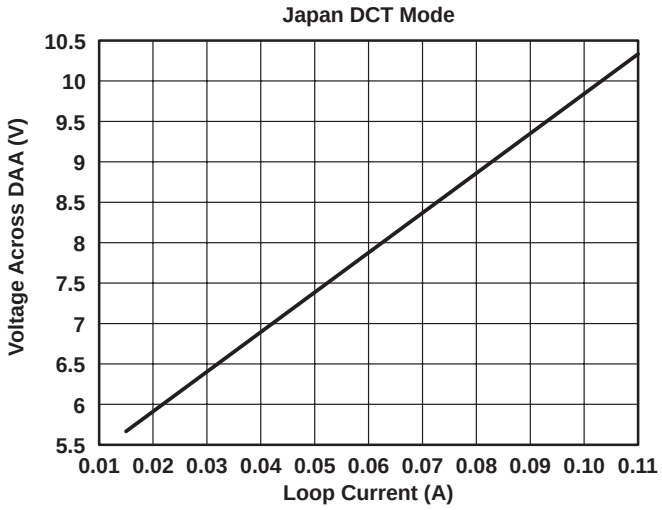


Figure 3−55. Japan Mode I/V Characteristics

Low Voltage mode (DCT[1:0] = 00b), shown in Figure 3−56, is the lowest line voltage mode supported on the DAA, with a transmit full scale level of –5 dBm. Higher transmit levels for DTMF dialing are also supported. See Section 3.19.2.16, DTMF Dialing. This low voltage mode is offered for situations that require very low line voltage operation. It is important to note that this mode should only be used when necessary, as the dynamic range will be significantly reduced and thus the DAA will not be able to transmit or receive large signals without clipping them.

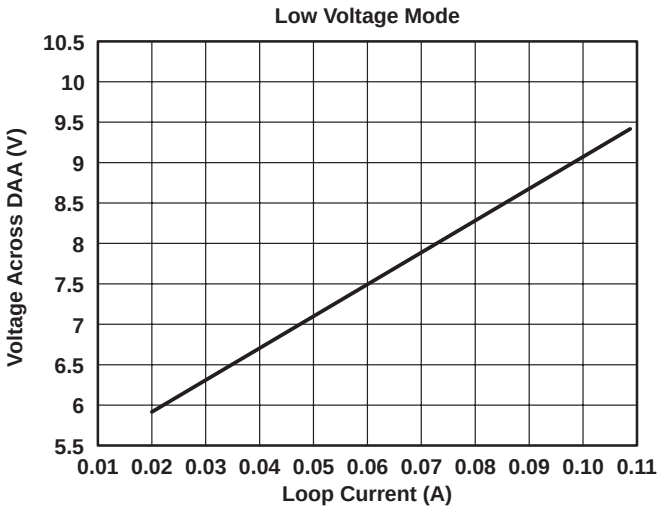


Figure 3−56. Low-Voltage Mode I/V Characteristics

3.19.2.12 DC Termination Considerations

Under certain line conditions, it may be beneficial to use other DC termination modes not intended for a particular world region. For instance, in countries that comply with the CTR21 standard, improved distortion characteristics can be seen for very low loop current lines by switching to FCC mode. Thus, after going off-hook in CTR21 mode, the loop current monitor bits (LVCS[4:0]) may be used to measure the loop current, and if LVCS[4:0] < 6, it is recommended that FCC mode be used.

Additionally, for very low voltage countries, such as Japan and Malaysia, the following procedure should be used to optimize distortion characteristics and maximize transmit levels:

1. When first going off-hook, use the Low Voltage mode with the VOL bit set to 1.
2. Measure the loop current using the LVCS[4:0] bits.
3. If LVCS[4:0] ≤ 2, maintain the current settings and proceed with normal operation.
4. If LVCS[4:0] > 2 or < 6, switch to Japan mode, leave the VOL bit set, and proceed with normal operation.
5. If LVCS[4:0] ≥ 6, switch to FCC mode, set the VOL bit to 0, and proceed with normal operation.

NOTE:

A single decision of DC termination mode following off-hook is appropriate for most applications. However, during PTT testing, a false DC termination I/V curve may be generated if the DC I/V curve is determined following a single off-hook event.

Finally, Australia has separate DC termination requirements for line seizure versus line hold. Japan mode may be used to satisfy both requirements. However, if a higher transmit level for modem operation is desired, switch to FCC mode 500 ms after the initial off-hook. This will satisfy the Australian DC termination requirements.

3.19.2.13 AC Termination

The DAA has two AC Termination impedances which are selected with the ACT bit.

ACT=0 is a real, nominal 600 W termination which satisfies the impedance requirements of FCC part 68, JATE, and other countries. This real impedance is set by circuitry internal to the DAA as well as the resistor R2 connected to the REXT pin.

ACT=1 is a complex impedance which satisfies the impedance requirements of Australia, New Zealand, South Africa, CTR21, and some European NET4 countries such as the UK and Germany. This complex impedance is set by circuitry internal to the DAA as well as the complex network formed by R12, R13, and C14 connected to the REXT2 pin.

3.19.2.14 Ring Detection

The ring signal is capacitively coupled from TIP and RING to the RNG1 and RNG2 pins. The DAA supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal as well as the ring signal. See Section 3.19.2.21, Caller ID. The ring detection threshold is programmable with the RT bit.

The ring detector output can be monitored in one of two ways. The first method uses the register bits RDTP, RDTN, and RDT. The second method uses the SDO output internal to the integrated system-side module.

The DSP must detect the frequency of the ring signal in order to distinguish a ring from pulse dialing by telephone equipment connected in parallel.

A positive ringing signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. RNG1 and RNG2 are pins 5 and 6 of the DAA. Conversely, a negative ringing signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2.

The first ring detect method uses the ring detect bits (RDTP, RDTN, and RDT). The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. Whenever the signal on RNG1-RNG2 is above the positive ring threshold the RDTP bit is set. Whenever the signal on RNG1-RNG2 is below the negative ring threshold the RDTN bit is set. When the signal on RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFWE bit is a 0 or a 1, a positive ringing signal will set the RDT bit for a period of time. The RDT bit will not be set for a negative ringing signal.

The RDT bit acts as a one shot. Whenever a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter counting down to zero, then the RDT bit will return to zero. The length of this count (in seconds) is 65536 divided by the sample rate. The RDT will also be reset to zero by an off-hook event.

The second ring detect method uses the internal serial output of the integrated system-side module (SDO) to transmit ring data. If the interface is active (PDL = 0) and the device is not off-hook or not in on-hook line monitor mode, the ring data will be sent by the system-side module to the host processor. The waveform on SDO depends on the state of the RFWE bit.

When the RFWE bit is 0, SDO will be –32768 (0x8000) while the RNG1-RNG2 voltage is between the thresholds. When a ring is detected, SDO will transition to +32767 while the ring signal is positive, then go back to –32768 while the ring is near zero and negative. Thus a near square wave is presented on SDO that swings from –32768 to +32767 in cadence with the ring signal.

When the RFWE bit is 1, SDO will sit at approximately +1228 while the RNG1-RNG2 voltage is between the thresholds. When the ring goes positive, SDO will transition to +32767. When the ring signal goes near zero, SDO will remain near 1228. Then as the ring goes negative, the SDO will transition to –32768. This will repeat in cadence with the ring signal.

The best way to observe the ring signal on SDO is simply to observe the MSB of the data. The MSB will toggle in cadence with the ring signal independent of the ring detector mode. This is adequate information for determining the ring frequency. The MSB of SDO will toggle at the same frequency as the ring signal.

3.19.2.15 Ringer Impedance

The ring detector in a typical DAA is AC coupled to the line with a large, 1 μF, 250 V decoupling capacitor. The ring detector on the DAA is also capacitively coupled to the line, but it is designed to use smaller, less expensive 1.8 nF capacitors. Inherently, this network produces a very high ringer impedance to the line on the order of 800 to 900 kW. This value is acceptable for the majority of countries, including FCC and CTR21.

Several countries including the Czech Republic, Poland, South Africa and South Korea, require a maximum ringer impedance. For Poland, South Africa, and South Korea, the maximum ringer impedance specification can be met with an internally synthesized impedance by setting the RZ bit in Register 16.

For Czech Republic designs, an additional network comprised of C15, R14, Z2, and Z3 is required. (See Figure 3−57 and Table 3−47.) This network is not required for any other country. However, if this network is installed, the RZ bit should not be set for any country.

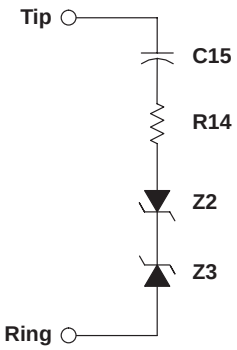


Figure 3−57. Ringer Impedance Network

Table 3−47. Current Values—Optional Ringer Impedance Network

SYMBOL	VALUE
C15	1 µF, 250 V
R14	7.5 kW, 1/4 W
Z2,Z3	5.6 V

3.19.2.16 DTMF Dialing

In CTR21 DC termination mode, the DIAL bit should be set during DTMF dialing if the LVCS[4:0] bits are less than 12. Setting this bit increases headroom for large signals. This bit should not be used during normal operation, or if the LVCS[4:0] bits are greater than 11.

In Japan DC termination mode, the system-side module attenuates the transmit output by 1.7 dB to meet headroom requirements. Similarly, in Low Voltage termination mode, the system-side module attenuates the transmit output by 4 dB. However, when DTMF dialing is desired in these modes, this attenuation must be removed. This is achieved by entering the FCC DC termination mode and setting either the FJM or the FLVM bits. When in the FCC DC termination modes, these bits will enable the respective lower loop current termination modes without the associated transmit attenuation. Increased distortion may be observed, which is acceptable during DTMF dialing. After DTMF dialing is complete, the attenuation should be enabled by returning to either the Japan DC termination mode (DCT[1:0] = 01b) or the Low Voltage termination mode (DCT[1:0] = 00b). The FJM and the FLVM bits have no effect in any other termination mode other than the FCC DC termination mode.

Higher DTMF levels may also be achieved if the amplitude is increased and the peaks of the DTMF signal are clipped at digital full scale (as opposed to wrapping). Clipping the signal will produce some distortion and intermodulation of the signal. Generally, somewhat increased distortion (between 10–20%) is acceptable during DTMF signaling. Several dB higher DTMF levels can be achieved with this technique, compared with a digital full scale peak signal.

3.19.2.17 Pulse Dialing

Pulse dialing is accomplished by going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have very tight specifications for pulse fidelity, including make and break times, make resistance, and rise and fall times. In a traditional solid-state DC holding circuit, there are a number of issues in meeting these requirements.

The DAA DC holding circuit has active control of the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries such as Italy, the Netherlands, South Africa, and Australia deal with the on-hook transition during pulse dialing. These tests provide an inductive DC feed, resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional way of dealing with this problem is to put a parallel RC shunt across the hookswitch relay. The capacitor is large (~1 μF, 250 V) and relatively expensive. In the DAA, the OHS bit can be used to slowly ramp down the loop current to pass these tests without requiring additional components.

3.19.2.18 Billing Tone Detection

"Billing tones" or "metering pulses" generated by the central office can cause modem connection difficulties. The billing tone is typically either a 12 kHz or 16 kHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone may be large enough to cause major errors related to the modem data. The DAA has a feature which allows the device to provide feedback as to whether a billing tone has occurred and when it ends.

Billing tone detection is enabled by setting the BTE bit. Billing tones less than 1.1 V_{PK} on the line will be filtered out by the low pass digital filter on the DAA. The ROV bit is set when a line signal is greater than 1.1 V_{PK}, indicating a receive overload condition. The BTD bit is set when a line signal (billing tone) is large enough to excessively reduce the line-derived power supply of the line-side device. When the BTD bit is set, the DC termination is changed to an 800 W DC impedance. This ensures minimum line voltage levels even in the presence of billing tones.

The OVL bit should be polled following a billing tone detection. When the OVL bit returns to zero, indicating that the billing tone has passed, the BTE bit should be written to zero to return the DC termination to its original state. It will take approximately one second to return to normal DC operating conditions. The BTD and ROV bits are sticky, and they must be written to zero to be reset. After the BTE, ROV, and BTD bits are all cleared, the BTE bit can be set to re-enable billing tone detection.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, may trigger the ROV or the BTD bits, after which the billing tone detector must be reset. The user should look for multiple events before qualifying whether billing tones are actually present.

Although the DAA will remain off-hook during a billing tone event, the received data from the line will be corrupted when a large billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This keeps the manufacturer from having to include a costly LC filter internal to the modem when it may only be necessary to support a few countries/customers.

Alternatively, when a billing tone is detected, the system software may notify the user that a billing tone has occurred. This notification can be used to prompt the user to contact the telephone company and have the billing tones disabled or to purchase an external LC filter.

3.19.2.19 Billing Tone Filter (Optional)

In order to operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. (The DAA can remain off-hook during a billing tone event, but modem data will be lost in the presence of large billing tone signals.) The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are fairly expensive and few countries supply billing tone support, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 3−58 shows an example billing tone filter. Figure 3−59 shows the billing tone filter and the ringer impedance network for the Czech Republic. Both of these circuits may be combined into a single external dongle.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 kHz and 16 kHz.

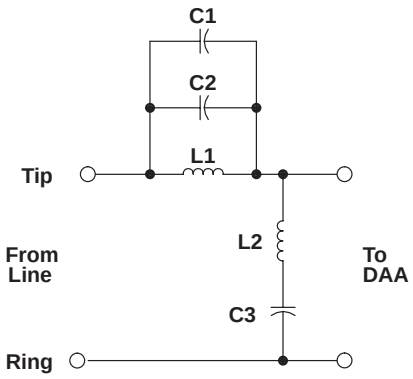


Figure 3−58. Billing Tone Filter

Table 3−48. Component Values—Optional Billing Tone Filters

SYMBOL	VALUE
C1,C2	0.027 μF, 50 V, ±10%
C3	0.01 μF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 W, ±10%
L2	10 mH, >40 mA, <10 W, ±10%

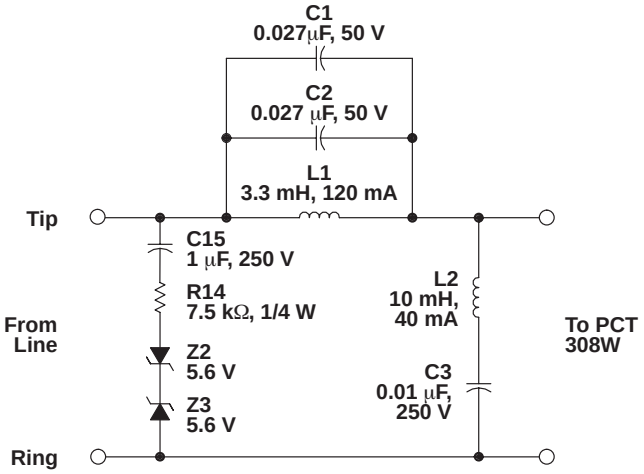


Figure 3−59. Dongle Applications Circuit

The billing tone filter affects the AC termination and return loss. The current complex AC termination will pass worldwide return loss specifications both with and without the billing tone filter by at least 3 dB. The AC termination is optimized for frequency response and hybrid cancellation, while having greater than 4 dB of margin with or without the dongle for South Africa, Australia, CTR21, German, and Swiss country-specific specifications.

3.19.2.20 On-Hook Line Monitor

The DAA allows the user to receive line activity when in an on-hook state. This is accomplished through a low-power ADC located on-chip that digitizes the signal passed across the RNG1/2 pins and then sends this signal digitally across the link to the system-side module. This mode is typically used to detect caller ID data (see Section 3.19.2.21, Caller ID). There are two low-power ADCs on the DAA. One is enabled by setting the ONHM bit in Register 5. This ADC draws approximately 450 mA of current from the line when activated. A lower power ADC also exists on the DAA, which enables a reduced current draw from the line of approximately 7 mA. This lower power ADC is enabled by setting the MODE bit (in conjunction with the ONHM bit) to 1. (See the MODE bit description in Section 3.19.1, DAA Control Registers.) Regardless of which ADC is being used, the on-hook line monitor function must be disabled before the device is taken off-hook. Thus, ensure that the ONHM bit is cleared before setting the OH bit.

The signal to the lower power ADC can be attenuated to accommodate larger signals. This is accomplished through the use of the ARX[2:0] bits. It is important to note that while these ARX bits provide gain to the normal receive path of the DAA, they also function as attenuation bits for the on-hook line monitor low power ADC. Attenuation settings include 0, 1, 2.2, 3.5, and 5 dB. It is recommended that the new lower power ADC be used for on-hook line monitoring.

3.19.2.21 Caller ID

The DAA provides the designer with the ability to pass caller ID data from the phone line to a caller ID decoder connected to the serial port.

3.19.2.22 Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook.

In systems where the caller ID data is passed on the phone line between the first and second rings, the following method should be utilized to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in Section 3.19.2.14, Ring Detection, determine when the first ring has completed.
2. Set the OFF/SQL2 bit. This bit resets the AC coupling network on the ring input in preparation for the caller ID data. This bit should not be cleared until after the caller ID data has been received.
3. Assert the MODE bit and then the ONHM bit. This enables the lower current caller ID ADC.
4. The low-power ADC (which is powered from the system chip, allowing for approximately 7 mA current draw from the line) then digitizes the caller ID data passed across the RNG 1/2 pins and presents the data to the DSP via the SDO signal internal to the integrated system-side module.
5. Clear the ONHM, MODE, and OFF/SQL2 bits after the caller ID data has been received but prior to the start of the second ring.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, the following method should be used to capture the caller ID data:

1. Enable full wave rectified ring detection with the RFWE bit.
2. Monitor the RDTP and RDTN register bits to identify whether a polarity reversal or a ring signal has occurred. A polarity reversal will trip either the RDTP or RDTN ring detection bits, and thus the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Once the signal has been identified as a battery reversal, the AC coupling network on the ring input must be reset in preparation for the caller ID data. Set the OFF/SLQ2 bit. This bit should not be cleared until after the caller ID data has been received.

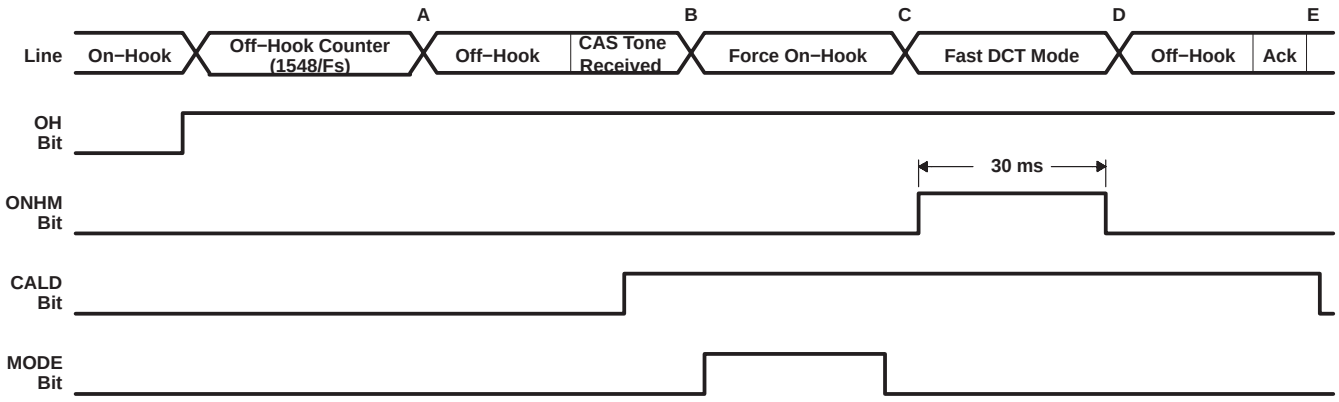
4. Assert the MODE bit and then the ONHM bit. This enables the lower current caller ID ADC.
5. The low-power ADC (which is powered from the system chip, allowing for approximately 7 mA current draw from the line) then digitizes the caller ID data passed across the RNG 1/2 pins and presents the data to the DSP via the SDO signal internal to the system-side module.
6. Clear the ONHM, MODE, and OFF/SLQ2 bits after the caller ID data has been received but prior to the start of the second ring.

3.19.3 Type II Caller ID

Type II Caller ID sends the CID data while the DAA is off-hook. This mode is often referred to as caller ID/call waiting (CID/CW). To receive the CID data while off-hook, the following procedure should be used (also see Figure 3−60):

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the line data. The host processor must detect the presence of this tone.
2. The DAA must then check to see if there is another parallel device on the same line. This is accomplished by briefly going on-hook, measuring the line voltage, and then returning to an off-hook state.
    a. Set the CALD bit to 1. This disables the calibration that automatically occurs when going off-hook.
    b. With the OH bit set to 1 and the ONHM bit set to 0, set the MODE bit to 1. This forces the DAA to go on-hook and disables the off-hook counter that is normally enabled when going back off-hook.
    c. Read the LVCS bits to determine the state of the line.
    d. If the LVCS bits read the typical on-hook line voltage, then there are no parallel devices active on the line, and CID data reception can be continued.
    e. If the LVCS bits read well below the typical on-hook line voltage, then there are one or more devices present and active on the same line that are not compliant with Type II CID. CID data reception should not be continued.
    f. Set the MODE bit to 0 to return to an off-hook state.
3. Immediately after returning to an off-hook state, the ONHM bit must be set and left enabled for at least 30 ms. This allows the line voltage to settle before transmitting or receiving any data. After 30 ms, the ONHM bit should be disabled to allow normal data transmission and reception.
4. If a non-compliant parallel device is present, then a reply tone is not sent by the host tone generator and the CO does not proceed with sending the CID data.
5. If all devices on the line are Type II CID compliant, then the host must mute its upstream data output to avoid the propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the host processor must then send an acknowledgement (ACK) tone back to the CO to request the transmission of the CID data.
6. The CO then responds with the CID data. After receiving this, the host processor unmutes the upstream data output and continues with normal operation.
7. The muting of the upstream data path by the host processor has the effect of muting the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.
8. The CALD bit can be set to 0 to re-enable the automatic calibration when going off-hook.

Due to the nature of the low-power ADC, the data presented on SDO could have up to a 10% DC offset. The caller ID decoder must either use a high pass or a band pass filter to accurately retrieve the caller ID data.



NOTES: A. The off-hook counter is used to prevent transmission or reception of data for 1548/Fs to allow time for the line voltage to settle. If the CALD bit is 0, an automatic calibration will also be performed during this time.
B. The caller alert signal (CAS) tone is transmitted from the CO, which signals an incoming call.
C. When the MODE bit is set while the device is off-hook, the device is forced on-hook. This is done to read the line voltage in the LVCS bits to detect parallel handsets. In this mode, no data is transmitted on the SDO pin.
D. When the device returns off-hook after being forced on-hook using the MODE bit, the normal off-hook counter is disabled. Additionally, if the CALD bit is set, the automatic calibration will not be performed. The fast DCT mode must be manually enabled for at least 30 ms in order to properly settle the line voltage. This is done by setting the ONHM bit after disabling the MODE bit.
E. After allowing the line voltage to settle in fast DCT mode, normal off-hook mode should be entered by disabling the ONHM bit. If CID data reception is desired, then the appropriate signal should be sent to the CO at this time.

Figure 3−60. Implementing Type II Caller ID on the DAA

3.19.3.1 Overload Protection

The DAA can detect if an overload condition is present which may damage the DAA circuit. The DAA may be damaged if excessive line voltage or loop current is sustained.

The overload protection circuit utilizes the LVCS bits to determine an excessive line current or voltage per the LVCS bit transfer functions outlined in Figure 3−51 and Figure 3−52.

When off-hook, if OPE is set and LVCS = 11111, the DC termination is disabled (800 W presented to the line), the hookswitch current is reduced, and the OPD bit is set.

NOTE:

If the OPE bit is enabled before going off-hook, the overload protection circuit could be activated by the line transients produced by going off-hook. To avoid this, the OPE bit should be 0 prior to going off-hook. This bit can then be set ~25 ms after going off-hook to enable the overload protection feature.

3.19.3.2 Gain Control

The DAA supports multiple receive gain and transmit attenuation settings. The receive path can support gains of 0, 3, 6, 9, and 12 dB, as selected with the ARX[2:0] bits. The receive path can also be muted with the RXM bit. The transmit path can support attenuations of 0, 3, 6, 9, and 12 dB, as selected with the ATX[2:0] bits. The transmit path can also be muted with the TXM bit.

The gain control bits ARXB and ATXB should be set to 0 at all times.

3.19.4 Country Code Settings

The DAA chip can be fully programmed to meet international requirements and is compliant with FCC, CTR21, JATE, and various other country-specific PTT specifications as shown in Table 3−49. In addition, the DAA has been designed to meet the most stringent global requirements for out-of-band energy, emissions, immunity, lightning surges, and safety. Table 3−49 shows the specific DAA settings used for several of the countries supported.

Table 3−49. Country-Specific Register Settings

REGISTER	16					17	18
COUNTRY	OHS	ACT	DCT[1:0]	RZ	RT	LIM	VOL
Australia†	1	1	01	0	0	0	0
Bulgaria	0	0 or 1	10	0	0	0	0
China†	0	0	01	0	0	0	0
CTR21†‡	0	0 or 1	11	0	0	1	0
Czech Republic§	0	1	10	0	0	0	0
FCC	0	0	10	0	0	0	0
Hungary	0	0	10	0	0	0	0
Japan†	0	0	01	0	0	0	0
Malaysia†¶	0	0	01	0	0	0	0
New Zealand	0	1	10	0	0	0	0
Philippines†	0	0	01	0	0	0	1
Poland#	0	0	10	1	1	0	0
Singapore	0	0	10	0	0	0	0
Slovakia	0	0 or 1	10	0	0	0	0
Slovenia	0	1	10	0	0	0	0
South Africa#	1	1	10	1	0	0	0
South Korea†#	0	0	01	1	0	0	0

† See Section 3.19.2.12, DC Termination Considerations, for more information.
‡ CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
§ See Section 3.19.2.15, Ringer Impedance.
¶ Supported for loop current ≥ 20 mA.
# The RZ bit in Register 16 should only be set for Poland, South Africa and South Korea if the ringer impedance network (C15, R14, Z2, Z3) is not populated.

3.19.4.1 Power Management

The DAA supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full power down mode. The power management modes are controlled by the PDN and PDL bits in Register 6.

On power up, or following a reset, the DAA is in reset operation. In this mode, the PDL bit is set, while the PDN bit is cleared. The system-side module is fully operational, except for the link. No communication between the system-side module and line-side device can occur during reset operation. Note that any register bits associated with the line-side device are not valid in this mode.

The most common mode of operation is the normal operation. In this mode, the PDL and PDN bits are cleared. The DAA is fully operational and the link is passing information between the system-side module and the line-side device. The desired sample rate should be programmed prior to entering this mode.

The DAA supports a low-power sleep mode. This mode supports the popular wake-up-on-ring feature of many modems. To enable it, the PDN bit must be set and the PDL bit then cleared. When the line-side device is in sleep mode, the host processor clock signal may be stopped or remain active to the system-side module, but it *must* be active before waking up the DAA. The system-side module is non-functional except for the link. To take the line-side device out of sleep mode, the system-side module should be reset.

In summary, the power down/up sequence for sleep mode is as follows:

1. Set the PDN bit and clear the PDL bit.
2. The system-side module clock may stay active or stop.

3. Restore the system-side module clock before initiating the power-up sequence.
4. Reset the system-side module (after system-side module clock is present).
5. Program registers to desired settings.

The DAA also supports an additional power-down mode. When both the PDN and PDL bits are set, the chipset enters a complete power-down mode and draws negligible current (deep sleep mode). In this mode, the ring detect function does not operate. Normal operation may be restored using the same process for taking the DAA out of sleep mode.

3.19.4.2 Calibration

The DAA initiates an auto-calibration by default whenever the device goes off-hook or experiences a loss in line power. Calibration is used to remove any offsets that may be present in the on-chip A/D converter which could affect the A/D dynamic range. Auto-calibration is typically initiated after the DAA DC termination stabilizes, and takes 512/Fs seconds to complete. Due to the large variation in line conditions and line card behavior that can be presented to the DAA, it may be beneficial to use manual calibration in lieu of auto-calibration.

Manual calibration should be executed as close to 512/Fs seconds as possible before valid transmit/receive data is expected.

The following steps should be taken to implement manual calibration:

1. The CALD (auto-calibration disable) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to one and then zero to begin and complete the calibration.
3. The calibration will be completed in 512/Fs seconds.

3.19.4.3 In-Circuit Testing

The DAA's advanced design provides the designer with an increased ability to determine system functionality during production line tests, as well as support for end-user diagnostics. Four loopback modes exist allowing increased coverage of system components. For three of the test modes, a line-side power source is needed. A standard phone line or equivalent test circuit can be used. In addition, an off-hook sequence must be performed to connect the power source to the line-side chip.

For the start-up test mode, no line-side power is necessary and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit is set (the default case), the line side is in a power-down mode and the system-side module is in a digital loop-back mode. In this mode, data received on SDI is passed through the internal filters and transmitted on SDO. This path will introduce approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters will exist between SDI and SDO. Clearing the PDL bit disables this mode and the SDO data is switched to the receive data from the line-side. When the PDL bit is cleared the FDT bit will become active, indicating the successful communication between the line-side and DSP-side. This can be used to verify that the link is operational.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirements:

1. Power up or reset.
2. Program the desired sample rate.
3. Enable the line side by clearing the PDL bit.
4. Issue off-hook
5. Delay 1548/Fs sec to allow calibration to occur.
6. Set the desired test mode.

The digital loopback mode allows the data pump to provide a digital input test pattern on the system-side module and receive that digital test pattern back on the system-side module. To enable this mode, set the DL bit. In this mode, the isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitor, C1 of Figure 3−24, to the line side device and returned across the same barrier. Note in this mode, the 0.9 dB attenuation and filter group delays also exist.

The analog loopback mode allows an external device to drive a signal on the telephone line into the line-side device and have it driven back out onto the line. This mode allows testing of external components connecting the RJ-11 jack (TIP and RING) to the line-side device. To enable this mode, set the AL bit.

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit and receive paths on the line-side chip and the external components in Figure 3−24. In this test mode, the data pump provides a digital test waveform on the system-side module. This data is passed across the isolation barrier, transmitted to and received from the line, passed back across the isolation barrier, and presented back to the data pump from the system-side module. To enable this mode, clear the HBE bit.

When the HBE bit is cleared, this will cause a DC offset which affects the signal swing of the transmit signal. In this test mode, it is recommended that the transmit signal be 12 dB lower than normal transmit levels. This lower level will eliminate clipping caused by the DC offset which results from disabling the hybrid. It is assumed in this test that the line AC impedance is nominally 600 W.

NOTE:

All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

3.19.4.4 Exception Handling

The DAA provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling DSP can read several status bits. The bit of highest importance is the frame detect bit FDT. This bit indicates that the system-side module and line-side device are communicating. During normal operation, the FDT bit can be checked before reading any bits that indicate information about the line side. If FDT is not set, the following bits related to the line side are invalid—RDT, RDTN, RDTP, LCS[3:0], CBID, REVB[3:0], LVCS[4:0], ROV, BTD, DOD, OPD, and OVL.

Following power-up and reset, the FDT bit is not set because the PDL bit defaults to 1. In this state, the link is not operating and no information about the line side can be determined. The user must program the desired sample rate and clear the PDL bit to activate the link. While the system and line side are establishing communication, the system-side does not generate $\overline{\text{FSYNC}}$ signals. Establishing communication will take less than 10 ms.

The FDT bit can also indicate if the line side executes an off-hook request successfully. If the line side is not connected to a phone line (i.e., the user fails to connect a phone line to the modem), the FDT bit remains cleared. The controlling processor must allow sufficient time for the line side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. If the FDT bit is high, the LVCS[4:0] bits indicate the amount of loop current flowing. If the FDT fails to be set following an off-hook request, the PDL bit in Register 6 must be set high for at least 1 ms to reset the line side.

Another useful bit is the communication link error (CLE) bit. The CLE bit indicates a time-out error for the link. This condition indicates a severe error in programming or possibly a defective line-side chip.

3.19.4.5 Revision Identification

The DAA provides the system designer the ability to determine the revision of the system-side module and/or the line-side device. The REVA[3:0] bits identify the revision of the system-side module. The REVB[3:0] and CBID bits identify the revision of the line-side device. Table 3−50 lists revision values for both chips and may contain future revisions not yet in existence.

Table 3−50. Revision Values

REVISION	SYSTEM-SIDE MODULE	LINE-SIDE DEVICE
C	1010	—
D		1100

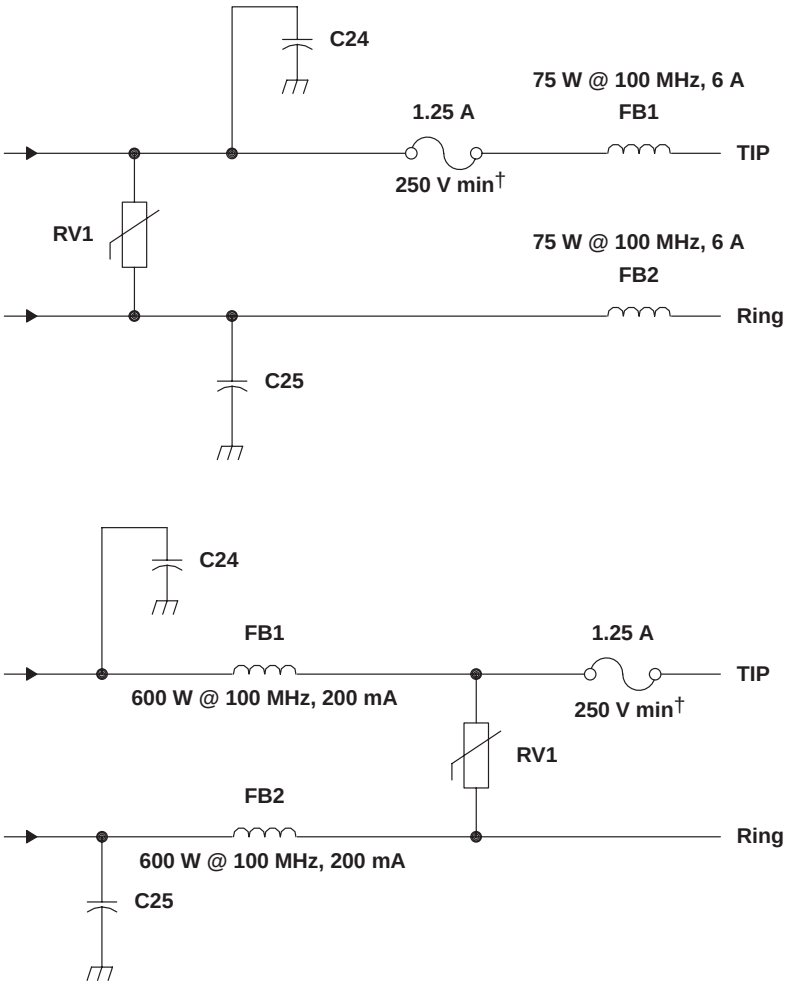
3.19.4.6 UL1950 3rd Edition

Although designs using the DAA comply with UL1950 3rd Edition and pass all over-current and over-voltage tests, there are still several issues to consider.

Figure 3−61 shows two designs that can pass the UL1950 overvoltage tests, as well as electromagnetic emissions. The top schematic of Figure 3−61 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 3−61 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, it is important to remember that compliance to UL1950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage tests will apply to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with your professional testing agency during the design of the product to determine which tests apply to your system.



† Teccor FI250T or equivalent.

Figure 3−61. Circuits That Pass All UL1950 Overvoltage Tests

3.19.4.7 CISPR22 Compliance

Several countries have adopted (or are expected to adopt) the CISPR22 standard. The European Union has adopted their version of the CISPR22 standard entitled EN55022. Effective August 1, 2001 compliance to the EN55022:1998 standard will be necessary to conform to the European Union's EMC Directive and display the CE mark on designs intended for sale in the European Union. It should be noted that L1 and L2 are only necessary for those products which are intended for sale in countries which have adopted CISPR22. If this is not the target market, then L1 and L2 can be replaced with 0 Ω resistors (or 100 mH inductors if the modem will be shipped to India). With L1/L2 as 0 W, C9 should be changed to 22 nF, 250 V.

While the typical schematic and global BOM achieve compliance, there are several system-dependent and country-dependent issues that should be considered. The first issue relates to the direct current resistance (DCR) of the inductors. If the selected inductors have a DCR of less than 3 W each, then countries which require 300 W or less of DC resistance at TIP and RING with 20 mA of loop current can be satisfied with the Japan DC termination mode. It is strongly recommended that users of the DAA adhere to Section 3.19.2.12, DC Termination Considerations, of the data sheet for their DC termination requirements.

The second issue relates to the power supply of the target system. If the target system does not provide a direct current connection between the target system's reference ground (this would be the same reference that DGND of the system-side device is connected to) and an external ground (often the third prong of a power plug), then smaller inductor values may be possible. This consideration is system dependent, and the impedance between the system ground and the external ground in the range of 500 kHz–10 MHz should be well known.

The final issues relate to the sample rate for which the target system will operate in all test conditions and the countries for which the system is targeted. For some systems, only a single sample rate is selected for the operation of the system. For these systems, compliance to CISPR22 can be achieved with smaller L1 and L2 inductors by placing a series capacitor-resistor in parallel with L1 and L2. Figure 3−62 shows the simple notch filter which is used with smaller L1/L2 inductors. Table 3−51 shows typical sample rates and the corresponding values used for C24, C25, C38, C39, L1, L2, R31, and R32.

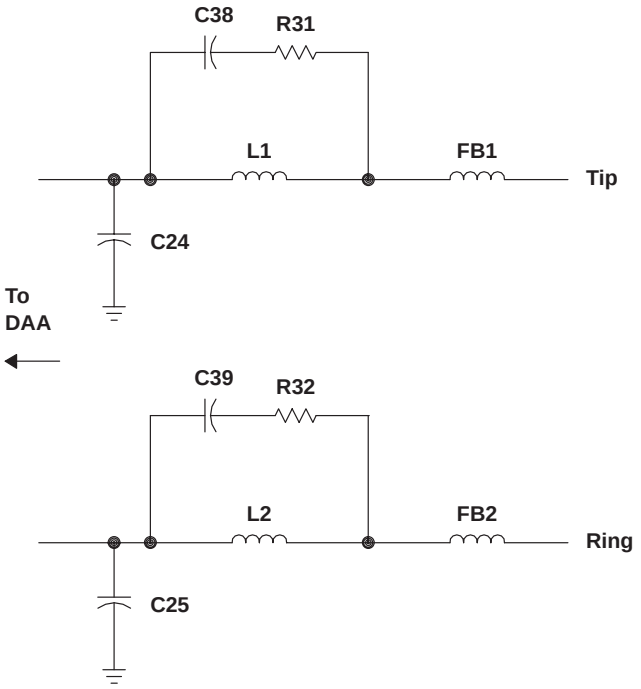


Figure 3−62. Notch Filter for CISPR22 Compliance Using a Fixed Single Sample Rate

Table 3−51. Fixed Sample Rates and Corresponding Notch Filter Component Values

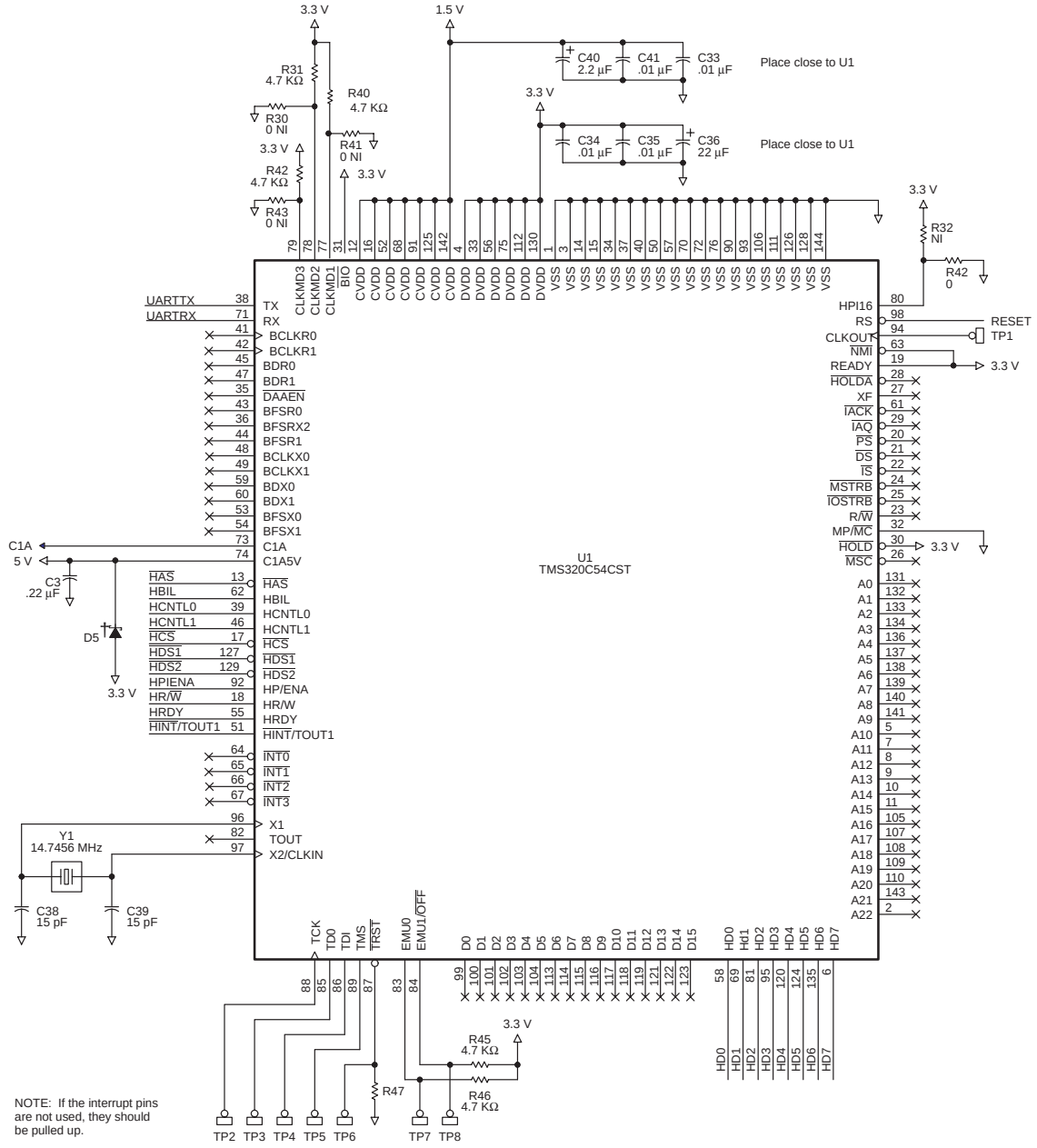
SAMPLE RATE	C24/C25	C38/C39	L1/L2	R31/R32
8000 Hz	1000 pF	68 pF	68 mH	365 W
9600 Hz	1000 pF	47 pF	68 mH	475 W

An additional alternative to the standard BOM may be used for systems that use multiple sample rates. L1 and L2 can be reduced to 220 mH, provided C24 and C25 are increased to 2200 pF. The increase of C24 and C25 to 2200 pF lowers the on-hook impedance to less than 30 kW. Therefore, compliance to countries such as Taiwan, Chile, and Argentina is not possible because they require on-hook impedances of 30 kW or greater.

Compliance to the updated CISPR22 standard is system-dependent and several factors must be considered to achieve compliance.

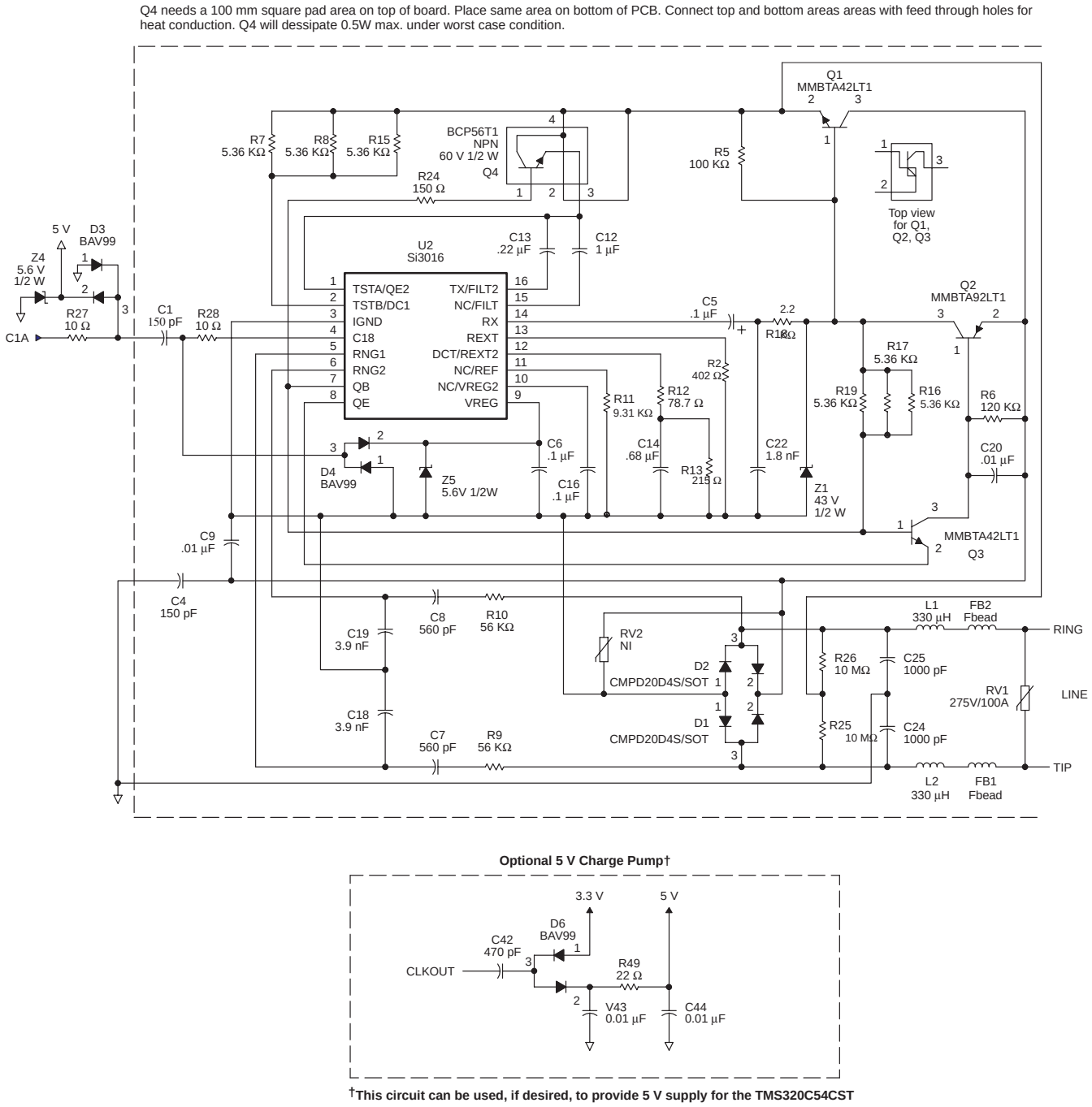
3.19.5 Hardware Reference Design

Figure 3−63 illustrates the pinout and external circuitry for the 54CST and Figure 3−64 illustrates the pinout and external circuitry for the Si3016. Table 3−52 provides a bill of materials for the reference design.



† D5 is required when using the optional charge pump. It is also required in systems where the 5-V supply can be more than 0.5 V below the 3.3-V supply during power-up or power-down.

Figure 3−63. TMS320C54CST Hardware Reference Design



†This circuit can be used, if desired, to provide 5 V supply for the TMS320C54CST

Figure 3−64. Si3016 Hardware Reference Design

Table 3−52. Bill of Materials

ITEM	QUANTITY	REFERENCE	VALUE	PCB FOOTPRINT	MFR PART NUMBER
1	2	C4, C1	150pF	1808 20% 3KV X7R	Required to be Y2-compliant capacitors
2	1	C5	.1µF	10% 50v Case A TANT	
3	2	C6, C16	.1µF	0603 10% 16v X7R	
4	2	C7, C8	560pF	0805 20% 250V X7R	
5	1	C9	.01µF	0805 20% 250V X7R	
6	5	C20, C33, C34, C35, C41	.01µF	0603 20% 16V X7R	
7	1	C12	1µF	20% 16v TANT Case A	
8	2	C3, C13	.22µF	0603 10% 16V X7R	
9	1	C14	.68µF	20% 16V TANT Case A	
10	2	C18, C19	3.9nF	0603 20% 16v X7R	
11	1	C22	1.8nF	0603 20% 50V X7R	
12	2	C24, C25	1000pF	1812 3KV X7R	Required to be Y2-compliant capacitors
13	1	C36	22µF	A case 6.3v	
14	2	C39, C38	15pF	0603 5% 50v NPO	
15	1	C40	2.2µF	A case 6.3v	
16	2	D2, D1	CMPD2004S	SOT-23	Central Semi
17	2	D4, D3	BAV99	SOT-23	Diodes Inc BAV99−7 On Semi Fairchild Zetex BAV99TA
18	2	FB2, FB1	Fbead	0805	Murata BLM21B102S
19	2	L1, L2	330µH		Sporton RCP0408−301K01
20	2	Q3, Q1	MMBTA42LT1	SOT-23	
21	1	Q2	MMBTA92LT1	SOT-23	
22	1	Q4	BCP56T1 NPN 60v 1/2W	SOT-223	
23	1	RV1	275V/100A	DO-214AA	ST SMP100-270LC Teccor P3100SB
24	1	R2	402	1206 1% 1/8W 1210 (SMTPCB pads)	
25	1	R5	100k	0603 1% 1/16W	
26	1	R6	120k	0603 5% 1/16W	
27	6	R7, R8, R15, R16, R17, R19	5.36k	1210 1% 1/4W	
28	2	R9, R10	56K	0805 5% 1/10W	
29	1	R11	9.31K	0603 1% 1/16W	
30	1	R12	78.7	0603 1% 1/16W	
31	1	R13	215	0603 1% 1/16W	
32	1	R18	2.2k	0805 5% 1/10W	

† D6 is required only if C1A5V is not greater than DV_{DD} – 0.5 V during power-up, see Section 5.2, Recommended Operating Conditions.
NOTE: Contact Texas Instruments to obtain an Excel spreadsheet version of this Bill of Materials, if desired.

Table 3−52. Bill of Materials (Continued)

ITEM	QUANTITY	REFERENCE	VALUE	PCB FOOTPRINT	MFR PART NUMBER
33	5	R31, R40, R42, R45, R46	4.7k	0603 5% 1/16W	
34	1	R24	150	0603 5% 1/16W	
35	2	R25, R26	10M	0805 5% 1/10W	
36	3	R30, R41, R43	0 NI	0603 5% 1/16W	(NI = not installed)
37	1	R32	NI	0603 5% 1/16W	(NI = not installed)
38	1	R47	470	0603 5% 1/16W	
39	1	R48	0	0603 5% 1/16W	
40	2	R27, R28	10	0805 5% 1/10W	
41	8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	TEST POINT	(not a part)	
42	1	U1	TMS320C54CST		
43	1	U2	Si3016	SOIC-16 (0.05 pitch, 0.153 body width)	
44	1	Y1	14.7456mhz	HC-49/US	Parallel, Fundamental, 30 Ω, 10 pF
45	1	Z1	43V 1/2W	SOD-123	Diodes Inc BZT52C43 General Semi MMSZ5260B
46	2	Z4, Z5	5.6V 1/2W	SOD-123	Diodes Inc BZT52C5V6-13 General Semi MMSZ5232B
47	1	D5	Schottky	2.5 x 5 mm	Panasonic MA2Q735 Toshiba CRS03 Rohm RB160L-40
OPTIONAL COMPONENTS					
1	1	C42	470pF	0603 10% 50V NPO	
2	2	C43, C44	.01µF	0603 20% 16V X7R	
3	1	D6†	BAV99	SOT-23	Diodes Inc. BAV99-7 On Semi Fairchild Zetex BAV99TA
4	1	R49	22	0603 5% 1/16W	

† D6 is required only if C1A5V is not greater than DV_{DD} – 0.5 V during power-up, see Section 5.2, Recommended Operating Conditions.
NOTE: Contact Texas Instruments to obtain an Excel spreadsheet version of this Bill of Materials, if desired.

3.19.6 General DAA Layout Guidelines

The integrated DAA provides a very high level of integration for modem designs. Integration of the analog front end (AFE) and hybrid, and the removal of the transformer, relays, and opto-couplers reduces the layout effort considerably. The DAA consists of two parts—the DSP-side and the line-side. When designing with the DAA, there are several layout guidelines that will assist the designer in attaining telecom, safety, and EMC approvals.

This document is divided into six main sections: operational items, analog performance related items, EMC items, safety items, assembly items, and thermal considerations. Operational items are defined as those items that must be followed to ensure functionality of the solution. Analog performance related items are layout recommendations that are pertinent to the analog performance of the solution. EMC items are those items that will affect the emissions/immunity performance of the solution. Safety items are layout issues that could impact safety requirements of a particular modem solution. Assembly items are items that should be noted to assist in assembly of the solution. Thermal considerations are those items that may affect operational performance due to extreme temperatures.

3.19.6.1 Operational Guidelines

Figure 3−65 depicts the placement of the chipset, some of the major discrete components, and the RJ11 connector. Note the placement of the DSP and the Si3016. Aligning these devices so that pins 73/74 of the DSP face pins 1–8 of the Si3016 will aid in following some of the more specific layout guidelines. Utilizing this placement will also allow the design to closely resemble the example layout, enabling the designer to directly follow these guidelines.

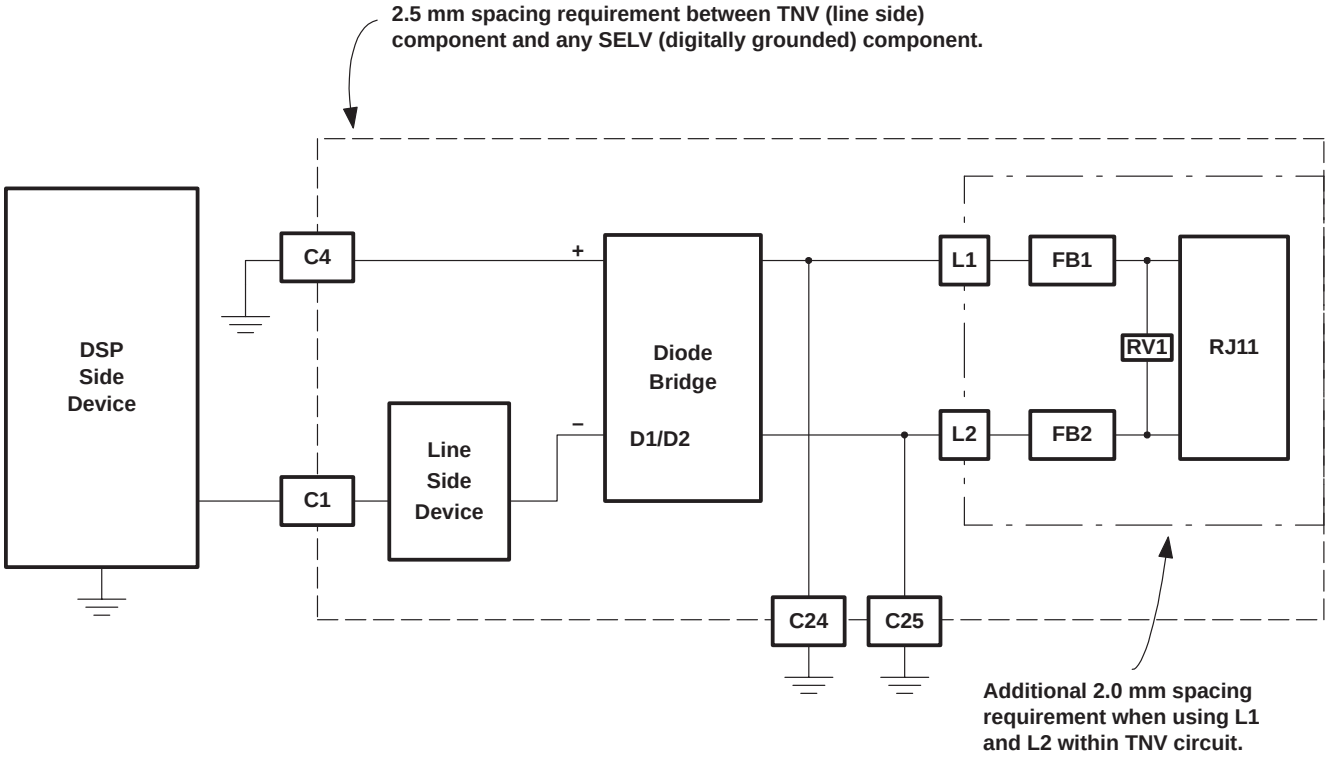


Figure 3−65. Chipset Diagram

3.19.6.2 Layout Requirements

For the line-side chip (U2), the primary layout considerations are the placement and routing of C6, C9, C16, D1, D2, and RV2.

Capacitors C6 and C16 provide regulation of the supplies powering U2. The loop formed by C6 to pins 3 and 9 and the loop formed by C16 to pins 3 and 10 should be made as small as possible. Figure 3−66 shows an example of how to minimize these loops. The trace back to pin 3 is thicker because multiple loops use this path. The thicker trace has a lower impedance, which lessens the effect of multiple currents in that trace.

Capacitor C9, dual diodes D1 and D2, and the MOV RV2 form a loop that should be minimized. C9 performs a low pass filter function on the transmit and receive signals. The inductance in the loop from C9 to the diode bridge (D1 and D2) can affect the ability of C9 to suppress out-of-band energy. See Figure 3−67 for a layout example.

The placement of capacitors C12 and C13 is also important because these components are in high gain loops. Noise in these loops may affect the signals at TIP and RING. The loop formed from pin 15 through C12 to pin 1 (QE2) and the loop formed from pin 16 though C13 to pin 1 should be routed as short as possible. Figure 3−66 illustrates an example of these loops. Also, the trace from Q4 pin 3 (emitter) should connect directly to the QE2 pin and should not share the same route as the C12 and C13 capacitors to QE2.

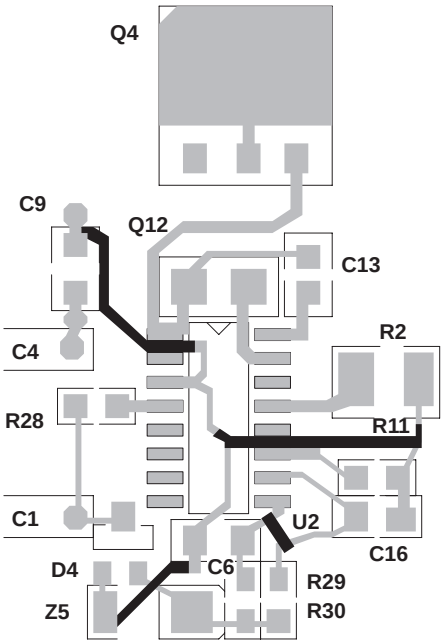


Figure 3−66. Routing for C6, C16, C12, C13, Q4, R2, and R11

3.19.6.3 Analog Performance

The components on the line side of the DAA are composed of a small digital interface section (capacitor barrier interface, converters, and control logic), and the remaining components are used for either analog circuits (hybrid, dc impedance, ac impedance, ringer impedance, etc.) or safety and EMC (surge protector, ferrite beads, EMC capacitors, etc.).

Routing all traces in the DAA section with 15 mil or greater traces when possible will ensure high overall analog performance of the silicon DAA. Furthermore, the DAA section should not use a ground plane for the IGND signal; instead the IGND signal should be routed using a 20 mil trace. Thermal considerations may also be affected by the size of the IGND trace. See Section 3.19.10, Thermal Considerations.

After placing C6, C12, C13, and C16, the designer should focus on placing R11 and routing the trace from Q4 pin 3 to U2 pin 1 using as small a loop as possible to ensure good analog performance. Due to the relatively high current that can flow in the trace from Q4 pin 3 to U2 pin 1, this trace should be routed separately from the trace coming from C12 and C13 to pin 1. This will ensure that the current from Q4 will not affect the sensitive C12 and C13 loops. Figure 3−66 illustrates an example of the placement and routing of R11, Q4, and U2.

3.19.7 EMC

Several sources conduct or radiate EMC from/to electronic apparatus. Among these are the following:

- Antenna loops formed by ICs and their decoupling capacitors
- PC-board traces carrying driving and driven-chip currents
- Common impedance coupling and crosstalk

To minimize EMC-related problems, all extraneous system noise and the effects of parasitic PC-board trace antennas must be reduced. Employment of an effective system shielding may also be necessary. The following section discusses how to minimize the EMC problems that can occur on the DAA design.

Capacitors C1, C2, C4, and C9 provide the path for the isolation currents. The typical application schematic recommends that C2 not be installed. If C2 is not installed, the isolation current flows in the following manner:

1. From the DSP C1A pin
2. Across C1 to pin 4 of the Si3016 (U2)
3. From pin 4 to pin 3 of U2
4. To C9
5. Across C9 to C4
6. And finally, across C4 to ground

Because the isolation signal operates around 2 MHz, it is important to keep the path of the signal as small as possible (see Figure 3−67).

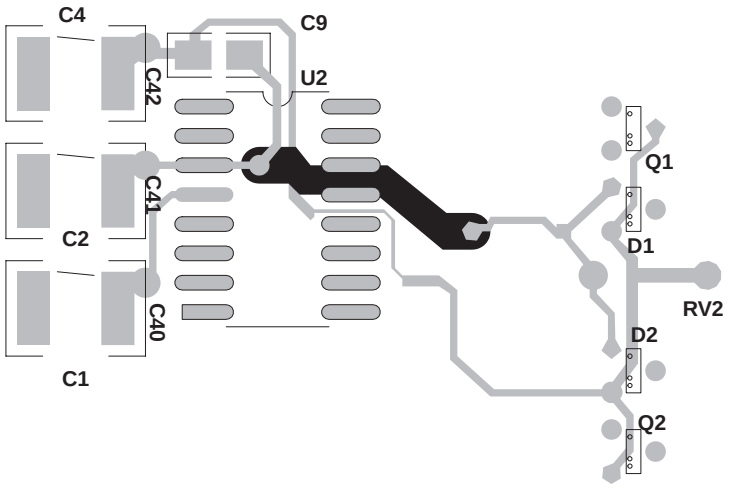


Figure 3−67. Isolation Interface and Diode Bridge

Short, direct routes using thick 20 mil minimum traces, should be used to connect the isolation capacitors to their respective pins. The GND side of these caps should be connected directly to ground, as close to the DSP as possible. The IGND side of C2 should connect directly to the IGND pin of the Si3016. It is acceptable to use a long trace to connect C4 to the Q1 pin 3 node, as long as there is an IGND trace that follows the C4 to Q1 trace.

For those designs that exhibit emission problems related to the isolation interface, the C30 capacitor may be installed. C30 will shunt some of the high frequency energy and reduce emissions due to the harmonics of the isolation link.

FB1, FB2, RV1, C24, C25, C31, and C32, and if implemented, a fuse should be placed as close as possible to the RJ11 as shown in Figure 3−68. It is important for the routing from the RJ11 connector through the ferrite beads FB1 and FB2 to be well matched. The routing to C24 and C25 should also be well matched. The distance from the TIP and RING connections on the RJ11 through the EMC capacitors C24 and C25 to chassis ground should be kept as short as possible. If possible, the routing through the ringer network to the line-side device pin 5 and pin 6 should also be well matched as shown in Figure 3−69.

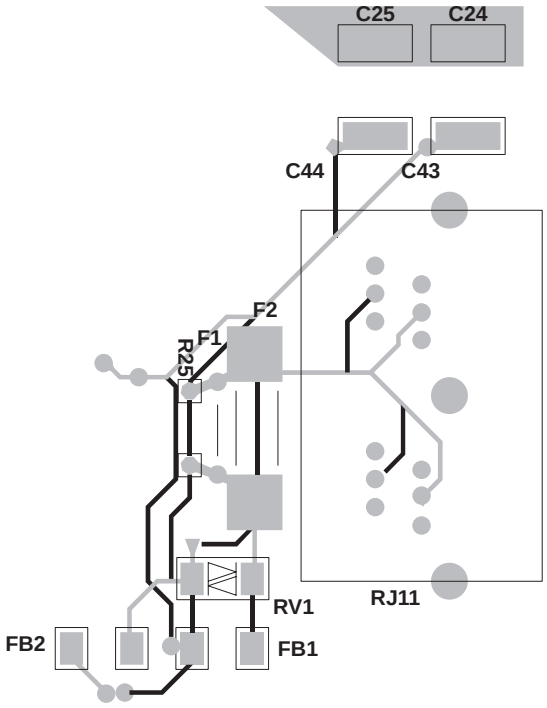


Figure 3−68. RJ11

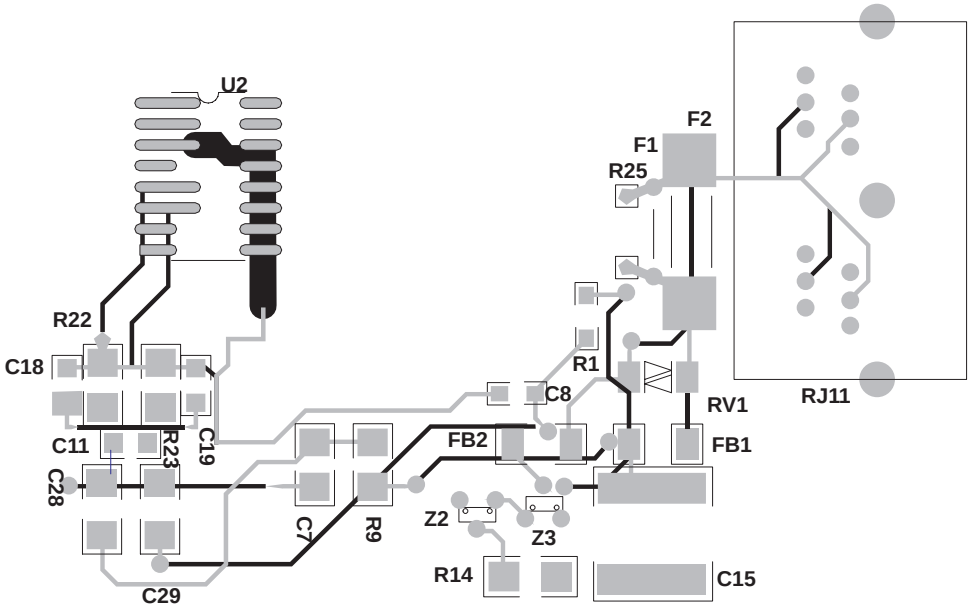


Figure 3−69. Ringer Network

Routing all the connections from RJ11 to FB1, FB2, RV1, C24, C25, C31, C32, and F1 using a 20 mil trace will improve the EMC performance of the solution.

Good general design practices should be followed to improve the EMC performance of the solution. This includes laying out the digital ground plane as small as possible and rounding off the corners. Placing series resistors on the clock signals near their source and ensuring that the traces from oscillators or crystals are made as short as possible will contribute to the overall emissions performance of the solution.

When using the DAA in unearthed systems, the designer should consider making some modifications to prevent common mode 50/60 Hz signals from entering the signal path. In an unearthed system, a large 50/60 Hz signal can be present between IGND (line-side pin 3) and digital ground. This signal is often as large as 50 V_{RMS}.

The primary consideration is to use well-matched capacitors which bridge the telephone network voltage (TNV) to the safety extra-low voltage (SELV). C1 should match C4, and C24 should match C25. Matching should be within 10%. To the extent that C1 and C24 does not equal C4 and C25, there will be a common mode to differential conversion of the 50/60 Hz signal. Typical common mode rejection of the 50/60 Hz signal is better than 95 dB.

A secondary consideration is capacitive coupling from DGND (SELV) to nodes on the line-side (TNV) circuitry. The most prevalent system design where capacitive coupling occurs is in mini PCI and MDC designs. However, this coupling always exists and can have a noticeable effect on analog performance when SELV is physically close to TNV.

For safety considerations, 3 mm spacing is recommended between TNV and SELV (international minimum is 2.5 mm). However, there are three nodes on the line side which require special consideration to ensure robust analog performance in unearthed systems:

- RX pin on Si3016
- FILT pin on Si3016
- FILT2 pin on Si3016

For these pins and the traces that connect to these pins, the following guidelines should be followed:

- Whenever possible, keep at least a 5 mm distance between these nodes and SELV.
- An IGND guard ring can be used on the board level. This IGND guard ring should be inserted between SELV and the nodes listed above. For FR4 board material, the IGND guard can be placed on any layer. Optimal placement would be for the IGND guard ring to be on the same layer as the nodes listed above. This guard ring allows SELV to couple into IGND rather than the nodes listed above.
- For designs (e.g., MDC, mini PCI designs) which have TNV circuitry in close proximity (< 5 mm) to a SELV plane, a Faraday shield can be used to protect against coupling. This coupling occurs through air between the SELV plane and the TNV nodes described above. A small IGND shield can be placed between the TNV nodes and the SELV plane. This plane allows the SELV to couple into IGND rather than the TNV nodes.

3.19.8 Safety

The layout of the modem circuitry, in particular the area of the circuit that is exposed to telephone network voltages (TNV), is subject to many safety compliance issues. It is recommended that all customers consult with their safety expert or consultant on the various regulations that could impact their designs. One of the most critical layout issues that relates to safety is to ensure that a minimum 2.5 mm (3 mm preferable) or 100 mil space is provided between safety extra low voltage (SELV) and TNV circuitry. Designs requiring 5 kV isolation between TNV and SELV should use 5 mm minimum spacing.

When L1 and L2 are included in the DAA, the spacing requirements between the TNV circuit and SELV needs to be increased from 2.5 mm to 3.5 mm. This increased spacing requirement compensates for the secondary peaking effects during longitudinal surges resulting from the addition of L1 and L2.

In addition to the increased spacing requirement between TNV and SELV, there is a second spacing requirement within the TNV circuit. During surge events, the voltage across the L1 and L2 inductors can be sufficient to create arcing to nearby TNV nodes. To prevent arcing, it is recommended the opposing terminals of the L1 and L2 inductors be isolated from each other by 2.0 mm. Thus, the nodes corresponding to RV1, FB1, FB2, RJ11, and one terminal of L1/L2, should be isolated by 2.0 mm from nodes that connect to the other terminal of L1/L2.

3.19.9 Assembly

There are several steps that can be taken in layout to ensure that the assembly process goes smoothly. For example, an assembly-related error is to install the polarized capacitors with the polarity backwards. This can be prevented by stenciling the board with a plus sign on the correct side of C12, C14, and C5 to indicate the proper orientation for the polarized capacitors. Also, indicating pin 1 on the board with a stencil marking improves the chances that the integrated circuits will be installed correctly. Thought should also be given to using several footprints for a given component to allow for multiple vendor choices. Popular components using multiple footprints are C1, C2, C4, C12, C24, C25, C31, C32, F1, and Z1. Taking these basic steps will assist in the assembly process and ease future troubleshooting.

3.19.10 Thermal Considerations

When using the DAA in common applications, there are several thermal considerations that should be taken into account. These thermal considerations will ensure that the device is not operating outside of the recommended operating conditions, thus protecting the device from possible degradation.

On small form factor printed circuit board (PCB) designs, the ability of the PCB to dissipate heat becomes a very important design consideration. These small designs will require additional mechanisms to remove the heat from the DAA. For applications with a PCB area of less than approximately 3000 mm^2, thermal design rules should be applied.

3.19.11 Layout Check List

Table 3−53 is a check list that the designer can use during layout. The items marked as required should be taken into consideration first.

Table 3−53. Layout Check List

✓	#	LAYOUT ITEMS	REQUIRED
		OPERATIONAL ITEMS	
	1	Small loop from C6 to U2 pin 9 and pin 3	Yes
	2	Small loop from C16 to U2 pin 10 and pin 3	Yes
	3	Small loop from C12 to U2 pin 15 and pin 1	Yes
	4	Small loop from C13 to U2 pin 16 and pin 1	Yes
	22	Copper pad heat sink is at least 0.08 sq. in. for Q4.	Yes
		ANALOG PERFORMANCE	
	5	Small loop from R11 to U2 pin 11 and pin 3	Yes
	6	Separate trace from Q4 pin 3 to U2 pin 1 than the trace from C12 and C13 to U2 pin 1	Yes
	7	Minimum of 15 mil traces in DAA section	
	8	Minimum of 20 mil trace for IGND	
	9	No ground plane in DAA section	Yes
	n/a	> 5 mm spacing between SELV and TNV nodes (RX, FILT, FILT2)	Yes
	n/a	IGND guard ring to protect TNV nodes (RX, FILT, FILT2)	Yes
	n/a	IGND Farady shield to protect TNV nodes (RX, FILT, FILT2)	Yes

Table 3−53. Layout Check List (Continued)

✓	#	LAYOUT ITEMS	REQUIRED
		EMC ITEMS	
	10	Small loop formed between U2, C1, C9, and C4.	Yes
	11	Minimum of 20 mil trace from DSP to C1, C9, and C4 and from U2 to C1 and C9	
	12	FB1, FB2, and RV1 placed as close as possible to the RJ11	Yes
	n/a	Routing from TIP and RING of the RJ11 through F1 to the ferrite beads is well matched	Yes
	16	Distance from TIP and RING through EMC capacitors C24 and C25 to Chassis Ground is short	Yes
	17	C9 is located near C4	
	n/a	C4 is located with C2 between DSP and U2	
	18	Minimum of 20 mil trace from RJ11 to FB1, FB2, RV1, C24, C25, C31, C32, and F1	
	19	Routing of TIP and RING signals from the RJ11 through the ringer networks to U2 pin 5 and pin 6 is well matched	
	20	Trace from D1 & D2 to IGND and to C4–C9 node is well matched and forms a small loop.	
	21	DGND return paths for C10 and C3 should be on component side.	
	n/a	Digital Ground plane is made as small as possible	
	n/a	Ground plane has rounded corners	
	n/a	Series resistors on clock signals are placed near source	
		SAFETY ITEMS	
	23	Additional 2 mm spacing for inductors (if necessary)	
	24	Minimum 2.5 mm (100 mils) between SELV and TNV (3.0 mm or higher recommended, Section 3.19.8, Safety)	Yes
	n/a	Space for fire enclosure	
		ASSEMBLY ITEMS	
	26	Polarity for C5 is negative side connects with U2 pin 14	
	27	Polarity for C12 is negative side connects with U2 pin 15	
	n/a	Polarity for C14 is negative side connects with U2 pin 3 (IGND)	

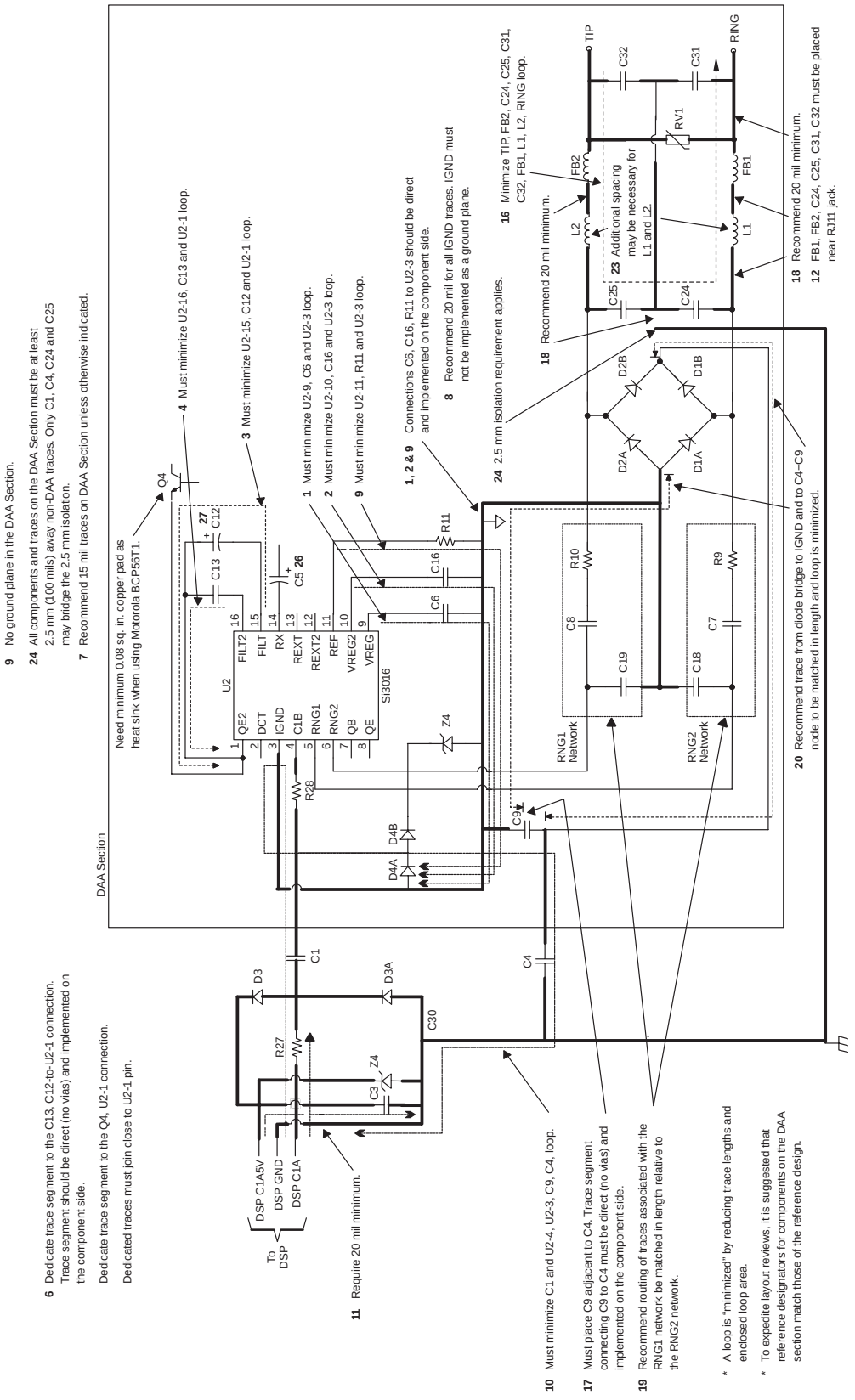


Figure 3–70. TMS320C54CST Modem Layout Guidelines

3.19.12 Additional TMS320C54CST-to-Si3016 Layout Guidelines

This section discusses layout issues specific to the TMS320C54CST. The layout guidelines in the previous section discuss the generic layout issues associated with the DAA circuit, especially the IC and components on the line side of the isolation barrier.

In TMS320C54CST, the line side device is the Si3016. The digital portion of the DAA is not a separate chip, but has been integrated into the TMS320C54CST DSP.

3.19.13 Capacitively Coupled Data Link

A digital data link carries samples of the modem signal and control information between the two parts of the DAA. The link is bidirectional and capacitively coupled for isolation. The link runs between C1A (pin 73) of the DSP and C1B (pin 4) of the Si3016.

The load capacitance on the C1A pin is critical. The driver is designed for a maximum load capacitance of 10 pF. Excessive capacitive load will degrade the link signal and may cause erratic operation or increased sensitivity to external noise sources.

3.19.14 DAA 5V

The DSP has an input pin, C1A5V (pin74), which is an input for a 5V supply used only by the C1A driver. This pin needs to be bypassed for low noise. There are also some surge protection components that connect to 5V. These connections should be short and direct.

3.19.15 Layout Guidelines

The following layout guidelines are intended to:

- Minimize the capacitive load on C1A
- Bypass the 5V supply
- Provide effective surge protection

The component reference designators refer to the TMS320C54CST reference design.

1. The DSP and the Si3016 should be located close together and oriented so that there is a short direct path from C1A to C1B. This path should be no longer than 25 mm.
2. The connection from C1A to C1B, through R27, C1, and R28 should be made with all components and circuit traces on the same side of the board (no vias).
3. There shall be no ground or power planes under C1, or R28. The planes may be removed under the trace from C1A to R27, and under R27, but it is not essential.
4. A 0.22 uF bypass capacitor should be connected to the C1A5V pin as close as possible to the pin, and the other side connected to a ground plane.
5. The connections from Z4 and D3 to the C1A5V pin should be as short and direct as possible. Avoid vias.
6. Some early versions of the Reference Design had a 10 pF cap from C1A to ground or from the junction of R27/C1 to ground. This was optional and intended for EMI suppression if needed. This cap should not be installed under any circumstances.

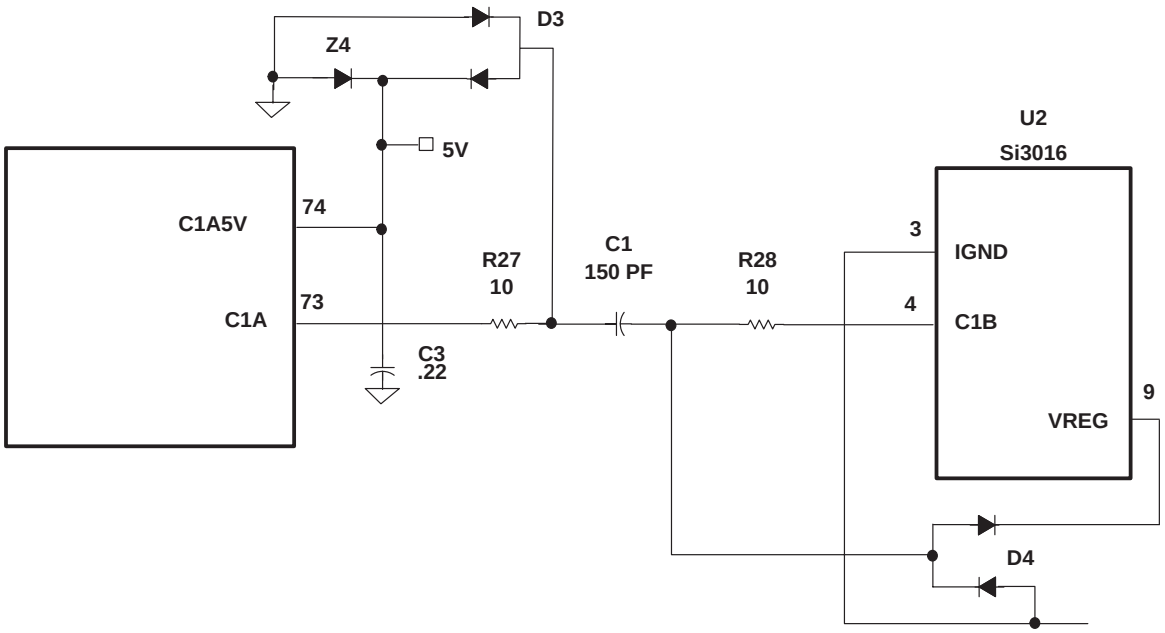


Figure 3−71. Partial Schematic

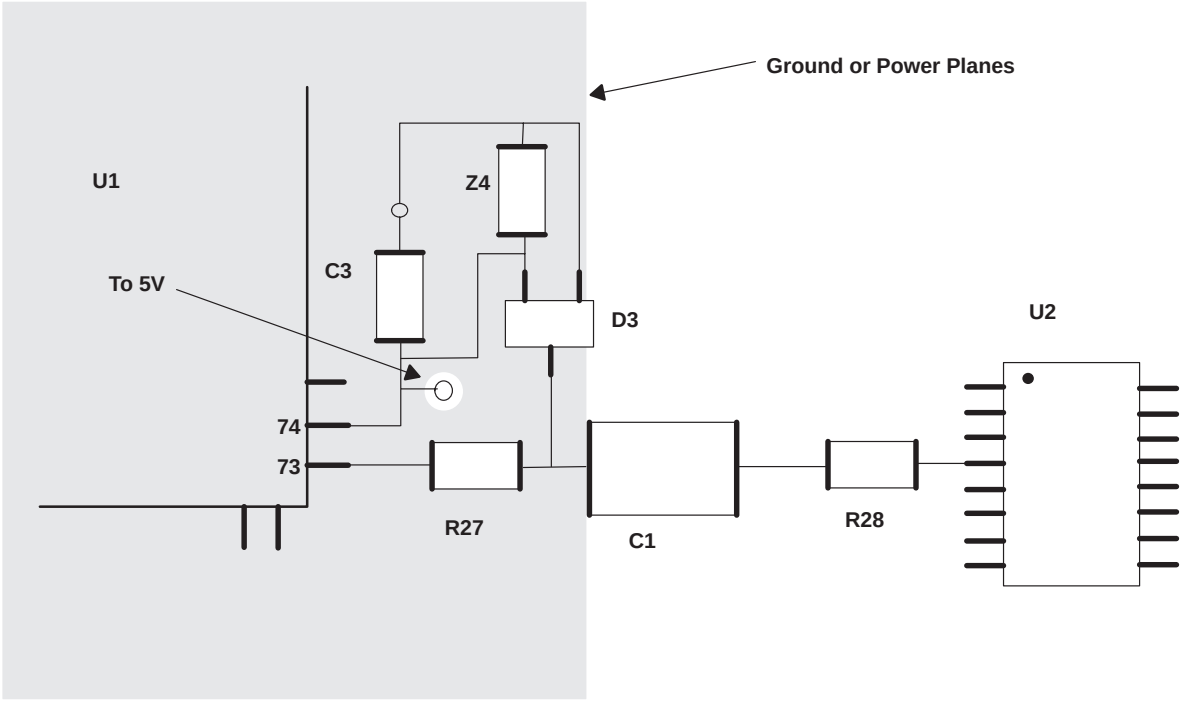


Figure 3−72. Example Layout

3.20 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 3−54.

Table 3−54. Interrupt Locations and Priorities

NAME	LOCATION DECIMAL	LOCATION HEX	PRIORITY	FUNCTION
$\overline{\text{RS}}$, SINTR	0	00	1	Reset (hardware and software reset)
$\overline{\text{NMI}}$, SINT16	4	04	2	Nonmaskable interrupt
SINT17	8	08	—	Software interrupt #17
SINT18	12	0C	—	Software interrupt #18
SINT19	16	10	—	Software interrupt #19
SINT20	20	14	—	Software interrupt #20
SINT21	24	18	—	Software interrupt #21
SINT22	28	1C	—	Software interrupt #22
SINT23	32	20	—	Software interrupt #23
SINT24	36	24	—	Software interrupt #24
SINT25	40	28	—	Software interrupt #25
SINT26	44	2C	—	Software interrupt #26
SINT27	48	30	—	Software interrupt #27
SINT28	52	34	—	Software interrupt #28
SINT29	56	38	—	Software interrupt #29
SINT30	60	3C	—	Software interrupt #30
$\overline{\text{INT0}}$, SINT0	64	40	3	External user interrupt #0
$\overline{\text{INT1}}$, SINT1	68	44	4	External user interrupt #1
$\overline{\text{INT2}}$, SINT2	72	48	5	External user interrupt #2
TINT0, SINT3	76	4C	6	Timer 0 interrupt
BRINT0, SINT4	80	50	7	McBSP #0 receive interrupt
BXINT0, SINT5	84	54	8	McBSP #0 transmit interrupt
BRINT2, SINT6	88	58	9	McBSP #2 receive interrupt (default)†
BXINT2, SINT7	92	5C	10	McBSP #2 transmit interrupt (default)†
$\overline{\text{INT3}}$, TINT1, SINT8	96	60	11	External user interrupt #3/Timer 1 interrupt‡
$\overline{\text{HINT}}$, SINT9	100	64	12	HPI interrupt
BRINT1, SINT10	104	68	13	McBSP #1 receive interrupt (default)†
BXINT1, SINT11	108	6C	14	McBSP #1 transmit interrupt (default)†
DMAC4,SINT12	112	70	15	DMA channel 4
DMAC5,SINT13	116	74	16	DMA channel 5
UART, SINT14	120	78	—	UART interrupt
Reserved	124−127	7C−7F	—	Reserved

† See Table 3−12 for other interrupt selections.
‡ The $\overline{\text{INT3}}$ and TINT1 interrupts are ORed together. To distinguish one from the other, one of these two interrupt sources must be inhibited.

3.20.1 IFR and IMR Registers

The bit layout of the interrupt flag register (IFR) and the interrupt mask register (IMR) is shown in Figure 3−73.

15	14	13	12	11	10	9	8
Reserved	UART	DMAC5	DMAC4	BXINT1	BRINT1	$\overline{\text{HINT}}$	$\overline{\text{INT3}}$†
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	6	5	4	3	2	1	0
BXINT2	BRINT2	BXINT0	BRINT0	TINT0	$\overline{\text{INT2}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read, W = Write

† Bit 8 reflects the status of either $\overline{\text{INT3}}$ or TINT1: these two interrupts are ORed together. To distinguish one from the other, one of these two interrupt sources must be inhibited.

Figure 3−73. IFR and IMR

4 Documentation Support

The following documents are available for the TMS320C54CST chip.

- *Client Side Telephony (CST) Chip Software User's Guide* (literature number SPRU029)
- *TMS320C54CST Bootloader Technical Reference* (literature number SPRA853)

Extensive documentation supports all TMS320™ DSP family of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the C5000™ platform of DSPs:

- *TMS320C54x™ DSP Functional Overview* (literature number SPRU307)
- Calculation of *TMS320LC54x Power Dissipation Application Report* (literature number SPRA164)
- Device-specific data sheets
- Complete user's guides
- Development support tools
- Hardware and software application reports

The five-volume *TMS320C54x DSP Reference Set* (literature number SPRU210) consists of:

- *Volume 1: CPU and Peripherals* (literature number SPRU131)
- *Volume 2: Mnemonic Instruction Set* (literature number SPRU172)
- *Volume 3: Algebraic Instruction Set* (literature number SPRU179)
- *Volume 4: Applications Guide* (literature number SPRU173)
- *Volume 5: Enhanced Peripherals* (literature number SPRU302)

The reference set describes in detail the TMS320C54x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Information regarding TI DSP products is also available on the Worldwide Web at *http://www.ti.com* uniform resource locator (URL).

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4.1 Device and Development Tool Support Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 DSP devices and support tools. Each TMS320 DSP comercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully-qualified production device

Support tool development evolutionary flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development support product

TMX and TMP devices and TMDX development−support tools are shipped with appropriate disclaimers describing their limitations and intended uses. Experimental devices (TMX) may not be representative of a final product and Texas Instruments reserves the right to change or discontinue these products without notice.

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate that the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320C54CST DSP.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to DV_{SS}. Figure 5−1 provides the test load circuit values for a 3.3-V device.

Supply voltage I/O range, DV_{DD} . . . . . −0.3 V to 4.0 V
Supply voltage core range, CV_{DD} . . . . . −0.3 V to 2.0 V
Input voltage range . . . . . −0.3 V to 4.5 V
Output voltage range . . . . . −0.3 V to 4.5 V
Operating case temperature range, T_C . . . . . 0°C to 100°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C

5.2 Recommended Operating Conditions

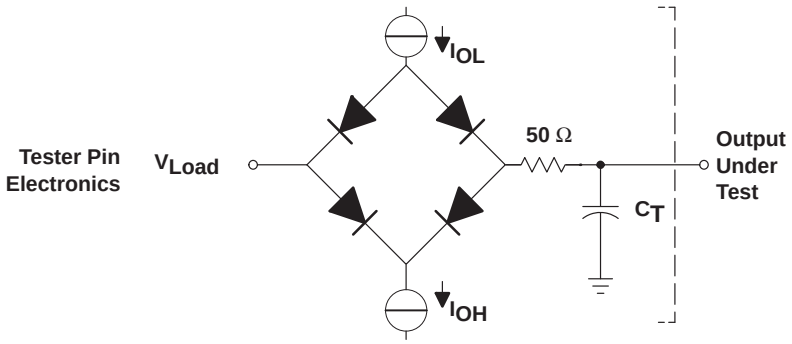
			MIN	NOM	MAX	UNIT
DV_{DD}	Device supply voltage, I/O †		2.7	3.3	3.6	V
CV_{DD}	Device supply voltage, core		1.42	1.5	1.65	V
C1A5V	Supply Voltage, DAA‡		4.75	5	5.25	V
DV_{SS}, CV_{SS}	Supply voltage, GND			0		V
V_{IH}	High-level input voltage, I/O	$\overline{RS}$, $\overline{INTn}$, $\overline{NMI}$, X2/CLKIN, $\overline{BIO}$, $\overline{TRST}$, Dn, An, HDn, CLKMDn, BCLKRn, BCLKXn, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, $\overline{HAS}$, RX, TCK	2.4		DV_{DD} + 0.3	V
		All other inputs	2		DV_{DD} + 0.3	
V_{IL}	Low-level input voltage		−0.3		0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		0		100	°C

† DV_{DD} must be > C1A5V − 3.3 V during power-up.
‡ C1A5V must be > DV_{DD} − 0.5 V during power-up.

5.3 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage‡		DV_{DD} = 3 V to 3.6 V, I_{OH} = MAX	2.4			V
			DV_{DD} = 2.7 V to 3 V, I_{OH} = MAX	2.2			
V_{OL}	Low-level output voltage‡		I_{OL} = MAX			0.4	V
I_{IZ}	Input current in high impedance	A[22:0]	DV_{DD} = MAX, V_O = DV_{SS} to DV_{DD}	−275		275	µA
I_I	Input current (V_I = DV_{SS} to DV_{DD})	X2/CLKIN		−40		40	µA
		$\overline{TRST}$	With internal pulldown	−10		800	µA
		HPIENA	With internal pulldown, $\overline{RS}$ = 0	−10		400	
		TMS, TCK, TDI, HPI§	With internal pullups	−400		10	
		D[15:0], HD[7:0]	Bus holders enabled, DV_{DD} = MAX☆	−275		275	
		All other input-only pins		−5		5	
I_{DDC}	Supply current, core CPU		CV_{DD} = 1.5 V, f_X = 120 MHz,¶ T_C = 25°C		60#		mA
I_{DDP}	Supply current, pins		DV_{DD} = 3.0 V, f_X = 120 MHz,¶ T_C = 25°C		20‖		mA
I_{DD}	Supply current, standby	IDLE2	PLL × 1 mode, 20 MHz input		2		mA
		IDLE3	Divide-by-two mode, CLKIN stopped		1□		mA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All values are typical unless otherwise specified.
‡ All input and output voltage levels except $\overline{RS}$, $\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$, X2/CLKIN, CLKMD1–CLKMD3 are LVTTL-compatible.
§ HPI input signals except for HPIENA.
¶ Clock mode: PLL × 1 with external source
# This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.
‖ This value was obtained with single-cycle external writes, CLKOFF = 0 and load = 15 pF. For more details on how this calculation is performed, refer to the *Calculation of TMS320LC54x Power Dissipation* application report (literature number SPRA164).
☆ $V_{IL(MIN)} \le V_I \le V_{IL(MAX)}$ or $V_{IH(MIN)} \le V_I \le V_{IH(MAX)}$
□ Material with high I_{DD} has been observed with an I_{DD} as high as 7 mA during high temperature testing.



Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{Load} = 1.5 V
C_T = 20-pF typical load circuit capacitance

Figure 5−1. 3.3-V Test Load Circuit

5.4 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don't care level

Letters and symbols and their meanings:

H	High
L	Low
V	Valid
Z	High impedance

5.5 Clock Options

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four or multiplied by one of several values to generate the internal machine cycle.

5.5.1 Internal Oscillator With External Crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN and by selecting the proper combination of CLKMD inputs. The frequency of CLKOUT is a multiple of the oscillator frequency. The multiply ratio is determined by the bit settings in the CLKMD register. The crystal should be fundamental-mode and parallel resonant, with a maximum effective series resistance specification of 30 Ω, power dissipation of 1 mW, and a load capacitance of 10 pF.

The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 5−2. The load capacitors, C_1 and C_2, should be chosen such that the equation below is satisfied. C_L in the equation is the load capacitance specified for the crystal (10 pF). C_1 and C_2 are typically 15 pF, but may need to be adjusted due to PC board stray capacitance.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5−1. Recommended Operating Conditions of Internal Oscillator With External Crystal (See Figure 5−2)

		NOM	UNIT
f_{clock}	Input clock frequency	14.7456	MHz

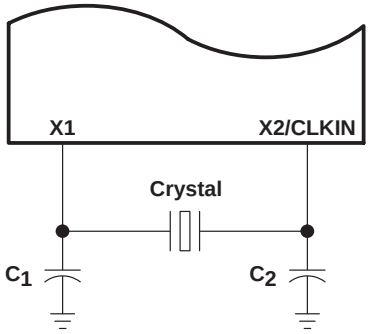


Figure 5−2. Internal Oscillator With External Crystal

5.5.2 Divide-By-Two and Divide-By-Four Clock Options

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in Section 3.10.

When an external clock source is used, the frequency injected must conform to specifications listed in Table 5−3.

An external frequency source can be used by applying an input clock to X2/CLKIN with X1 left unconnected.

Table 5−2 shows the configuration options for the CLKMD pins that generate the external divide-by-2 or divide-by-4 clock option.

Table 5−2. Clock Mode Pin Settings for the Divide-By-2 and By Divide-by-4 Clock Options

CLKMD1	CLKMD2	CLKMD3	CLOCK MODE
0	0	0	1/2, PLL and oscillator disabled
1	0	1	1/4, PLL disabled
1	1	1	1/2, PLL disabled

Table 5−3 and Table 5−4 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−3).

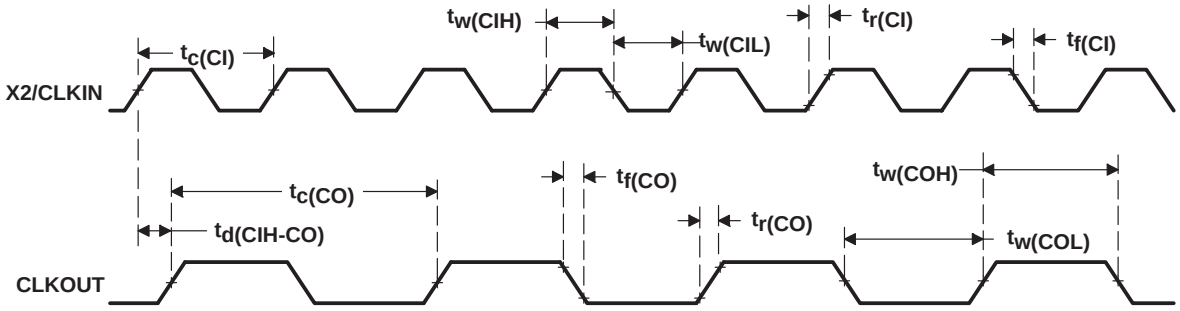
Table 5−3. Divide-By-2 and Divide-by-4 Clock Options Timing Requirements

		MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	20		ns
$t_{f(CI)}$	Fall time, X2/CLKIN		4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN		4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	4		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	4		ns

Table 5−4. Divide-By-2 and Divide-by-4 Clock Options Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	8.33†		‡	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high to CLKOUT high/low	4	7	11	ns
$t_{f(CO)}$	Fall time, CLKOUT		1		ns
$t_{r(CO)}$	Rise time, CLKOUT		1		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H − 3	H	H + 3	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H − 3	H	H + 3	ns

† It is recommended that the PLL clocking option be used for maximum frequency operation.
‡ This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.



NOTE A: The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.

Figure 5−3. External Divide-by-Two Clock Timing

5.5.3 Multiply-By-N Clock Option (PLL Enabled)

The frequency of the reference clock provided at the X2/CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle. The selection of the clock mode and the value of N is described in Section 3.10. Following reset, the software PLL can be programmed for the desired multiplication factor. Refer to the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131) for detailed information on programming the PLL.

When an external clock source is used, the external frequency injected must conform to specifications listed in Table 5−5.

Table 5−5 and Table 5−6 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−4).

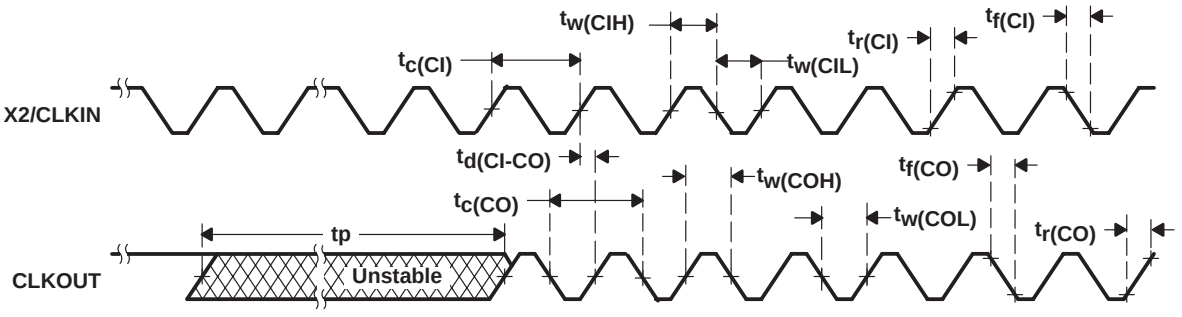
Table 5−5. Multiply-By-N Clock Option Timing Requirements

			MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	Integer PLL multiplier N (N = 1−15)†	20	200	ns
		PLL multiplier N = x.5†	20	100	
		PLL multiplier N = x.25, x.75†	20	50	
$t_{f(CI)}$	Fall time, X2/CLKIN			4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN			4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low		4		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high		4		ns

† N is the multiplication factor.

Table 5−6. Multiply-By-N Clock Option Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	8.33			ns
$t_{d(CI-CO)}$	Delay time, X2/CLKIN high/low to CLKOUT high/low	4	7	11	ns
$t_{f(CO)}$	Fall time, CLKOUT		2		ns
$t_{r(CO)}$	Rise time, CLKOUT		2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low		H		ns
$t_{w(COH)}$	Pulse duration, CLKOUT high		H		ns
t_p	Transitory phase, PLL lock-up time			30	μs



NOTE A: The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.

Figure 5−4. Multiply-by-One Clock Timing

5.6 Memory and Parallel I/O Interface Timing

5.6.1 Memory Read

External memory reads can be performed in consecutive or nonconsecutive mode under control of the CONSEC bit in the BSCR. Table 5−7 and Table 5−8 assume testing over recommended operating conditions with $\overline{\text{MSTRB}}$ = 0 and H = 0.5$t_{c(CO)}$ (see Figure 5−5 and Figure 5−6).

Table 5−7. Memory Read Timing Requirements

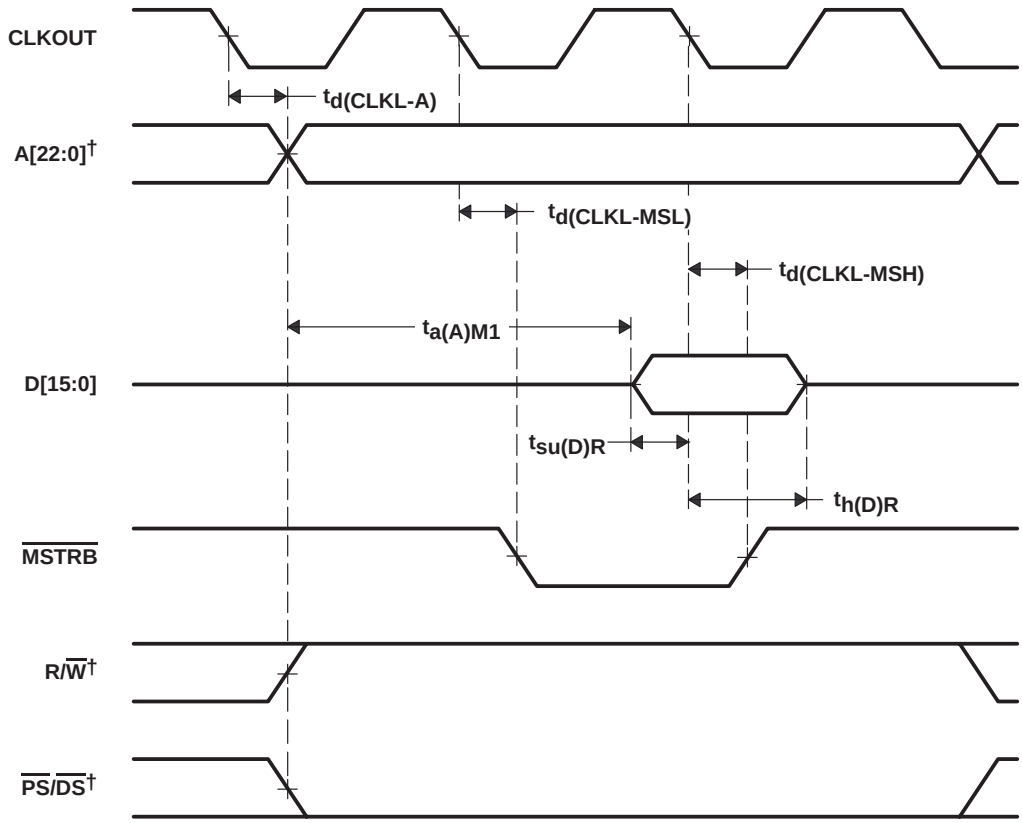
			MIN	MAX	UNIT
$t_{a(A)M1}$	Access time, read data access from address valid, first read access†	For accesses not immediately following a HOLD operation		4H−9	ns
		For read accesses immediately following a HOLD operation		4H−11	ns
$t_{a(A)M2}$	Access time, read data access from address valid, consecutive read accesses†			2H−9	ns
$t_{su(D)R}$	Setup time, read data valid before CLKOUT low		7		ns
$t_{h(D)R}$	Hold time, read data valid after CLKOUT low		0		ns

† Address,R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

Table 5−8. Memory Read Switching Characteristics

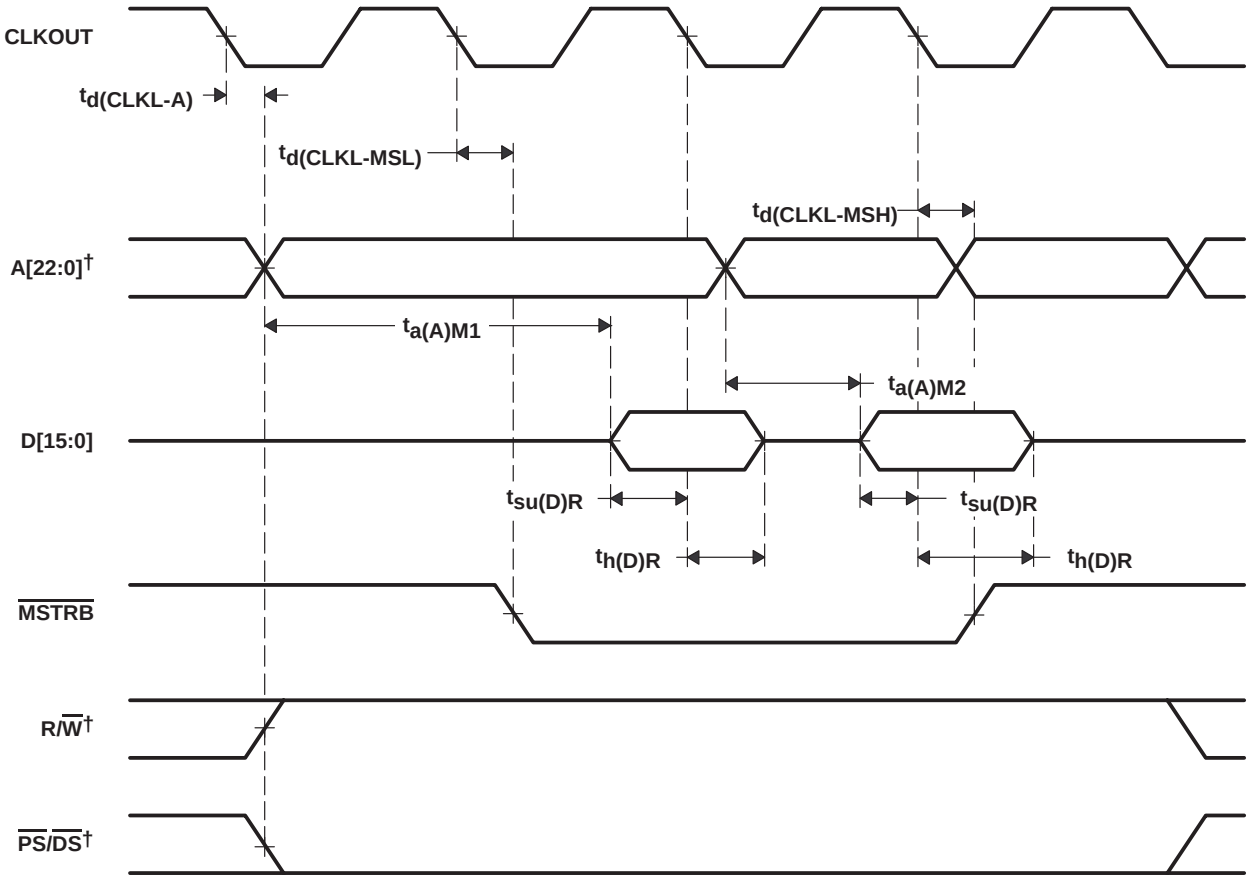
PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	−1	4	ns
		For read accesses immediately following a HOLD operation	−1	6	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low		−1	4	ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high		0	4	ns

† Address,R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.



† Address,R/W, PS, DS, and IS timings are all included in timings referenced as address.

Figure 5−5. Nonconsecutive Mode Memory Reads



† Address,R/W, PS, DS, and IS timings are all included in timings referenced as address.

Figure 5−6. Consecutive Mode Memory Reads

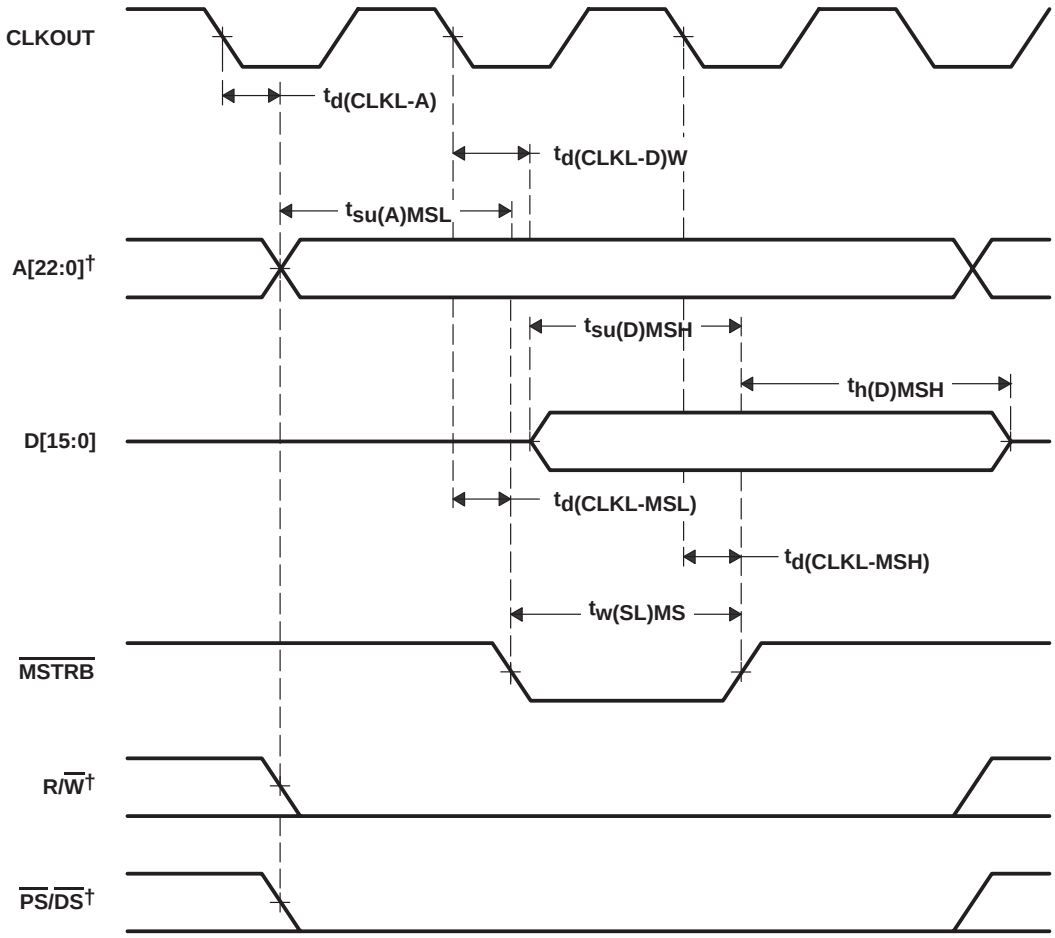
5.6.2 Memory Write

Table 5−9 assumes testing over recommended operating conditions with $\overline{\text{MSTRB}}$ = 0 and H = 0.5$t_{c(CO)}$ (see Figure 5−7).

Table 5−9. Memory Write Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	− 1	4	ns
		For read accesses immediately following a HOLD operation	− 1	6	ns
$t_{su(A)MSL}$	Setup time, address valid before $\overline{\text{MSTRB}}$ low†	For accesses not immediately following a HOLD operation	2H − 3		ns
		For read accesses immediately following a HOLD operation	2H − 5		ns
$t_{d(CLKL-D)W}$	Delay time, CLKOUT low to data valid		− 1	5	ns
$t_{su(D)MSH}$	Setup time, data valid before $\overline{\text{MSTRB}}$ high		2H − 5	2H +6	ns
$t_{h(D)MSH}$	Hold time, data valid after $\overline{\text{MSTRB}}$ high		2H − 5	2H + 6	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low		− 1	4	ns
$t_{w(SL)MS}$	Pulse duration, $\overline{\text{MSTRB}}$ low		2H − 2		ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high		0	4	ns

† Address, R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.



† Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

Figure 5−7. Memory Write ($\overline{MSTRB}$ = 0)

5.6.3 I/O Read

Table 5−10 and Table 5−11 assume testing over recommended operating conditions, $\overline{\text{IOSTRB}}$ = 0, and H = 0.5$t_{c(CO)}$ (see Figure 5−8).

Table 5−10. I/O Read Timing Requirements

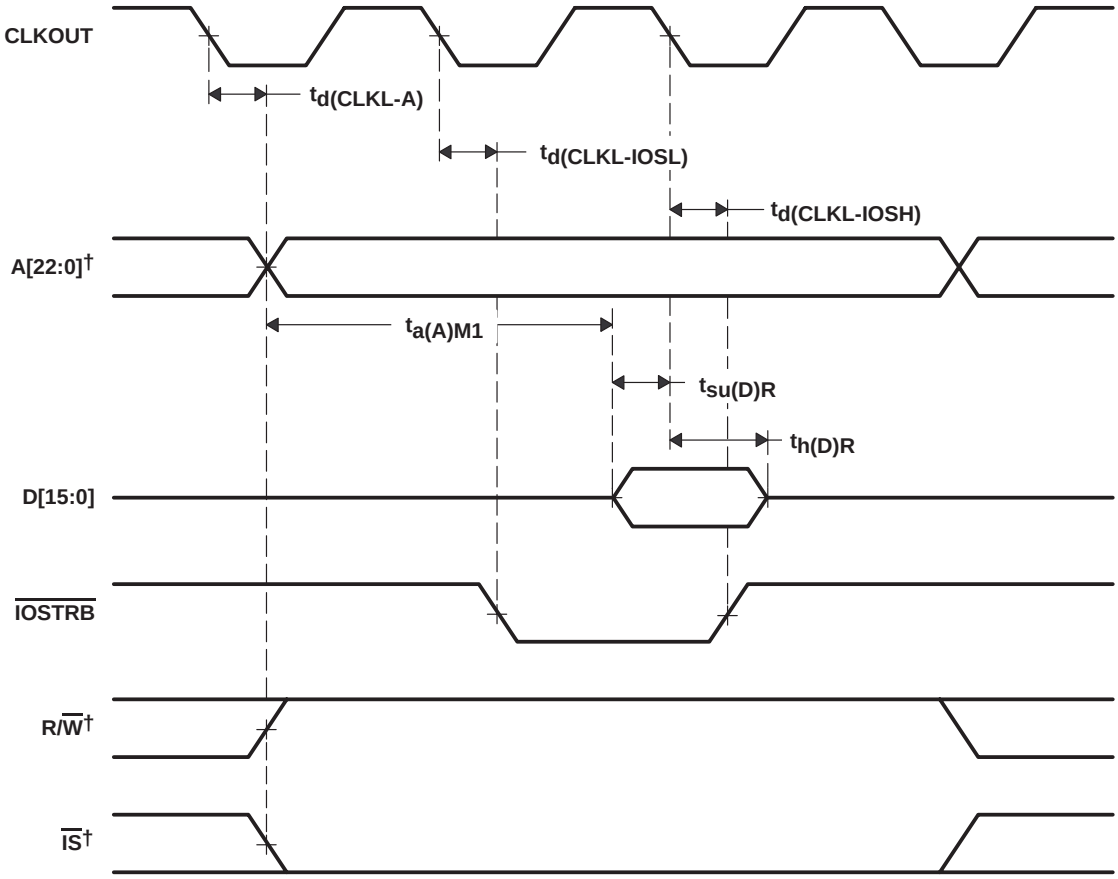
			MIN	MAX	UNIT
$t_{a(A)M1}$	Access time, read data access from address valid, first read access†	For accesses not immediately following a HOLD operation		4H − 9	ns
		For read accesses immediately following a HOLD operation		4H − 11	ns
$t_{su(D)R}$	Setup time, read data valid before CLKOUT low		7		ns
$t_{h(D)R}$	Hold time, read data valid after CLKOUT low		0		ns

† Address R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are included in timings referenced as address.

Table 5−11. I/O Read Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	− 1	4	ns
		For read accesses immediately following a HOLD operation	− 1	6	ns
$t_{d(CLKL-IOSL)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ low		− 1	4	ns
$t_{d(CLKL-IOSH)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ high		0	4	ns

† Address R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are included in timings referenced as address.



† Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

Figure 5−8. Parallel I/O Port Read ($\overline{IOSTRB}$ = 0)

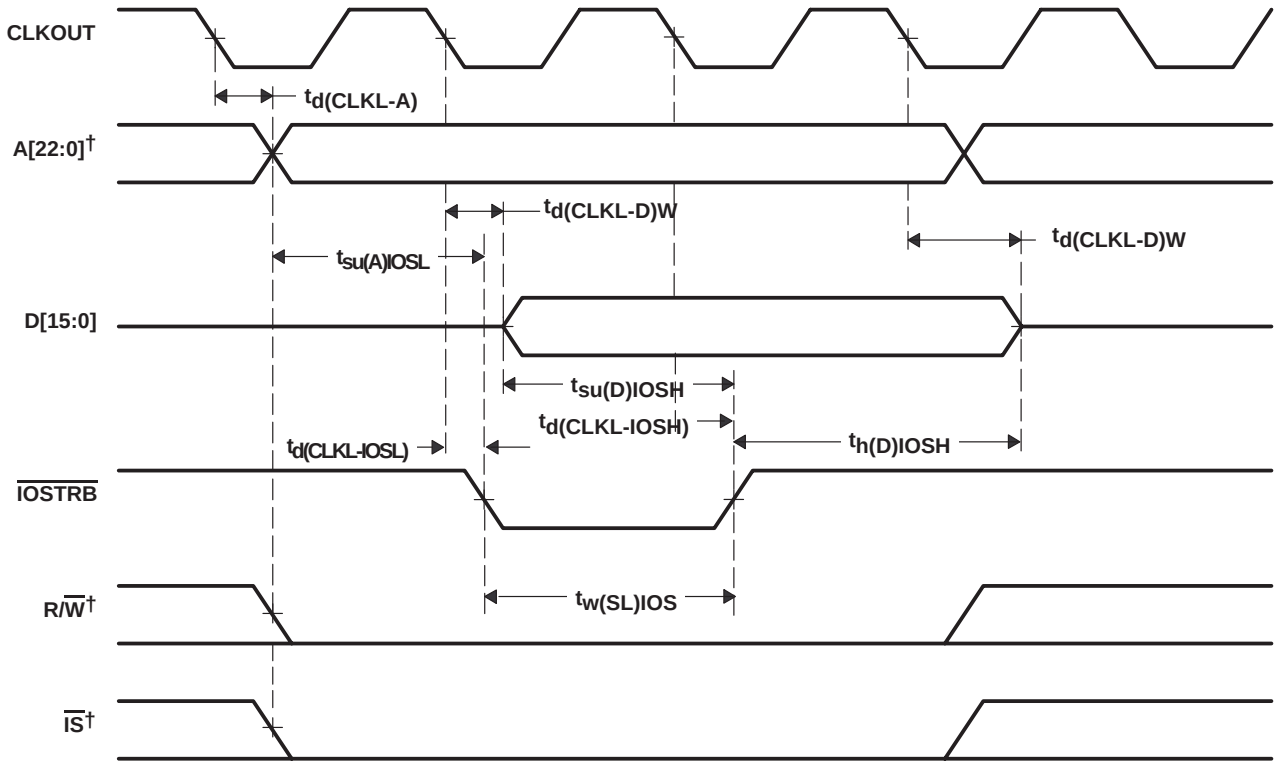
5.6.4 I/O Write

Table 5−12 assumes testing over recommended operating conditions, $\overline{\text{IOSTRB}}$ = 0, and H = 0.5$t_{c(CO)}$ (see Figure 5−9).

Table 5−12. I/O Write Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid†	For accesses not immediately following a HOLD operation	− 1	4	ns
		For read accesses immediately following a HOLD operation	− 1	6	ns
$t_{su(A)IOSL}$	Setup time, address valid before $\overline{\text{IOSTRB}}$ low†	For accesses not immediately following a HOLD operation	2H − 3		ns
		For read accesses immediately following a HOLD operation	2H − 5		ns
$t_{d(CLKL-D)W}$	Delay time, CLKOUT low to write data valid		− 1	4	ns
$t_{su(D)IOSH}$	Setup time, data valid before $\overline{\text{IOSTRB}}$ high		2H − 5	2H + 6	ns
$t_{h(D)IOSH}$	Hold time, data valid after $\overline{\text{IOSTRB}}$ high		2H − 5	2H + 6	ns
$t_{d(CLKL-IOSL)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ low		− 1	4	ns
$t_{w(SL)IOS}$	Pulse duration, $\overline{\text{IOSTRB}}$ low		2H − 2		ns
$t_{d(CLKL-IOSH)}$	Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ high		0	4	ns

† Address R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are included in timings referenced as address.



† Address, R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

Figure 5−9. Parallel I/O Port Write ($\overline{\text{IOSTRB}}$ = 0)

5.7 Ready Timing for Externally Generated Wait States

Table 5−13 and Table 5−14 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−10, Figure 5−11, Figure 5−12, and Figure 5−13).

Table 5−13. Ready Timing Requirements for Externally Generated Wait States†

		MIN	MAX	UNIT
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	7		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	0		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after $\overline{MSTRB}$ low‡		4H − 4	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after $\overline{MSTRB}$ low‡	4H		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after $\overline{IOSTRB}$ low‡		4H − 4	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after $\overline{IOSTRB}$ low‡	4H		ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.
‡ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

Table 5−14. Ready Switching Characteristics for Externally Generated Wait States†

PARAMETER		MIN	MAX	UNIT
$t_{d(MSCL)}$	Delay time, $\overline{MSC}$ low to CLKOUT low	− 1	4	ns
$t_{d(MSCH)}$	Delay time, CLKOUT low to $\overline{MSC}$ high	− 1	4	ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.

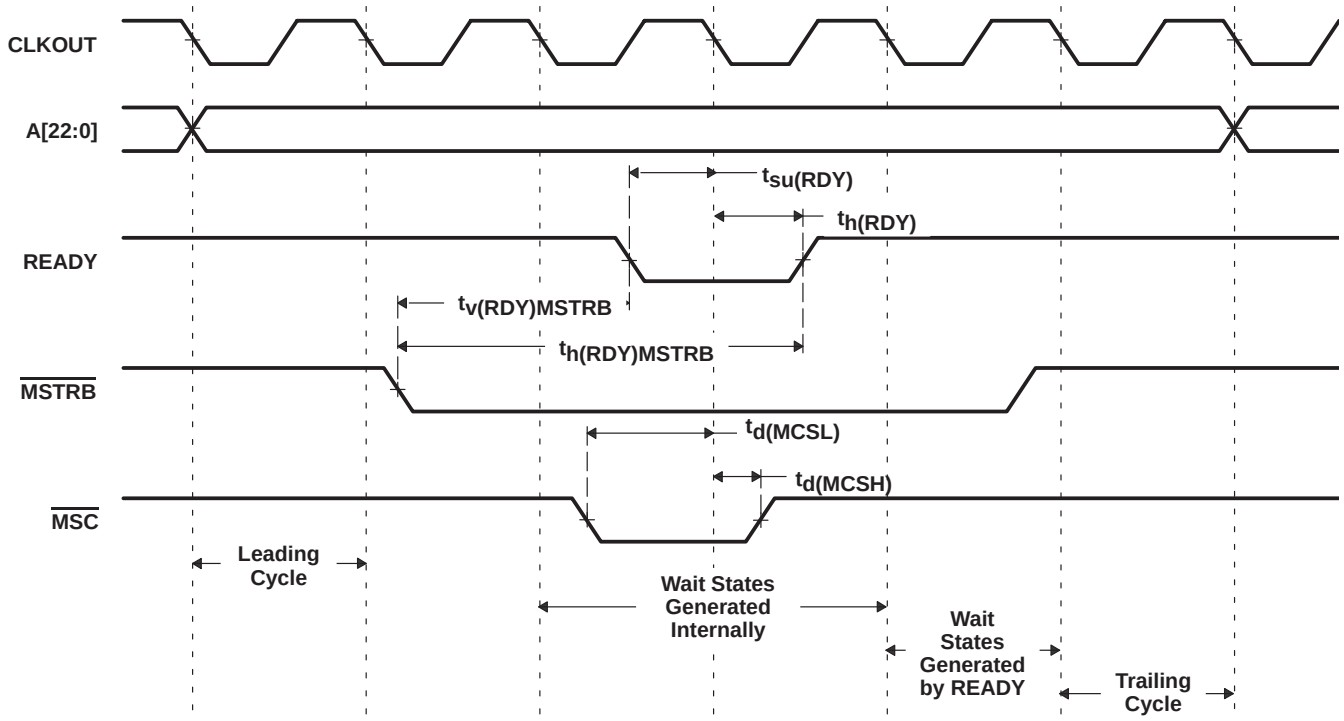


Figure 5−10. Memory Read With Externally Generated Wait States

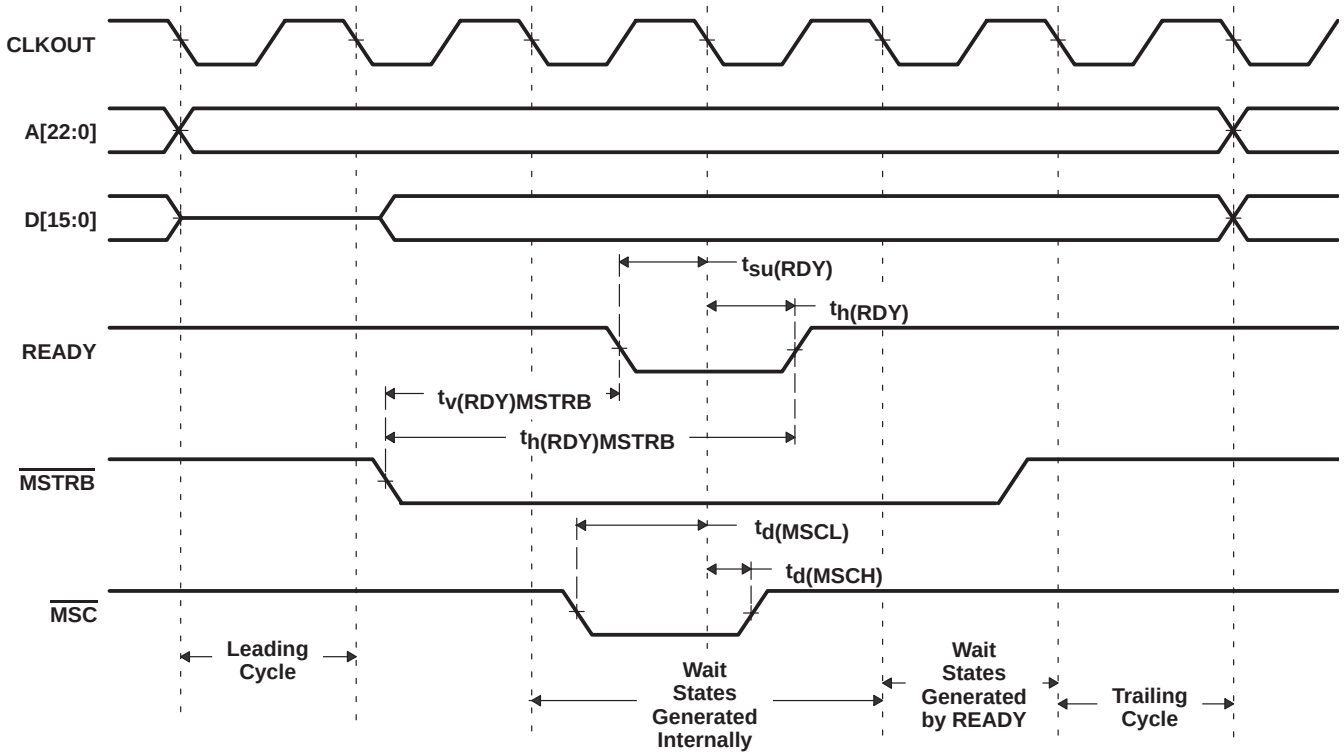


Figure 5−11. Memory Write With Externally Generated Wait States

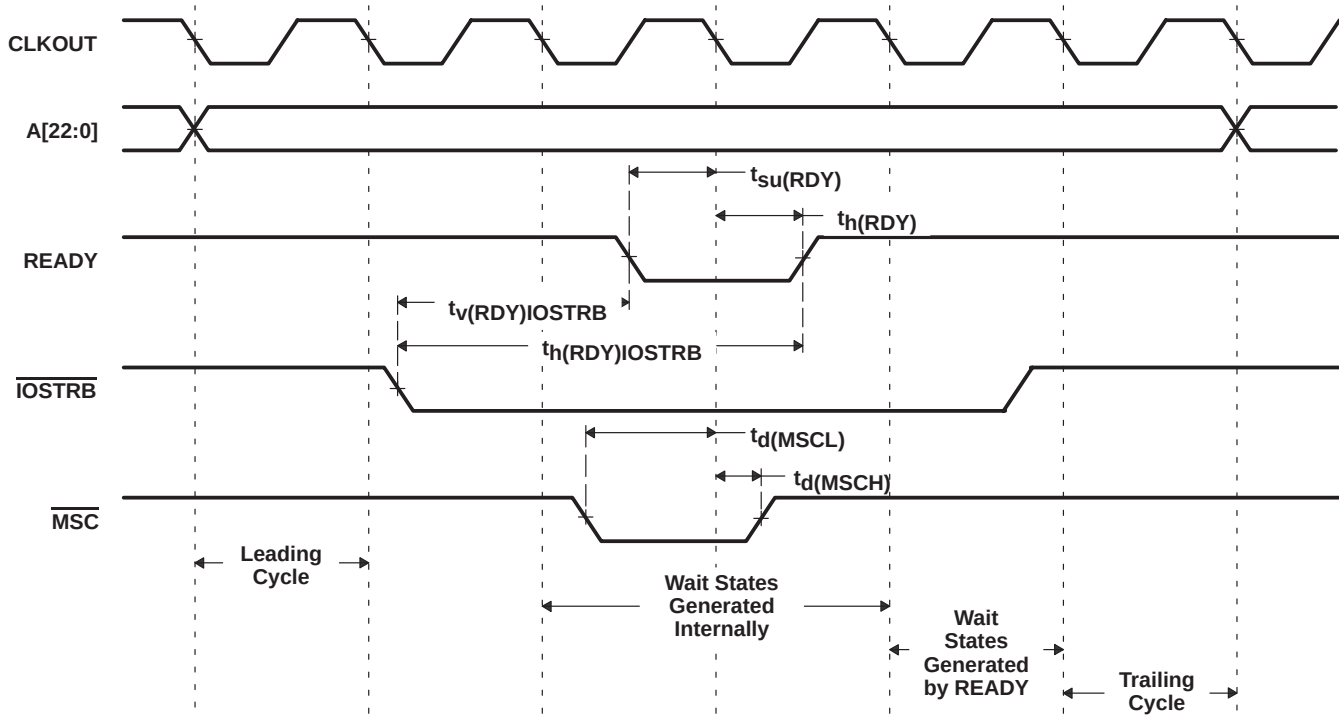


Figure 5−12. I/O Read With Externally Generated Wait States

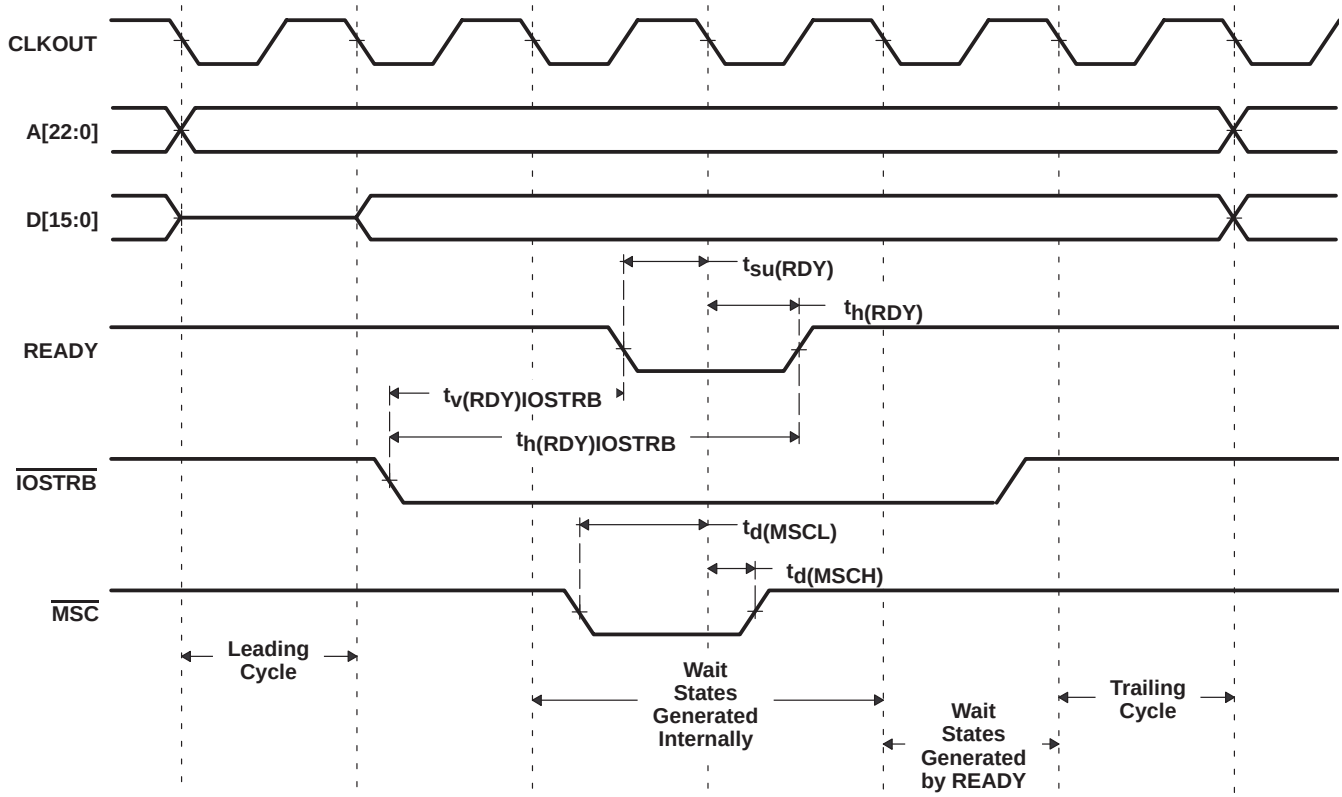


Figure 5−13. I/O Write With Externally Generated Wait States

5.8 $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings

Table 5−15 and Table 5−16 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−14).

Table 5−15. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing Requirements

		MIN	MAX	UNIT
$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low duration	4H+8		ns
$t_{su(HOLD)}$	Setup time, $\overline{\text{HOLD}}$ before CLKOUT low	7		ns

Table 5−16. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{dis(CLKL-A)}$	Disable time, Address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ high impedance from CLKOUT low		3	ns
$t_{dis(CLKL-RW)}$	Disable time, R/$\overline{\text{W}}$ high impedance from CLKOUT low		3	ns
$t_{dis(CLKL-S)}$	Disable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ high impedance from CLKOUT low		3	ns
$t_{en(CLKL-A)}$	Enable time, Address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ valid from CLKOUT low		2H+4	ns
$t_{en(CLKL-RW)}$	Enable time, R/$\overline{\text{W}}$ enabled from CLKOUT low		2H+3	ns
$t_{en(CLKL-S)}$	Enable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ enabled from CLKOUT low	2	2H+3	ns
$t_{v(HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ low after CLKOUT low	− 1	4	ns
	Valid time, $\overline{\text{HOLDA}}$ high after CLKOUT low	− 1	4	ns
$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low duration	2H−3		ns

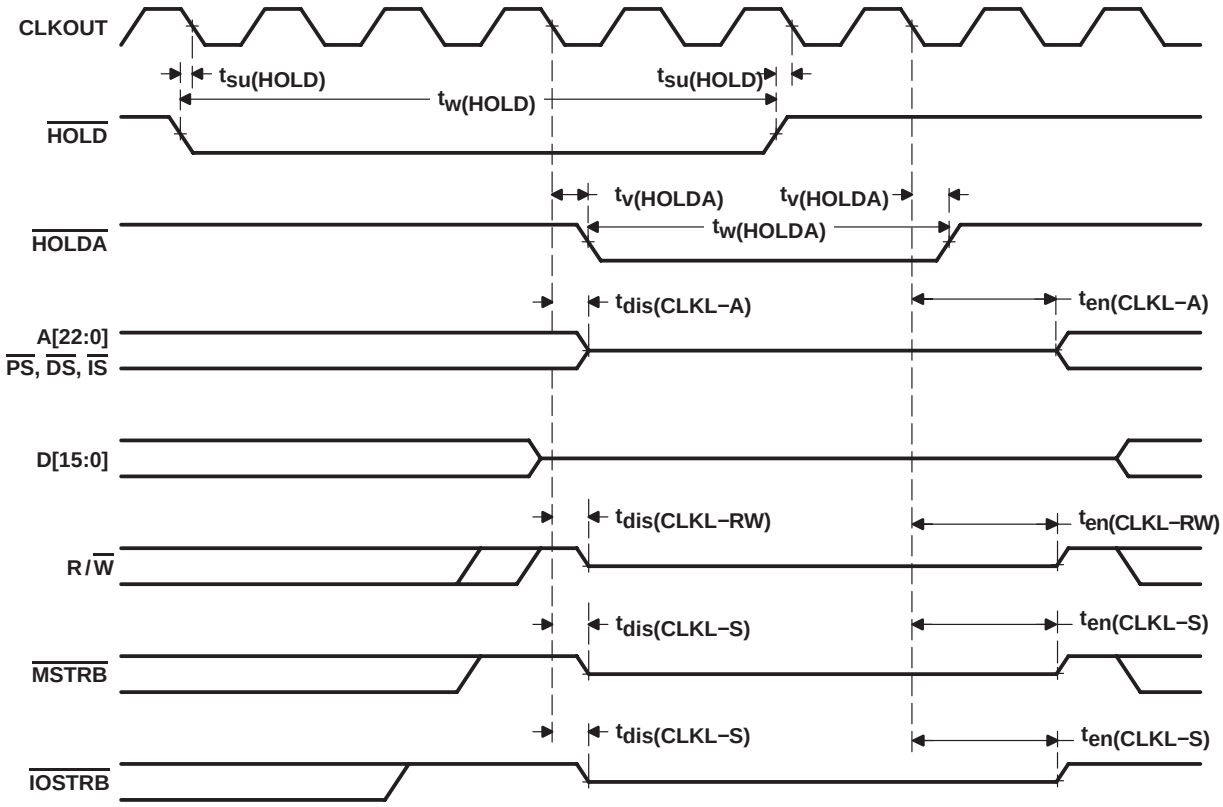


Figure 5−14. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings (HM = 1)

5.9 Reset, $\overline{\text{BIO}}$, Interrupt, and MP/$\overline{\text{MC}}$ Timings

Table 5−17 assumes testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−15, Figure 5−16, and Figure 5−17).

Table 5−17. Reset, $\overline{\text{BIO}}$, Interrupt, and MP/$\overline{\text{MC}}$ Timing Requirements

		MIN	MAX	UNIT
$t_{h(RS)}$	Hold time, $\overline{\text{RS}}$ after CLKOUT low	3		ns
$t_{h(BIO)}$	Hold time, $\overline{\text{BIO}}$ after CLKOUT low	4		ns
$t_{h(INT)}$	Hold time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, after CLKOUT low†	1		ns
$t_{h(MPMC)}$	Hold time, MP/$\overline{\text{MC}}$ after CLKOUT low	4		ns
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RS}}$ low‡§	4H+3		ns
$t_{w(BIO)S}$	Pulse duration, $\overline{\text{BIO}}$ low, synchronous	2H+3		ns
$t_{w(BIO)A}$	Pulse duration, $\overline{\text{BIO}}$ low, asynchronous	4H		ns
$t_{w(INTH)S}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (synchronous)	2H+2		ns
$t_{w(INTH)A}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (asynchronous)	4H		ns
$t_{w(INTL)S}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (synchronous)	2H+2		ns
$t_{w(INTL)A}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (asynchronous)	4H		ns
$t_{w(INTL)WKP}$	Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low for IDLE2/IDLE3 wakeup	8		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RS}}$ before X2/CLKIN low¶	3		ns
$t_{su(BIO)}$	Setup time, $\overline{\text{BIO}}$ before CLKOUT low	7		ns
$t_{su(INT)}$	Setup time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, $\overline{\text{RS}}$ before CLKOUT low	7		ns
$t_{su(MPMC)}$	Setup time, MP/$\overline{\text{MC}}$ before CLKOUT low	5		ns

† The external interrupts ($\overline{\text{INT0}}$−$\overline{\text{INT3}}$, $\overline{\text{NMI}}$) are synchronized to the core CPU by way of a two-flip-flop synchronizer that samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1−0−0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

‡ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{\text{RS}}$ must be held low for at least 50 µs to ensure synchronization and lock-in of the PLL.

§ Note that $\overline{\text{RS}}$ may cause a change in clock frequency, therefore changing the value of H.

¶ The diagram assumes clock mode is divide-by-2 and the CLKOUT divide factor is set to no-divide mode (DIVFCT=00 field in the BSCR).

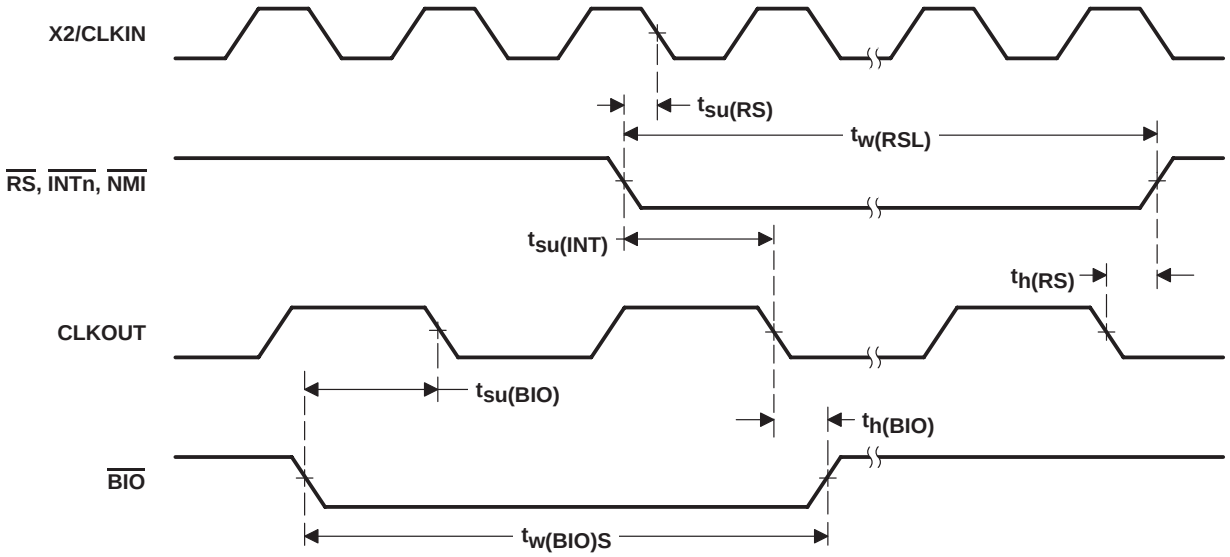


Figure 5−15. Reset and $\overline{\text{BIO}}$ Timings

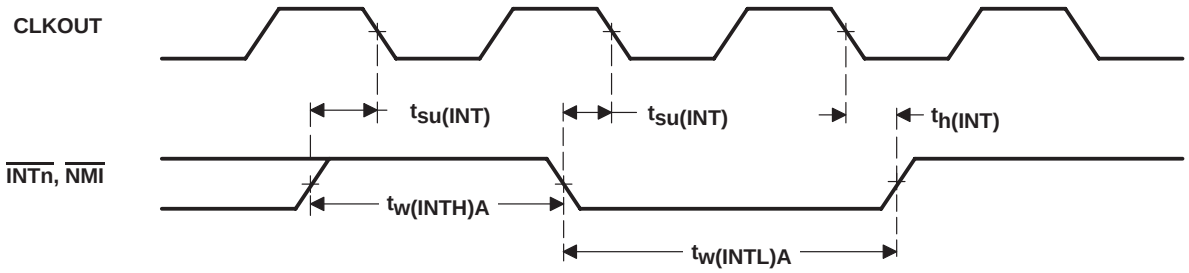


Figure 5−16. Interrupt Timing

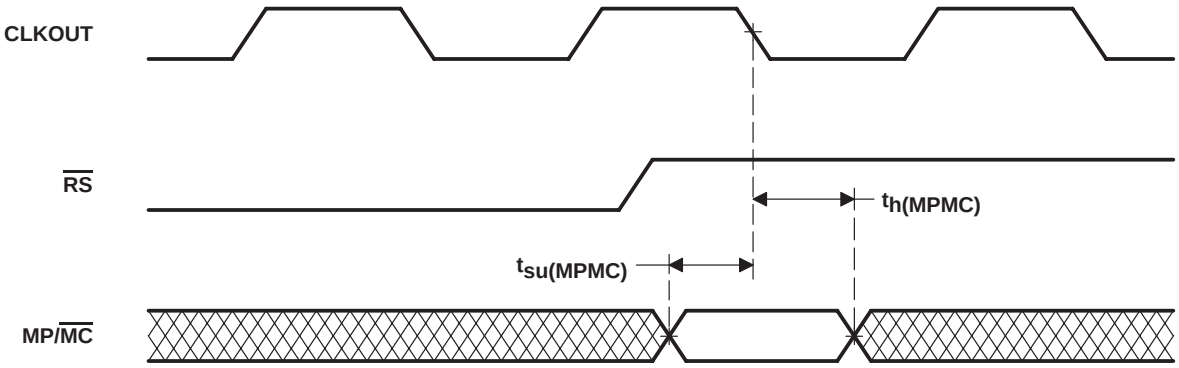


Figure 5−17. MP/$\overline{MC}$ Timing

5.10 Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Timings

Table 5−18 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−18).

Table 5−18. Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CLKL-IAQL)}$	Delay time, CLKOUT low to $\overline{IAQ}$ low	− 1	4	ns
$t_{d(CLKL-IAQH)}$	Delay time, CLKOUT low to $\overline{IAQ}$ high	− 1	4	ns
$t_{d(A)IAQ}$	Delay time, $\overline{IAQ}$ low to address valid		2	ns
$t_{d(CLKL-IACKL)}$	Delay time, CLKOUT low to $\overline{IACK}$ low	− 1	4	ns
$t_{d(CLKL-IACKH)}$	Delay time, CLKOUT low to $\overline{IACK}$ high	− 1	4	ns
$t_{d(A)IACK}$	Delay time, $\overline{IACK}$ low to address valid		2	ns
$t_{h(A)IAQ}$	Hold time, address valid after $\overline{IAQ}$ high	− 2		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{IACK}$ high	− 2		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low	2H − 2		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low	2H − 2		ns

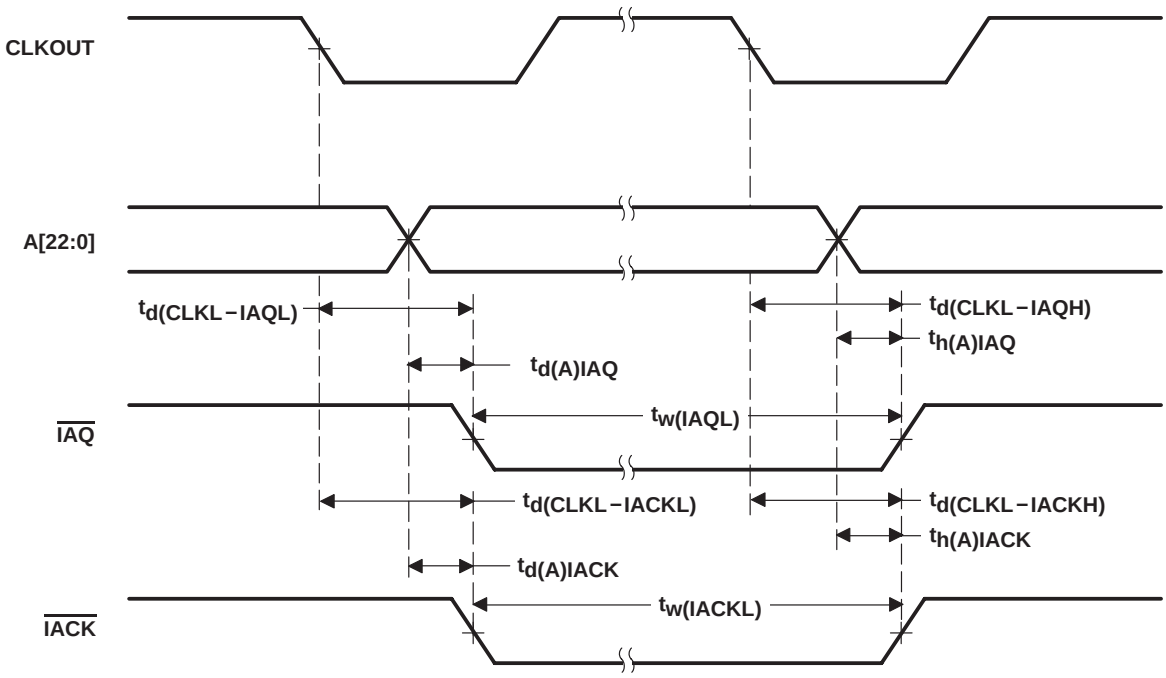


Figure 5−18. Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Timings

5.11 External Flag (XF) and TOUT Timings

Table 5−19 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−19 and Figure 5−20).

Table 5−19. External Flag (XF) and TOUT Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(XF)}$	Delay time, CLKOUT low to XF high	− 1	4	ns
	Delay time, CLKOUT low to XF low	− 1	4	
$t_{d(TOUTH)}$	Delay time, CLKOUT low to TOUT high	− 1	4	ns
$t_{d(TOUTL)}$	Delay time, CLKOUT low to TOUT low	− 1	4	ns
$t_{w(TOUT)}$	Pulse duration, TOUT	2H − 4		ns

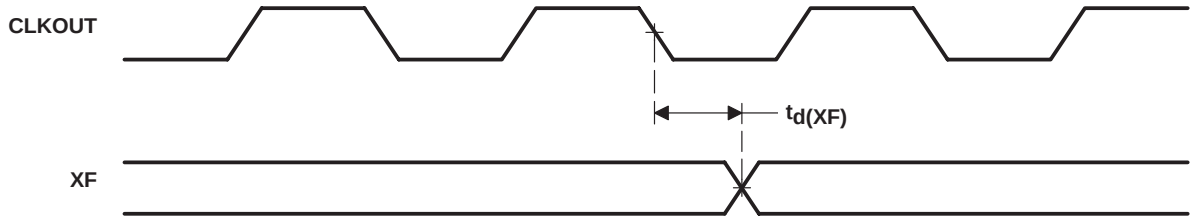


Figure 5−19. External Flag (XF) Timing

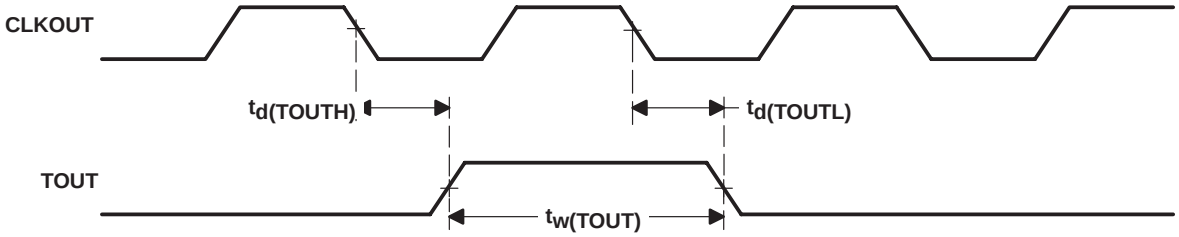


Figure 5−20. TOUT Timing

5.12 Multichannel Buffered Serial Port (McBSP) Timing

5.12.1 McBSP Transmit and Receive Timings

Table 5−20 and Table 5−21 assume testing over recommended operating conditions (see Figure 5−21 and Figure 5−22).

Table 5−20. McBSP Transmit and Receive Timing Requirements†

			MIN	MAX	UNIT
$t_{c(BCKRX)}$	Cycle time, BCLKR/X	BCLKR/X ext	4P‡		ns
$t_{w(BCKRX)}$	Pulse duration, BCLKR/X high or BCLKR/X low	BCLKR/X ext	2P−1‡		ns
$t_{su(BFRH-BCKRL)}$	Setup time, external BFSR high before BCLKR low	BCLKR int	8		ns
		BCLKR ext	1		
$t_{h(BCKRL-BFRH)}$	Hold time, external BFSR high after BCLKR low	BCLKR int	1		ns
		BCLKR ext	2		
$t_{su(BDRV-BCKRL)}$	Setup time, BDR valid before BCLKR low	BCLKR int	7		ns
		BCLKR ext	1		
$t_{h(BCKRL-BDRV)}$	Hold time, BDR valid after BCLKR low	BCLKR int	2		ns
		BCLKR ext	3		
$t_{su(BFXH-BCKXL)}$	Setup time, external BFSX high before BCLKX low	BCLKX int	10		ns
		BCLKX ext	1		
$t_{h(BCKXL-BFXH)}$	Hold time, external BFSX high after BCLKX low	BCLKX int	0		ns
		BCLKX ext	2		
$t_{r(BCKRX)}$	Rise time, BCKR/X	BCLKR/X ext		6	ns
$t_{f(BCKRX)}$	Fall time, BCKR/X	BCLKR/X ext		6	ns

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ P = 0.5 * processor clock

Table 5−21. McBSP Transmit and Receive Switching Characteristics†

PARAMETER				MIN	MAX	UNIT
$t_{c(BCKRX)}$	Cycle time, BCLKR/X		BCLKR/X int	4P‡		ns
$t_{w(BCKRXH)}$	Pulse duration, BCLKR/X high		BCLKR/X int	D − 1§	D + 1§	ns
$t_{w(BCKRXL)}$	Pulse duration, BCLKR/X low		BCLKR/X int	C − 1§	C + 1§	ns
$t_{d(BCKRH-BFRV)}$	Delay time, BCLKR high to internal BFSR valid		BCLKR int	− 3	3	ns
			BCLKR ext	0	12	ns
$t_{d(BCKXH-BFXV)}$	Delay time, BCLKX high to internal BFSX valid		BCLKX int	− 1	5	ns
			BCLKX ext	2	10	
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BCLKX high to BDX high impedance following last data bit of transfer		BCLKX int		6	ns
			BCLKX ext		10	
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	DXENA = 0#	BCLKX int	− 1¶	10	ns
			BCLKX ext	2	20	
$t_{d(BFXH-BDXV)}$	Delay time, BFSX high to BDX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode		BFSX int	−1¶	7	ns
			BFSX ext	2	11	

† CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ P = 0.5 * processor clock
§ T = BCLKRX period = (1 + CLKGDV) * 2P
C = BCLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
D = BCLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ Minimum delay times also represent minimum output hold times.
# The transmit delay enable (DXENA) feature of the McBSP is not implemented on the TMS320C54CST.

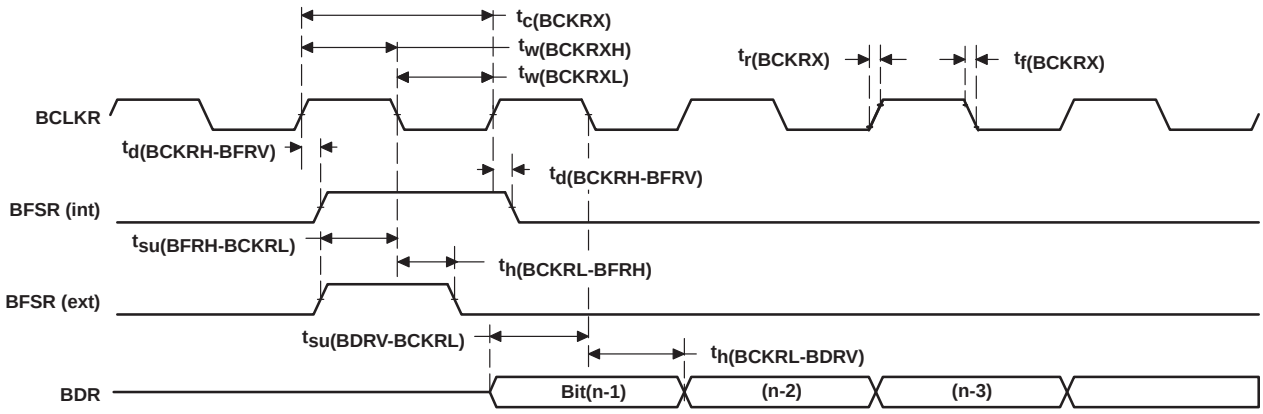


Figure 5−21. McBSP Receive Timings

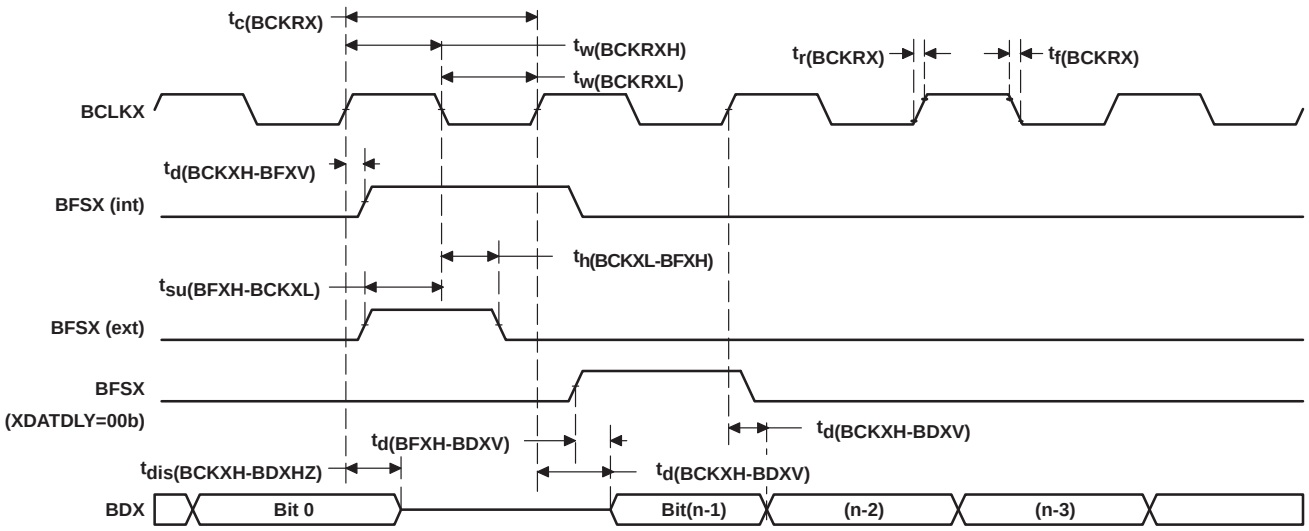


Figure 5−22. McBSP Transmit Timings

5.12.2 McBSP General-Purpose I/O Timing

Table 5−22 and Table 5−23 assume testing over recommended operating conditions (see Figure 5−23).

Table 5−22. McBSP General-Purpose I/O Timing Requirements

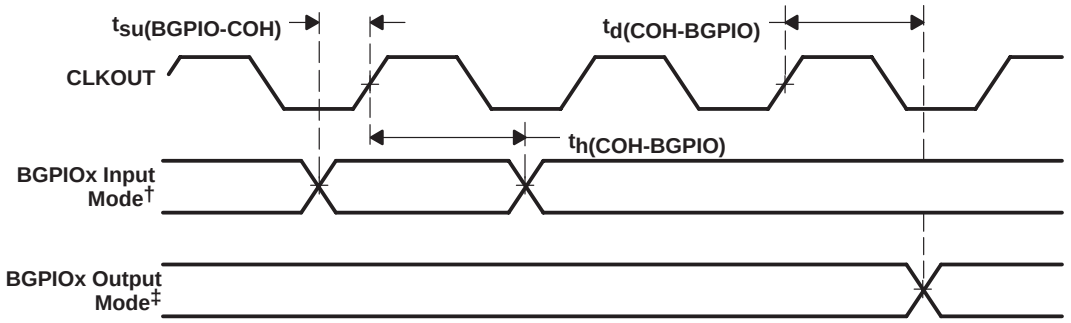
		MIN	MAX	UNIT
$t_{su(BGPIO-COH)}$	Setup time, BGPIOx input mode before CLKOUT high†	7		ns
$t_{h(COH-BGPIO)}$	Hold time, BGPIOx input mode after CLKOUT high†	0		ns

† BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.

Table 5−23. McBSP General-Purpose I/O Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(COH-BGPIO)}$	Delay time, CLKOUT high to BGPIOx output mode‡	− 2	4	ns

‡ BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.



† BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.
‡ BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.

Figure 5−23. McBSP General-Purpose I/O Timings

5.12.3 McBSP as SPI Master or Slave Timing

Table 5−24 to Table 5−31 assume testing over recommended operating conditions (see Figure 5−24, Figure 5−25, Figure 5−26, and Figure 5−27).

Table 5−24. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	12		2 − 6P‡		ns
$t_{h(BCKXL-BDRV)}$	Hold time, BDR valid after BCLKX low	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−25. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXL-BFXL)}$	Hold time, BFSX low after BCLKX low¶	T − 3	T + 4			ns
$t_{d(BFXL-BCKXH)}$	Delay time, BFSX low to BCLKX high#	C − 4	C + 3			ns
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXL-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX low	C − 2	C + 3			ns
$t_{dis(BFXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BFSX high			2P− 4‡	6P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid			4P+ 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

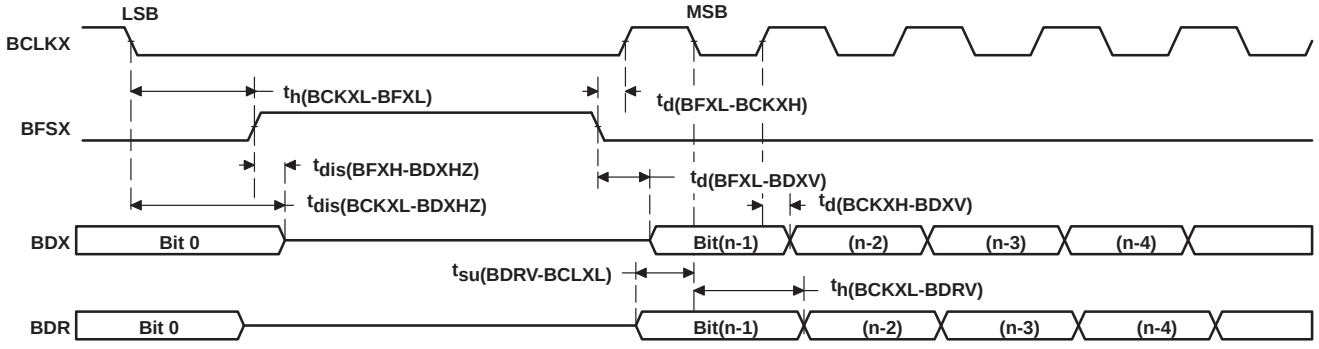


Figure 5−24. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5−26. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	12		2 − 6P‡		ns
$t_{h(BCKXH-BDRV)}$	Hold time, BDR valid after BCLKX high	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−27. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXL-BFXL)}$	Hold time, BFSX low after BCLKX low¶	C −3	C + 4			ns
$t_{d(BFXL-BCKXH)}$	Delay time, BFSX low to BCLKX high#	T − 4	T + 3			ns
$t_{d(BCKXL-BDXV)}$	Delay time, BCLKX low to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXL-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX low	− 2	4	6P − 4‡	10P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid	D − 2	D + 4	4P + 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

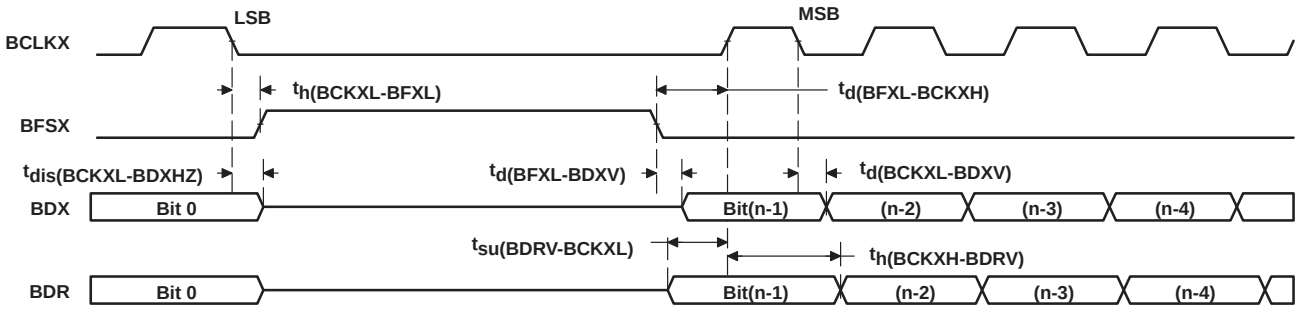


Figure 5−25. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 5−28. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXH)}$	Setup time, BDR valid before BCLKX high	12		2 − 6P‡		ns
$t_{h(BCKXH-BDRV)}$	Hold time, BDR valid after BCLKX high	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−29. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXH-BFXL)}$	Hold time, BFSX low after BCLKX high¶	T − 3	T + 4			ns
$t_{d(BFXL-BCKXL)}$	Delay time, BFSX low to BCLKX low#	D − 4	D + 3			ns
$t_{d(BCKXL-BDXV)}$	Delay time, BCLKX low to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX high	D − 2	D + 3			ns
$t_{dis(BFXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BFSX high			2P − 4‡	6P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid			4P + 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

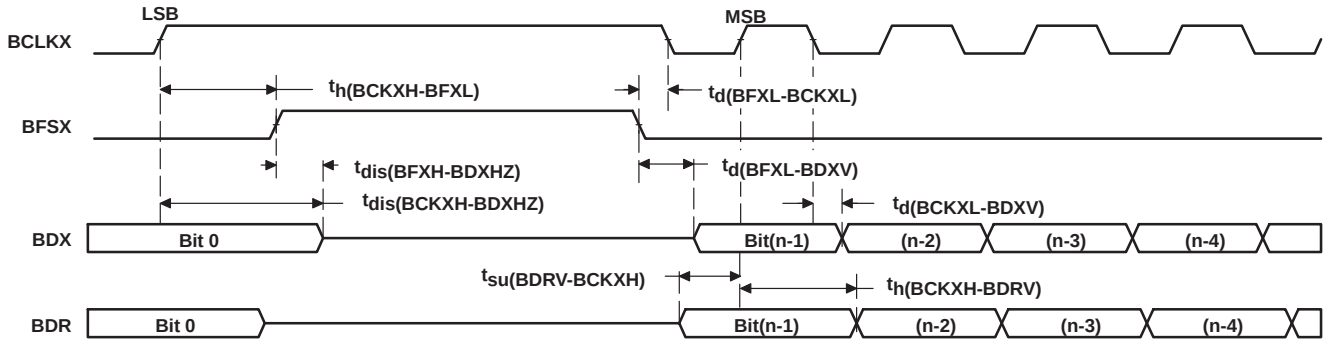


Figure 5−26. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 5−30. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†

		MASTER		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(BDRV-BCKXL)}$	Setup time, BDR valid before BCLKX low	12		2 − 6P‡		ns
$t_{h(BCKXL-BDRV)}$	Hold time, BDR valid after BCLKX low	4		5 + 12P‡		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock

Table 5−31. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†

PARAMETER		MASTER§		SLAVE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(BCKXH-BFXL)}$	Hold time, BFSX low after BCLKX high¶	D − 3	D + 4			ns
$t_{d(BFXL-BCKXL)}$	Delay time, BFSX low to BCLKX low#	T − 4	T + 3			ns
$t_{d(BCKXH-BDXV)}$	Delay time, BCLKX high to BDX valid	− 4	5	6P + 2‡	10P + 17‡	ns
$t_{dis(BCKXH-BDXHZ)}$	Disable time, BDX high impedance following last data bit from BCLKX high	− 2	4	6P − 4‡	10P + 17‡	ns
$t_{d(BFXL-BDXV)}$	Delay time, BFSX low to BDX valid	C − 2	C + 4	4P + 2‡	8P + 17‡	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 0.5 * processor clock
§ T = BCLKX period = (1 + CLKGDV) * 2P
C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

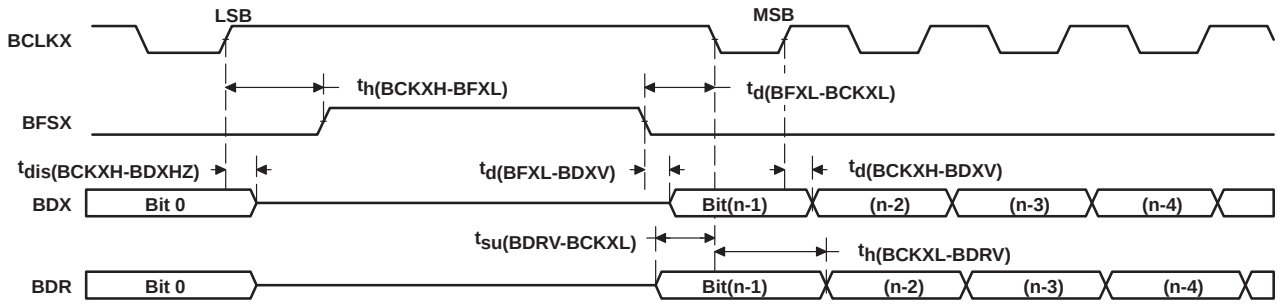


Figure 5−27. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.13 Host-Port Interface Timing

5.13.1 HPI8 Mode

Table 5−32 and Table 5−33 assume testing over recommended operating conditions and P = 0.5 * processor clock (see Figure 5−28 through Figure 5−31). In the following tables, DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$. HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.). HAD stands for HCNTL0, HCNTL1, and HR/$\overline{W}$.

Table 5−32. HPI8 Mode Timing Requirements

		MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HBIL valid before DS low (when $\overline{HAS}$ is not used), or HBIL valid before $\overline{HAS}$ low	6		ns
$t_{h(DSL-HBV)}$	Hold time, HBIL valid after DS low (when $\overline{HAS}$ is not used), or HBIL valid after $\overline{HAS}$ low	3		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before DS low	8		ns
$t_{w(DSL)}$	Pulse duration, DS low	13		ns
$t_{w(DSH)}$	Pulse duration, DS high	7		ns
$t_{su(HDV-DSH)}$	Setup time, HD valid before DS high, HPI write	3		ns
$t_{h(DSH-HDV)W}$	Hold time, HD valid after DS high, HPI write	2		ns
$t_{su(GPIO-COH)}$	Setup time, HDx input valid before CLKOUT high, HDx configured as general-purpose input	3		ns
$t_{h(GPIO-COH)}$	Hold time, HDx input valid before CLKOUT high, HDx configured as general-purpose input	0		ns

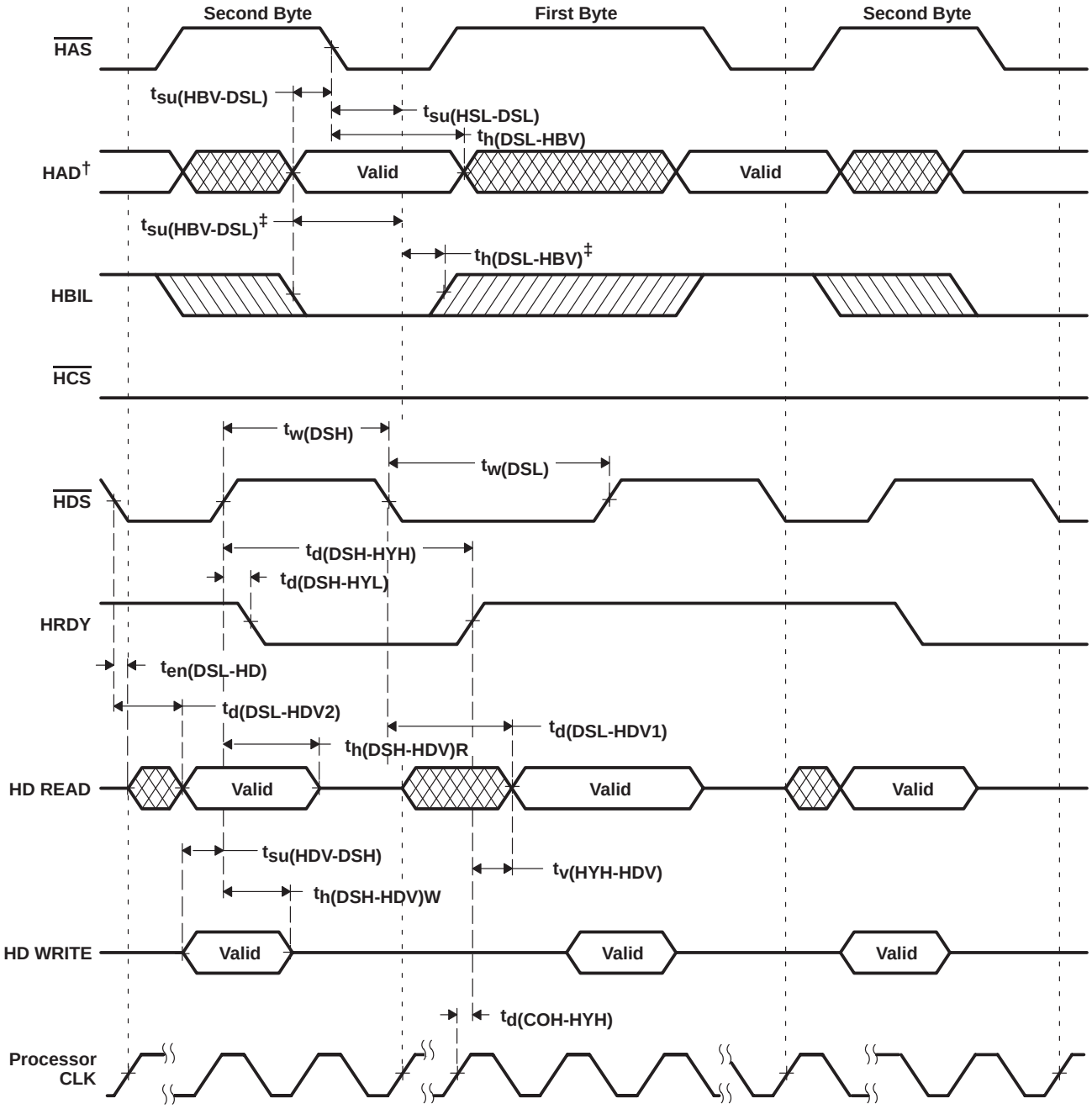
Table 5−33. HPI8 Mode Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{en(DSL-HD)}$	Enable time, HD driven from DS low		0	10	ns
$t_{d(DSL-HDV1)}$	Delay time, DS low to HD valid for first byte of an HPI read	Case 1a: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} < I8H$†		18P+10−$t_{w(DSH)}$	ns
		Case 1b: Memory accesses when DMAC is active in 32-bit mode and $t_{w(DSH)} \geq I8H$†		36P+10−$t_{w(DSH)}$	
		Case 1c: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)} \geq I8H$†		10	
		Case 1d: Memory accesses when DMAC is active in 32-bit mode and $t_{w(DSH)} \geq I8H$†		10	
		Case 2a: Memory accesses when DMAC is inactive and $t_{w(DSH)} < 10H$†		10P+15−$t_{w(DSH)}$	
		Case 2b: Memory accesses when DMAC is inactive and $t_{w(DSH)} \geq 10H$†		10	
		Case 3: Register accesses		10	
$t_{d(DSL-HDV2)}$	Delay time, DS low to HD valid for second byte of an HPI read			10	ns
$t_{h(DSH-HDV)R}$	Hold time, HD valid after DS high, for a HPI read		2		ns
$t_{v(HYH-HDV)}$	Valid time, HD valid after HRDY high			2	ns
$t_{d(DSH-HYL)}$	Delay time, DS high to HRDY low‡			8	ns
$t_{d(DSH-HYH)}$	Delay time, DS high to HRDY high‡	Case 1a: Memory accesses when DMAC is active in 16-bit mode†		18P+6	ns
		Case 1b: Memory accesses when DMAC is active in 32-bit mode†		36P+6	
		Case 2: Memory accesses when DMAC is inactive†		10P+6	
		Case 3: Write accesses to HPIC register§		6P+6	
$t_{d(HCS-HRDY)}$	Delay time, $\overline{HCS}$ low/high to HRDY low/high			6	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT high to HRDY high			9	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT high to $\overline{HINT}$ change			6	ns
$t_{d(COH-GPIO)}$	Delay time, CLKOUT high to HDx output change. HDx is configured as a general-purpose output			5	ns

† DMAC stands for direct memory access controller (DMAC). The HPI8 shares the internal DMA bus with the DMAC, thus HPI8 access times are affected by DMAC activity.

‡ The HRDY output is always high when the $\overline{HCS}$ input is high, regardless of DS timings.

§ This timing applies when writing a one to the DSPINT bit or $\overline{HINT}$ bit of the HPIC register. All other writes to the HPIC occur asynchronously, and do not cause HRDY to be deasserted.



† HAD refers to HCNTL0, HCNTL1, and HR/$\overline{W}$.
‡ When $\overline{HAS}$ is not used ($\overline{HAS}$ always high)

Figure 5−28. Using $\overline{HDS}$ to Control Accesses ($\overline{HCS}$ Always Low)

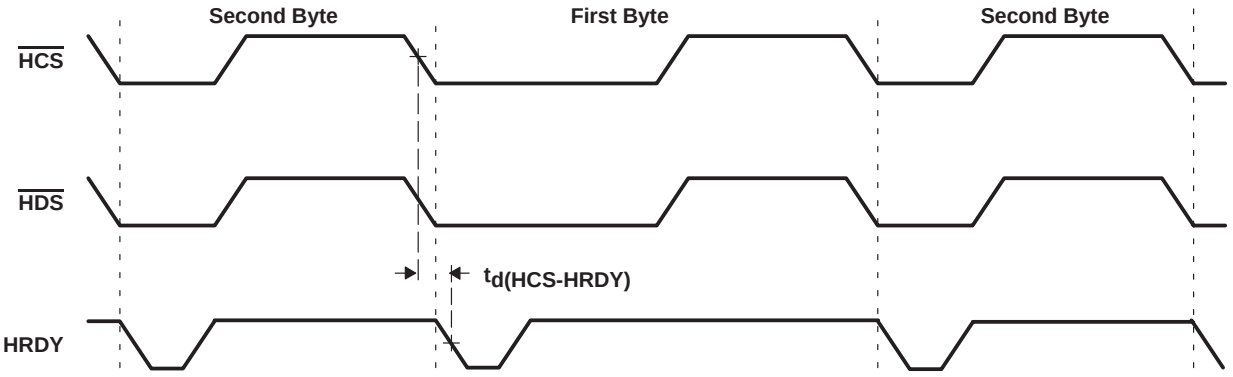


Figure 5−29. Using $\overline{\text{HCS}}$ to Control Accesses

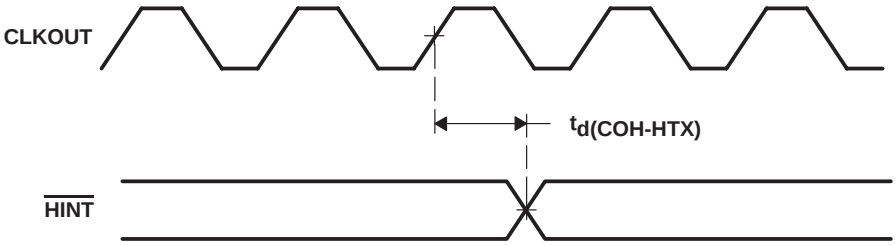
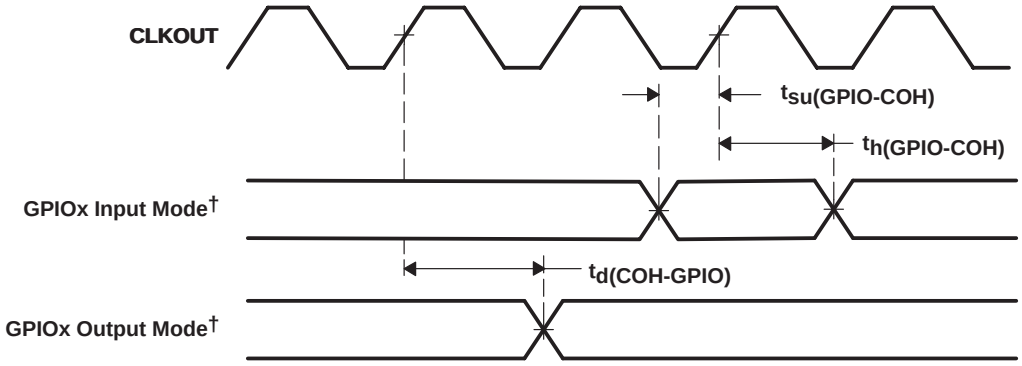


Figure 5−30. $\overline{\text{HINT}}$ Timing



† GPIOx refers to HD0, HD1, HD2, ...HD7, when the HD bus is configured for general-purpose input/output (I/O).

Figure 5−31. GPIOx† Timings

5.13.2 HPI16 Mode

Table 5−34 and Table 5−35 assume testing over recommended operating conditions and P = 0.5 * processor clock (see Figure 5−32 through Figure 5−34). In the following tables, DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$, and HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.). These timings are shown assuming that $\overline{HDS}$ is the signal controlling the transfer. See the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for addition information.

Table 5−34. HPI16 Mode Timing Requirements

				MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HR/$\overline{W}$ valid before DS falling edge			6		ns
$t_{h(DSL-HBV)}$	Hold time, HR/$\overline{W}$ valid after DS falling edge			5		ns
$t_{su(HAV-DSH)}$	Setup time, address valid before DS rising edge (write)			5		ns
$t_{su(HAV-DSL)}$	Setup time, address valid before DS falling edge (read)			−(4P − 6)		ns
$t_{h(DSH-HAV)}$	Hold time, address valid after DS rising edge			1		ns
$t_{w(DSL)}$	Pulse duration, DS low			30		ns
$t_{w(DSH)}$	Pulse duration, DS high			10		ns
$t_{c(DSH-DSH)}$	Cycle time, DS rising edge to next DS rising edge	Memory accesses with no DMA activity.	Reads	10P + 30		ns
			Writes	10P + 10		
		Memory accesses with 16-bit DMA activity.	Reads	16P + 30		
			Writes	16P + 10		
		Memory accesses with 32-bit DMA activity.	Reads	24P + 30		
			Writes	24P + 10		
$t_{su(HDV-DSH)W}$	Setup time, HD valid before DS rising edge			8		ns
$t_{h(DSH-HDV)W}$	Hold time, HD valid after DS rising edge, write			2		ns

Table 5−35. HPI16 Mode Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(DSL-HDD)}$	Delay time, DS low to HD driven		0	10	ns
$t_{d(DSL-HDV1)}$	Delay time, DS low to HD valid for first word of an HPI read	Case 1a: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_{W(DSH)}$ was < 18H		32P +20 − $t_{W(DSH)}$	ns
		Case 1b: Memory accesses not immediately following a write when DMAC is active in 16-bit mode		16P + 20	
		Case 1c: Memory accesses initiated immediately following a write when DMAC is active in 32-bit mode and $t_{W(DSH)}$ was < 26H		48P +20 − $t_{W(DSH)}$	
		Case 1d: Memory access not immediately following a write when DMAC is active in 32-bit mode		24P + 20	
		Case 2a: Memory accesses initiated immediately following a write when DMAC is inactive and $t_{W(DSH)}$ was < 10H		20P +20 − $t_{W(DSH)}$	
		Case 2b: Memory accesses not immediately following a write when DMAC is inactive		10P + 20	
$t_{d(DSH-HYH)}$	Delay time, DS high to HRDY high	Memory writes when no DMA is active		10P + 5	ns
		Memory writes with one or more 16-bit DMA channels active		16P + 5	
		Memory writes with one or more 32-bit DMA channels active		24P + 5	
$t_{v(HYH-HDV)}$	Valid time, HD valid after HRDY high			7	ns
$t_{h(DSH-HDV)R}$	Hold time, HD valid after DS rising edge, read		1	6	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT rising edge to HRDY high			5	ns
$t_{d(DSL-HYL)}$	Delay time, DS low to HRDY low			12	ns
$t_{d(DSH-HYL)}$	Delay time, DS high to HRDY low			12	ns

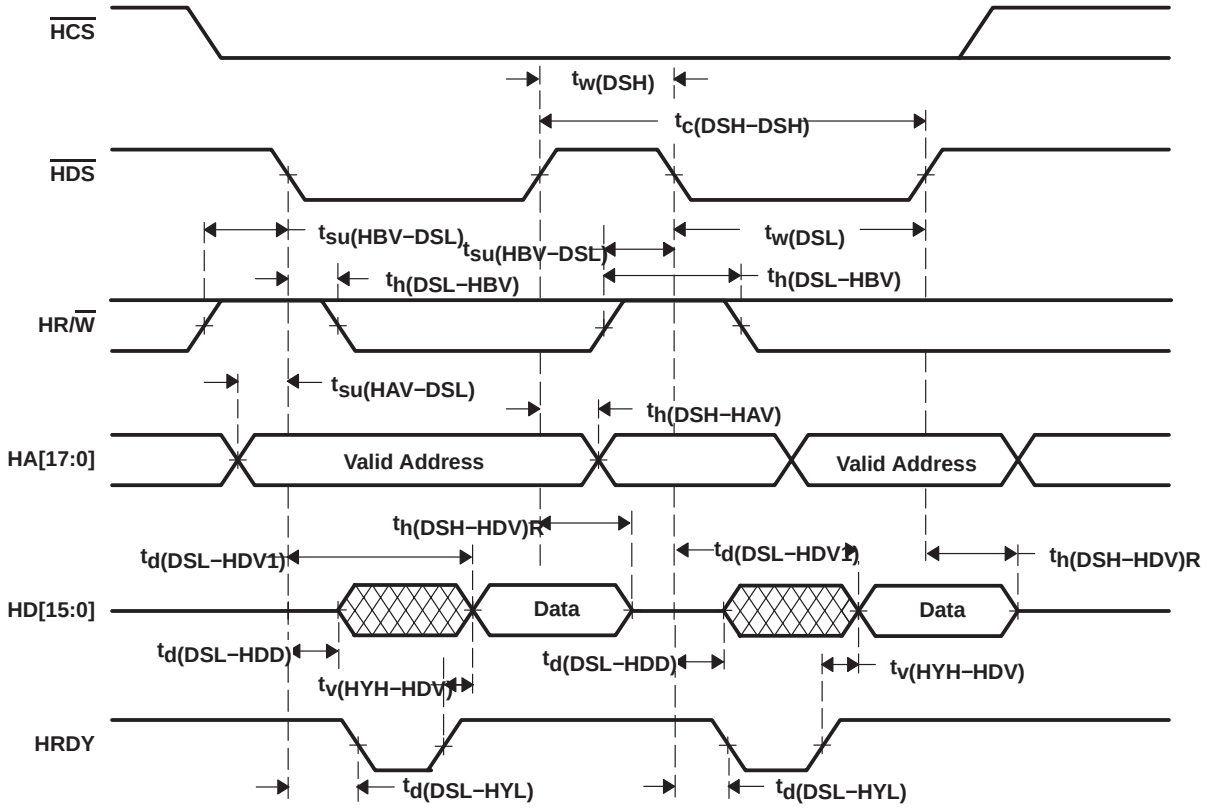


Figure 5−32. Nonmultiplexed Read Timings

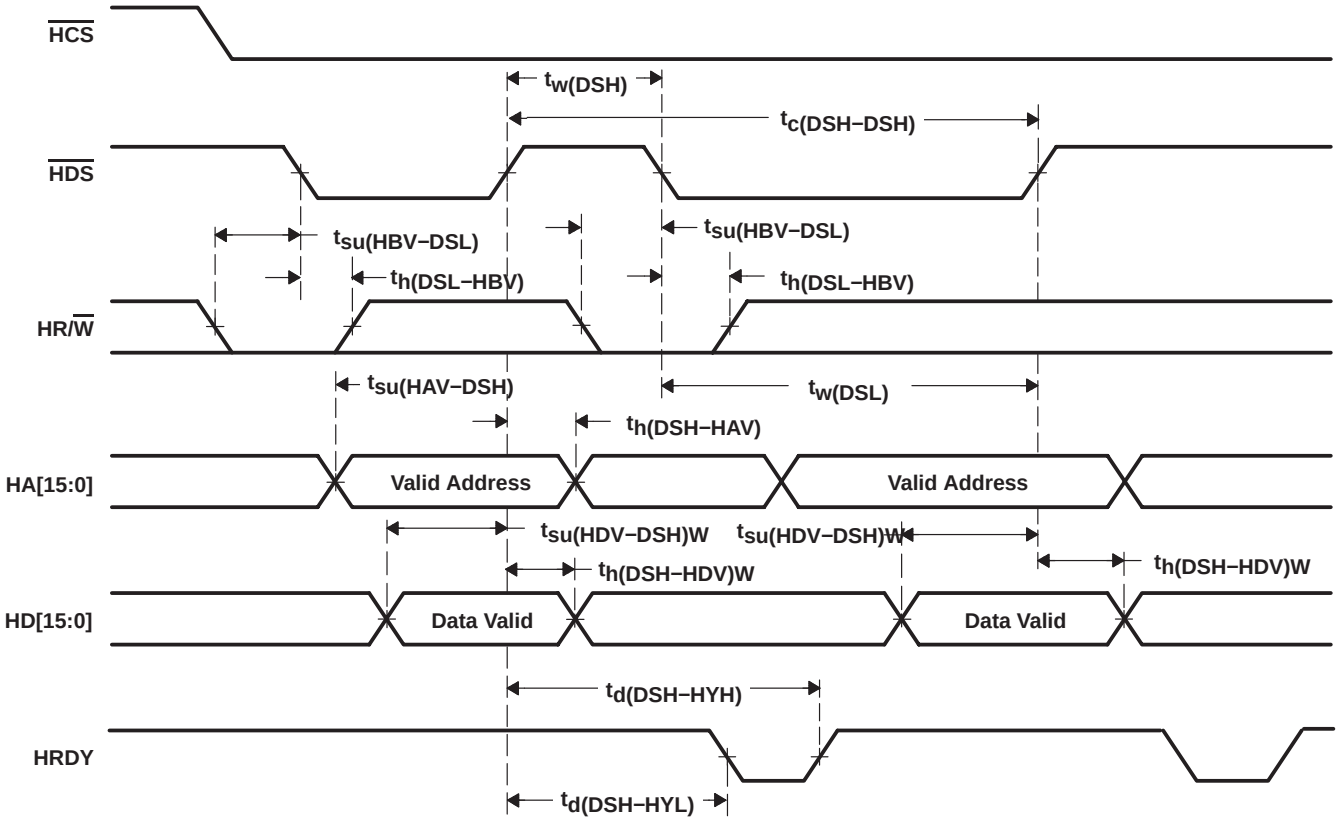


Figure 5−33. Nonmultiplexed Write Timings

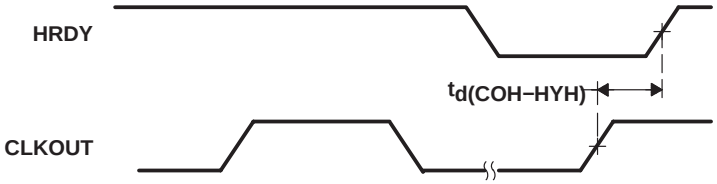


Figure 5−34. HRDY Relative to CLKOUT

5.14 UART Timing

Table 5−36 to Table 5−37 assume testing over recommended operating conditions (see Figure 5−35).

Table 5−36. UART Timing Requirements

		MIN	MAX	UNIT
$t_{w(UDB)R}$	Pulse width, receive data bit	0.99U†	1.01U†	ns
$t_{w(USB)R}$	Pulse width, receive start bit	0.99U†	1.01U†	ns

† U = UART baud time = 1/programmed baud rate

Table 5−37. UART Switching Characteristics

PARAMETER		MIN	MAX	UNIT
f_{baud}	Maximum programmable baud rate		5	MHz
$t_{w(UDB)X}$	Pulse width, transmit data bit	U − 2†	U + 2†	ns
$t_{w(USB)X}$	Pulse width, transmit start bit	U − 2†	U + 2†	ns

† U = UART baud time = 1/programmed baud rate

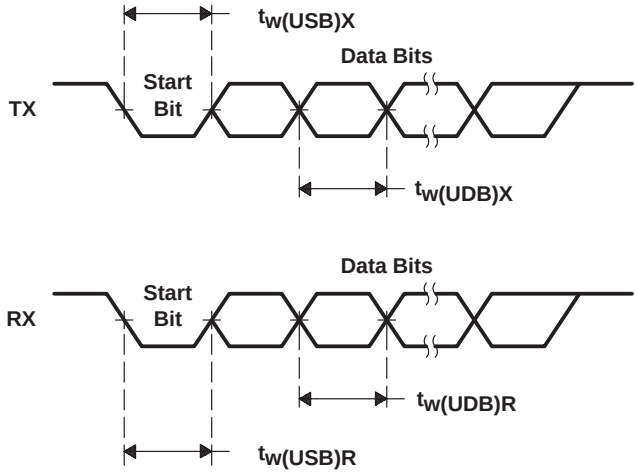


Figure 5−35. UART Timings

6 Mechanical Data

6.1 Si3016 Mechanical Data

Si3016 **16-PIN SMALL OUTLINE PLASTIC PACKAGE (SOIC)**

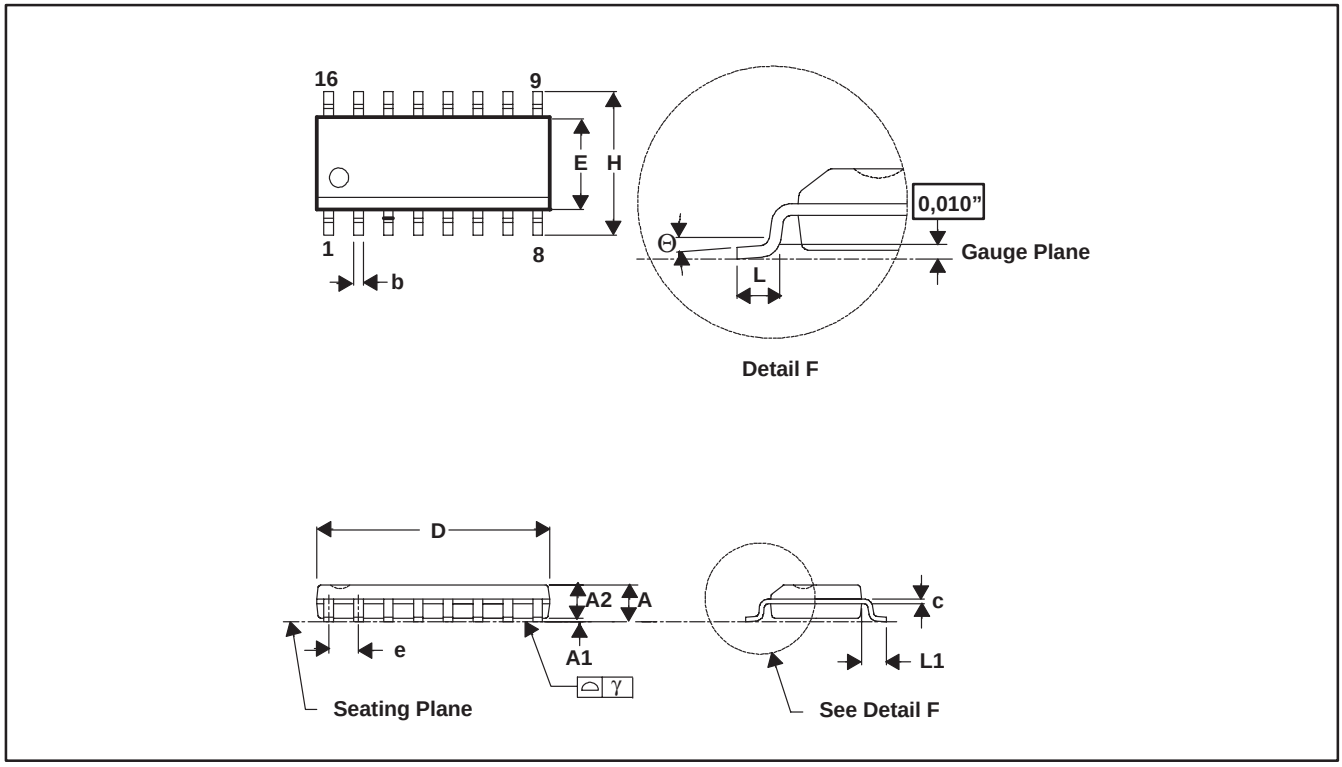


Figure 6−1. Si3016 16-Pin Small Outline Plastic Package (SOIC)

Table 6−1. Package Diagram Dimensions

CONTROLLING DIMENSION: MM				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.051	0.059	1.30	1.50
b	0.013	0.020	0.330	0.51
c	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC	—	1.27 BSC	—
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
L1	0.042 BSC	—	1.07 BSC	—
γ	—	0.004	—	0.10
θ	0°	8°	0°	8°

6.2 Package Thermal Resistance Characteristics

Table 6−2 provides the estimated thermal resistance characteristics for the recommended package types used on the TMS320C54CST DSP.

Table 6−2. Thermal Resistance Characteristics

PARAMETER	GGU PACKAGE	PGE PACKAGE	UNIT
$R_{\Theta JA}$	38	56	°C/W
$R_{\Theta JC}$	5	5	°C/W

6.3 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TMS320C54CSTGGU	NRND	BGA MICROSTAR	GGU	144	160	TBD	SNPB	Level-3-220C-168 HR	Samples Not Available
TMS320C54CSTPGE	NRND	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
TMS320C54CSTZGU	NRND	BGA MICROSTAR	ZGU	144	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Samples Not Available

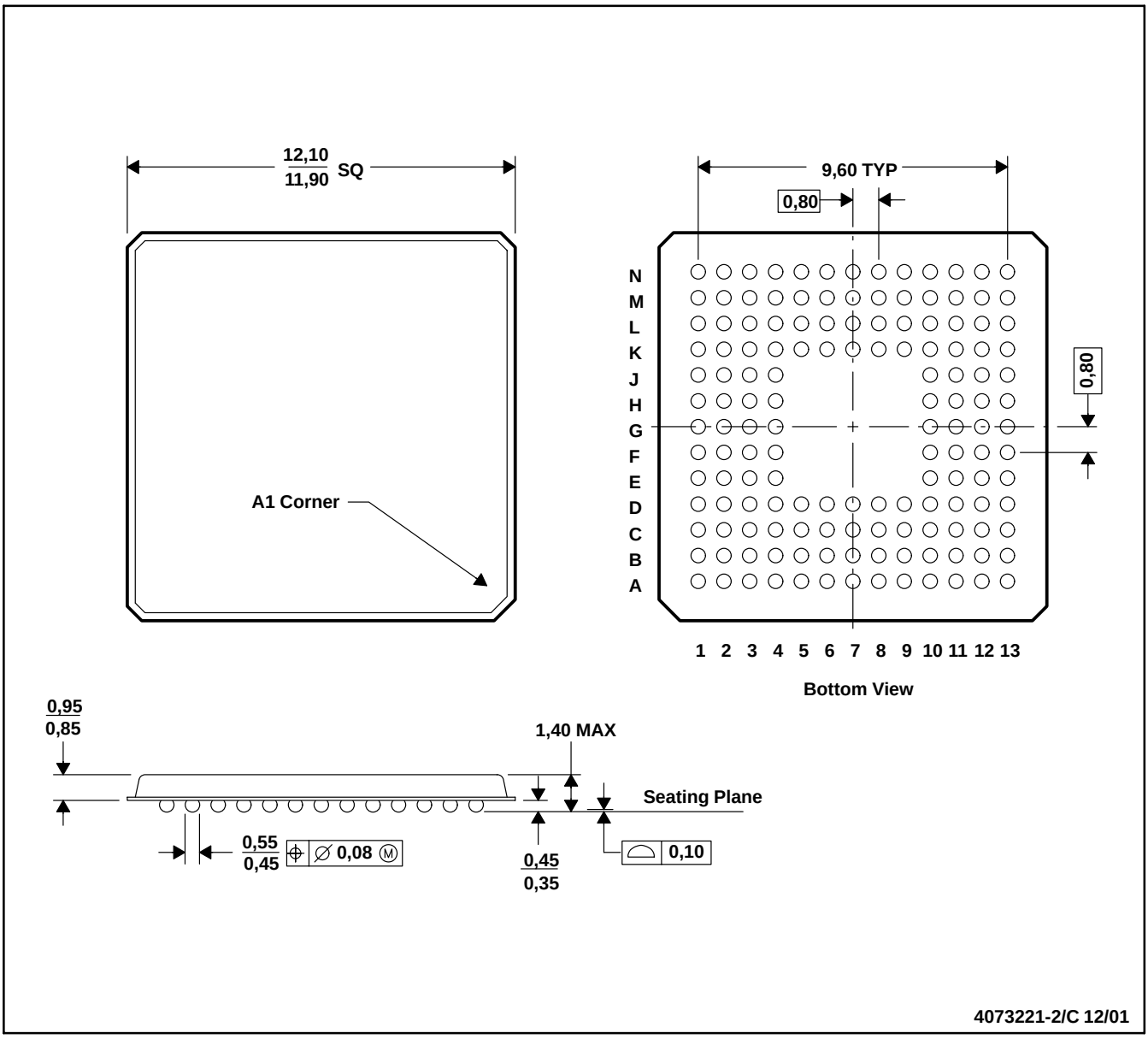
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MPBG021C – DECEMBER 1996 – REVISED MAY 2002

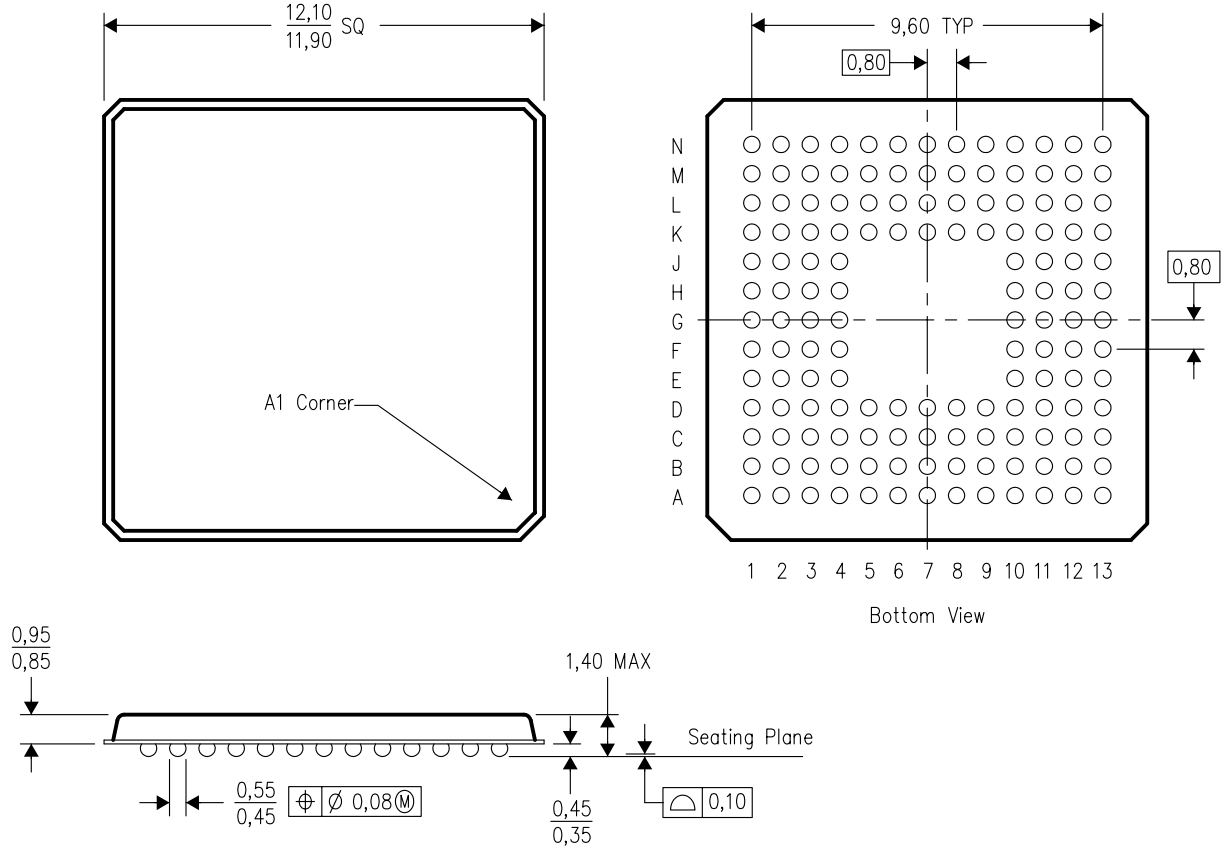
GGU (S–PBGA–N144) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments Incorporated.

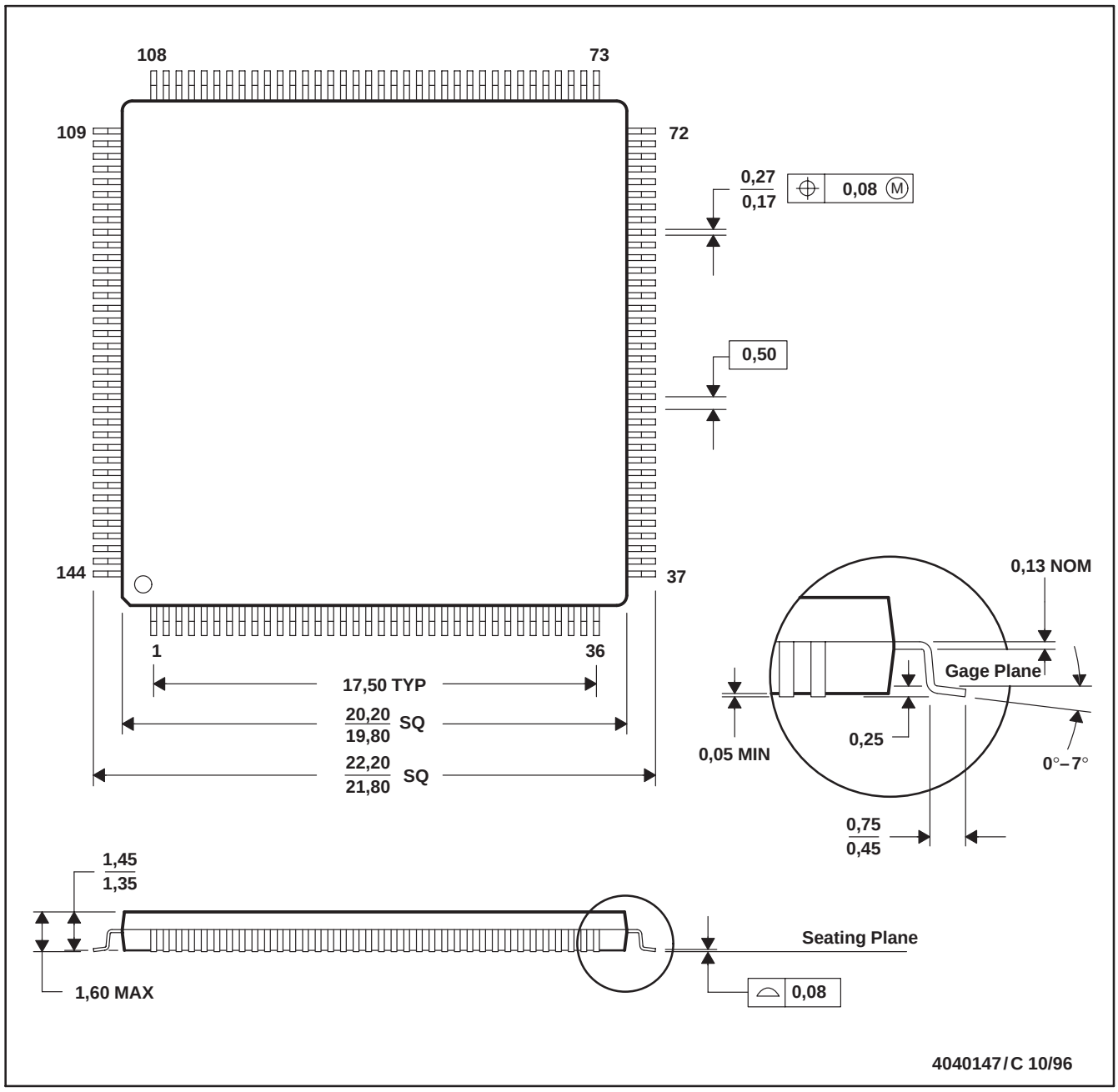
ZGU (S–PBGA–N144) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration
D. This is a lead–free solder ball design.

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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