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[^0]
## FSA9280A

# USB Port Multimedia Switch Featuring Automatic Select and Accessory Detection 

Features
$\left.\begin{array}{|l|r|}\hline \text { Signals } & \text { Audio, USB, UART, USB Charging } \\ \hline \begin{array}{l}\text { Switch } \\ \text { Mechanism }\end{array} & \begin{array}{r}\text { Automatic Switching with } \\ \text { Available Interrupt }\end{array} \\ \hline \begin{array}{l}\text { Accessory } \\ \text { Detection }\end{array} & \begin{array}{r}\text { Headsets (Headphone/MIC/Remote) } \\ \text { USB Data Port (SDP) } \\ \text { UART Serial Link }\end{array} \\ \hline \text { USB Chargers (Car-Kit, CDP, DCP) } \\ \text { Factory-Mode } \\ \text { TTY Converter }\end{array}\right\}$

## Description

The FSA9280A is a high-performance multimedia switch featuring automatic switching and accessory detection for the USB port. This switch allows sharing of a common USB port to pass audio, USB data / charging, as well as factory programmability. In addition, the FSA9280A integrates detection of accessories; such as headphones, headsets (MIC / button), car chargers, USB chargers, and UART data cables; with the ability to use a common USB connector. The FSA9280A can be programmed for manual or automatic switching of data paths based on accessory detected. FSA9280A includes an integrated 28 V over-voltage and 1.5A over-current protected FET.

## Applications

- Mobile Phones \& Portable Media Players


## Related Resources

- FSA9280A Evaluation Board
- Evaluation Board Users Guide
- For samples, questions or board requests; please contact analogswitch@fairchildsemi.com


Figure 1. Typical Application

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## Block Diagram



Figure 2. Block Diagram

## Pin Configuration



Figure 3. Pin Assignments (Top View)

Pin Descriptions

| Name | Pin \# | Type | Default State | Description |
| :---: | :---: | :---: | :---: | :---: |
| USB Interface |  |  |  |  |
| DP_HOST | 4 | Signal Path | Open | D+ signal switch path, dedicated USB port to be connected to the resident USB transceiver on the phone |
| DM_HOST | 5 | Signal Path | Open | D- signal switch path, dedicated USB port to be connected to the resident USB transceiver on the phone |
| Audio Interface |  |  |  |  |
| Audio_L | 2 | Signal Path | Open | Left audio channel from mobile phone audio-out CODEC |
| Audio_R | 1 | Signal Path | Open | Right audio channel from mobile phone audio-out CODEC |
| MIC | 3 | Signal Path | Open | Connected to the mobile phone audio CODEC MIC input pin |
| UART Interface |  |  |  |  |
| TxD | 7 | Signal Path | Open | Transmitter (Tx) from resident UART on the mobile phone |
| RxD | 6 | Signal Path | Open | Receiver (Rx) from resident UART on the mobile phone |

## Connector Interface

| ID_CON | 20 | Signal Path | Open | Connected to the USB connector ID pin and used for detecting accessories or button presses |
| :---: | :---: | :---: | :---: | :---: |
| DP_CON | 19 | Signal Path | Open | Connected to the USB connector D+ pin; depending on the signaling mode, this pin can be switched to DP_HOST, Audio_R, or RxD pins |
| DM_CON | 18 | Signal Path | Open | Connected to the USB connector D - pin; depending on the signaling mode, this pin can switched to DM_HOST, Audio_L, or TxD pins |
| $V_{\text {bus_In }}$ | 17 | Power Path | N/A | Input voltage supply pin to be connected to the $\mathrm{V}_{\text {BUS }}$ pin of the USB connector |
| Power Interface |  |  |  |  |
| $V_{\text {bat }}$ | 11 | Power | N/A | Input voltage supply pin to be connected to the mobile phone battery output or to an internal regulator on the phone |
| $\mathrm{V}_{\text {DIIO }}$ | 9 | Power | N/A | Baseband processor interface I/O supply pin |
| GND | Exposed Center Pad | Ground | N/A | Ground (center ground pad of package makes electrical contact) |

Charger Interface

| VBUS_OUT | 15 | Power Path | N/A | Output voltage supply pin to be connected to the source voltage pin on <br> the charger IC |
| :---: | :---: | :---: | :---: | :---: |
| CHG_DET | 16 | Open-Drain <br> Output | $\mathrm{Hi}-\mathrm{Z}$ | Open-drain active LOW output, used to signal the charger IC that a <br> charger has been attached |

## Factory Interface

| JIG | $\mathbf{1 0}$ | Open-Drain <br> Output | Hi-Z | Output control signal driven by the FSA9280A and used by the processor <br> for factory test modes |
| :---: | :---: | :---: | :---: | :---: |
| BOOT | $\mathbf{8}$ | CMOS <br> Output | LOW | Output control signal driven by the FSA9280A and used by the processor <br> for factory test modes |
| $\mathbf{I}^{2}$ C Interface |  |  |  |  |
| I2C_SCL | $\mathbf{1 4}$ | Input | $\mathrm{Hi}-\mathrm{Z}$ | $\mathrm{I}^{2} \mathrm{C}$ serial clock signal to be connected to the phone-based I ${ }^{2} \mathrm{C}$ master |
| I2C_SDA | $\mathbf{1 3}$ | Open-Drain <br> I/O | $\mathrm{Hi}-\mathrm{Z}$ | I $^{2} \mathrm{C}$ serial data signal to be connected to the phone-based $\mathrm{I}^{2} \mathrm{C}$ master |
| INTB | $\mathbf{1 2}$ | CMOS <br> Output | LOW | Interrupt active LOW output used to prompt the phone baseband <br> processor to read the I ${ }^{2} \mathrm{C}$ register bits, indicates a change in ID_CON pin <br> status or accessory attach status |

## 1. Functionality

The FSA9280A offers a complete solution for a single 5-pin USB interface. Through built-in detection algorithms that monitor the ID and $V_{\text {Bus }}$ pins of the USB interface, the FSA9280A allows seamless sharing of the interface between HS USB, FS USB or UART, and audio sources. The FSA9280A also offers a complete solution for multiple types of USB chargers. The FSA9280A detects different USB charger types and has a dedicated charger IC interface to allow charging through the devices and dynamic current control by the charger IC based on the type of charger detected. Additional over-current protection (OCP) and up to 28 V over-voltage tolerance (OVT) is provided.

The detection features are capable of monitoring the ID pin of the USB interface to detect a full array of USB accessories, including audio accessories with up to 12 buttons.

### 1.1. Functional Overview

The FSA9280A is designed for minimal software requirements for proper operation. The flow diagram below shows the basic steps of operation and contains references to more detailed information.


## 2. Power-up \& Reset

The FSA9280A does not need special power sequencing for correct operation. The main power of the device is provided by either $\mathrm{V}_{\text {bus_in }}$ or $\mathrm{V}_{\text {bat }}$. If $\mathrm{V}_{\text {bus_in }}$ is not present and $\mathrm{V}_{\text {bat }}$ is applied, $\mathrm{V}_{\mathrm{BAT}}$ is used to power the device. $\mathrm{V}_{\mathrm{DDIO}}$ is only used for $I^{2} \mathrm{C}$ interface and interrupt processing.

Table 1 summarizes the enabled features of each power state of the FSA9280A. The valid voltages levels for each power supply can be found in Section 9.2.

Table 1 - Power States Summary

| Valid <br> $V_{\text {Bus in }}$ | $\begin{aligned} & \text { Valid } \\ & V_{\text {BAT }} \end{aligned}$ | $\begin{aligned} & \text { Valid } \\ & \text { V }_{\text {DDIO }}{ }^{(1)} \end{aligned}$ | Power State | Enabled Functionality |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Charging through FET | Processor Communication ( ${ }^{2} \mathrm{C}$ \& Interrupts) | Detection |
| NO | NO | NO | Power Down | NO | NO | NO |
| NO | NO | YES ${ }^{(2)}$ |  | ILLEGAL STATE |  |  |
| NO | YES | NO | Powered from $\mathrm{V}_{\text {BAT }}$ | NO | NO | YES |
| NO | YES | YES | Powered from $\mathrm{V}_{\text {BAT }}$ | NO | YES | YES |
| YES | NO | NO | Powered from $\mathrm{V}_{\text {BUS_IN }}$ | Yes | NO | YES |
| YES | YES | NO | Powered from $\mathrm{V}_{\text {BAT }}$ | YES | NO | YES |
| YES | NO | YES ${ }^{(2)}$ | Powered from $\mathrm{V}_{\text {Bus_ı }}$ | YES | YES | YES |
| YES | YES | YES | Powered from $\mathrm{V}_{\text {BAT }}$ | YES | YES | YES |

## Notes:

1. $V_{\text {DDIO }}$ is expected to be the same supply used by the baseband I/O's.
2. This is not a typical state: both $\mathrm{V}_{\mathrm{BAT}}$ and $\mathrm{V}_{\mathrm{DDIO}}$ are typically provided simultaneously.

### 2.1. Reset

When the device is reset, all the registers are initialized to the default values shown in Table 7 and all switch paths are open. After reset or power up, the FSA9280A enters Standby Mode and is ready to detect accessories sensed on its $V_{\text {Bus_In }}$ and / or ID_CON pins.

### 2.1.1. Hardware Reset

There are three hardware reset mechanisms:

- Power-on reset caused by the initial rising edge of $\mathrm{V}_{\text {BUS }}$ or $V_{\text {bat }}$
- The falling edge of $\mathrm{V}_{\text {DDII }}$.
- With V signals LOW for at least 30 ms .


## Note:

3. $I^{2} \mathrm{C}$ controllers that implement clock stretching could cause reset. In this case, GPIOs could be used for the $I^{2} \mathrm{C}$ interface.

### 2.1.2. Software Reset

The device can be reset through software by writing to the Reset bit in the Register (1BH).

## 3. $I^{2} \mathrm{C}$

The FSA9280A integrates a fast-mode $I^{2} \mathrm{C}$ slave controller compliant with the $I^{2} \mathrm{C}$ specification version 2.1 requirements. The FSA9280A $I^{2} \mathrm{C}$ interface runs up to 400 KHz .

The slave address is shown in Table 2. Status information and configuration occurs via the $\mathrm{I}^{2} \mathrm{C}$ interface.

Please see Section 9.7 for more information.

Table $2-I^{2} C$ Slave Address

| Name | Size (Bits) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Slave Address | 8 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | Read / Write |



Note: Single Byte write is initiated by Master with P immediately following first data byte.

Figure 4. $\quad I^{2} C$ Write Sequence


Figure 5. $\quad I^{2} C$ Read Sequence


## 4. Configuration

FSA9280A requires minimal configuration for proper detection and reporting. The following steps can be followed for full configuration. In many cases, only Step 5 needs to be implemented for proper operation.

1. Write Control register (02h) to configure different switching configurations and wait timing.
2. Write Interrupt Mask 1 and 2 registers ( $05 \mathrm{~h}, 06 \mathrm{~h}$ ) to mask any interrupts not required in the application.

## 5. Detection

The FSA9280A detection algorithms monitor both the $\mathrm{V}_{\text {Bus }}$ and ID pins of the USB interface. Based on the detection results, multiple registers are updated and the INTB pin is asserted to indicate to the baseband processor that an accessory was detected and to read the registers for the complete information.
3. Write Timing Set $1(08 \mathrm{~h})$ register to program required key-press timing and ADC-detection timing.
4. Write Timing Set 2 (09h) register to program required Switching Wait timing and Long Key Press timing.
5. Write Control register (02h) to clear INT Mask bit. This enables interrupts to the baseband.

The detection algorithm allows the application to control the timing of the detection algorithm and the configuration of the internal switches. The flow diagram in Figure 7 shows the operation of the detection algorithm.

The FSA9280A monitors both $\mathrm{V}_{\text {BUs_IN }}$ and ID_CON to detect accessories. The ID_CON detection is a "resistive detection" that detects the resistance to GND on the ID_CON pin to
determine which accessory is attached. Table 3 shows the assignment of accessories based on resistor values.

Table 3. ID_CON Accessory Detection

| Binary Value ${ }^{(4)}$ | ID_CON Resistance to GND |  |  | Accessory Detected ${ }^{(5)}$ |
| :---: | :---: | :---: | :---: | :---: |
|  | Min. | Typ. | Max. |  |
| 00000 | GND | GND | GND | DO NOT USE |
| 00001 | $1.9 \mathrm{k} \Omega$ | $2.0 \mathrm{k} \Omega$ | $2.1 \mathrm{k} \Omega$ | Audio Send/End Button |
| 00010 | $2.470 \mathrm{k} \Omega$ | $2.604 \mathrm{k} \Omega$ | $2.730 \mathrm{k} \Omega$ | Audio Remote S1 Button ${ }^{(6)}$ |
| 00011 | $3.050 \mathrm{k} \Omega$ | $3.208 \mathrm{k} \Omega$ | 3.370 k ת | Audio Remote S2 Button ${ }^{(6)}$ |
| 00100 | $3.810 \mathrm{k} \Omega$ | $4.014 \mathrm{k} \Omega$ | $4.210 \mathrm{k} \Omega$ | Audio Remote S3 Button ${ }^{(6)}$ |
| 00101 | $4.58 \mathrm{k} \Omega$ | $4.82 \mathrm{k} \Omega$ | $5.06 \mathrm{k} \Omega$ | Audio Remote S4 Button ${ }^{(6)}$ |
| 00110 | $5.73 \mathrm{k} \Omega$ | $6.03 \mathrm{k} \Omega$ | $6.33 \mathrm{k} \Omega$ | Audio Remote S5 Button ${ }^{(6)}$ |
| 00111 | $7.63 \mathrm{k} \Omega$ | $8.03 \mathrm{k} \Omega$ | $8.43 \mathrm{k} \Omega$ | Audio Remote S6 Button ${ }^{(6)}$ |
| 01000 | $9.53 \mathrm{k} \Omega$ | $10.03 \mathrm{k} \Omega$ | $10.53 \mathrm{k} \Omega$ | Audio Remote S7 Button ${ }^{(6)}$ |
| 01001 | $11.43 \mathrm{k} \Omega$ | $12.03 \mathrm{k} \Omega$ | $12.63 \mathrm{k} \Omega$ | Audio Remote S8 Button ${ }^{(6)}$ |
| 01010 | $13.74 \mathrm{k} \Omega$ | $14.46 \mathrm{k} \Omega$ | $15.18 \mathrm{k} \Omega$ | Audio Remote S9 Button ${ }^{(6)}$ |
| 01011 | $16.40 \mathrm{k} \Omega$ | $17.26 \mathrm{k} \Omega$ | $18.12 \mathrm{k} \Omega$ | Audio Remote S10 Button ${ }^{(6)}$ |
| 01100 | $19.48 \mathrm{k} \Omega$ | $20.50 \mathrm{k} \Omega$ | $21.53 \mathrm{k} \Omega$ | Audio Remote S11 Button ${ }^{(6)}$ |
| 01101 | $22.87 \mathrm{k} \Omega$ | $24.07 \mathrm{k} \Omega$ | $25.27 \mathrm{k} \Omega$ | Audio Remote S12 Button ${ }^{(6)}$ |
| 01110 | $27.27 \mathrm{k} \Omega$ | $28.70 \mathrm{k} \Omega$ | $30.14 \mathrm{k} \Omega$ | Reserved Accessory \#1 |
| 01111 | $32.3 \mathrm{k} \Omega$ | $34.0 \mathrm{k} \Omega$ | $35.7 \mathrm{k} \Omega$ | Reserved Accessory \#2 |
| 10000 | $38.19 \mathrm{k} \Omega$ | $40.20 \mathrm{k} \Omega$ | $42.21 \mathrm{k} \Omega$ | Reserved Accessory \#3 |
| 10001 | $47.41 \mathrm{k} \Omega$ | $49.90 \mathrm{k} \Omega$ | $52.40 \mathrm{k} \Omega$ | Reserved Accessory \#4 |
| 10010 | $61.66 \mathrm{k} \Omega$ | $64.90 \mathrm{k} \Omega$ | $68.15 \mathrm{k} \Omega$ | Reserved Accessory \#5 |
| 10011 | $76.1 \mathrm{k} \Omega$ | $80.7 \mathrm{k} \Omega$ | $84.1 \mathrm{k} \Omega$ | DO NOT USE |
| 10100 | $96.9 \mathrm{k} \Omega$ | $102.0 \mathrm{k} \Omega$ | $107.1 \mathrm{k} \Omega$ | DO NOT USE |
| 10101 | $115 \mathrm{k} \Omega$ | $121 \mathrm{k} \Omega$ | $127 \mathrm{k} \Omega$ | TTY Converter |
| 10110 | $143 \mathrm{k} \Omega$ | $150 \mathrm{k} \Omega$ | $157 \mathrm{k} \Omega$ | UART Cable |
| 10111 | $190 \mathrm{k} \Omega$ | $200 \mathrm{k} \Omega$ | $206 \mathrm{k} \Omega$ | USB: See Table 4 |
| 11000 | $247.3 \mathrm{k} \Omega$ | $255 \mathrm{k} \Omega$ | $262.7 \mathrm{k} \Omega$ | Factory Mode Boot OFF-USB |
| 11001 | $292 \mathrm{k} \Omega$ | $301 \mathrm{k} \Omega$ | $310 \mathrm{k} \Omega$ | Factory Mode Boot ON-USB |
| 11010 | $347 \mathrm{k} \Omega$ | $365 \mathrm{k} \Omega$ | $383 \mathrm{k} \Omega$ | Audio Cradle |
| 11011 | $428.7 \mathrm{k} \Omega$ | $442.0 \mathrm{k} \Omega$ | $455.3 \mathrm{k} \Omega$ | USB: See Table 4 |
| 11100 | $507.3 \mathrm{k} \Omega$ | $523 \mathrm{k} \Omega$ | $538.7 \mathrm{k} \Omega$ | Factory Mode Boot OFF-UART |
| 11101 | $600.4 \mathrm{k} \Omega$ | $619 \mathrm{k} \Omega$ | $637.6 \mathrm{k} \Omega$ | Factory Mode Boot ON-UART |
| 11110 | $750 \mathrm{k} \Omega$ | $1000 \mathrm{k} \Omega$ | $1050 \mathrm{k} \Omega$ | Audio Type 1 with Remote ${ }^{(8)}$ |
|  | $750 \mathrm{k} \Omega$ | $1002 \mathrm{k} \Omega$ | $1050 \mathrm{k} \Omega$ | Audio Type 1 / Only Send-End ${ }^{(8)}$ |
| 11111 | $20 \mathrm{M} \Omega^{(7)}$ | Open ${ }^{(7)}$ |  | USB Mode, Dedicated Charger or Accessory Detach |

## Notes:

4. The binary values are reported in the binary register ( 07 h ) with each valid accessory detection.
5. The accessory type is reported in the Device Type 1 (0Bh), Device Type 2 (0Bh), Button 1 (0Ch), and Button 2 (0Dh) registers with each valid accessory detection.
6. These resistor values are created by multiple standard resistor values in series to form the button presses on the wired remote (see Figure 12).
7. For the ID float, ID "open" is recommended; otherwise, capacitance should be minimized.
8. Audio devices with remote and audio devices with only send/end are both reported as Audio Type 1 in the Device Type 1 register (see the Audio Accessory Detection section below). Type 1 is for passive resistor audio accessories and a future Audio Type 2 is designated for active audio accessories.


Figure 8. ID-Based Accessories, No $\mathrm{V}_{\text {bus_ı }}$ Attach Timing with Default Switching Wait Bits of 10 ms

### 5.1. USB Port Detection

The multiple types of USB 2.0 ports that the FSA9280A can detect are summarized in Table 4. These devices are unique in that $\mathrm{V}_{\text {BUS }}$ must be present to detect these accessories.

Table 4. ID_CON and $V_{\text {Bus_in }}$ Detection for USB Devices

| $\begin{gathered} \text { ADC } \\ \text { Value }^{(9)} \end{gathered}$ | $\mathrm{V}_{\text {Bus_In }}$ | DP_CON | DP_CON | ID_CON Resistance to GND |  |  | Accessory Detected ${ }^{(10)}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| 10111 | 5 V | X | X | 190k $\Omega$ | 200k $\Omega$ | 206k $\Omega$ | Car Kit Type 1 Charger ${ }^{(11)}$ |
| 11011 | 5 V | X | X | $428.7 \mathrm{k} \Omega$ | $442 \mathrm{k} \Omega$ | $455.3 \mathrm{k} \Omega$ | Car Kit Type 2 Charger ${ }^{(11)}$ |
| 11111 | 5V | (12) | (12) | $20 \mathrm{M} \Omega$ | Open | Open | USB Dedicated Charging Port, Travel Adapter or Dedicated Charger (DCP) |
| 11111 | 5 V | (12) | (12) | $20 \mathrm{M} \Omega$ | Open | Open | USB Charging Downstream Port (CDP) |
| 11111 | 5 V | (12) | (12) | $20 \mathrm{M} \Omega$ | Open | Open | USB Standard Downstream Port (SDP) |

## Notes:

9. The ADC values are reported in the ADC register ( 07 h ) with an each valid accessory detection.
10. The accessory type is reported in the Device Type 1 ( 0 Bh ) and Car Kit Status (0Eh) registers with an each valid accessory detection.
11. Follows the ANSI/CEA-936-A USB Car Kit specification.
12. The FSA9280A follow the Battery Charging 1.1 specification, which uses DP_CON and DM_CON to determine what USB accessory is attached (refer to the specification for details).

The following figures show the attach timing of the USB accessories and the relationship between the INTB assertion and the CHG_DET assertion. FSA9280A implements the optional data contact detection (DCD) feature of the USB Battery Charging specification. The DCD detection ensures


Figure 9. USB Dedicated Charging Port (DCP) or Charging Downstream Port (CDP) Attach Timing


Figure 10. USB Standard Downstream Port Attach Timing


Figure 11. Car Kit Type 1 and 2 Attach Timing

### 5.2. Audio Accessory Detection

Audio accessories are detected when the ID_CON pin resistance to GND is approximately $1 \mathrm{M} \Omega$. Configurations for this audio accessory shown in Figure 12 and Figure 13.


Figure 12. Audio Accessory with Just Send/End Button (1\% or 5\% Resistors)


Figure 13. Audio Accessory with Full Wired Remote Control (1\% Resistors)

The FSA9280A can detect and differentiate between regular key presses, long key presses, and a stuck key. The definition of the key press timing is user configurable by
writing the Timing Set 1 (08h) and Timing Set 2 (09h) registers. Timing diagrams for the key press detection are shown below in Figure 14 and Figure 15.


Figure 15. Long Key-Press Timing Diagram

### 5.3. OCP and OVP Detection

With $\mathrm{V}_{\text {BUS_IN }}$ greater than $6.8 \mathrm{~V}, \mathrm{~V}_{\text {BUS_IN }}$ is disconnected, protecting the FSA9280A and all application circuitry from excess voltage. This block is capable of withstanding continuous 28 V in Shutdown Mode. Upon entering Shutdown Mode, the OVP_EN bit in the Interrupt 1 register is set HIGH and an interrupt is sent to the baseband. The Over-Current Protection (OCP) feature limits current through the charger FET to $\leq 1.5 \mathrm{~A}$. The FSA9280A automatically senses an over-current event, shuts down $V_{\text {busout, and }}$ reports this to the baseband by asserting OCP_EN in the Interrupt 1 register. OCP Mode is only implemented when $\mathrm{V}_{\text {BUS_IN }}$ is provided by the attached accessory. Removal of an OVP or OCP condition triggers another interrupt sent to the processor clearing the OCP_EN and/or the OVP_EN bits and setting the OCP_OVP_DIS bit in the Interrupt 1 register.

## 6. Processor Communication

Typical communication steps between the processor and the FSA9280A during accessory detection are:

1. INTB asserted LOW, indicating change in accessory detection.
a) CHG_DET asserted LOW if USB charger detected.
2. Processor reads Interrupt registers to determine which event occurred.
a) Interrupt 1 (03h): Indicates if an attach, detach, key press, long key press, long key release, OVP / OCP event, or OVP / OCP event recovery was detected. Each bit can be masked by setting the corresponding bit in the Interrupt Mask 1 (05h) register.
b) Interrupt 2 (04h): Indicates if a reserved accessory, ADC change, stuck key, or stuck key recovery was detected. Each bit can be masked by setting the corresponding bit in the Interrupt Mask 2 (06h) register.
3. Processor reads Status registers to determine exact accessory detected.
a) Device Type 1 (0Ah): Indicates which USB, Car Kit UART, or audio accessory was detected.
b) Device Type 2 (0Bh): Indicates which factory mode was detected or if a TTY cable was detected.
c) Button 1 (0Ch \& ODh): Indicates which button press was detected with Audio Type 1 accessories.
d) Car Kit Status (0Eh): Indicates which type of car kit charger was detected.

### 6.1. Interrupts

The baseband processor recognizes interrupt signals by observing the INTB signal, which is active LOW. Interrupts are masked upon reset or power up via the INT Mask register bit (bit 0 of Control register, address 02h in Table 7. Register Map) and INTB pin defaults LOW right after this reset or power up. After the INT Mask bit is cleared by the baseband processor, the INTB pin is driven HIGH in preparation for a future interrupt. When an interruptible event
occurs, INTB transitions LOW and returns HIGH when the processor reads the Interrupt register at address 03h. Subsequent to the initial power up or reset; if the processor writes a " 1 " to INT Mask bit when the system is already powered up, the INTB pin stays HIGH and ignores all interrupts until the INT Mask bit is cleared. If an event happens that would ordinarily cause an interrupt when the INT Mask bit is set, the INTB pin is LOW for $\mathrm{t}_{\text {INT_mAsk }}$ after the INT Mask bit is cleared.


Figure 16. Power-up Interrupt Timing Diagram


Figure 17. $V_{\text {DDIO }}$ Reset Interrupt Timing Diagram


Figure 18. INT Mask to INTB Interrupt Timing Diagram

## 7. Switch Configuration

FSA9280A devices have two modes of operation when configuring the internal switches. The FSA9280A can autoconfigure the switches or the switches can be configured manually by the processor. Typical applications can use the Auto-Configuration Mode and do not require interaction with the baseband to configure the switches correctly.

Table 5. Auto-Configurations


Note:
13. Use of FS USB on the UART path requires manual switching, as described in Section 11.4 - Systems with Multiple USB Controllers.

### 7.1. Manual Switching

Manual switching is enabled by writing the following registers:

- Manual Switch 1 (13h): Configures the switches for DM_CON, DP_CON, and VBUs_IN.
- Manual Switch 2 (14h): Configures the CHG_DET, BOOT, and JIG pins.


## 8. Active Signal Performance

### 8.1. USB Data



Figure 19. Pass Through Eye Compliance Testing Input Signal


Figure 20. USB 2.0 Eye Compliance Test Results at Output

### 8.2. FS USB



Figure 21. FS USB Eye Compliance for UART Path

### 8.3. Audio



Figure 22. THD+N Plot for Audio Channels

## 9. Electrical Specifications

### 9.1. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter |  |  | Min. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {BAT }} / \mathrm{V}_{\text {DDIO }}$ | Supply Voltage from Battery / Baseband |  |  | -0.5 | 6.0 | V |
| $\mathrm{V}_{\text {BUS_IN }}$ | Supply Voltage from Micro-USB Connector |  |  | -0.5 | 28.0 | V |
| $\mathrm{V}_{\text {Sw }}$ | Switch I/O Voltage | USB |  | -1.0 | $\mathrm{V}_{\text {BUS }}+0.5$ | V |
|  |  | Stereo / Mono Audio Path Active |  | -1.5 | $\mathrm{V}_{\mathrm{BAT}}+0.5$ |  |
|  |  | All Other Channels |  | -0.5 | $\mathrm{V}_{\text {BAT }}+0.5$ |  |
| $\mathrm{I}_{\text {K }}$ | Input Clamp Diode Current |  |  | -50 |  | mA |
| $\mathrm{I}_{\text {CHG }}$ | Charger Detect CHG_DET Pin Current Sink Capability |  |  |  | 30 | mA |
| Isw | Switch I/O Current (Continuous) | USB |  |  | 50 | mA |
|  |  | Audio |  |  | 60 |  |
|  |  | All Other Channels |  |  | 50 |  |
| $I_{\text {SWPEAK }}$ | Peak Switch Current (Pulsed at 1ms Duration, <10\% Duty Cycle) | USB |  |  | 150 | mA |
|  |  | Audio |  |  | 150 |  |
|  |  | Charger FET |  |  | 2 | A |
|  |  | All Other Channels |  |  | 150 | mA |
| $\mathrm{T}_{\text {STG }}$ | Storage Temperature Range |  |  | -65 | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{J}}$ | Maximum Junction Temperature |  |  |  | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{L}}$ | Lead Temperature (Soldering, 10 Seconds) |  |  |  | +260 | ${ }^{\circ} \mathrm{C}$ |
| ESD | IEC 61000-4-2 System ESD | USB Connector Pins (DP_CON, DM_CON, $\mathrm{V}_{\text {Bus_IN, }}$ ID_CON) to GND | Air Gap <br> Contact | 15.0 8.0 |  | kV |
|  | Human Body Model, JEDEC JESD22-A114 | JIG, BOOT, INTB |  | 3.5 |  |  |
|  |  | All Other Pins, Including DP_CON, DM_CON,ID_CON and VBUS_IN |  | 5.0 |  |  |
|  | Charged Device Model, JEDEC JESD22-C101 |  | All Pins | 2.0 |  |  |

### 9.2. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter |  | Min. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {BAT }}$ | Battery Supply Voltage ${ }^{(14)}$ |  | 3.0 | 4.4 | V |
| $V_{\text {BUSIN }}$ | Supply Voltage from V ${ }_{\text {BUS_IN }}$ Pin $^{(15)}$ |  | 4.0 | 5.5 | V |
| $\mathrm{V}_{\text {DDIO }}$ | Processor Supply Voltage |  | 1.8 | 3.6 | V |
| $\mathrm{V}_{\text {SW }}$ | Switch I/O Voltage | USB Path Active | 0 | 3.6 | V |
|  |  | Audio Path Active | -1.2 | 1.2 |  |
|  |  | All Other Pins | 0 | 5.0 |  |
| $1 \mathrm{D}_{\text {CAP }}$ | Capacitive Load on ID_CON Pin for Reliable Accessory Detection |  |  | 1.0 | nF |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature |  | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |

## Note:

14. Fairchild does not guarantee operation below 3.0 V .
15. Between 5.5 to OVP starting voltage, the charger FET is still closed so that charger IC can charge battery even with 5.9~6.0V travel adaptor.

### 9.3. Switch Path DC Electrical Characteristics

All typical values are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| Symbol | Parameter | $\mathrm{V}_{\mathrm{BAT}}(\mathrm{V})$ | Conditions | $\mathrm{T}_{\mathrm{A}}=-40$ to $+85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Host Interface Pins (JIG, BOOT, INTB, CHG-DET) |  |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage ${ }^{(16)}$ | 3.0 to 4.4 | $\mathrm{I}_{\text {он }}=2 \mathrm{~mA}$ | $\begin{aligned} & 0.7 x \\ & V_{\text {DDIO }} \end{aligned}$ |  |  | V |
| VoL | Output Low Voltage | 3.0 to 4.4 | $\mathrm{l}_{\mathrm{OL}}=10 \mathrm{~mA}$ |  |  | 0.4 | V |

Switch OFF Characteristics

| loff | Power-Off Leakage Current | 0 | All Data Ports Except MIC $\mathrm{V}_{\mathrm{sw}}=0 \mathrm{~V}$ to 4.4 V |  |  | 10 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{NO}}$ | Switch Open Leakage Current with Device Powered | 3.0 to 4.4 | $\mathrm{V}_{\mathrm{BAT}}=4.4 \mathrm{~V}$; I/O Pins=0.3V, 4.1 V , or Floating, Except MIC | -0.100 | 0.001 | 0.100 | $\mu \mathrm{A}$ |
| lidshrt | Short-Circuit Current ${ }^{(17)}$ | 3.0 to 4.4 | Current Limit if ID_CON=0V |  | 5 |  | mA |
| USB Switch ON Path |  |  |  |  |  |  |  |
| USB Analog Signal Range |  | 3.0 to 4.4 |  | 0 |  | 3.6 | V |
| Ronusb | USB Switch On Resistance ${ }^{(18)}$ | 3.0 to 4.4 | $\mathrm{V}_{\mathrm{D}+/ \mathrm{D}-}=0 \mathrm{~V}, 0.4 \mathrm{~V}, \mathrm{I}_{\mathrm{ON}=8 \mathrm{~mA}}$ |  | 8 | 10 | $\Omega$ |

Charging FET ON Path

| Vovp | Over-Voltage Protection (OVP) Threshold Voltage |  | 6.2 | 6.8 | 7.2 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ronfet | Charging FET On Resistance ${ }^{(17)}$ | $\mathrm{V}_{\text {BUS_IN }}=4.2 \mathrm{~V}-5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{ON}}=1 \mathrm{~A}$ |  | 200 |  | $\mathrm{m} \Omega$ |
| locp | Over-Current Protection (OCP) Threshold Current ${ }^{(17)}$ | $\mathrm{V}_{\text {BUS_IN }}=5.2 \mathrm{~V}$ | 1.1 | 1.3 | 1.5 | A |

Audio_R/Audio_L Switch ON Paths

| Audio Analog Signal Range | 3.0 to 4.4 |  | -1.2 |  | 3.0 | V |  |
| :---: | :---: | :---: | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {ON }}$ | Audio Switch On Resistance ${ }^{(18)}$ | 3.0 to 4.4 | $\mathrm{~V}_{\mathrm{LR}}=-0.8 \mathrm{~V}, 0.8 \mathrm{~V}, \mathrm{I}_{\mathrm{ON}}=30 \mathrm{~mA}$, |  |  | 3 | $\Omega$ |
| $\mathrm{R}_{\text {FLAT }}$ | Audio R R ${ }_{\text {ON }}$ Flatness ${ }^{(19)}$ | 3.0 to 4.4 | $\mathrm{f}=0-470 \mathrm{kHz}$ |  |  | 0.1 | $\Omega$ |

MIC and UART Switch ON Paths

| Analog Signal Range ${ }^{(20)}$ |  | 3.0 to 4.4 |  | 0 |  | 5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ron | MIC Path ON Resistance | 3.0 to 4.4 | $\mathrm{V}_{\mathrm{sw}}=0 \mathrm{~V}, 4.4 \mathrm{~V}, \mathrm{l}_{\mathrm{on}}=30 \mathrm{~mA}$ |  | 40 |  | $\Omega$ |
|  | UART Path ON Resistance ${ }^{(17)}$ |  |  |  | 25 | 30 |  |

## Total Current Consumption

| ICcSL | Battery Supply Standby Mode <br> Current (No Accessory Attached) | 3.0 to 4.4 | No Accessory Static Current <br> During Standby Mode | 10 | 25 | $\mu \mathrm{~A}$ |
| :---: | :--- | :---: | :--- | :---: | :---: | :---: |
| ICcsLwA | Battery Supply Standby Mode <br> Current with Accessory <br> Attached | 3.8 | With Accessory Static Current <br> During Standby Mode | 30 | 40 | $\mu \mathrm{~A}$ |

## Notes:

16. Does not apply to CHG_DET or JIG pins because they are open drain.
17. Limits based on electrical characterization data.
18. On resistance is the voltage drop between the two terminals at the indicated current through the switch.
19. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.
20. The MIC bias applied by the baseband should not exceed 2.8 V .
21. Applies to all accessories except Audio Type 1 and Factory-Mode accessories.

### 9.4. Capacitance

| Symbol | Parameter | $V_{B A T}$ <br> (V) | Condition | $\mathrm{T}_{\mathrm{A}}=-40$ to $+85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Conusb | DP_CON, DM_CON On Capacitance (USB Mode) | 3.8 | $\mathrm{V}_{\text {BIAS }}=0.2 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |  | 8 |  | pF |

### 9.5. Switch Path AC Electrical Characteristics

All typical values are for $\mathrm{V}_{\mathrm{BAT}}=3.8 \mathrm{~V}$ at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| Symbol | Parameter |  | Condition | $\mathrm{T}_{\mathrm{A}}=-40$ to $+85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min. | Typ. | Max. |  |
| Xtalk | Active Channel Crosstalk DP_CON to DM_CON | Audio Mode |  | $\mathrm{f}=20 \mathrm{kHz}, \mathrm{R}_{\mathrm{T}}=32 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ |  | -50 |  | dB |
|  |  | USB Mode | $\mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{T}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ |  | -60 |  |  |  |
|  |  |  | $\mathrm{f}=240 \mathrm{MHz}, \mathrm{R}_{\mathrm{T}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ |  | -40 |  |  |  |
| OIRR | Off Isolation | Audio Mode | $\mathrm{f}=20 \mathrm{kHz}, \mathrm{R}_{\mathrm{T}}=32 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ |  | -90 |  | dB |  |
|  |  | USB Mode | $\mathrm{f}=1 \mathrm{MHz}, \mathrm{R}_{\mathrm{T}}=50 \Omega, \mathrm{C}_{L}=0 \mathrm{pF}$ |  | -90 |  |  |  |
| PSRR | Power Supply Rejection Ratio, MIC on $\mathrm{V}_{\text {BUS_I }}$ |  | Power Supply Noise 300 mV vp, $\mathrm{f}=217 \mathrm{~Hz}$ |  | -100 |  | dB |  |
| THD | Total Harmonic Distortion (Audio Path) |  | 20 Hz to $20 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=32 / 16 \Omega$, Input Signal Range $2 \mathrm{~V}_{\mathrm{PP}}$ |  | 0.03 |  | \% |  |
|  |  |  | 20 Hz to $20 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=32 / 16 \Omega$, Input Signal Range -1.2 V to 1.2 V |  | 0.05 |  |  |  |
| tsk(P) | Skew of Opposite Transitions of the Same Output (USB Mode) |  | $\begin{aligned} & \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{t}}=750 \mathrm{ps}(10-90 \%) \text { at } 240 \mathrm{MHz}, \\ & \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=50 \Omega \end{aligned}$ |  | 30 |  | ps |  |
| $\mathrm{t}_{\text {I2CRST }}$ | Time When I2C_SDA and I2C_SCL Both LOW to Cause a Reset |  | See Figure 6 | 30 |  |  | ms |  |
| tintmask | Time after INT Mask Cleared to "0" until INTB Goes LOW to Signal the Interrupt after Interruptible Event while INT Mask Bit Set to "1" |  | See Figure 18 |  | 10 |  | ms |  |
| $t_{\text {sDPDET }}$ | Time from $\mathrm{V}_{\text {bus_in }}$ Valid to $\mathrm{V}_{\text {Bus_out }}$ Valid with Charger FET Closed and USB Switches Closed for USB Standard Downstream Port |  | See Figure 10 |  | 130 |  | ms |  |
| $\mathrm{t}_{\text {chgout }}$ | Time from $\mathrm{V}_{\text {Bus_In }}$ Valid to $\mathrm{V}_{\text {bus_out }}$ Valid with the Charger FET Closed for Both USB Charging Ports (CDP and DCP) |  | See Figure 9 |  | 170 |  | ms |  |
| $\mathrm{t}_{\text {carkit }}$ | Time from V ${ }_{\text {bus_ı }}$ Valid to Car Kit Type 1 or Type 2 Charger Detected |  | See Figure 11 |  | 200 |  | ms |  |
| $\mathrm{t}_{\text {chg }}$ | Time from $V_{\text {bus_out }}$ Valid to CHG_DET Output LOW for Both USB Charging Ports (CDP and DCP) and for Car Kit Chargers |  | See Figure 9, Figure 11 |  | 100 |  | ms |  |
| tidDet | Time from ID_CON Not F Signal Accessory Attache Resistance-Based Only ( | ting to INTB LOW to that is ID_CON us_ın Not Valid) | See Figure 8 |  | 200 |  | ms |  |
| $\mathrm{t}_{\text {Jigvbus }}$ | Time from $V_{\text {Bus_in }}$ Valid to JIG LOW and $V_{\text {Bus_out }}$ Valid with Charger FET Closed for Both Factory Mode Operation with $V_{\text {BUS_in }}$ Present |  | See Figure 25 |  | 200 |  | ms |  |
|  | Time from V ${ }_{\text {Bus_IN }}$ Valid to JIG LOW for Factory Mode Operation without $\mathrm{V}_{\text {BUs_in }}$ Present |  | See Figure 26 |  | 200 |  | ms |  |

## 9.6. $I^{2} \mathrm{C}$ Controller DC Characteristics

| Symbol | Parameter |  | Fast Mode (400kHz) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min. | Max. | Units |
| $\mathrm{V}_{\text {IL }}$ | Low-Level Input Voltage |  | -0.5 | $0.3 \mathrm{~V}_{\text {DDIO }}$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-Level Input Voltage |  | $0.7 \mathrm{~V}_{\text {DDIO }}$ |  | V |
| $\mathrm{V}_{\mathrm{HYS}}$ | Hysteresis of Schmitt Trigger Inputs | $\mathrm{V}_{\text {DDIO }}>2 \mathrm{~V}$ | $0.05 \mathrm{~V}_{\text {DdIO }}$ |  | V |
|  |  | $\mathrm{V}_{\text {DDIO }}<2 \mathrm{~V}$ | $0.1 \mathrm{~V}_{\text {DDIO }}$ |  |  |
| $\mathrm{V}_{\text {OL1 }}$ | Low-Level Output Voltage at 3mA Sink Current (Open-Drain) | $\mathrm{V}_{\text {DIIO }} \times 2 \mathrm{~V}$ | 0 | 0.4 | V |
|  |  | $\mathrm{V}_{\text {DIIO }}<2 \mathrm{~V}$ |  | $0.2 \mathrm{~V}_{\text {DDIO }}$ |  |
| 112 C | Input Current of I2C_SDA and I2C_SCL Pins, Input Voltage 0.26V to 2.34V |  | -10 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{Cl}_{1}$ | Capacitance for Each I/O Pin |  |  | 10 | pF |

## 9.7. $I^{2} \mathrm{C}$ AC Electrical Characteristics \& Register Map

| Symbol | Parameter | Fast Mode |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Max. | Unit |
| $\mathrm{f}_{\mathrm{SCL}}$ | SCL Clock Frequency | 0 | 400 | kHz |
| $\mathrm{t}_{\text {HD; STA }}$ | Hold Time (Repeated) START Condition | 0.6 |  | $\mu \mathrm{s}$ |
| tıow | LOW Period of SCL Clock | 1.3 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {HIGH }}$ | HIGH Period of SCL Clock | 0.6 |  | $\mu \mathrm{s}$ |
| tsu;STA | Set-up Time for Repeated START Condition | 0.6 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {HD; DAT }}$ | Data Hold Time | 0 | 0.9 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {Su;DAT }}$ | Data Set-up Time ${ }^{(22)}$ | 100 |  | ns |
| $\mathrm{tr}_{r}$ | Rise Time of SDA and SCL Signals ${ }^{(23)}$ | $20+0.1 \mathrm{C}_{\mathrm{b}}$ | 300 | ns |
| $t_{f}$ | Fall Time of SDA and SCL Signals ${ }^{(23)}$ | $20+0.1 \mathrm{C}_{\mathrm{b}}$ | 300 | ns |
| tsu;Sto | Set-up Time for STOP Condition | 0.6 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {BUF }}$ | BUS-Free Time between STOP and START Conditions | 1.3 |  | $\mu \mathrm{s}$ |
| tsp | Pulse Width of Spikes that Must Be Suppressed by the Input Filter | 0 | 50 | ns |

## Notes:

22. A fast-mode $\mathrm{I}^{2} \mathrm{C}$-Bus $®$ device can be used in a standard-mode $\mathrm{I}^{2} \mathrm{C}$-Bus system, but the requirement $\mathrm{t}_{\text {Su;DAT }} \geq \square 250 \mathrm{~ns}$ must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $\mathrm{t}_{r_{-} \max }+\mathrm{t}_{\text {SU;DAT }}=1000+250$ $=1250 \mathrm{~ns}$ (according to the standard-mode I ${ }^{2} \mathrm{C}$ bus specification) before the SCL line is released.
23. $\mathrm{C}_{\mathrm{b}}$ equals the total capacitance of one BUS line in pF . If mixed with high-speed devices, faster fall times are allowed according to the $I^{2} \mathrm{C}$ specification.


Figure 23. Definition of Timing for Full-Speed Mode Devices on the $I^{2} C$ Bus
Table 6. $1^{2} \mathrm{C}$ Slave Address

| Name | Size (Bits) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Slave Address | 8 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | R/W |

Table 7. Register Map

| Address | Register | Type | Reset Value | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 01H | Device ID | Read | 00000000 | Version ID: 0xb001 |  |  |  |  | Vendor ID (Fairchild): 000 |  |  |
| 02H | Control | Read / Write | 00011111 | Reserved: <br> - Read XXX <br> - Write 000 |  |  | Switch Open | ADC Interrupt Disable | Manual Switch | Configuration Delay | Global Interrupt Mask |
|  |  |  |  |  |  |  | 0: Open All switches | 0 : Report interrupt when detection is complete on ID_CON | 0 : Automatic configuration disabled, switch configuration based on Manual Switch registers (13H, 14H) | 0: After wait time expires delay configuration indefinitely until this bit is written to 1 by host | 0: Does not Mask Interrupts |
|  |  |  |  |  |  |  | 1: Switch based on detection | 1: ADC change interrupt is disabled | 1: Automatic configuration is enabled | 1: If wait time has expired configure the switches immediately (See figure 2(flow chart)) | 1: Mask interrupts |
| 03H | Interrupt 1 | Read/ Clear | 00000000 | OVP \& OCP Recovery | OCP Event | OVP Event | Long Key Release | Long Key Press | Key Press | Detach | Attach |
|  |  |  |  | 0: OVP and/or OCP event not recovered | 0: No OCP event | 0: No OVP event | 0: No Interrupt |  |  |  |  |
|  |  |  |  | 1: OVP and/or OCP event recovered | 1: OCP event | 1: OVP event | 1: Long key release detected | 1: Long key press detected | 1: Key press detected | 1: Accessory detached | 1: Accessory attached |
| 04H | Interrupt 2 | Read/ Clear | 00000000 | Reserved: <br> - Read XXX <br> - Write 000 |  |  | Stuck Key Recovery | Stuck Key | ADC Change | Reserved Attach | Reserved: <br> - Read X <br> - Write 0 |
|  |  |  |  |  |  |  | 0: No Interrupt |  |  |  |  |
|  |  |  |  |  |  |  | 1: Stuck key recovered | 1: Stuck key detected | 1: Valid ADC detection | 1: Reserved accessory attached |  |
| 05H | Interrupt Mask 1 | Read/ Write | 00000000 | OVP \& OCP | OCP | OVP | Long Key Release | Long Key Press | Key Press | Detach | Attach |
|  |  |  |  | 0: No Interrupt Mask |  |  |  |  |  |  |  |
|  |  |  |  | 1: Mask Interrupt 1 [OVP \& OCP Recovery] | 1: Mask Interrupt 1 [OCP Event] | 1: Mask Interrupt 1 [OVP Event] | 1: Mask Interrupt 1 [Long Key Release] | 1: Mask Interrupt 1 [Long Key Press] | 1: Mask Interrupt 1 [Key Press] | 1: Mask Interrupt 1 [Detach] | 1: Mask Interrupt 1 [Attach] |
| 06H | Interrupt Mask 2 | Read / Write | 00000000 | Reserved: <br> - Read XXX <br> - Write 000 |  |  | Stuck Key Recovery | Stuck Key | ADC Change | Reserved Attach | Reserved: <br> - Read X <br> - Write 0 |
|  |  |  |  |  |  |  | 0: No Interrupt Mask |  |  |  |  |
|  |  |  |  |  |  |  | 1: Mask Interrupt 2 [Stuck Key Recovery] | $\begin{gathered} \text { 1: Mask - } \\ \text { Interrupt 2 } 2 \text { Stuck } \\ \text { Key] } \\ \hline \end{gathered}$ | 1: Mask Interrupt 2 [ADC Change] | 1: Mask - Interrupt 2 [Reserved Attach] |  |
| 07H | ADC | Read | 00011111 | Reserved: - Read XXX, - Write 000 |  |  | ADC Value (See Table 8) |  |  |  |  |
| 08H | Timing Set 1 | Read / Write | 00000000 | Key Press Time (See Table 8) |  |  | ADC Detection Time (See Table 8) |  |  |  |  |
| 09H | Timing Set 2 | Read / Write | 00000000 | Switching Wait Time (See Table 8) |  |  | Long Key Press Time (See Table 8) |  |  |  |  |

Continued on the following page...

| Address | Register | Type | Reset Value | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OAH | Device Type 1 | Read | 00000000 | Reserved: <br> - Read X <br> - Write 0 | $\begin{array}{\|c\|} \hline \text { USB Charging } \\ \text { (DCP) } \end{array}$ | $\begin{aligned} & \text { USB Charging } \\ & \text { (CDP) } \\ & \hline \end{aligned}$ | Car Kit Charger | UART | USB Data (SDP) | Reserved: <br> - Read X <br> - Write 0 | $\begin{gathered} \text { Audio Type } \\ 1 \\ \hline \end{gathered}$ |
|  |  |  |  |  | 0: No detect |  |  |  |  |  | 0 : No detect |
|  |  |  |  |  | 1: USB dedicated charging port (DCP) detected | 1: USB charging downstream port (CDP) detected | 1: Car Kit charger detected | 1: UART detected | 1: USB standard downstream port (SDP) detected |  | 1: Audio Type 1 accessory detected |
| OBH | Device Type 2 | Read | 00000000 | Reserved: <br> - Read XX <br> - Write 00 |  | TTY | Reserved: <br> - Read X <br> - Write 0 | Factory Mode - See Table 9 |  |  |  |
|  |  |  |  |  |  | 0: No detect |  | 0: No detect |  |  |  |
|  |  |  |  |  |  | 1: TTY detected |  | 1: Jig: UART - <br> Boot_OFF | 1: Jig: UART Boot ON | 1: Jig: USB - Boot_OFF | $\begin{gathered} \text { 1: Jig: USB - } \\ \text { Boot_ON } \end{gathered}$ |
| OCH | Button 1 | Read | 00000000 | Button 7 | Button 6 | Button 5 | Button 4 | Button 3 | Button 2 | Button 1 | Send End |
|  |  |  |  | 0: Not Pressed |  |  |  |  |  |  |  |
|  |  |  |  | 1: Pressed |  |  |  |  |  |  |  |
| ODH | Button 2 | Read | 00000000 | Reserved: <br> - Read XX <br> - Write 00 |  | Key Press Error | Button 12 | Button 11 | Button 10 | Button 9 | Button 8 |
|  |  |  |  |  |  | $\begin{array}{\|c} \hline 0: \begin{array}{c} \text { No Key Press } \\ \text { Error } \end{array} \\ \hline \end{array}$ | 0: Not Pressed |  |  |  |  |
|  |  |  |  |  |  | 1: Key Press Error detected (too short) | 1: Pressed |  |  |  |  |
|  |  |  |  | Reserved: <br> - Read XXXXXX <br> - Write 000000 |  |  |  |  |  | Charger Type |  |
| OEH | Car Kit Status | Read | 00000000 |  |  |  |  |  |  | 00: No connection <br> 01: Reserved Charger <br> 10: Car Kit charger type 1 <br> 11: Car Kit charger type 2 |  |
| OFH | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 10H | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 11H | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 12H | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
|  |  |  |  | DM_CON Connection |  |  | DP_CON Connection |  |  | $\mathrm{V}_{\text {bus }}$ Connection |  |
| 13H | Manual Switch 1 | Read / Write | 00000000 | 000: Open DM_CON switch <br> 001: DM_CON connected to DM_HOST of USB port <br> 010: DM_CON connected to Audio_L <br> 011: DM_CON connected to TxD of UART port |  |  | 000: Open DP_CON switch <br> 001: DP_CON connected to DP_HOST of USB port <br> 010: DP_CON connected to Audio_R <br> 011: DP_CON connected to RxD of UART port |  |  | 00: Open VBUS switch <br> 01: VBUS_OUT connected to VBUS_IN (Host - current sourced from the phone to accessory, max. load current is 5 mA ) 10: VBUS_IN connected to MIC <br> 11: VBUS_IN connected to VBUS_OUT (Standard USB - phone sinks current from attached accessory) |  |
| 14H | Manual Switch 2 | Read / Write | 00000000 | Reserved: <br> - Read XXX <br> - Write 000 |  |  | CHG_DET | BOOT | JIG | Reserved: <br> - Read XXX <br> - Write 000 |  |
|  |  |  |  |  |  |  | 0 : High Impedance | 0: Low | 0 : High Impedance |  |  |
|  |  |  |  |  |  |  | 1: Low | 1: High | 1: Low |  |  |

Continued on the following page..

| Address | Register | Type | Reset Value | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 15H | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 16H | Reserved | N/A | XXXXXXX0 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 17H | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 18H | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 19H | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 1AH | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 1BH | Reset | R/W | X0001000 | Reserved: <br> - Read XXXXXXX, <br> - Write 0000100 |  |  |  |  |  |  | Reset <br> 0: No <br> Reset <br> 1: Reset <br> (Always <br> reads 0) |
| 1CH | Reserved | N/A | XXXXX001 | Reserved: - Read XXXXXXXX, - Write 00000001 |  |  |  |  |  |  |  |
| 1DH | Reserved | N/A | 00000000 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  | VBus_ın VALID $0:$ V $_{\text {Bus_ın }}$ Not Valid $1: V_{\text {Bus_ın }}$ Valid | Reserved: <br> - Read X, Write 0 |
| 1EH | Reserved | N/A | $\underset{X}{\mid X X X X X X}$ | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 1FH | Reserved | N/A |  | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |
| 20 H | DCD <br> Configuration | Read/Write | XXXXXX00 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  | Enable DCD <br> Timeout <br> 0: DCD Timeout <br> Not Enabled <br> 1: DCD Timeout <br> Enabled | Reserved: Read XX, - Write 00 |  |
| 21H | Reserved | N/A | XXXXXX00 | Reserved: - Read XXXXXXXX, - Write 00000000 |  |  |  |  |  |  |  |

Table 8 - Timing for Timing Set 1 \& 2 Registers

| Setting Value ${ }^{(24)}$ | ADC Detection Time | Key Press Time | Long Key Press Time | Switching Wait Time |
| :---: | :---: | :---: | :---: | :---: |
| 0000 | 50 ms | 100 ms | 300 ms | 10 ms |
| 0001 | 100 ms | 200 ms | 400 ms | 30 ms |
| 0010 | 150 ms | 300 ms | 500 ms | 50 ms |
| 0011 | 200 ms | 400 ms | 600 ms | 70 ms |
| 0100 | 300 ms | 500 ms | 700 ms | 90 ms |
| 0101 | 400 ms | 600 ms | 800 ms | 110 ms |
| 0110 | 500 ms | 700 ms | 900 ms | 130 ms |
| 0111 | 600 ms | 800 ms | 1000 ms | 150 ms |
| 1000 | 700 ms | 900 ms | 1100 ms | 170 ms |
| 1001 | 800 ms | 1000 ms | 1200 ms | 190 ms |
| 1010 | 900 ms |  | 1300 ms | 210 ms |
| 1011 | 1000 ms |  | 1400 ms |  |
| 1100 |  |  | 1500 ms |  |
| $1101-1111$ |  |  |  |  |

## Note:

24. Each of the four registers can have unique register setting values.

### 9.8. Factory Modes

The FSA9280A has four dedicated Factory Modes that allow efficient factory testing of a platform. Factory Modes are initiated with the attachment of special test hardware, called a "JIG box" used for factory testing. FSA9280A automatically configures switch paths to any factory-mode accessories when $\mathrm{V}_{\text {DDIO }}$ is present, without detaching and attaching the micro-USB cable. Since the processor may not be awake when a factory-mode accessory is detected, $I^{2} C$ read acknowledge is not required, nor does the FSA9280A employ a switching wait timer found in the Timing Set 2 register for the initial switch configuration. A change of resistor on the ID_CON pin dynamically switches between factory modes and auto-configures the appropriate switch paths without detaching and attaching the cable.

JIG output signals when a factory-mode accessory is plugged in and BOOT output signals the baseband processor to boot up, allowing tests to be conducted with and without the baseband processor powered up. As soon as the factory-mode cable is removed, the FSA9280A returns to a standard accessory flow that requires a device detach between accessory type configurations changes (except Audio Type 1 accessory described in the Audio Accessory Detection section above). The typical key sensing for Audio Type 1 accessories for wired remote is not active for factory-mode test.

### 9.8.1. Factory-Mode Accessory Detection

The different factory-mode accessories with the associated resistor values ( $1 \%$ standard resistors) on the ID_CON pin, the JIG and BOOT logic states, and switch configurations are listed in Table 9.

## Notes:

25. The charger FET closes for factory-mode BOOT ON-UART or factory-mode BOOT OFF-UART if VBUS_IN is valid only during the time when the cable is first plugged in or a new ID_CON resistor is detected.
26. Audio-type device configuration is entered as part of the factory-mode flow shown in Figure 24 where the ID_CON pin is not monitored for key presses and JIG remains LOW until the factory jig box is detached from the phone. MIC is not connected in this audio type case. Figure 24 provides the attach flow diagram for the JIG box accessory. If any of the factory modes is first entered and JIG=LOW; then and only then, can the ID_CON resistor ( $1 \mathrm{M} \Omega$ ) dynamically switch to Audio Type 1 accessory without a cable detach. For the latter case, factory-mode Audio Type 1 accessory autoconfigures the switches such that: Audio_L = DM_CON.
27. MIC is left unconnected.
28. The typical key sensing for Audio Type 1 accessories for wired remote is not active for this factory-mode test.


Figure 24. Factory Mode Flow


Figure 25. FACTORY Box Attach Timing (VBus_in Valid)


Figure 26. FACTORY Box Attach Timing without $\mathrm{V}_{\text {BUs_IN }}$
10. Reference Schematic


Figure 27. Reference Schematic

## 11. Layout Guidelines

### 11.1. PCB Layout Guidelines for High-Speed USB Signal Integrity

1. Place FSA9280A as close to the USB controller as possible. Shorter traces mean less loss, less chance of picking up stray noise, and may radiate less EMI.
a) Keep the distance between the USB controller and the device less than one inch (<1in).
b) For best results, this distance should be $<18 \mathrm{~mm}$. This keeps it less than one quarter ( $1 / 4$ ) of the transmission electrical length.
2. Use an impedance calculator to ensure $90 \Omega$ differential impedance for DP_COM/DM_CON lines.
3. Select the best transmission line for the application.
a) For example, for a densely populated board, select an edge-coupled differential stripline.
4. Minimize the use of vias and keep HS USB lines on same plane in the stack.
a) Vias are an interruption in the impedance of the transmission line and should be avoided.
b) Try to avoid routing schemes that generally force the use of at least two vias: one on each end to get the signal to and from the surface.
5. Cross lines, only if necessary, orthogonally to avoid noise coupling (traces running in parallel couple).
6. If possible, separate HS USB lines with GND to improve isolation
a) Routing GND, power, or components close to the transmission lines can create impedance discontinuities.
7. Match transmission line pairs as much as possible to improve skew performance.
8. Avoid sharp bends in PCB traces; a chamfer or rounding is generally preferred.
9. Place decoupling for power pins as close to the device as possible.
a) Use low-ESR capacitors for decoupling if possible.
b) A tuned PI filter should be used to negate the effects of switching power supplies and other noise sources if needed.

### 11.2. Layout for GSM/TDMA Buzz Reduction

There are two possible mechanisms for TDMA/GSM noise to negatively impact the FSA9280A device's performance. The first is the result of large current draw by the phone transmitter during active signaling when the transmitter is at full or almost full power. With the phone transmitter dumping large amounts of current in the phone GND plane; it is possible for there to be temporary voltage excursions in the GND plane if not properly designed. This noise can be coupled back up through the GND plane into the FSA9280A device and, although the FSA9280A has very good isolation; if the GND noise amplitude is large enough, it can result in noise coupling to the $\mathrm{V}_{\text {Bus_in/mic }}$ pin. The second path for GSM noise is through electromagnetic coupling onto the signal lines themselves.
In most cases, the noise introduced as a result of this noise is on the $\mathrm{V}_{\text {BAT }}$ and/or GND supply rails. Following are recommendations for PCB board design that help address these two sources of TDMA/GSM noise.

1. Provide a wide, low-impedance GND return path to both the FSA9280A and to the power amplifier that sources the phone transmit block.
2. Provide separate GND connections to PCB GND plane for each device. Do not share GND return paths between devices.
3. Add as large a decoupling capacitor as possible ( $\geq 1 \mu \mathrm{~F}$ ) between the $\mathrm{V}_{\text {bat }}$ pin and GND to shunt any power supply noise away from the FSA9280A. Also add decoupling capacitance at the PA (see the reference application schematic in Figure 27 for recommended decoupling capacitor values).
4. Add $33 p F$ shunt capacitors on any PCB nodes with the potential to collect radiated energy from the phone transmitter. At a minimum, add these 33 pF capacitors to the MIC pin (see Figure 27).
5. Add a series $R_{\text {BAT }}$ resistor prior to the decoupling capacitor on the $\mathrm{V}_{\text {BAT }}$ pin to attenuate noise prior to reaching the FSA9280A.

## 11.3. $\mathrm{V}_{\text {Bus_out }}$ Load Timing Requirements

The FSA9280A includes over-current protection (OCP) used to protect the FSA9280A and any downstream devices from a high-current event. In addition, the FSA9280A has an inrush-limiting feature that helps protect against high-current transient currents during initial charger FET closure. For these two reasons, it is recommended that the system designer delay current draw >250mA from the FSA9280A $V_{\text {bus_out }}$ pin until at least 10 ms after $\mathrm{V}_{\text {bus_out }}$ is valid. Failure to observe this timing requirement could result in false OCP triggering and, in some cases, could result in the FSA9280A staying in OCP Mode until the load is removed and re-attached.

### 11.4.Systems with Multiple USB Controllers

Many phone platforms have separate full-speed and highspeed controllers; however, the FSA9280A only has one designated USB switch path. The FSA9280A high-speed USB path is only designed to allow one HS USB controller to be multiplexed on to the USB connector. To allow for multiple USB controllers on the USB port, it may be tempting to use one of Fairchild's existing USB switches to multiplex the HS and FS controllers onto the shared HS USB switch path of the FSA9280A, as illustrated in Figure 28. It is NOT recommended that the USB signals be multiplexed at the input the FSA9280A DP_Host or DM_Host pins for the following reasons:

- The FSA9280A employs a passive USB switch path. It does not buffer, amplify, or enhance the USB signal in any way. The FSA9280A is designed to have minimal impact on the HS USB eye performance; however, there is some limited reduction in signal amplitude and edge rate resulting from the inherent resistance and capacitance of the USB switch within the FSA9280A.
- Standard USB switches like the FSUSB42 are also passive and cannot improve a USB signal. They result in a slight degradation of the HS USB signal as well.
- When placed in series, as shown in Figure 28, the cumulative effect of the two series passive USB switches impacts the HS eye performance and could result in failure of the HS eye mask test per the USB 2.0 specification.
- When factoring in the additional routing required for the two switches in series and the additional signal path discontinuities introduced, the likelihood of eye degradation is increased.


Figure 28. NOT RECOMMENDED - Multiplexing High-Speed and Full-Speed USB onto the DP_Host, DM_Host
For the reasons outlined above, it is recommend that only the HS USB controller be connected to the FSA9280A DP_Host and DM_Host pins. The following solutions are recommended for those applications that require both a HS and FS USB controller. The FSA9280A must be used for all of these solutions since it has the available UART switch path. The HS USB signal is highly sensitive and should only be routed through the specially designed HS USB signal path of the FSA9280A. Conversely, the FS USB signal operates at much slower data rates, which makes it much more resilient to signal path discontinuities. FS USB only
operates at 12 Mbps and has a full 3.6 V swing, which makes it much less sensitive to capacitive loading. Compared to HS USB, FS USB has a large voltage swing, which makes it less sensitive to switch on resistance. Therefore, the FS USB signal can be alternately routed through the UART signal path. Figure 29 provides an alternative application diagram.


Figure 29. RECOMMENDED Configuration for Systems with High-Speed, Full-Speed, and UART

In every case where the FS USB path is not routed through the dedicated USB path of the FSA9280A, the phone designers must place the FSA9280A into manual mode to configure the switch path properly. On initial attachment of a USB accessory, the FSA9280A detects and auto-configures for USB, resulting in the DP_Con and DM_Con pins being connected to the DP_Host and DM_Host pins, respectively. In this configuration, the HS USB controller is automatically connected and no further action is needed by the baseband to send and receive data from the HS controller. For the application shown in Figure 29, the FSA9280A must be changed to manual mode to enable FS USB through the UART TxD and RxD switch paths. After initial USB detection and attach signaled by the FSA9280A, do the following:

1. Write the hex value ' 1 A ' to the Control register ( 02 h ) (see Table 7. Register Map). This enables Manual Switch Mode and the FSA9280A automatically opens all switch paths, breaking the HS USB signal path and forcing the USB host to re-enumerate when the FS device is configured.
2. To configure the FSA9280A switch paths such that the FS device is connected through the UART switch path, write the hex value ' 6 Ch ' into the Manual Switch register (13h) $>125 \mu \mathrm{~s}$ later to ensure enumeration. This connects the RxD and TxD to DP_CON and DM_CON, respectively.
3. When FS USB data communication is complete, disable manual switch mode by writing '1E' back in to the Control register (02h).
4. Configure the FSUSB42 input select back to the UART source to allow UART communication.

## Physical Dimensions



Figure 30. 20-Lead Ultrathin Molded Leadless Package (UMLP), $3 \times 4 \times 0.55 \mathrm{~mm}, 0.5 \mathrm{~mm}$ Pitch

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| Part Number | Operating Temperature Range | Top Mark | Package |
| :---: | :---: | :---: | :---: |
| FSA9280AUMX | -40 to $+85^{\circ} \mathrm{C}$ | 9280 A | $20-$ Lead Ultrathin Molded Leadless <br> Package (UMLP), $3 \times 4 \times 0.55 \mathrm{~mm}, 0.5$ Pitch |

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