SPI Interface, 1 Ω R_{ON}, ±5 V, 12 V, 5 V, 3.3 V, Mux Configurable, Quad SPST Switch

Data Sheet **ADGS1612**

FEATURES

- SPI interface with error detection
  - Includes CRC, invalid read/write address, and SCLK count error detection
  - Supports burst mode and daisy-chain mode
  - Industry-standard SPI Mode 0 and SPI Mode 3 interface compatible
- Guaranteed break-before-make switching allowing external wiring of switches to deliver multiplexer configurations
- 1 Ω typical on resistance at 25°C
- 0.23 Ω typical on resistance flatness at 25°C
- V_{SS} to V_{DD} analog signal range
  - Fully specified at ±5 V, 12 V, 5 V, and 3.3 V
  - ±3.3 V to ±8 V dual-supply operation
  - 3.3 V to 16 V single-supply operation
- 1.8 V logic compatibility with 2.7 V ≤ V_L ≤ 3.3 V
- 4 mm × 4 mm, 24-lead LFCSP package

APPLICATIONS

- Communication systems
- Medical systems
- Audio and video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

FUNCTIONAL BLOCK DIAGRAM

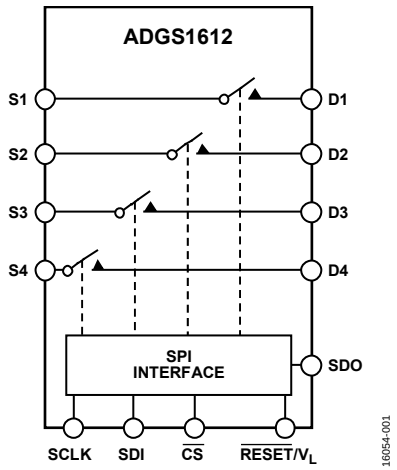

Figure 1.

GENERAL DESCRIPTION

The ADGS1612 contains four independent single-pole/single-throw (SPST) switches. A serial peripheral interface (SPI) controls the switches. The SPI interface has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read/write address detection, and serial clock (SCLK) count error detection.

It is possible to daisy-chain multiple ADGS1612 devices together. Daisy-chaining enables the configuration of multiple devices with a minimal amount of digital lines. The ADGS1612 can also operate in burst mode to decrease the time between SPI commands.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The ultralow on resistance (R_{ON}) of these switches make them ideal solutions for data acquisition and gain switching applications where low R_{ON} and low distortion are critical. The R_{ON} profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. The ADGS1612 exhibits break-before-make switching action for use in multiplexer applications. Note that throughout this data sheet, the multifunction pin, $\overline{\text{RESET}}/V_L$, is referred to either by the entire pin name or by a single function of the pin, for example, V_L, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. The SPI interface removes the need for parallel conversion and logic traces and reduces general-purpose input/output (GPIO) channel count.
2. Daisy-chain mode removes additional logic traces when multiple devices are used.
3. CRC, invalid read/write address, and SCLK count error detection ensure a robust digital interface.
4. CRC error detection capabilities allow the use of the ADGS1612 in safety critical systems.
5. Guaranteed break-before-make switching allows the use of the ADGS1612 in multiplexer configurations with external wiring.
6. Minimum distortion.

Rev. 0 Document Feedback

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REVISION HISTORY

1/2018—Revision 0: Initial Version

SPECIFICATIONS

±5 V DUAL SUPPLY

Positive supply (V_{DD}) = 5 V ± 10%, negative supply (V_{SS}) = −5 V ± 10%, digital supply (V_L) = 2.7 V to 5.5 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	1			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 29
	1.2	1.4	1.6	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance Match Between Channels, ΔR_{ON}	0.04			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.08	0.09	0.1	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	0.23			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.28	0.32	0.37	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.2			nA typ	V_S = V_D = ±4.5 V; see Figure 28
	±0.4	±1.5	±10.0	nA max	
DIGITAL OUTPUT					
Output Voltage					
Low, V_{OL}			0.4	V max	I_{SINK} = 5 mA
			0.2	V max	I_{SINK} = 1 mA
Output Current, Low (I_{OL}) or High (I_{OH})	0.001			µA typ	V_{OUT} = V_{GND} or V_L
			±0.1	µA max	
Digital Output Capacitance, C_{OUT}	4			pF typ	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2	V min	3.3 V < V_L ≤ 5.5 V
			1.35	V min	2.7 V ≤ V_L ≤ 3.3 V
Low, V_{INL}			0.8	V max	3.3 V < V_L ≤ 5.5 V
			0.8	V max	2.7 V ≤ V_L ≤ 3.3 V
Input Current, Low (I_{INL}) or High (I_{INH})	0.001			µA typ	V_{IN} = V_{GND} or V_L
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	385			ns typ	R_L = 300 Ω, C_L = 35 pF
	480	485	485	ns max	V_S = 2.5 V; see Figure 36
Off Time, t_{OFF}	250			ns typ	R_L = 300 Ω, C_L = 35 pF
	305	335	360	ns max	V_S = 2.5 V; see Figure 36
Break-Before-Make Time Delay, t_D	175			ns typ	R_L = 300 Ω, C_L = 35 pF
			115	ns min	V_{S1} = V_{S2} = 2.5 V, see Figure 35
Charge Injection, Q_{INJ}	120			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 37
Off Isolation	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 31
Channel to Channel Crosstalk	−93			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 33
−3 dB Bandwidth	34			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
Insertion Loss	−0.08			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Off Switch Source Capacitance, C_S (Off)	63			pF typ	V_S = 0 V, f = 1 MHz
Off Switch Drain Capacitance, C_D (Off)	63			pF typ	V_S = 0 V, f = 1 MHz
On Switch Capacitance, C_D (On), C_S (On)	154			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Positive Supply Current, I_{DD}	0.01			µA typ	All switches open
			1	µA max	
	0.01			µA typ	All switches closed, V_L = 5.5 V
			1	µA max	
	130			µA typ	All switches closed, V_L = 2.7 V
			220	µA max	
Digital Supply Current, I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Inactive, SCLK = 1 MHz	14			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	7			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
SCLK = 50 MHz	390			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	210			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
Inactive, SDI = 1 MHz	15			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	7.5			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
SDI = 25 MHz	230			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	120			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
Negative Supply Current, I_{SS}	0.01			µA typ	Digital inputs = 0 V or V_L
			1	µA max	
V_{DD}/V_{SS}			±3.3	V min	GND = 0 V
			±8	V max	GND = 0 V

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 2.7 V to 5.5 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	0.95			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 29
	1.1	1.25	1.45	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels, ΔR_{ON}	0.03			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.06	0.07	0.08	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	0.2			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.23	0.27	0.32	Ω max	
LEAKAGE CURRENTS					V_{DD} = 10.8 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.2			nA typ	V_S = V_D = 1 V/10 V; see Figure 28
	±0.4	±1.5	±10.0	nA max	
DIGITAL OUTPUT					
Output Voltage					
Low, V_{OL}			0.4	V max	I_{SINK} = 5 mA
			0.2	V max	I_{SINK} = 1 mA
Output Current, Low (I_{OL}) or High (I_{OH})	0.001			µA typ	V_{OUT} = V_{GND} or V_L
			±0.1	µA max	
Digital Output Capacitance, C_{OUT}	4			pF typ	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2	V min	3.3 V < V_L ≤ 5.5 V
			1.35	V min	2.7 V ≤ V_L ≤ 3.3 V
Low, V_{INL}			0.8	V max	3.3 V < V_L ≤ 5.5 V
			0.8	V max	2.7 V ≤ V_L ≤ 3.3 V
Input Current, Low (I_{INL}) or High (I_{INH})	0.001			µA typ	V_{IN} = V_{GND} or V_L
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	365			ns typ	R_L = 300 Ω, C_L = 35 pF
	460	470	470	ns max	V_S = 8 V; see Figure 36
Off Time, t_{OFF}	190			ns typ	R_L = 300 Ω, C_L = 35 pF
	235	260	280	ns max	V_S = 8 V; see Figure 36
Break-Before-Make Time Delay, t_D	200			ns typ	R_L = 300 Ω, C_L = 35 pF
			140	ns min	V_{S1} = V_{S2} = 8 V, see Figure 35
Charge Injection, Q_{INJ}	140			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 37
Off Isolation	−65			dB typ	RL = 50 Ω, CL = 5 pF, f = 100 kHz; see Figure 31
Channel to Channel Crosstalk	−93			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion Plus Noise, THD + N	0.012			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 33
−3 dB Bandwidth	34			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
Insertion Loss	−0.07			MHz typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Off Switch Source Capacitance, C_S (Off)	60			dB typ	V_S = 6 V, f = 1 MHz
Off Switch Drain Capacitance, C_D (Off)	60			pF typ	V_S = 6 V, f = 1 MHz
On Switch Capacitance, C_D (On), C_S (On)	154			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 12 V
Positive Supply Current, I_{DD}	0.01			µA typ	All switches open
			1	µA max	
	320			µA typ	All switches closed, V_L = 5.5 V
			480	µA max	
	320			µA typ	All switches closed, V_L = 2.7 V
			480	µA max	
Digital Supply Current, I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Inactive, SCLK = 1 MHz	14			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	7			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
SCLK = 50 MHz	390			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	210			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
Inactive, SDI = 1 MHz	15			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	7.5			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
SDI = 25 MHz	230			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	120			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
V_{DD}			3.3	V min	GND = 0 V, V_{SS} = 0 V
			16	V max	GND = 0 V, V_{SS} = 0 V

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, V_L = 2.7 V to 5.5 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	1.7			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA; see Figure 29
	2.15	2.4	2.7	Ω max	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.09	0.12	0.15	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	0.4			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.53	0.55	0.6	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V or 4.5 V, V_D = 4.5 V/1 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.2			nA typ	V_S = V_D = 1 V/4.5 V; see Figure 28
	±0.4	±1.5	±10.0	nA max	
DIGITAL OUTPUT					
Output Voltage					
Low, V_{OL}			0.4	V max	I_{SINK} = 5 mA
			0.2	V max	I_{SINK} = 1 mA
Output Current, Low (I_{OL}) or High (I_{OH})	0.001			µA typ	V_{OUT} = V_{GND} or V_L
			±0.1	µA max	
Digital Output Capacitance, C_{OUT}	4			pF typ	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2	V min	3.3 V < V_L ≤ 5.5 V
			1.35	V min	2.7 V ≤ V_L ≤ 3.3 V
Low, V_{INL}			0.8	V max	3.3 V < V_L ≤ 5.5 V
			0.8	V max	2.7 V ≤ V_L ≤ 3.3 V
Input Current, Low (I_{INL}) or High (I_{INH})	0.001			µA typ	V_{IN} = V_{GND} or V_L
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	405			ns typ	R_L = 300 Ω, C_L = 35 pF
	510	515	525	ns max	V_S = 2.5 V; see Figure 36
Off Time, t_{OFF}	290			ns typ	R_L = 300 Ω, C_L = 35 pF
	365	410	455	Ns max	V_S = 2.5 V; see Figure 36
Break-Before-Make Time Delay, t_D	165			ns typ	R_L = 300 Ω, C_L = 35 pF
			95	ns min	V_{S1} = V_{S2} = 2.5 V, see Figure 35
Charge Injection, Q_{INJ}	72			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 37
Off Isolation	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 31
Channel to Channel Crosstalk	−93			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion Plus Noise, THD + N	0.093			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 3.5 V p-p ; see Figure 33
−3 dB Bandwidth	38			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
Insertion Loss	−0.15			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Off Switch Source Capacitance, C_S (Off)	72			pF typ	V_S = 2.5 V, f = 1 MHz
Off Switch Drain Capacitance, C_D (Off)	72			pF typ	V_S = 2.5 V, f = 1 MHz
On Switch Capacitance, C_D (On), C_S (On)	160			pF typ	V_S = 2.5 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
Positive Supply Current, I_{DD}	0.01			µA typ	All switches open
			1	µA max	
	0.01			µA typ	All switches closed, V_L = 5.5 V
			1	µA max	
	130			µA typ	All switches closed, V_L = 2.7 V
			220	µA max	
Digital Supply Current, I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Inactive, SCLK = 1 MHz	14			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	7			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
SCLK = 50 MHz	390			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	210			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
Inactive, SDI = 1 MHz	15			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	7.5			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
SDI = 25 MHz	230			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	120			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
V_{DD}			3.3	V min	GND = 0 V, V_{SS} = 0 V
			16	V max	GND = 0 V, V_{SS} = 0 V

3.3 V SINGLE SUPPLY

V_{DD} = 3.3 V, V_{SS} = 0 V, V_L = 2.7 V to 3.3 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	3.2	3.4	3.6	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA, V_{DD} = 3.3 V, V_{SS} = 0 V; see Figure 29
On Resistance Match Between Channels, ΔR_{ON}	0.06	0.07	0.08	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
On Resistance Flatness, $R_{FLAT(ON)}$	1.2	1.3	1.4	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.3 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 32
	±0.3	±1.0	±6.0	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.2				V_S = V_D = 0.6 V/3 V; see Figure 28
	±0.4	±1.5	±10.0	V max	
DIGITAL OUTPUT					
Output Voltage					
Low, V_{OL}			0.4	V max	I_{SINK} = 5 mA
			0.2	V max	I_{SINK} = 1 mA
Output Current, Low (I_{OL}) or High (I_{OH})	0.001			µA typ	V_{OUT} = V_{GND} or V_L
			±0.1	µA max	
Digital Output Capacitance, C_{OUT}	4			pF typ	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			1.35	V min	
Low, V_{INL}			0.8	V max	
Input Current, Low (I_{INL}) or High (I_{INH})	0.001			µA typ	V_{IN} = V_{GND} or V_L
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	545			ns typ	R_L = 300 Ω, C_L = 35 pF
	720	730	735	ns max	V_S = 1.5 V; see Figure 36
Off Time, t_{OFF}	470			ns typ	R_L = 300 Ω, C_L = 35 pF
	630	695	760	ns max	V_S = 1.5 V; see Figure 36
Break-Before-Make Time Delay, t_D	155			ns typ	R_L = 300 Ω, C_L = 35 pF
			50	ns min	V_{S1} = V_{S2} = 1.5 V, see Figure 35
Charge Injection, Q_{INJ}	50			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 37
Off Isolation	−65			dB typ	C_L = 5 pF, f = 100 kHz; see Figure 31
Channel to Channel Crosstalk	−93			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30
Total Harmonic Distortion Plus Noise, THD + N	0.18			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p; see Figure 33
−3 dB Bandwidth	50			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
Insertion Loss	−0.27			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Off Switch Source Capacitance, C_S (Off)	76			pF typ	V_S = 1.5 V, f = 1 MHz
Off Switch Drain Capacitance, C_D (Off)	76			pF typ	V_S = 1.5 V, f = 1 MHz
On Switch Capacitance, C_D (On), C_S (On)	160			pF typ	V_S = 1.5 V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 3.3 V
Positive Supply Current, I_{DD}	0.01			µA typ	All switches open
			1	µA max	
	0.01			µA typ	All switches closed, V_L = 3.3 V
			1	µA max	
Digital Supply Current, I_L					
Inactive	3.2			µA typ	Digital inputs = 0 V or V_L
			4.8	µA max	
Inactive, SCLK = 1 MHz	7			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
SCLK = 50 MHz	210			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
Inactive, SDI = 1 MHz	7.5			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
SDI = 25 MHz	120			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
Active at 50 MHz	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
V_{DD}			3.3	V min	GND = 0 V, V_{SS} = 0 V
			16	V max	GND = 0 V, V_{SS} = 0 V

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5. Four Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +5 V, V_{SS} = −5 V (θ_{JA} = 60°C/W)	315	194	106	mA max
V_{DD} = 12 V, V_{SS} = 0 V (θ_{JA} = 60°C/W)	330	200	108	mA max
V_{DD} = 5 V, V_{SS} = 0 V (θ_{JA} = 60°C/W)	249	161	96	mA max
V_{DD} = 3.3 V, V_{SS} = 0 V (θ_{JA} = 60°C/W)	203	137	87	mA max

Table 6. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +5 V, V_{SS} = −5 V (θ_{JA} = 60°C/W)	566	292	126	mA max
V_{DD} = 12 V, V_{SS} = 0 V (θ_{JA} = 60°C/W)	591	301	127	mA max
V_{DD} = 5 V, V_{SS} = 0 V (θ_{JA} = 60°C/W)	450	251	120	mA max
V_{DD} = 3.3 V, V_{SS} = 0 V (θ_{JA} = 60°C/W)	366	218	113	mA max

TIMING CHARACTERISTICS

V_L = 2.7 V to 5.5 V; GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 7.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	20	ns min	SCLK period
t_2	8	ns min	SCLK high pulse width
t_3	8	ns min	SCLK low pulse width
t_4	10	ns min	$\overline{CS}$ falling edge to SCLK rising edge
t_5	6	ns min	Data setup time
t_6	8	ns min	Data hold time
t_7	10	ns min	SCLK active edge to $\overline{CS}$ rising edge
t_8	20	ns max	$\overline{CS}$ falling edge to SDO data available
t_9[1]	20	ns max	SCLK falling edge to SDO data available
t_{10}	20	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
t_{11}	20	ns min	$\overline{CS}$ high time between SPI commands
t_{12}	8	ns min	$\overline{CS}$ falling edge to SCLK becomes stable
t_{13}	8	ns min	$\overline{CS}$ rising edge to SCLK becomes stable

[1] Measured with the 1 kΩ pull-up resistor to V_L and 20 pF load. The t_9 parameter determines the maximum SCLK frequency when SDO is used.

Timing Diagrams

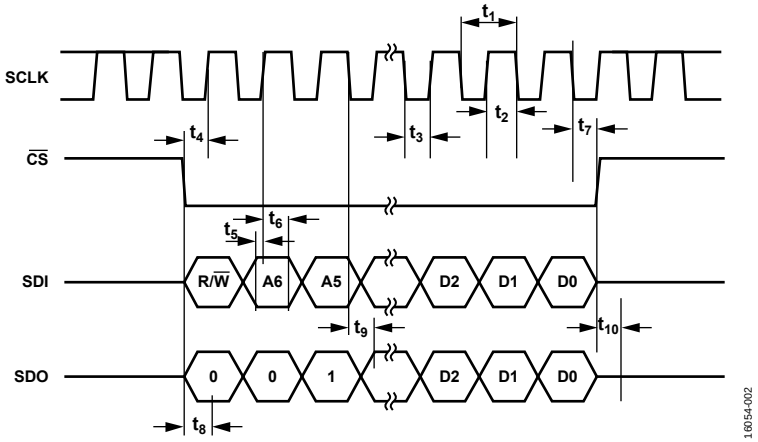


Figure 2. Addressable Mode Timing Diagram

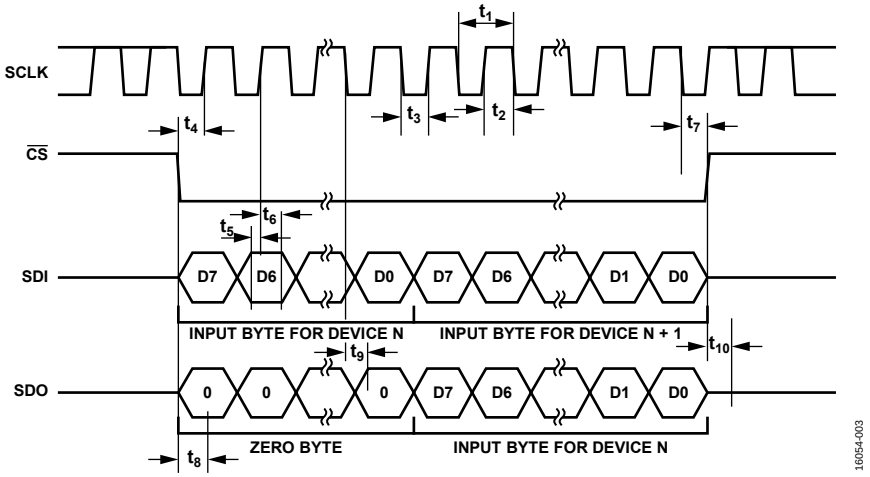


Figure 3. Daisy-Chain Timing Diagram

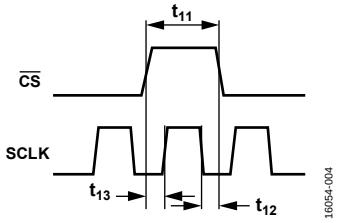


Figure 4. SCLK/$\overline{CS}$ Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
$\overline{RESET}$/V_L to GND	
V_{DD} ≤ 5.5 V	−0.3V to V_{DD} + 0.3 V
V_{DD} > 5.5 V	−0.3 V to +6 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	−0.3 V to +6 V
Peak Current, Sx or Dx Pins[2]	546 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2, 3]	Data + 15%
Temperature Ranges	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb-Free	260°C

[1] Overvoltages at the digital, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.
[3] See Table 5 and Table 6.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-17[1]	60	13	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

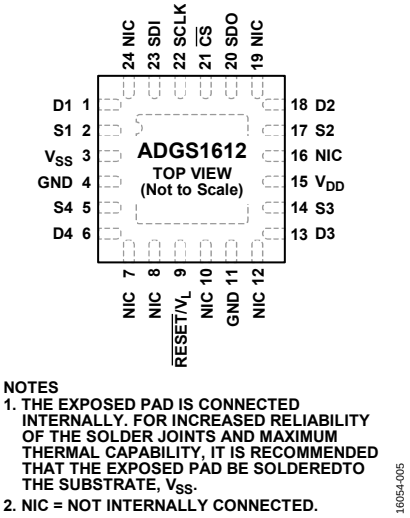


Figure 5. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Drain Terminal 1. This pin can be an input or an output.
2	S1	Source Terminal 1. This pin can be an input or an output.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, tie this pin to ground.
4, 11	GND	Ground (0 V) Reference.
5	S4	Source Terminal 4. This pin can be an input or an output.
6	D4	Drain Terminal 4. This pin can be an input or an output.
7, 8, 10, 12, 16, 19, 24	NIC	Not Internally Connected. These pins are not internally connected.
9	$\overline{RESET}/V_L$	Reset/Logic Power Supply Input. Under normal operation, drive the $\overline{RESET}/V_L$ pin with a 2.7 V to 5.5 V supply. Pull the pin low to complete a hardware reset. All switches are opened, and the appropriate registers are set to their default settings.
13	D3	Drain Terminal 3. This pin can be an input or an output.
14	S3	Source Terminal 3. This pin can be an input or an output.
15	V_{DD}	Most Positive Power Supply Potential.
17	S2	Source Terminal 2. This pin can be an input or an output.
18	D2	Drain Terminal 2. This pin can be an input or an output.
20	SDO	Serial Data Output. This pin can be used for daisy-chaining a number of these devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Pull this open-drain output to V_L with an external resistor.
21	$\overline{CS}$	Active Low Control Input. $\overline{CS}$ is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it powers on the SCLK buffers and enables the input shift register. Data is transferred in on the falling edges of the following clocks. Taking $\overline{CS}$ high updates the switch condition.
22	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK. Data is transferred at rates of up to 50 MHz.
23	SDI	Serial Data Input. Data is captured on the positive edge of the serial clock input.
	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the substrate, V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

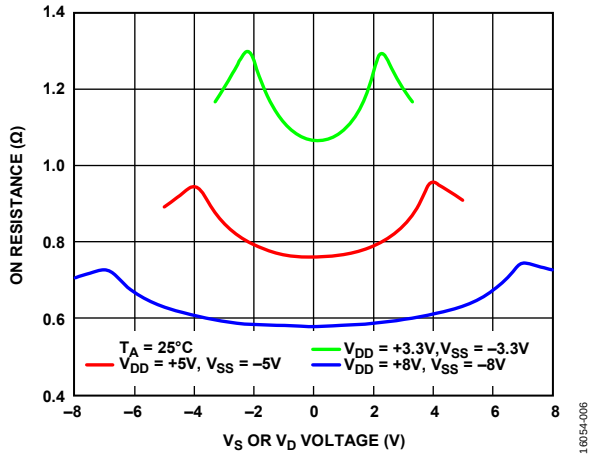


Figure 6. On Resistance (R_{ON}) as a Function of V_S, V_D (Dual Supply)

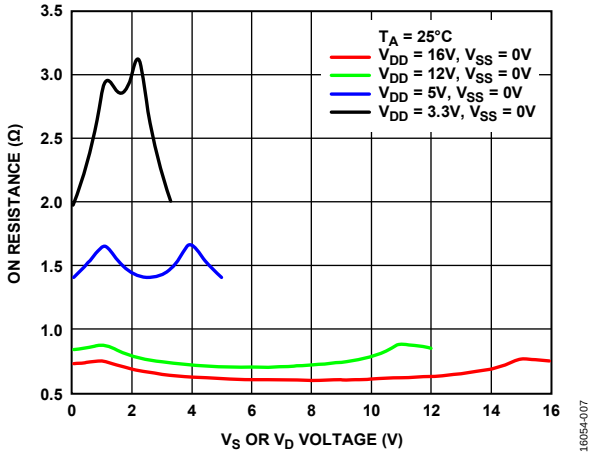


Figure 7. On Resistance (R_{ON}) as a Function of V_S, V_D (Single Supply)

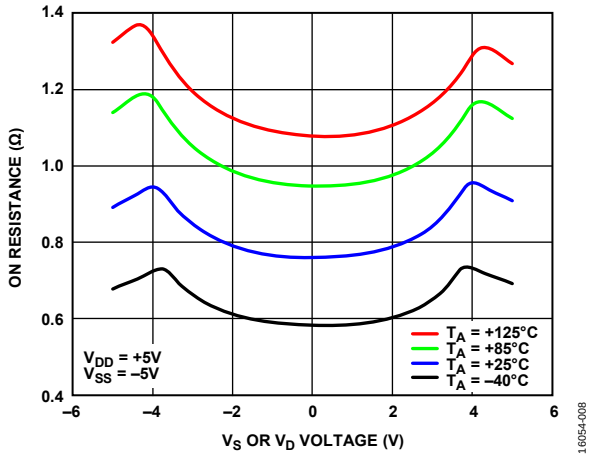


Figure 8. On Resistance (R_{ON}) as a Function of V_S (V_D) for Various Temperatures, ±5 V Dual Supply

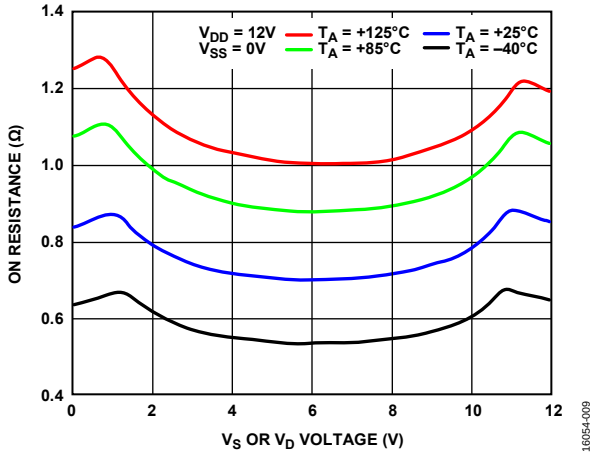


Figure 9. On Resistance (R_{ON}) as a Function of V_S (V_D) for Various Temperatures, 12 V Single Supply

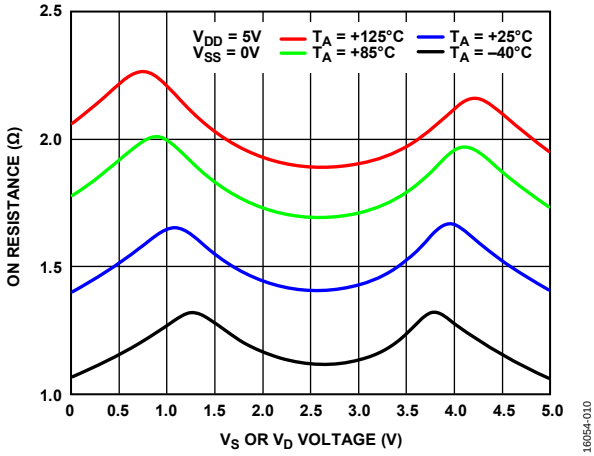


Figure 10. On Resistance (R_{ON}) as a Function of V_S (V_D) for Various Temperatures, 5 V Single Supply

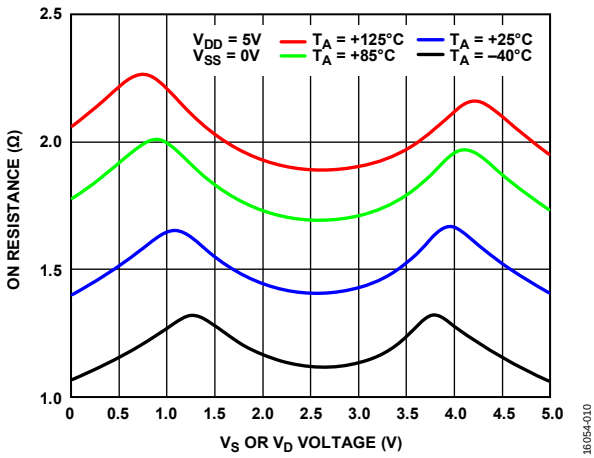


Figure 11. On Resistance (R_{ON}) as a Function of V_S (V_D) for Various Temperatures, 3.3 V Single Supply

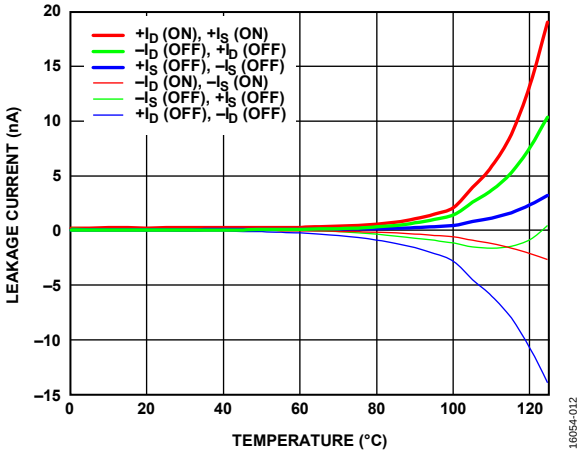


Figure 12. Leakage Current vs. Temperature, ±5 V Dual Supply

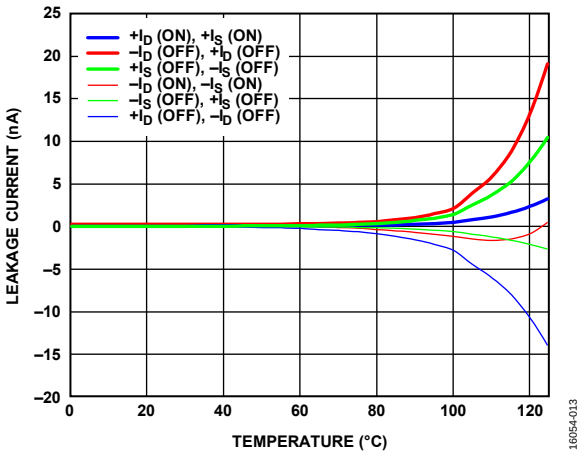


Figure 13. Leakage Current vs. Temperature, 12 V Single Supply

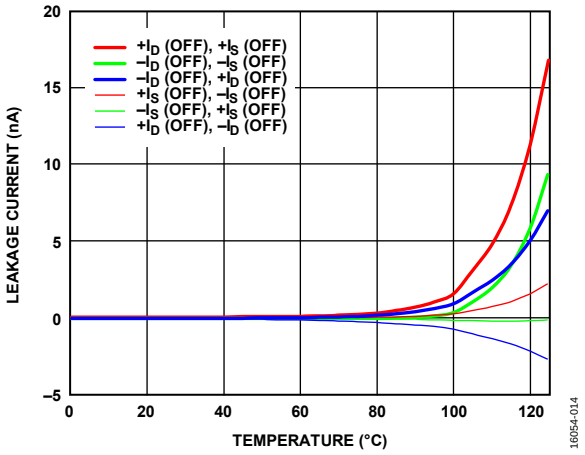


Figure 14. Leakage Current vs. Temperature, 5 V Single Supply

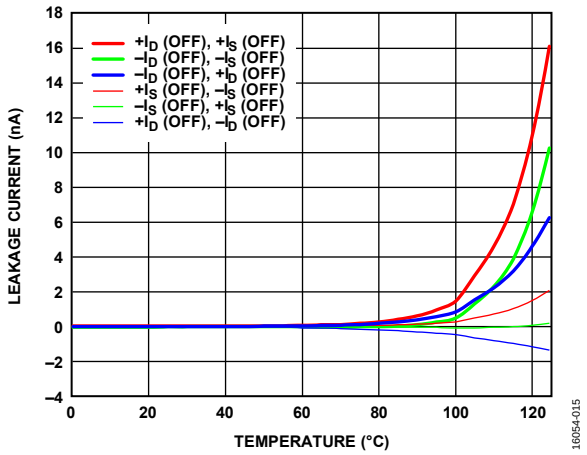


Figure 15. Leakage Current vs. Temperature, 3.3 V Single Supply

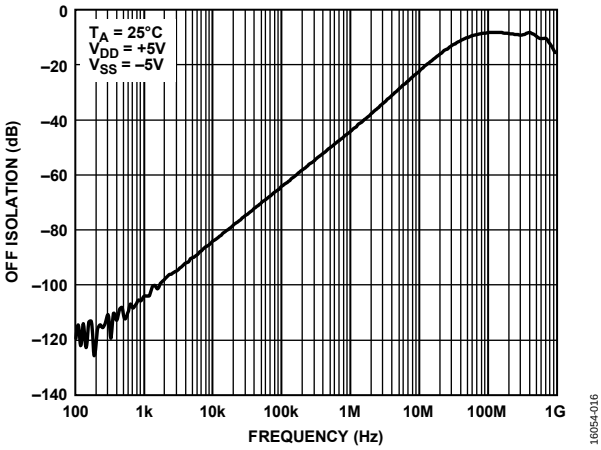


Figure 16. Off Isolation vs. Frequency, ±5 V Dual Supply

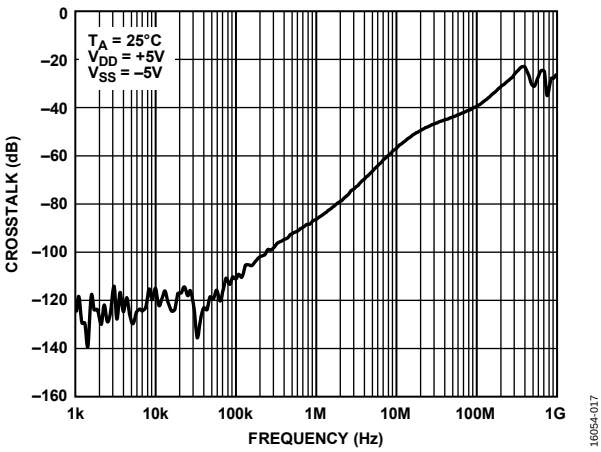


Figure 17. Crosstalk vs. Frequency, ±5 V Dual Supply

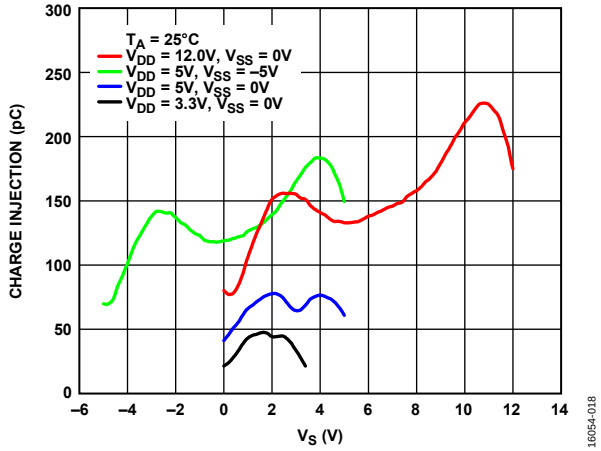


Figure 18. Charge Injection vs. Source Voltage, V_S

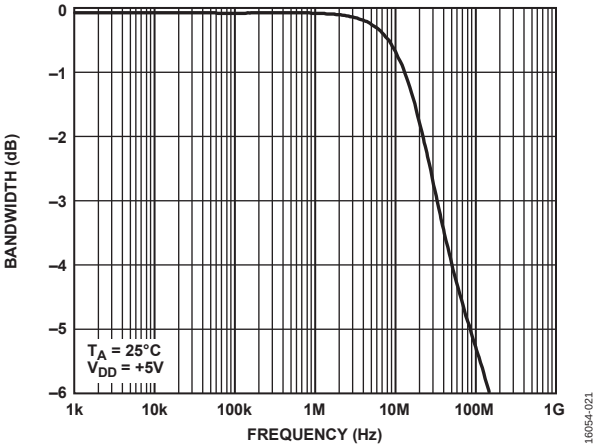


Figure 21. Bandwidth

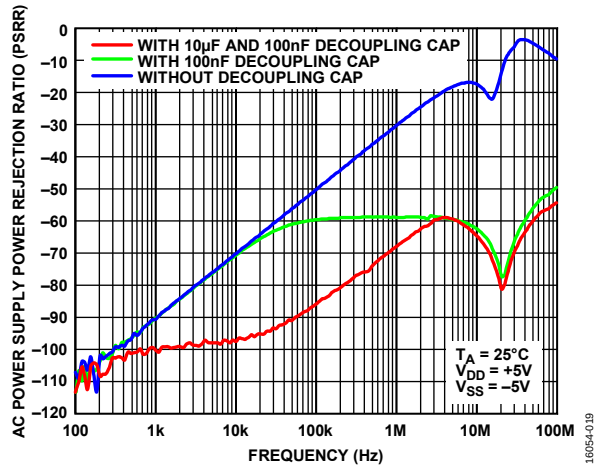


Figure 19. AC Power Supply Power Rejection Ratio (AC PSRR) vs. Frequency, ±5 V Dual Supply

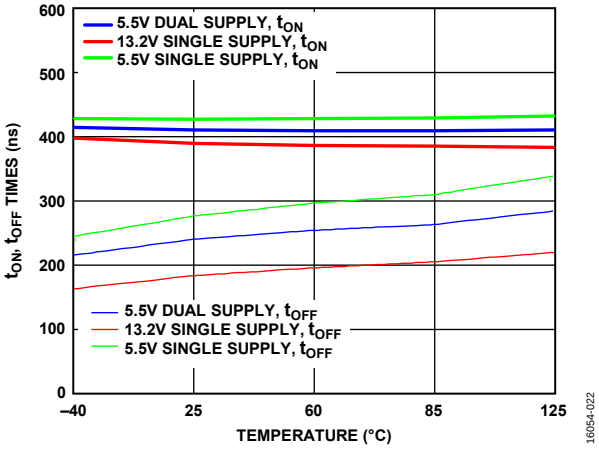


Figure 22. t_{ON}, t_{OFF} Times vs. Temperature, V_L = 5.5 V

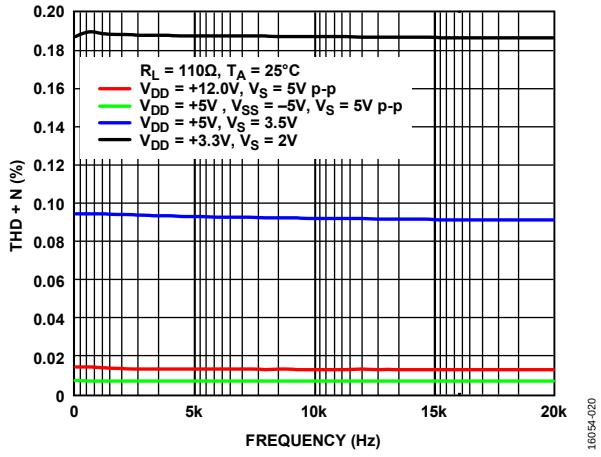


Figure 20. THD + N vs. Frequency, ±5 V Dual Supply

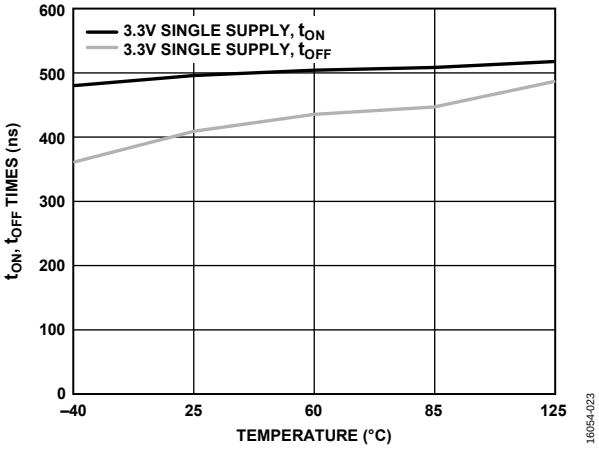


Figure 23. t_{ON}, t_{OFF} Times vs. Temperature, V_L = 3.3 V

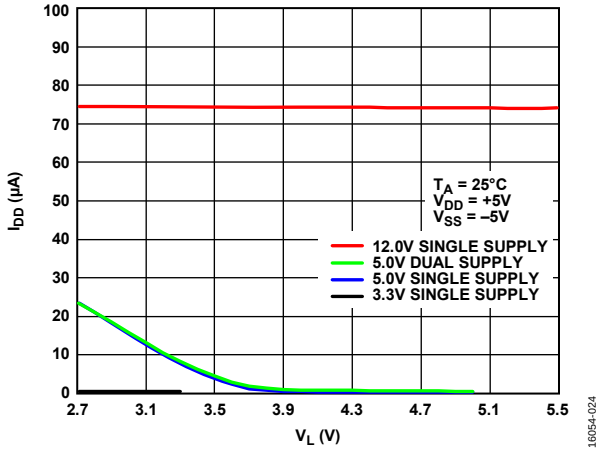


Figure 24. I_{DD} vs. V_L

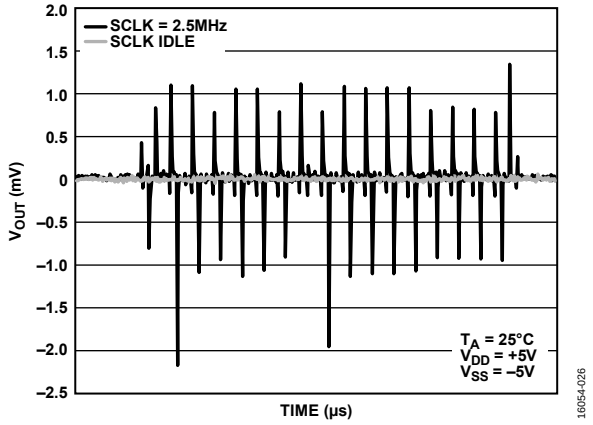


Figure 26. Digital Feedthrough

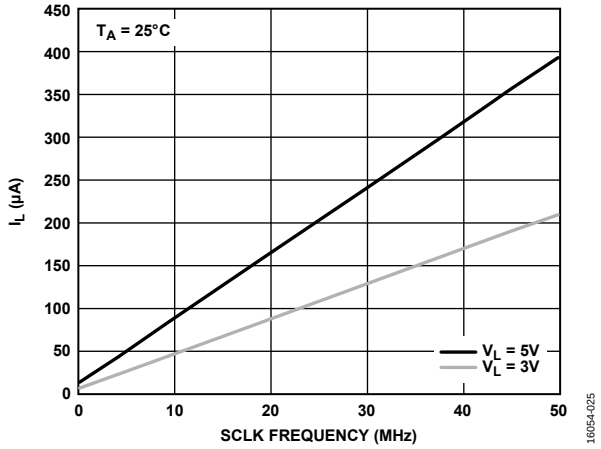


Figure 25. I_L vs. SCLK Frequency When $\overline{CS}$ Is High

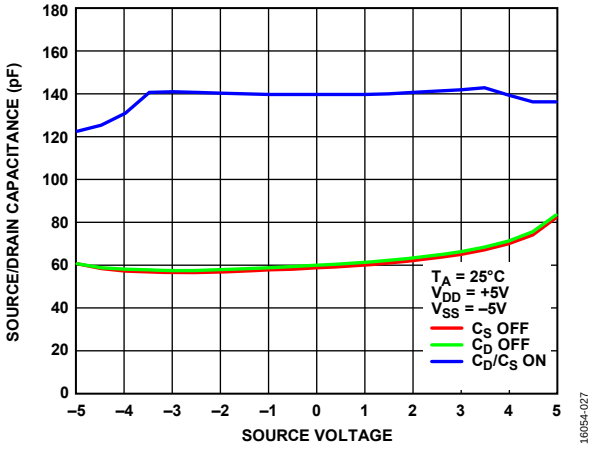


Figure 27. Source/Drain Capacitance vs. Source Voltage (V_S)

TEST CIRCUITS

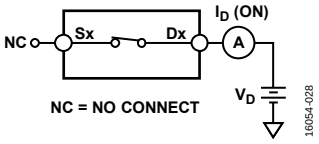


Figure 28. On Leakage

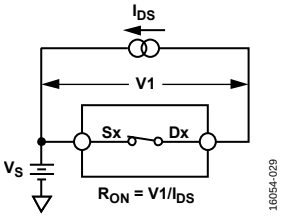


Figure 29. On Resistance

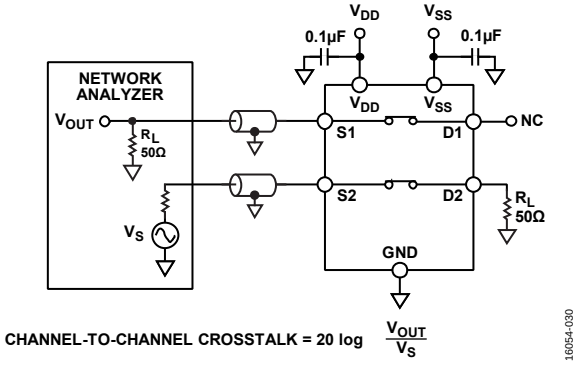


Figure 30. Channel to Channel Crosstalk

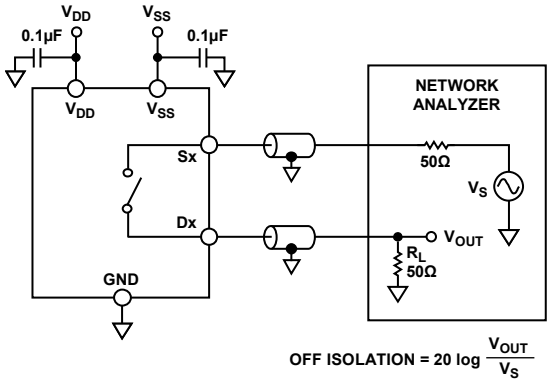


Figure 31. Off Isolation

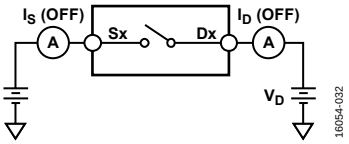


Figure 32. Off Leakage

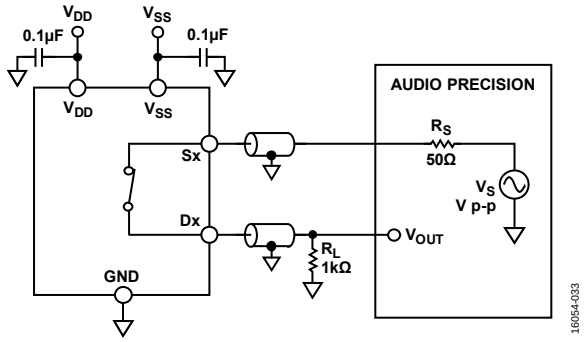


Figure 33. THD + N

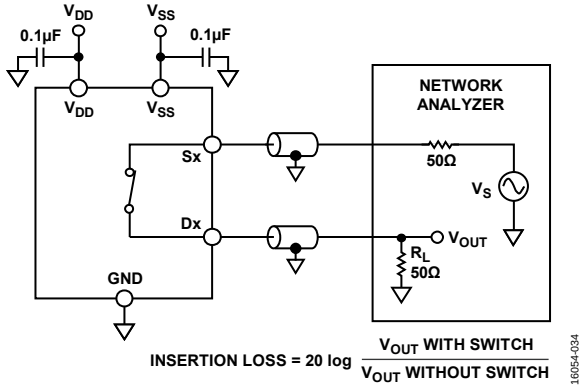


Figure 34. Bandwidth

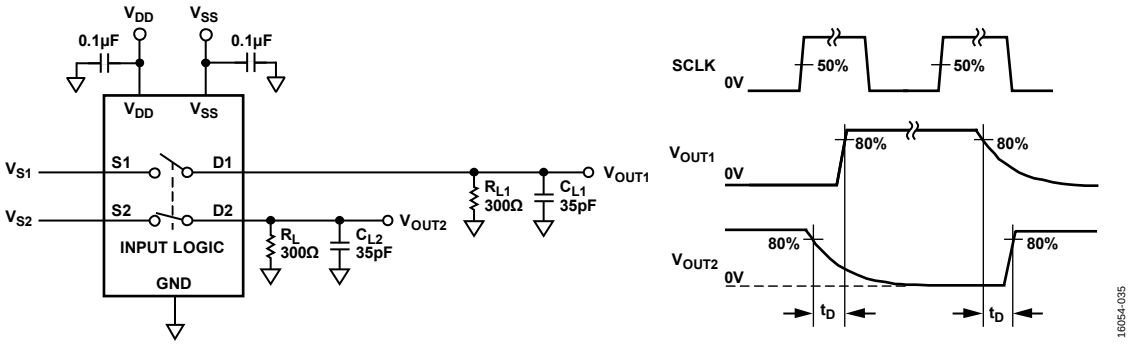


Figure 35. Break-Before-Make Time Delay, t_D

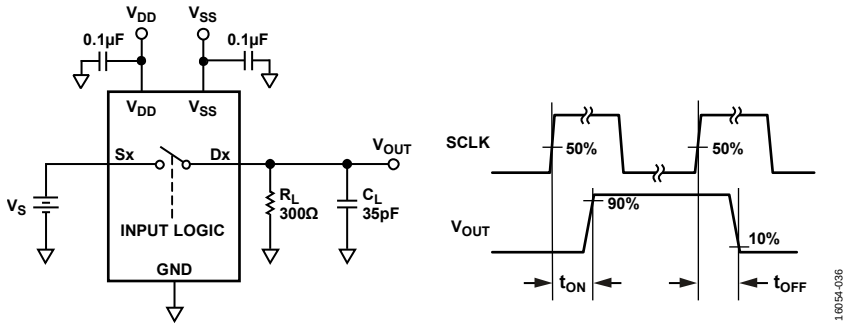


Figure 36. Switching Times

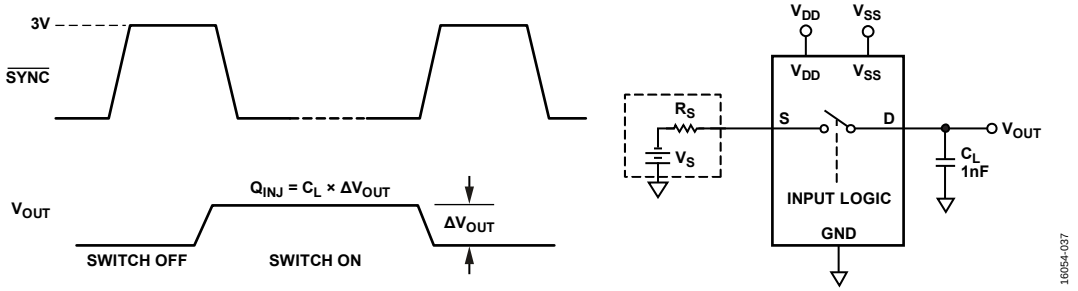
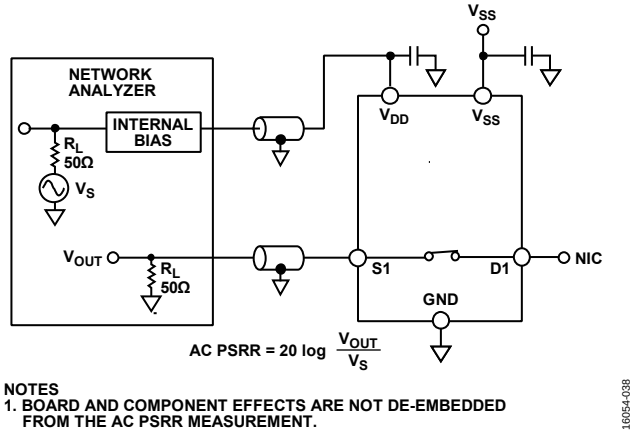


Figure 37. Charge Injection



NOTES
1. BOARD AND COMPONENT EFFECTS ARE NOT DE-EMBEDDED FROM THE AC PSRR MEASUREMENT.

Figure 38. AC PSRR

TERMINOLOGY

I_{DD}
I_{DD} is the positive supply current.

I_{SS}
I_{SS} is the negative supply current.

V_D, V_S
V_D and V_S are the analog voltages on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} is the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
$R_{FLAT (ON)}$ is the difference between the maximum and minimum values of on resistance, measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) are the channel leakage currents with the switch on.

I_{DS}
I_{DS} is the drain to source current.

V1
V1 is the voltage drop across the switch, Sx, to Dx.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} is the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) is the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) is the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) are the on switch capacitances, measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} is the delay between applying the digital control input and the output switching on.

t_{OFF}
t_{OFF} is the delay between applying the digital control input and the output switching off.

t_D
t_D is the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion Plus Noise (THD + N)
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)
AC PSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. AC PSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATION

The ADGS1612 is a set of serially controlled, quad SPST switches with error detection features. SPI Mode 0 and SPI Mode 3 can be used with the device, and it operates with SCLK frequencies of up to 50 MHz. The default mode for the ADGS1612 is address mode, in which the registers of the device are accessed by a 16-bit SPI command bounded by $\overline{CS}$. The SPI command becomes 24-bit if the user enables CRC error detection. Other error detection features include SCLK count error and invalid read/write error. If any of these SPI interface errors occur, they are detectable by reading the error flags register. The ADGS1612 can also operate in two other modes, namely burst mode and daisy-chain mode.

The interface pins of the ADGS1612 are $\overline{CS}$, SCLK, SDI, and SDO. Hold $\overline{CS}$ low when using the SPI interface. Data is captured on the SDI pin on the rising edge of SCLK, and data is propagated out on the SDO pin on the falling edge of SCLK. SDO has an open-drain output; thus, connect a pull-up resistor to this output. When not pulled low by the ADGS1612, SDO is in a high impedance state.

ADDRESS MODE

Address mode is the default mode for the ADGS1612 on power-up. A single SPI frame in address mode is bounded by a $\overline{CS}$ falling edge and the succeeding $\overline{CS}$ rising edge. The SPI frame is composed of 16 SCLK cycles. The timing diagram for address mode is shown in Figure 39. The first SDI bit indicates whether the SPI command is a read or write command. When the first bit is set to 0, a write command is issued, and if the first bit is set to 1, a read command is issued. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command, because during these clock cycles, SDO propagates out the data contained in the addressed register.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the ninth to the 16th SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

During any SPI command, SDO sends out eight alignment bits on the first eight SCLK falling edges. The alignment bits observed at SDO are 0x25.

ERROR DETECTION FEATURES

Protocol and communication errors on the SPI interface are detectable. There are three detectable errors: incorrect SCLK error detection, invalid read and write address error detection, and CRC error detection. Each of these errors has a corresponding enable bit in the error configuration register. In addition, there is an error flag bit for each of these errors in the error flags register.

Cyclic Redundancy Check (CRC) Error Detection

The CRC error detection feature extends a valid SPI frame by eight SCLK cycles. These eight extra cycles are needed to send the CRC byte for that SPI frame. The CRC byte is calculated by the SPI block using the 16-bit payload: the R/$\overline{W}$ bit, Address Bits[6:0], and Data Bits[7:0]. The CRC polynomial used in the SPI block is $x^8 + x^2 + x^1 + 1$ with a seed value of 0. For a timing diagram with CRC enabled, see Figure 40. Register writes occur at the 24th SCLK rising edge with CRC error checking enabled.

During an SPI write, the microcontroller/CPU provides the CRC byte through SDI. The SPI block checks the CRC byte just before the 24th SCLK rising edge. On this same edge, the register write is prevented if an incorrect CRC byte is received by the SPI interface. The CRC error flag is asserted in the error flags register in the case of the incorrect CRC byte being detected.

During an SPI read, the CRC byte is provided to the microcontroller through SDO.

The CRC error detection feature is disabled by default and can be configured by the user through the error configuration register.

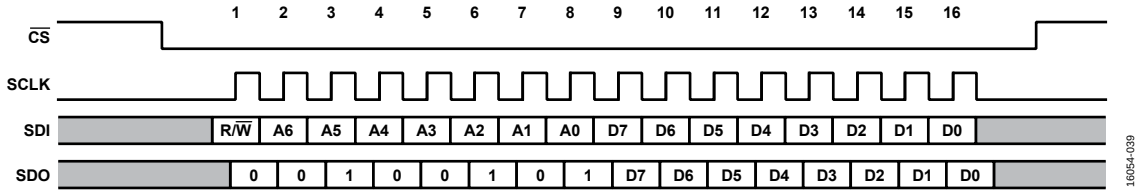


Figure 39. Address Mode Timing Diagram

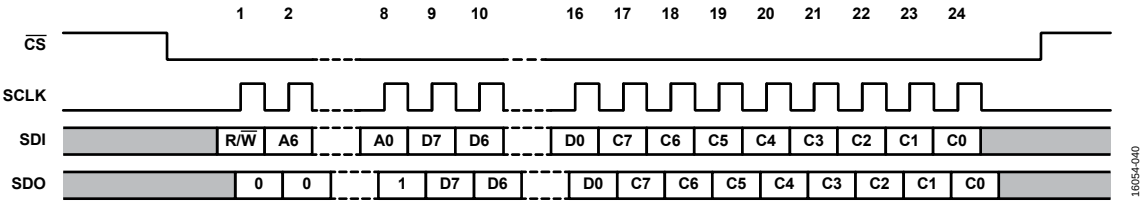


Figure 40. Timing Diagram with CRC Enabled

SCLK Count Error Detection

SCLK count error detection allows the user to detect if an incorrect number of SCLK cycles are sent by the microcontroller or CPU. When in address mode, with CRC disabled, 16 SCLK cycles are expected. If 16 SCLK cycles are not detected, the SCLK count error flag asserts in the error flags register. When less than 16 SCLK cycles are received by the device, a write to the register map never occurs. When the ADGS1612 receives more than 16 SCLK cycles, a write to the memory map still occurs at the 16th SCLK rising edge, and the flag asserts in the error flags register. With CRC enabled, the expected number of SCLK cycles is 24. SCLK count error detection is enabled by default and can be configured by the user through the error configuration register.

Invalid Read/Write Address Error

An invalid read/write address error detects when a nonexistent register address is a target for a read or write. In addition, this error asserts when a write to a read only register is attempted. The invalid read/write address error flag asserts in the error flags register when an invalid read/write address error occurs. The invalid read/write address error is detected on the ninth SCLK rising edge, which means a write to the register never occurs when an invalid address is targeted. Invalid read/write address error detection is enabled by default and can be disabled by the user through the error configuration register.

CLEARING THE ERROR FLAGS REGISTER

To clear the error flags register, write the special 16-bit SPI frame, 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must also send the correct CRC byte to complete an error clear command. At the 16th or 24th SCLK rising edge, the error flags register resets to zero.

BURST MODE

The SPI interface can accept consecutive SPI commands without the need to deassert the $\overline{CS}$ line, which is called burst mode. Burst mode is enabled through the burst enable register. This mode uses the same 16-bit command to communicate with the device. In addition, the response of the device at SDO is still aligned with the corresponding SPI command. Figure 41 shows an example of SDI and SDO during burst mode.

The invalid read/write address and CRC error checking functions operate similarly during burst mode as they do during address mode. However, SCLK count error detection operates in a slightly different manner. The total number of SCLK cycles within a given $\overline{CS}$ frame are counted, and if the total is not a multiple of 16 or a multiple of 24 when CRC is enabled, the SCLK count error flag asserts.

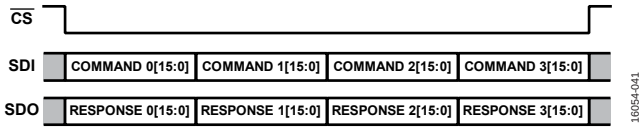


Figure 41. Burst Mode Frame

SOFTWARE RESET

When in address mode, the user can initiate a software reset. To do so, write two consecutive SPI commands, namely 0xA3 followed by 0x05, targeting Register 0x0B. After a software reset, all register values are set to default.

DAISY-CHAIN MODE

The connection of several ADGS1612 devices in a daisy-chain configuration is possible, and Figure 42 shows this setup. All devices share the same $\overline{CS}$ and SCLK line, whereas the SDO pin of a device forms a connection to the SDI pin of the next device, creating a shift register. In daisy-chain mode, SDO is an eight-cycle delayed version of SDI. When in daisy-chain mode, all commands target the switch data register. Therefore, it is not possible to make configuration changes while in daisy-chain mode.

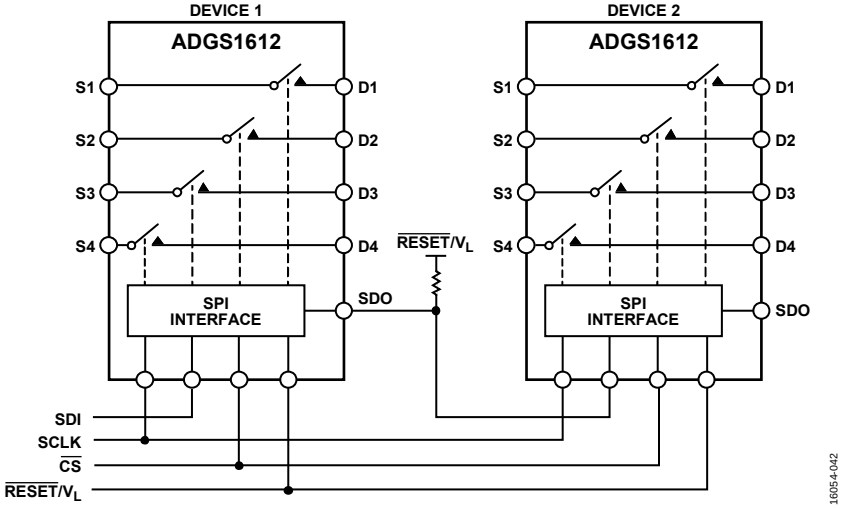


Figure 42. Two SPI Controlled Switches Connected in a Daisy-Chain Configuration

The ADGS1612 can only enter daisy-chain mode when in address mode by sending the 16-bit SPI command, 0x2500 (see Figure 43). When the ADGS1612 receives this command, the SDO of the device sends out the same command because the alignment bits at SDO are 0x25, which allows multiple daisy-connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 44. When $\overline{CS}$ goes high, Device 1 writes Command 0, Bits[7:0] to its switch data register, Device 2 writes Command 1, Bits[7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering daisy-chain mode, the first eight bits sent out by SDO on each device in the chain are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads in data on SDI while data is propagated out of SDO on an SCLK falling edge. The expected number of SCLK cycles must be a multiple of eight before $\overline{CS}$ goes high; if this is not the case, the SPI interface sends the last eight bits received to the switch data register.

POWER-ON RESET

The digital section of the ADGS1612 enters an initialization phase during V_L power-up. This initialization also occurs after a hardware or software reset. After V_L power-up or a reset, ensure that a minimum of 120 µs from the time of power-up or reset before any SPI command is issued. Ensure that V_L does not drop out during the 120 µs initialization phase because this may result in incorrect operation of the ADGS1612.

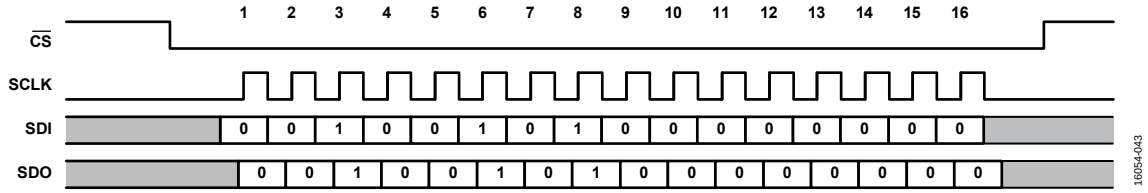


Figure 43. SPI Command to Enter Daisy-Chain Mode

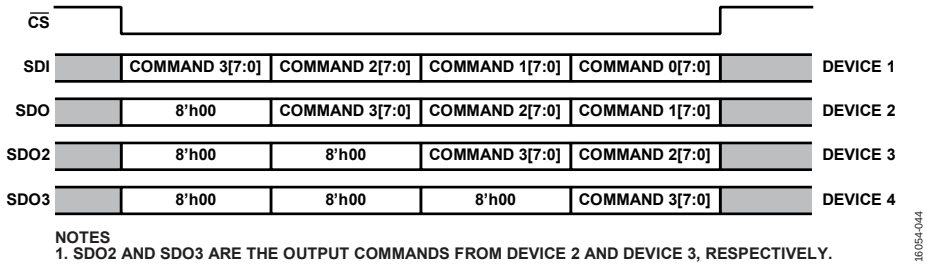


Figure 44. Example of an SPI Frame When Four ADGS1612 Devices Are Connected in Daisy-Chain Mode

APPLICATIONS INFORMATION

BREAK-BEFORE-MAKE SWITCHING

The ADGS1612 exhibits break-before-make switching action, which allows the use of the device in multiplexer applications. A multiplexer can be achieved by externally hardwiring the device in the mux configuration that is required, as shown in Figure 45.

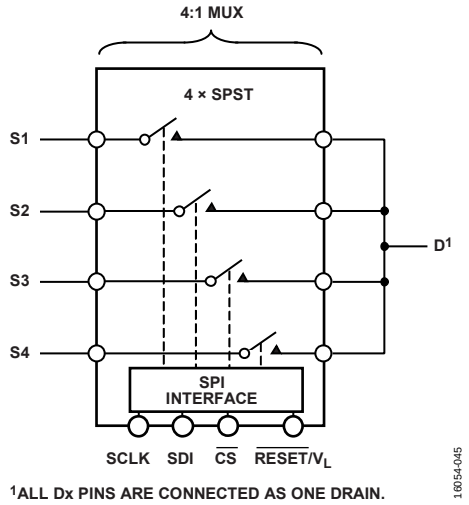


Figure 45. SPI Controlled Switch Configured as a 4:1 Mux

DIGITAL INPUT BUFFERS

There are input buffers present on the digital inputs pins, $\overline{CS}$, SCLK, and SDI. These buffers are active at all times. Therefore, there is current draw from the V_L supply if SCLK or SDI is toggling, regardless of whether $\overline{CS}$ is active. For typical values of this current draw, refer to the Specifications section and Figure 26.

POWER SUPPLY RAILS

To guarantee correct operation of the ADGS1612, 0.1 µF decoupling capacitors are required.

The ADGS1612 can operate with bipolar supplies between ±3.3 V and ±8 V. The supplies on V_{DD} and V_{SS} do not have to be symmetrical; however, the V_{DD} to V_{SS} range must not exceed 16 V. The ADGS1612 can also operate with single supplies between 3.3 V and 16 V with V_{SS} connected to GND.

The voltage range that can be supplied to V_L is from 2.7 V to 5.5 V.

The device is fully specified at ±5 V, 12 V, 5 V, and 3.3 V analog supply voltage ranges.

REGISTER SUMMARY

Table 11. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x01	SW_DATA	[7:0]	RESERVED				SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/W
0x02	ERR_CONFIG	[7:0]	RESERVED					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/W
0x03	ERR_FLAGS	[7:0]	RESERVED					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	[7:0]	RESERVED							BURST_MODE_EN	0x00	R/W
0x0B	SOFT_RESETB	[7:0]	SOFT_RESETB								0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x01, Reset: 0x00, Name: SW_DATA

The switch data register controls the status of the four switches of the ADGS1612.

Table 12. Bit Descriptions for SW_DATA

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
3	SW4_EN		Enable bit for SW4.	0x0	R/W
		0	SW4 open.		
		1	SW4 closed.		
2	SW3_EN		Enable bit for SW3.	0x0	R/W
		0	SW3 open.		
		1	SW3 closed.		
1	SW2_EN		Enable bit for SW2.	0x0	R/W
		0	SW2 open.		
		1	SW2 closed.		
0	SW1_EN		Enable bit for SW1.	0x0	R/W
		0	SW1 open.		
		1	SW1 closed.		

ERROR CONFIGURATION REGISTER

Address: 0x02, Reset: 0x06, Name: ERR_CONFIG

The error configuration register allows the user to enable or disable the relevant error features as required.

Table 13. Bit Descriptions for ERR_CONFIG

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
2	RW_ERR_EN		Enable bit for detecting an invalid read/write address.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
1	SCLK_ERR_EN		Enable bit for detecting the correct number of SCLK cycles in an SPI frame. When CRC is disabled and burst mode is disabled, 16 SCLK cycles are expected. When CRC is enabled and burst mode is disabled, 24 SCLK cycles are expected. A multiple of 16 SCLK cycles is expected when CRC is disabled and burst mode is enabled. A multiple of 24 SCLK cycles is expected when CRC is enabled and burst mode is enabled.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
0	CRC_ERR_EN		Enable bit for CRC error detection. SPI frames must be 24 bits wide when enabled.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

ERROR FLAGS REGISTER

Address: 0x03, Reset: 0x00, Name: ERR_FLAGS

The error flags register allows the user to determine if an error occurred. To clear the error flags register, the special 16-bit SPI command, 0x6CA9, must be written to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, then the user must include the correct CRC byte during the SPI write for the clear error flags register command to complete.

Table 14. Bit Descriptions for ERR_FLAGS

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	RESERVED		These bits are reserved and are set to 0.	0x0	R
2	RW_ERR_FLAG		Error flag for invalid read/write address. The error flag asserts during an SPI read if the target address does not exist. The error flag also asserts when the target address of an SPI write does not exist or is read only.	0x0	R
		0	No error.		
		1	Error.		
1	SCLK_ERR_FLAG		Error flag for the detection of the correct number of SCLK cycles in an SPI frame.	0x0	R
		0	No error.		
		1	Error.		
0	CRC_ERR_FLAG		Error flag that determines if a CRC error occurs during a register write.	0x0	R
		0	No error.		
		1	Error.		

BURST ENABLE REGISTER

Address: 0x05, Reset: 0x00, Name: BURST_EN

The burst enable register allows the user to enable or disable burst mode. When enabled, the user can send multiple consecutive SPI commands without deasserting $\overline{CS}$.

Table 15. Bit Descriptions for BURST_EN

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
0	BURST_MODE_EN		Burst mode enable bit.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

SOFTWARE RESET REGISTER

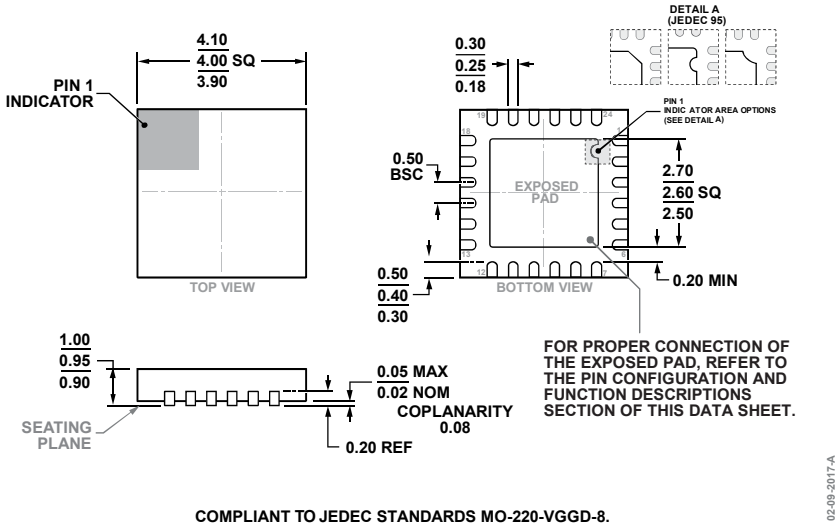
Address: 0x0B, Reset: 0x00, Name: SOFT_RESETB

This software reset register is used to perform a software reset. Consecutively write 0xA3 and 0x05 to this register, and the device registers reset to their default states.

Table 16. Bit Descriptions for SOFT_RESETB

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	SOFT_RESETB		To perform a software reset, consecutively write 0xA3 followed by 0x05 to this register.	0x0	R/W

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 46. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.95 mm Package Height
(CP-24-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADGS1612BCPZ	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-17
ADGS1612BCPZ-RL7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-17
EVAL-ADGS1612SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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