

# 74HC4040; 74HCT4040

## 12-stage binary ripple counter

Rev. 03 — 14 September 2005

Product data sheet

## 1. General description

The 74HC4040; 74HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4040B series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4040; 74HCT4040 are 12-stage binary ripple counters with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of  $\overline{CP}$ .

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of  $\overline{CP}$ .

Each counter stage is a static toggle flip-flop.

## 2. Features

- Multiple package options
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114-C exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

## 4. Quick reference data

**Table 1: Quick reference data**  
 $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Type 74HC4040</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay					
	$\overline{CP}$ to Q0	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	14	-	ns
	Qn to Qn+1	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	8	-	ns

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**Table 1: Quick reference data ...continued** $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{max}$	maximum operating frequency	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	90	-	MHz
$C_i$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	$V_I = GND\text{ to }V_{CC}$	-	20	-	pF
<b>Type 74HCT4040</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay					
	$\overline{CP}$ to Q0	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	16	-	ns
	Qn to Qn+1	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	8	-	ns
$f_{max}$	maximum operating frequency	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	79	-	MHz
$C_i$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	$V_I = GND\text{ to }V_{CC} - 1.5\text{ V}$	-	20	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V.

## 5. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74HC4040N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC4040D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4040DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4040PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4040BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4040N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HCT4040D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

Table 2: Ordering information ...continued

Type number	Package			Version
	Temperature range	Name	Description	
74HCT4040DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4040PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4040BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

## 6. Functional diagram

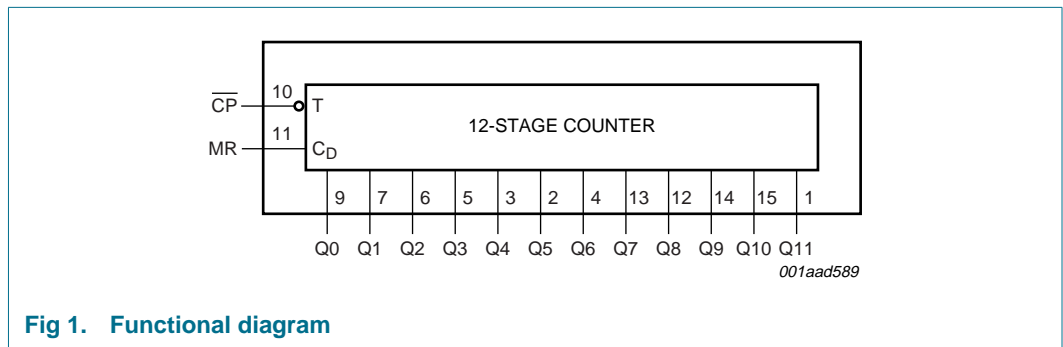


Fig 1. Functional diagram

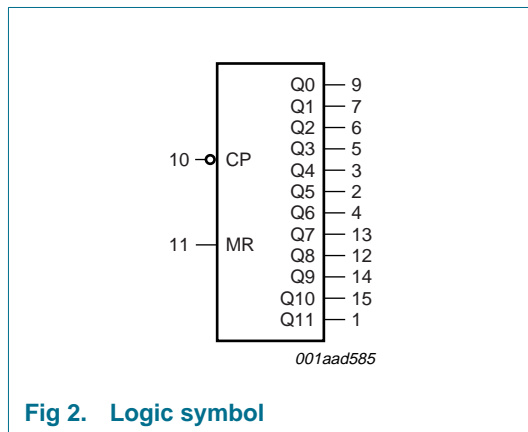


Fig 2. Logic symbol

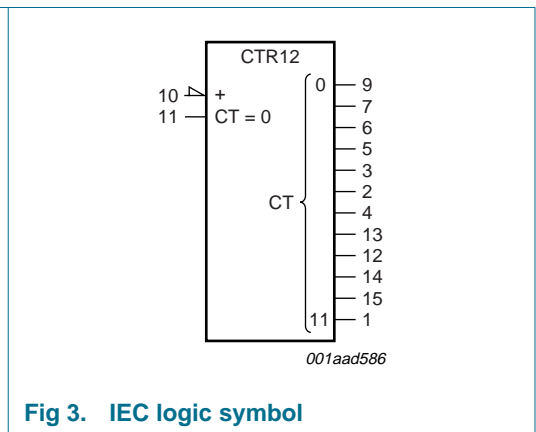
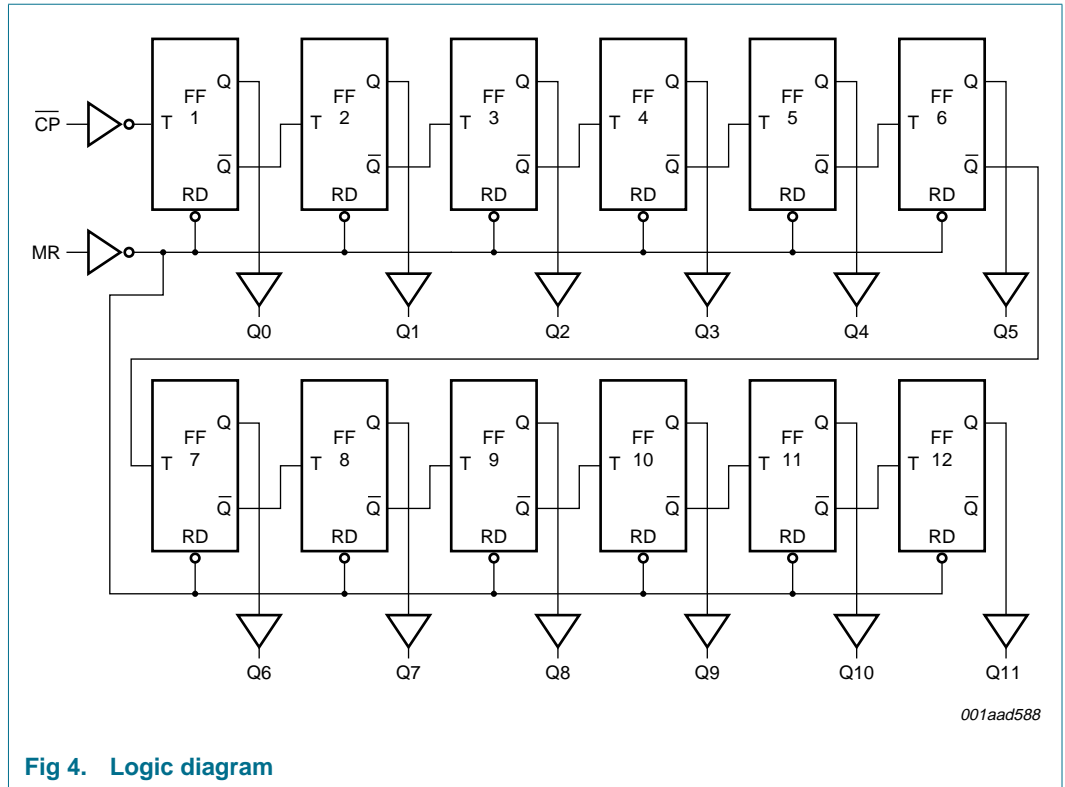
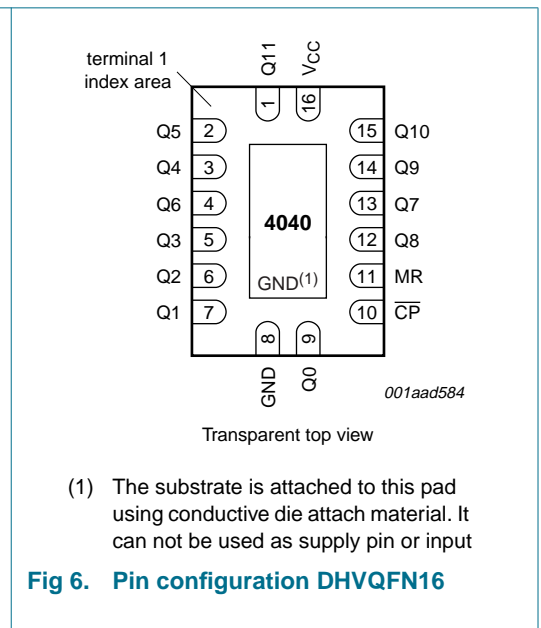
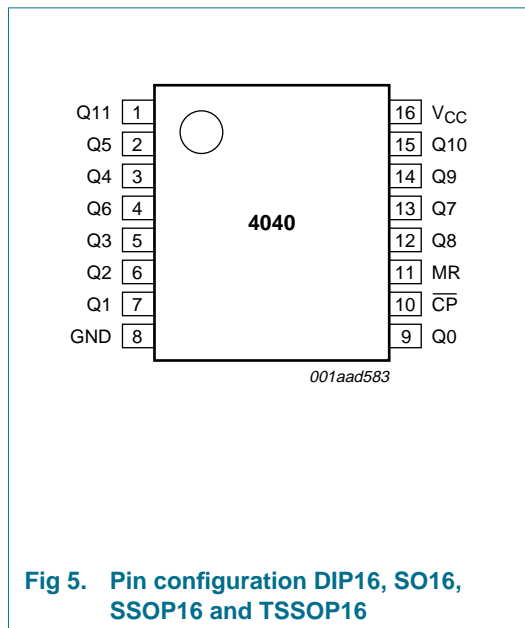


Fig 3. IEC logic symbol



## 7. Pinning information

### 7.1 Pinning



## 7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
Q11	1	output 11
Q5	2	output 5
Q4	3	output 4
Q6	4	output 6
Q3	5	output 3
Q2	6	output 2
Q1	7	output 1
GND	8	ground (0 V)
Q0	9	output 0
$\overline{\text{CP}}$	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
Q8	12	output 8
Q7	13	output 7
Q9	14	output 9
Q10	15	output 10
V <sub>CC</sub>	16	positive supply voltage

## 8. Functional description

### 8.1 Function table

Table 4: Function table

Input		Output
CP	MR	Q0 to Q11
↑	L	no change
↓	L	count
X	H	L

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 ↑ = LOW-to-HIGH clock transition;  
 ↓ = HIGH-to-LOW clock transition.

8.2 Timing diagram

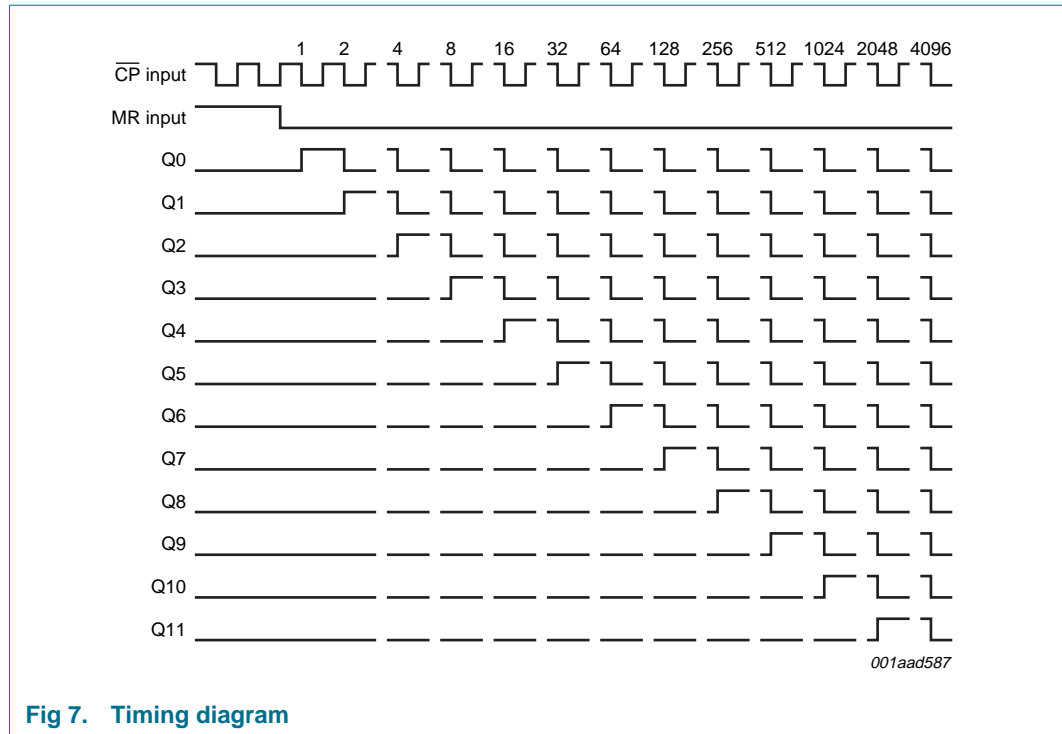


Fig 7. Timing diagram

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	quiescent supply current		-	$\pm 50$	mA
$I_{GND}$	ground current		-	$\pm 50$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$	[1]		
	DIP16 package		-	750	mW
	SO16, SSOP16, TSSOP16 and DHVQFN16 packages		-	500	mW

[1] For DIP16 packages: above 70 °C,  $P_{tot}$  derates linearly with 12 mW/K.  
 For SO16, SSOP16, TSSOP16 and DHVQFN16 packages, above 70 °C,  $P_{tot}$  derates linearly with 8 mW/K.

## 10. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>type 74HC4040</b>						
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	see <a href="#">Section 11</a> and <a href="#">12</a> per device	-40	-	+125	°C
$t_r, t_f$	input rise and fall times	except for Schmitt-trigger inputs				
		$V_{CC} = 2.0\text{ V}$	-	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	400	ns
<b>type 74HCT4040</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	see <a href="#">Section 11</a> and <a href="#">12</a> per device	-40	-	+125	°C
$t_r, t_f$	input rise and fall times	except for Schmitt-trigger inputs				
		$V_{CC} = 2.0\text{ V}$	-	-	-	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	-	ns

## 11. Static characteristics

**Table 7: Static characteristics for 74HC4040**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	V
	$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	5.81	-	V	

**Table 7: Static characteristics for 74HC4040 ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	0.1	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	μA
C <sub>I</sub>	input capacitance		-	3.5	-	pF
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.84	-	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V;	5.34	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.33	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	80.0	μA
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V



**Table 7: Static characteristics for 74HC4040 ...continued**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.7	-	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V;	5.2	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	-	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	160.0	µA

**Table 8: Static characteristics for 74HCT4040**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	0.1	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	µA
ΔI <sub>CC</sub>	additional quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A				
		$\overline{CP}$	-	85	306	µA
		MR	-	110	396	µA
C <sub>I</sub>	input capacitance		-	3.5	-	pF
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	V

**Table 8: Static characteristics for 74HCT4040 ...continued**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	-	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.84	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.33	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	80.0	$\mu\text{A}$
$\Delta I_{CC}$	additional quiescent supply current	$V_I = V_{CC} - 2.1 \text{ V}; V_{CC} = 4.5 \text{ V}$ to $5.5 \text{ V}; I_O = 0 \text{ A}$				
		$\overline{CP}$	-	-	383	$\mu\text{A}$
		MR	-	-	495	$\mu\text{A}$
<b><math>T_{amb} = -40 \text{ }^\circ\text{C}</math> to <math>+125 \text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to $5.5 \text{ V}$	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to $5.5 \text{ V}$	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	-	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.7	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.4	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	160.0	$\mu\text{A}$
$\Delta I_{CC}$	additional quiescent supply current	$V_I = V_{CC} - 2.1 \text{ V}; V_{CC} = 4.5 \text{ V}$ to $5.5 \text{ V}; I_O = 0 \text{ A}$				
		$\overline{CP}$	-	-	417	$\mu\text{A}$
		MR	-	-	539	$\mu\text{A}$

## 12. Dynamic characteristics

**Table 9: Dynamic characteristics for type 74HC4040**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ . For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$t_{PHL}, t_{PLH}$	propagation delay $\overline{CP}$ to $Q_0$	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	-	47	150	ns
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	17	30	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	14	-	ns
	propagation delay $Q_n$ to $Q_{n+1}$	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	-	28	100	ns
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	10	20	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	8	-	ns
$t_{PHL}$	propagation delay MR to $Q_n$	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	-	61	185	ns
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	22	37	ns
		$V_{CC} = 6.0\text{ V}$ ; $C_L = 50\text{ pF}$	-	18	31	ns
$t_{THL}, t_{TLH}$	output transition time	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	-	19	75	ns
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	7	15	ns
		$V_{CC} = 6.0\text{ V}$ ; $C_L = 50\text{ pF}$	-	6	13	ns
$t_W$	clock pulse width HIGH or LOW	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	80	14	-	ns
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	16	5	-	ns
	master reset pulse width; HIGH	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	80	22	-	ns
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	16	8	-	ns
$t_{rec}$	recovery time MR to $\overline{CP}$	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	50	8	-	ns
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	10	3	-	ns
		$V_{CC} = 6.0\text{ V}$ ; $C_L = 50\text{ pF}$	9	2	-	ns
$f_{max}$	maximum operating frequency	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0\text{ V}$ ; $C_L = 50\text{ pF}$	6.0	27	-	MHz
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	30	82	-	MHz
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	90	-	MHz
$C_{PD}$	power dissipation capacitance		-	20	-	pF

**Table 9: Dynamic characteristics for type 74HC4040 ...continued** $GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ . For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b><math>T_{\text{amb}} = -40\text{ °C to }+85\text{ °C}</math></b>							
$t_{\text{PHL}}, t_{\text{PLH}}$	propagation delay $\overline{\text{CP}}$ to Q0	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	190	ns	
		$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	38	ns	
		$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	33	ns	
	propagation delay Qn to Qn+1	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	125	ns	
$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$		-	-	25	ns		
	$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	21	ns		
$t_{\text{PHL}}$	propagation delay MR to Qn	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	230	ns	
		$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	46	ns	
		$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	39	ns	
$t_{\text{THL}}, t_{\text{TLH}}$	output transition time	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	95	ns	
		$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	19	ns	
		$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	-	-	16	ns	
$t_{\text{W}}$	clock pulse width HIGH or LOW	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	100	-	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	20	-	-	ns	
		$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	17	-	-	ns	
	master reset pulse width; HIGH	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	100	-	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	20	-	-	ns	
		$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	17	-	-	ns	
	$t_{\text{rec}}$	recovery time MR to $\overline{\text{CP}}$	see <a href="#">Figure 8</a>				
			$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	65	-	-	ns
$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$			13	-	-	ns	
$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$			11	-	-	ns	
$f_{\text{max}}$	maximum operating frequency	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	4.8	-	-	MHz	
		$V_{\text{CC}} = 4.5\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	24	-	-	MHz	
		$V_{\text{CC}} = 6.0\text{ V}$ ; $C_{\text{L}} = 50\text{ pF}$	28	-	-	MHz	

**Table 9: Dynamic characteristics for type 74HC4040 ...continued**GND = 0 V;  $t_r = t_f = 6$  ns. For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay $\overline{CP}$ to Q0	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	-	-	225	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	-	-	45	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	-	-	38	ns
	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	-	-	150	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	-	-	30	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	-	-	26	ns
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	-	-	280	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	-	-	56	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	-	-	48	ns
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	-	-	110	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	-	-	22	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	-	-	19	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	120	-	-	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	24	-	-	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	20	-	-	ns
	master reset pulse width; HIGH	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	120	-	-	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	24	-	-	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	20	-	-	ns
t <sub>rec</sub>	recovery time MR to $\overline{CP}$	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	75	-	-	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	15	-	-	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	13	-	-	ns
f <sub>max</sub>	maximum operating frequency	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	4.0	-	-	MHz
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	20	-	-	MHz
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	24	-	-	MHz

[1] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;f<sub>o</sub> = output frequency in MHz;Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs;C<sub>L</sub> = output load capacitance in pF;V<sub>CC</sub> = supply voltage in V.

**Table 10: Dynamic characteristics for type 74HCT4040**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ . For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$t_{PHL}, t_{PLH}$	propagation delay $\overline{CP}$ to Q0	see <a href="#">Figure 8</a>				
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	19	40	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	16	-	ns
	propagation delay Qn to Qn+1	see <a href="#">Figure 8</a>				
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	10	20	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	8	-	ns
$t_{PHL}$	propagation delay MR to Qn	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	-	23	45	ns
$t_{THL}, t_{TLH}$	output transition time	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	-	7	15	ns
$t_W$	clock pulse width HIGH or LOW	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	16	7	-	ns
	master reset pulse width; HIGH	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	16	6	-	ns
$t_{rec}$	recovery time MR to $\overline{CP}$	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	10	2	-	ns
$f_{max}$	maximum operating frequency	see <a href="#">Figure 8</a>				
		$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$	30	72	-	MHz
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	79	-	MHz
$C_{PD}$	power dissipation capacitance per package		[1] -	20	-	pF
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>						
$t_{PHL}, t_{PLH}$	propagation delay $\overline{CP}$ to Q0	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	-	-	50	ns
	propagation delay Qn to Qn+1	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	-	-	25	ns
$t_{PHL}$	propagation delay MR to Qn	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	-	-	56	ns
$t_{THL}, t_{TLH}$	output transition time	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	-	-	19	ns
$t_W$	clock pulse width HIGH or LOW	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	20	-	-	ns
	master reset pulse width; HIGH	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	20	-	-	ns
$t_{rec}$	recovery time MR to $\overline{CP}$	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	13	-	-	ns
$f_{max}$	maximum operating frequency	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	24	-	-	MHz
<b><math>T_{amb} = -40\text{ °C to }+125\text{ °C}</math></b>						
$t_{PHL}, t_{PLH}$	propagation delay $\overline{CP}$ to Q0	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a> ;	-	-	60	ns
	propagation delay Qn to Qn+1	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a>	-	-	30	ns

**Table 10: Dynamic characteristics for type 74HCT4040 ...continued**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ . For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$	propagation delay MR to Qn	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a>	-	-	68	ns
$t_{THL}, t_{TLH}$	output transition time	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a>	-	-	22	ns
$t_W$	clock pulse width HIGH or LOW	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a>	24	-	-	ns
	master reset pulse width; HIGH	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a>	24	-	-	ns
$t_{rec}$	recovery time MR to $\overline{CP}$	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a>	15	-	-	ns
$f_{max}$	maximum operating frequency	$V_{CC} = 4.5\text{ V}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 8</a>	20	-	-	MHz

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

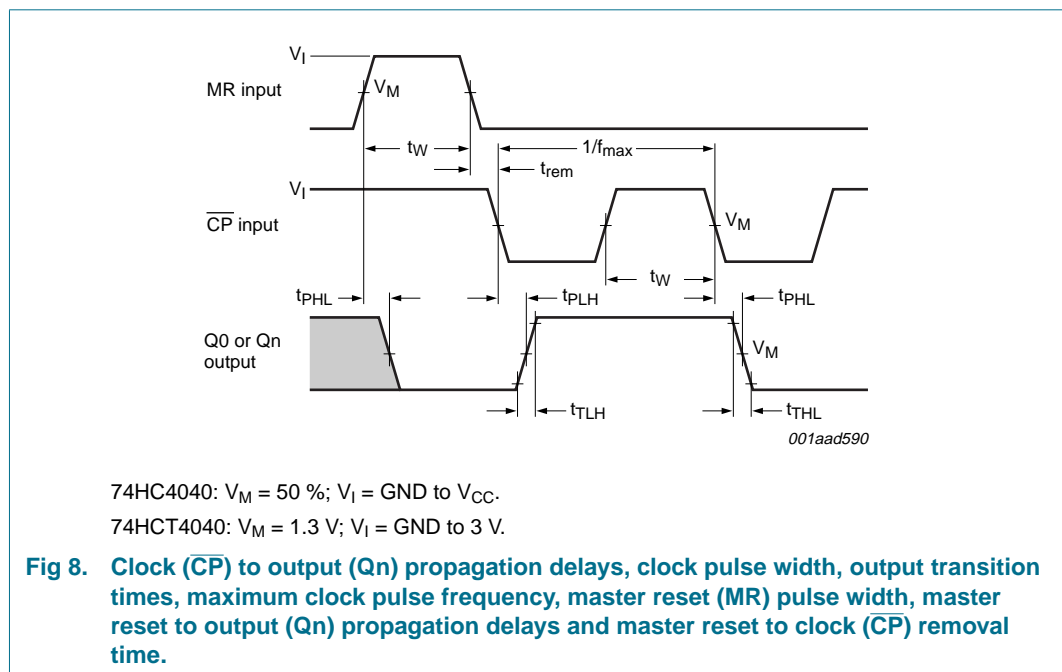
$f_o$  = output frequency in MHz;

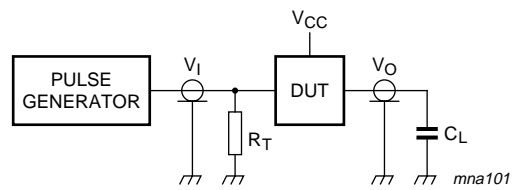
$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V.

### 13. Waveforms





Definitions for test circuit:

$C_L$  = load capacitance including jig and probe capacitance (See [Section 12](#) for the value).

$R_T$  = termination resistance should be equal to output impedance  $Z_O$  of the pulse generator.

**Fig 9. Test circuit**



14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

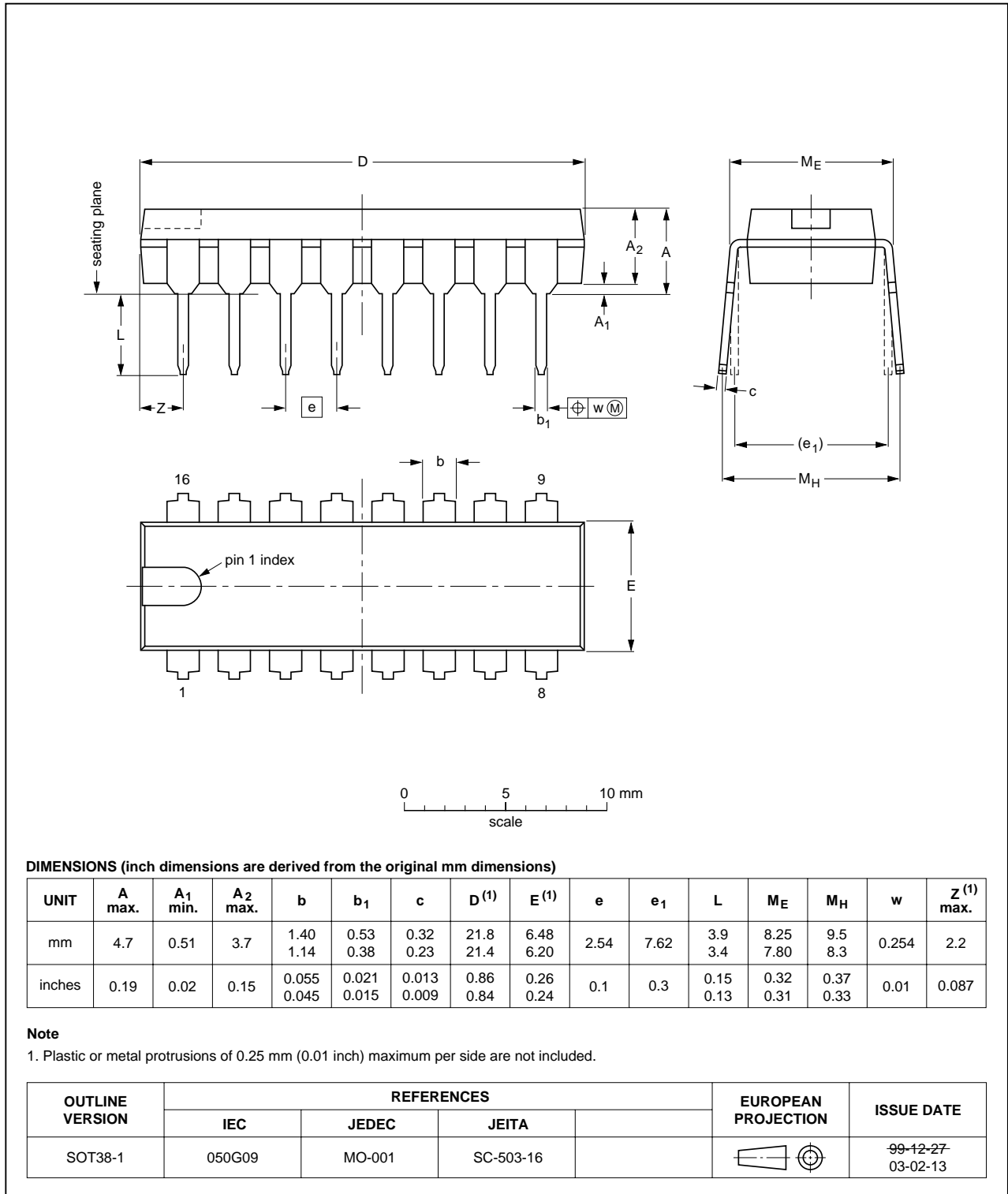


Fig 10. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

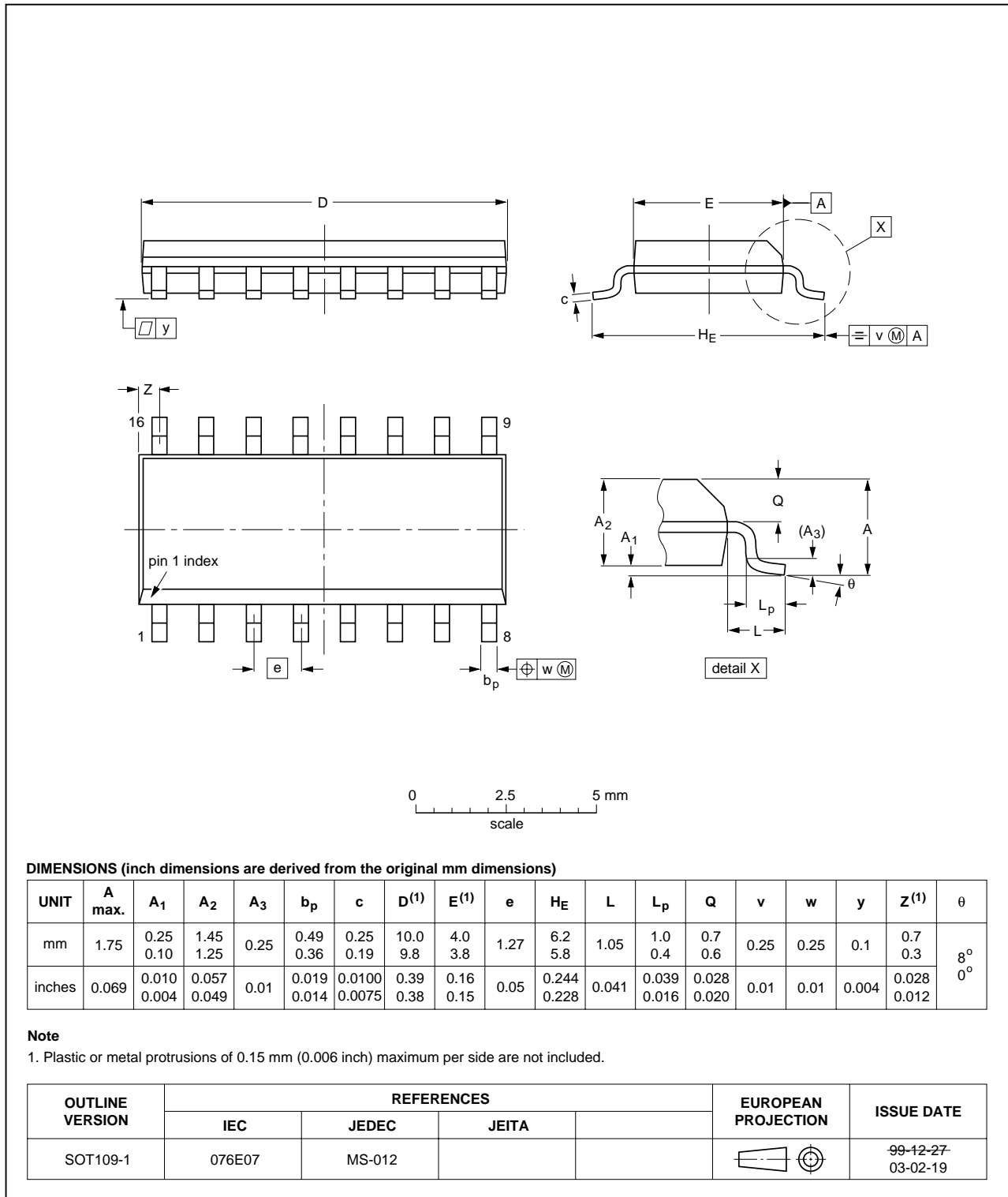


Fig 11. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

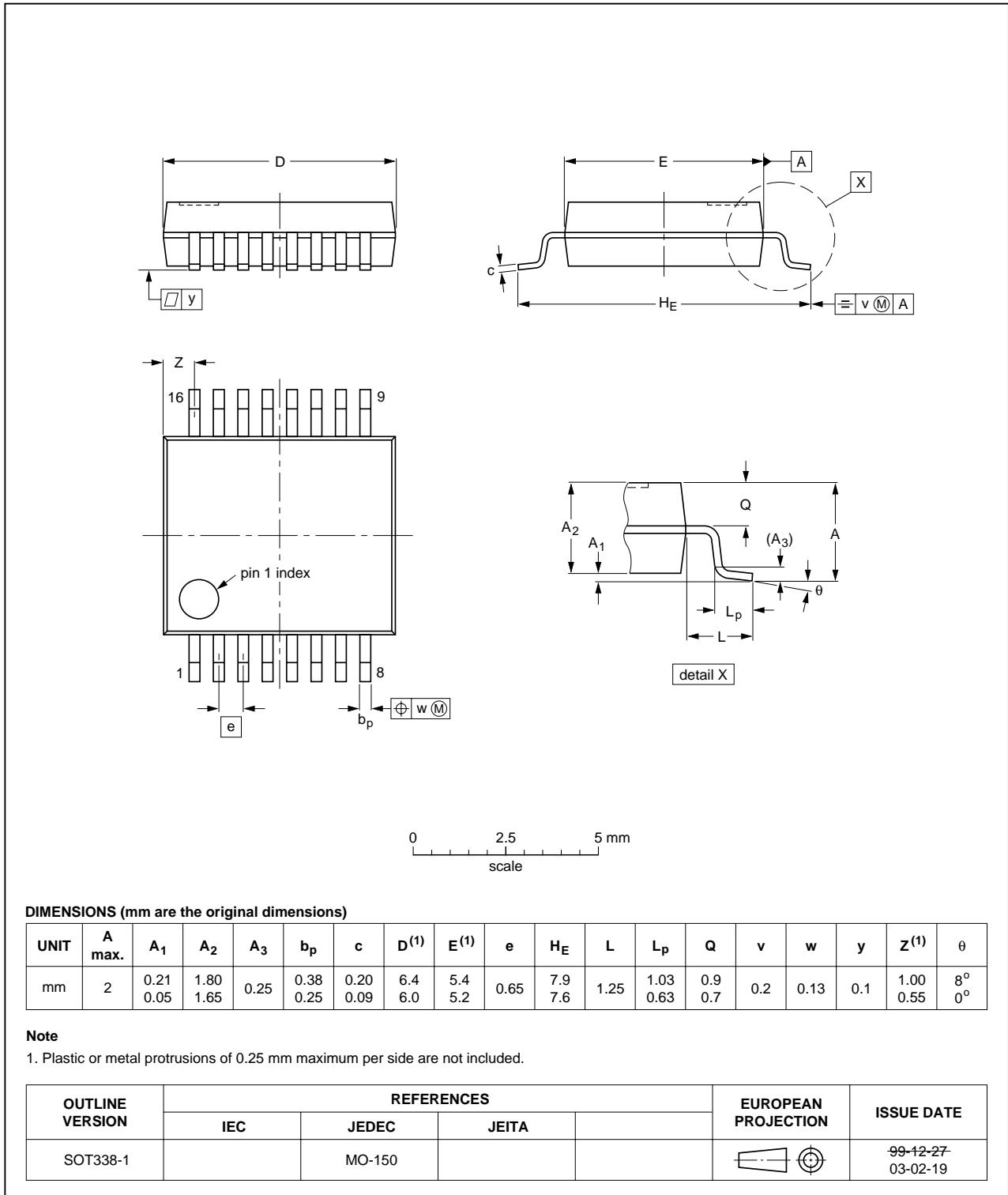


Fig 12. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

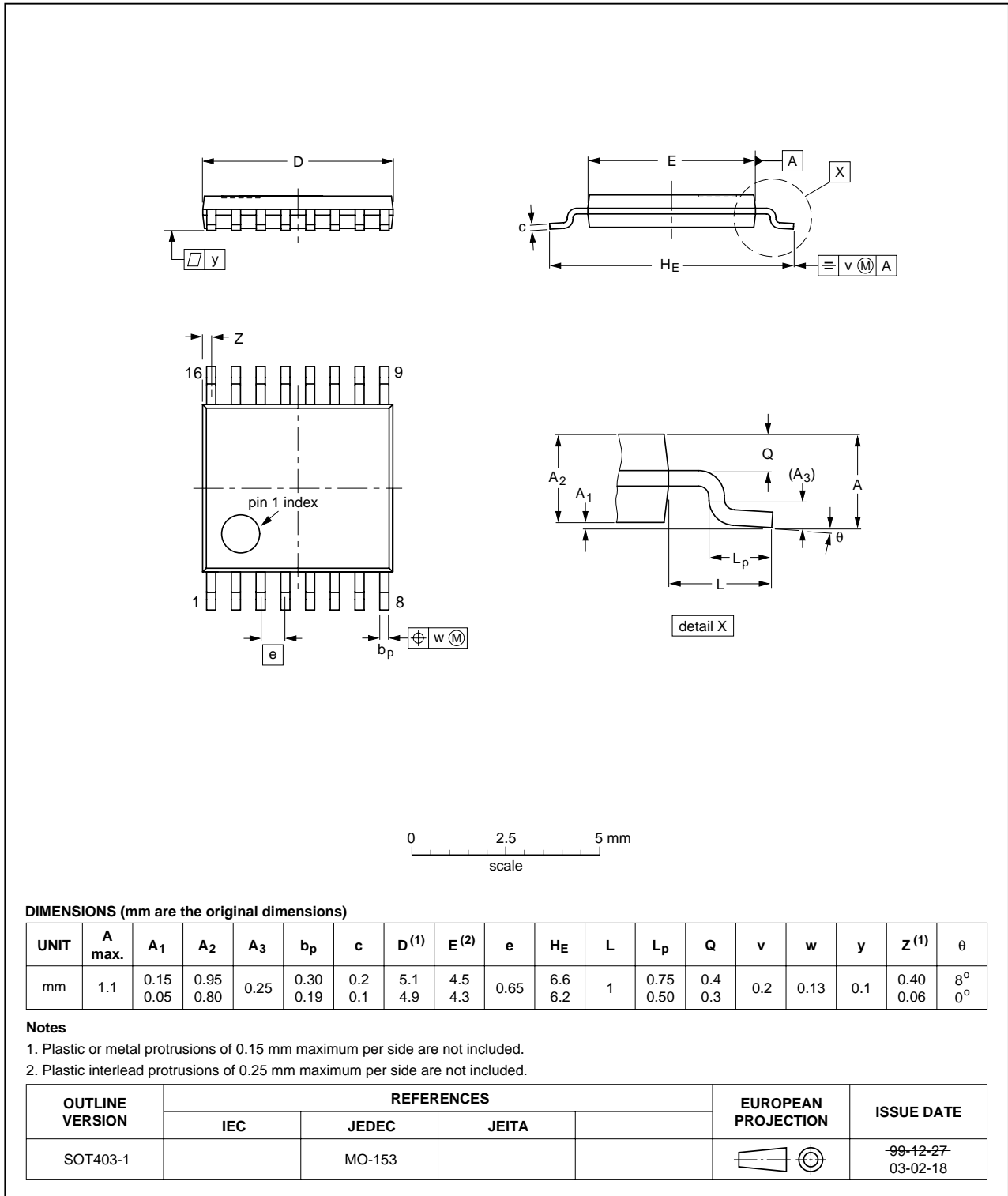


Fig 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

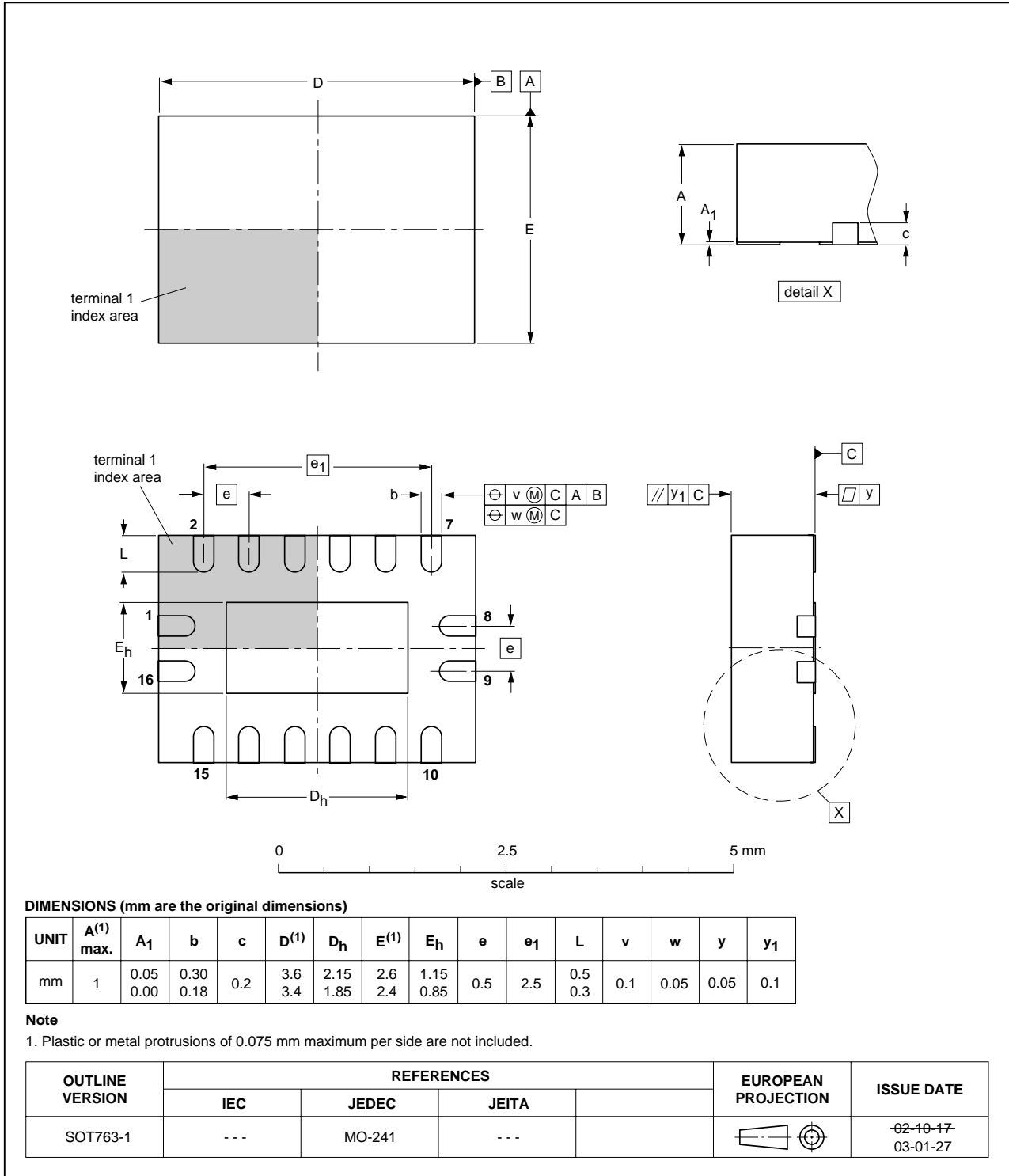


Fig 14. Package outline SOT763-1 (DHVQFN16)

## 15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT4040_3	20050914	Product data sheet	-	-	74HC_HCT4040_CNV_2
Modifications: <ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors</li> <li>• Reference to family specifications is replaced by the actual information: <a href="#">Section 5 "Ordering information"</a>, <a href="#">Section 7 "Pinning information"</a>, <a href="#">Section 9 "Limiting values"</a>, <a href="#">Section 10 "Recommended operating conditions"</a>, <a href="#">Section 11 "Static characteristics"</a>, <a href="#">Figure 9 "Test circuit"</a></li> <li>• <a href="#">Section 14 "Package outline"</a> (DHVQFN16) added</li> </ul>					
74HC_HCT4040_CNV_2	19901231	Product specification	-	-	-

## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 17. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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