SILEGO

GreenPAK
Programmable Mixed Signal Array

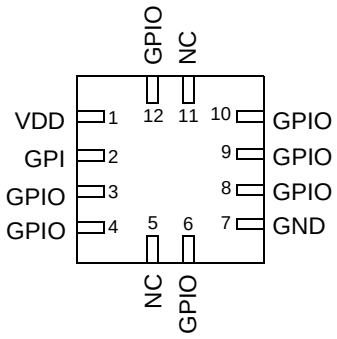
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macro Cells
- 1.8 V (±5%) to 5 V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free 12-pin STQFN: 1.6 x 1.6 x 0.55 mm, 0.4 mm pitch

Applications

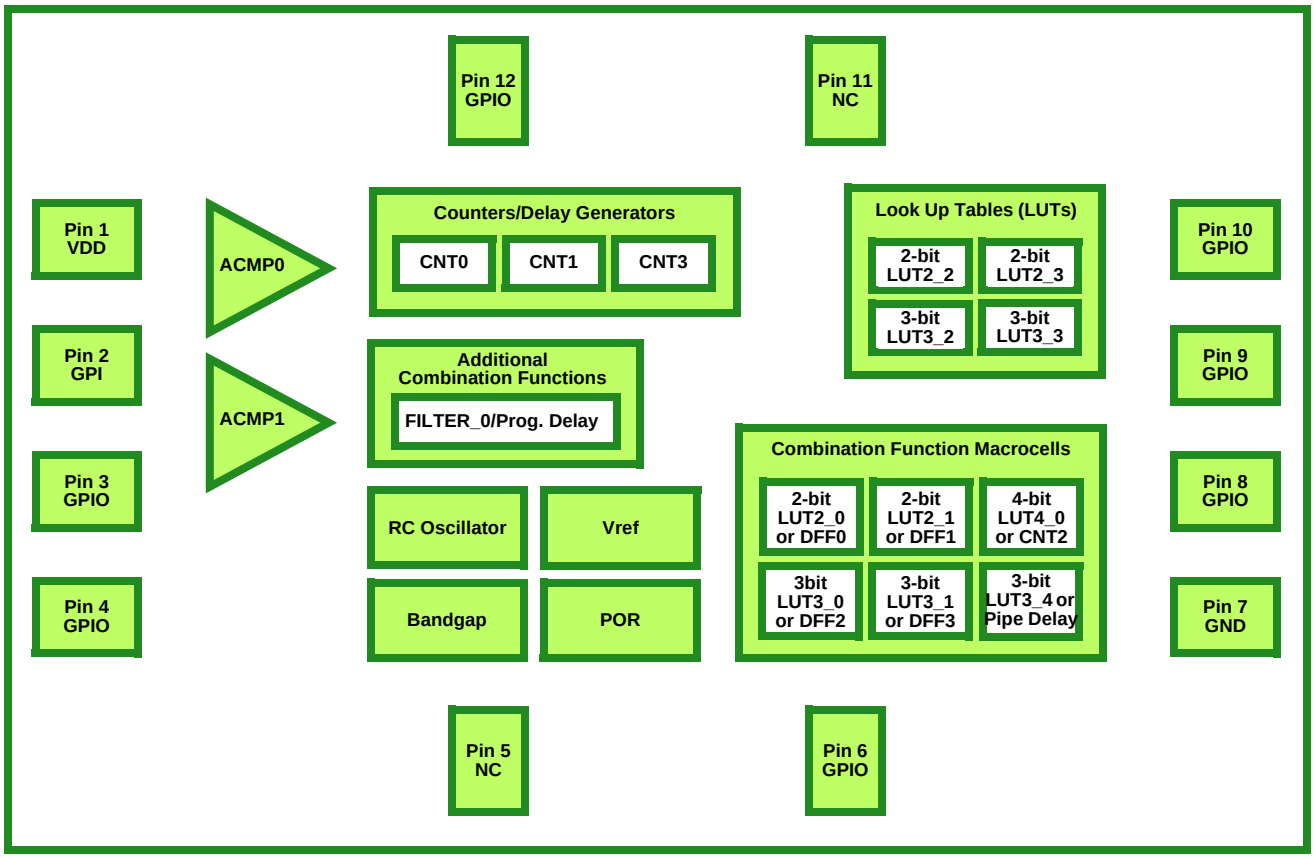
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



STQFN-12
(Top View)

Block Diagram



Preliminary

1.0 Overview

The SLG46110 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macro cells of the SLG46110. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macro cells in the device include the following:

- Two Analog Comparators (ACMP)
- Four Combinatorial Look Up Tables (LUTs)
  - Two 2-bit LUTs
  - Two 3-bit LUTs
- Six Combination Function Macro cell
  - Two Selectable FF/Latch or 2-bit LUTs
  - Two Selectable FF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage / 2 output
  - One Selectable Counter/Delay or 4-bit LUT
  - One Programmable Delay / Deglitch Filter
- Three Counter / Delay Generators (CNT/DLY)
  - Three 8-bit counter/delays with external clock/reset
- Four D Flip-Flop / Latches (DFF) (Part of Combination Function Macrocell)
- Pipe Delay – 8 stage/2 output (Part of Combination Function Macrocell)
- One Bandgap
- RC Oscillator (RC OSC)

2.0 Pin Description

2.1 Functional and Programming Pin Description

Pin #	Pin Name	Function	Programming Function
1	VDD	Power Supply	Power Supply
2	GPI	General Purpose Input	V_{PP} (Programming Voltage)
3	GPIO	General Purpose I/O or Analog Comparator 0 (+)	Programming ID Pin
4	GPIO	General Purpose I/O or Analog Comparator 0 (-)	N/A
5	NC	No Connect	N/A
6	GPIO	General Purpose I/O or Analog Comparator 1 (+) with OE	N/A
7	GND	Ground	N/A
8	GPIO	General Purpose I/O	Programming Mode Control
9	GPIO	General Purpose I/O or POR Output	Programming SDIO Pin
10	GPIO	General Purpose I/O with OE and Vref output	Programming SRDWB Pin
11	NC	No Connect	N/A
12	GPIO	General Purpose I/O or External Clock Input	Programming SCL Pin

3.0 User Programmability

The SLG46110 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the I/O Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Silego to integrate into a production process.

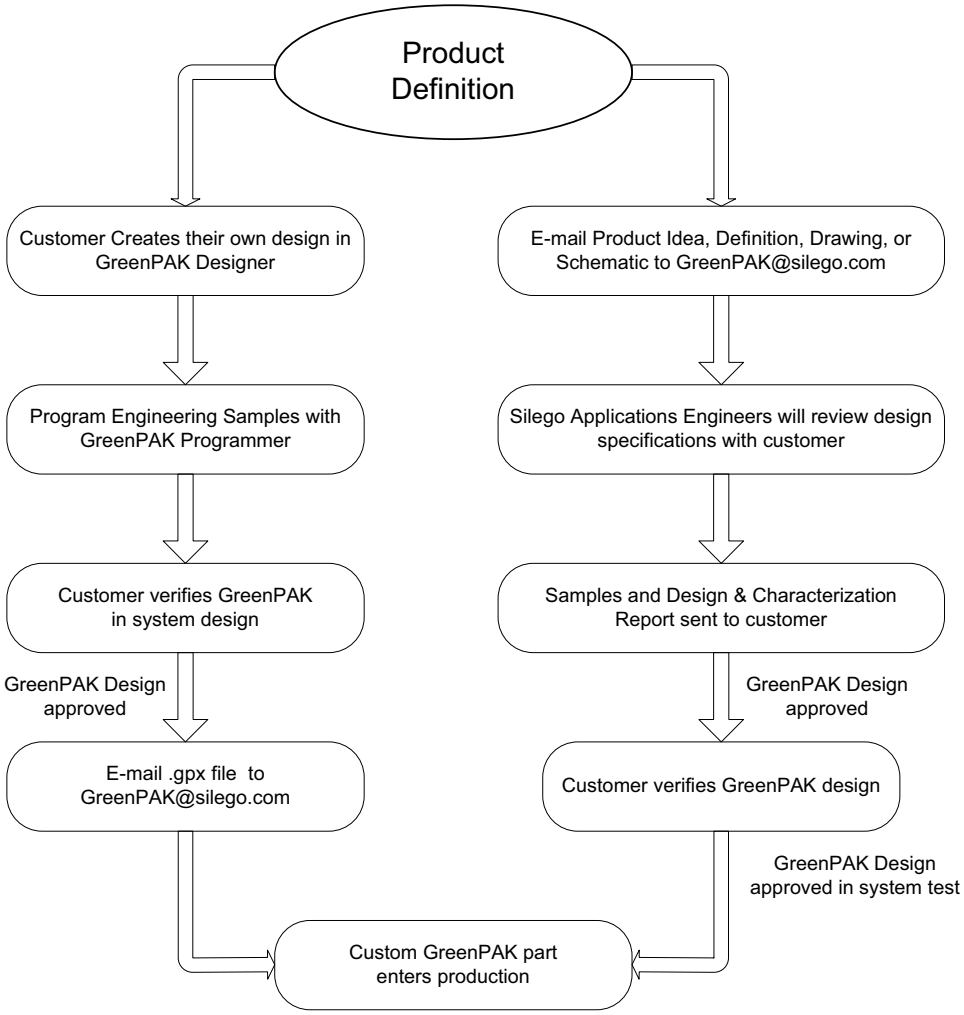


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46110V	12-pin STQFN
SLG46110VTR	12-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	-0.3	7	V
Current at Input Pin	-1.0	1.0	mA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V
Moisture Sensitivity Level	1		

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.5	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{AIR}	Analog Input Voltage Range	ACMP with voltage gain divider	0	--	V_{DD}	V
		ACMP without voltage gain divider	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD}	V
		Low-Level Logic Input	0.980	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN} = 1.8 V	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0 V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100 µA, 1X Driver	1.680	1.790	--	V
		PMOS OD, I_{OH} = 100 µA, 1X Driver	1.680	1.790	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Driver	1.702	1.795	--	V
		PMOS OD, I_{OH} = 100 µA, 2X Driver	1.702	1.795	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100 µA, 1X Driver	--	0.020	0.030	V
		Push-Pull, I_{OL} = 100 µA, 2X Driver	--	0.010	0.020	V
		Open Drain, I_{OL} = 100 µA, 1X Driver	--	0.010	0.020	V
		Open Drain, I_{OL} = 100 µA, 2X Driver	--	0.010	0.010	V
I_{OH}	HIGH-Level Output Current	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Driver	1.043	1.400	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1X Driver	1.036	1.407	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Driver	2.150	2.707	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2X Driver	2.200	2.719	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.15 V, 1X Driver	0.76	1.339	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Driver	1.52	2.661	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Driver	1.53	2.669	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Driver	3.06	5.133	--	mA
T_{SU}	Startup Time	from VDD rising past 1.6 V	--	1	--	ms

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.75	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{AIR}	Analog Input Voltage Range	ACMP with voltage gain divider	0	--	V_{DD}	V
		ACMP without voltage gain divider	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V_{DD}	V
		Low-Level Logic Input	1.130	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN} = 3.3 V	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0 V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull; I_{OH} = 3 mA, 1X Driver	2.710	3.090	--	V
		PMOS OD; I_{OH} = 3 mA, 1X Driver	2.730	3.090	--	V
		Push-Pull; I_{OH} = 3 mA, 2X Driver	2.870	3.190	--	V
		PMOS OD; I_{OH} = 3 mA, 2X Driver	2.870	3.190	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull; I_{OL}= 3 mA, 1X Driver	--	0.180	0.28	V
		Push-Pull; I_{OL} = 3 mA, 2X Driver	--	0.090	0.13	V
		Open Drain; I_{OL} = 3 mA, 1X Driver	--	0.090	0.13	V
		Open Drain; I_{OL} = 3 mA, 2X Driver	--	0.050	0.07	V
I_{OH}	HIGH-Level Output Current	Push-Pull; V_{OH} = 2.4 V, 1X Driver	5.830	10.184	--	mA
		PMOS OD; V_{OH} = 2.4 V, 1X Driver	6.010	10.206	--	mA
		Push-Pull; V_{OH} = 2.4 V, 2X Driver	11.264	19.655	--	mA
		PMOS OD; V_{OH} = 2.4 V, 2X Driver	12.010	19.703	--	mA
I_{OL}	LOW-Level Output Current	Push-Pull; V_{OL} = 0.4 V, 1X Driver	4.06	6.440	--	mA
		Push-Pull; V_{OL} = 0.4 V, 2X Driver	8.13	12.358	--	mA
		Open Drain; V_{OL} = 0.4 V, 1X Driver	8.13	12.405	--	mA
		Open Drain; V_{OL} = 0.4 V, 2X Driver	16.26	22.897	--	mA
T_{SU}	Startup Time	from VDD rising past 1.6 V	--	1	--	ms

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	1.0	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{AIR}	Analog Input Voltage Range	ACMP with voltage gain divider	0	--	V_{DD}	V
		ACMP without voltage gain divider	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.640	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.160	--	V_{DD}	V
		Low-Level Logic Input	1.230	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN} = 5 V	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0 V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 5 mA, 1X Driver	4.150	4.730	--	V
		PMOS OD, I_{OH} = 5 mA, 1X Driver	4.180	4.740	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Driver	4.300	4.860	--	V
		PMOS OD, I_{OH} = 5 mA, 2X Driver	4.330	4.860	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 5 mA, 1X Driver	--	0.230	0.330	V
		Push-Pull, I_{OL} =5 mA, 2X Driver	--	0.120	0.160	V
		Open Drain, I_{OL} = 5 mA, 1X Driver	--	0.120	0.160	V
		Open Drain, I_{OL} = 5 mA, 2X Driver	--	0.070	0.090	V
I_{OH}	HIGH-Level Output Current	Push-Pull, V_{OH} = 2.4 V, 1X Driver	21.808	29.099	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Driver	21.980	29.170	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Driver	40.598	56.078	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Driver	43.092	56.338	--	mA
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.4 V, 1X Driver	6.010	9.730	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Driver	11.585	19.460	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Driver	11.756	19.460	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Driver	19.120	35.621	--	mA
T_{SU}	Startup Time	from VDD rising past 1.6 V	--	1	--	ms

6.0 Summary of Macro Cell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV

6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pin (Pin 10)

6.5 Combinational Logic Look Up Tables (LUTs – 4 total)

- Two 2-bit Lookup Tables
- Two 3-bit Lookup Tables

6.6 Combination Function Macrocells (7 total)

- Two Selectable FF/Latch or 2-bit LUTs
- Two Selectable FF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- One Selectable CNT/DLY or 4-bit LUT
- One Programmable Delay or Deglitch Filter

6.7 Delays/Counters (3 total)

- Three 8-bit delays/counters with external clock/reset: Range 1-255 clock cycles

6.8 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1-8 stage selectable outputs.

6.9 Programmable Delay

- 125 ns/250 ns/375 ns/500 ns @ 3.3 V
- Includes Edge Detection function

6.10 Additional Logic Functions (Part of Combination Function Macrocell)

- One Deglitch filter macro cell

6.11 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First Stage Clock pre=divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider control with two outputs, OUT0 and OUT1 (8): selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

7.0 I/O Pins

The SLG46110 has a total of 8 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Normal Mode pin definitions are as follows:

- Pin 1: V_{DD} Power Supply
- Pin 2: General Purpose Input
- Pin 3: General Purpose I/O or Analog Comparator 0 (+)
- Pin 4: General Purpose I/O or Analog Comparator 0 (-)
- Pin 5: No Connect
- Pin 6: General Purpose I/O or Analog Comparator 1 (+) with OE
- Pin 7: Ground
- Pin 8: General Purpose I/O
- Pin 9: General Purpose I/O or POR Output
- Pin 10: General Purpose I/O with OE and Vref Output
- Pin 11: No Connect
- Pin 12: General Purpose I/O or External Clock Input

Programming Mode pin definitions are as follows:

- Pin 1: V_{DD} Power Supply
- Pin 2: V_{PP} Programming Voltage
- Pin 3: Programming ID Pin
- Pin 7: Ground
- Pin 8: Programming Mode Control
- Pin 9: Programming SDIO Pin
- Pin 10: Programming SRDWB Pin
- Pin 12: Programming SCL Pin

Of the 8 user defined I/O pins on the SLG46110, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input. Pins 3, 4, and 6 can also be configured to serve as analog inputs to the on-chip comparators.

7.2 Output Modes

Pins 3, 4, 6, 8, 9, 10, and 12 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 1. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	reg <380:379>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	reg <382:381>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 2. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	reg <385:383>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 3 Pull Up/Down Resistor Value Selection	reg <387:386>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <388>	0: Pull Down Resistor 1: Pull Up Resistor
PIN3 Driver Strength Selection	reg <389>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 3. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control	reg <392:390>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 4 Pull Up/Down Resistor Value Selection	reg <394:393>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	reg <395>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 4 Driver Strength Selection	reg <396>	0: 1X 1: 2X

7.4.4 PIN 6 Register Settings

Table 4. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control (sig_PIN6_oe=0)	reg <398:397>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input
PIN 6 Mode Control (sig_PIN6_oe =1)	reg <400:399>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 6 Pull Up/Down Resistor Value Selection	reg <402:401>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	reg <403>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.5 PIN 8 Register Settings

Table 5. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	reg <406:404>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 8 Pull Up/Down Resistor Value Selection	reg <408:407>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	reg <409>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <410>	0: 1X 1: 2X

7.4.6 PIN 9 Register Settings

Table 6. PIN 9 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 9 Mode Control	reg <413:411>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 9 Pull Up/Down Resistor Value Selection	reg <415:414>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 9 Pull Up/Down Resistor Selection	reg <416>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <417>	0: 1X 1: 2X

7.4.7 PIN 10 Register Settings

Table 7. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control (sig_PIN10_oe =0)	reg <419:418>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input / Output
PIN 10 Mode Control (sig_PIN10_oe =1)	reg <419:418>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 10 Pull Up/Down Resistor Value Selection	reg <423:422>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	reg <424>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.8 PIN 12 Register Settings

Table 8. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control	reg <427:425>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 12 Pull Up/Down Resistor Value Selection	reg <429:428>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	reg <430>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 Driver Strength Selection	reg <431>	0: 1X 1: 2X

7.5 GPI IO Structure

7.5.1 GPI IO Structure (for Pin 2)

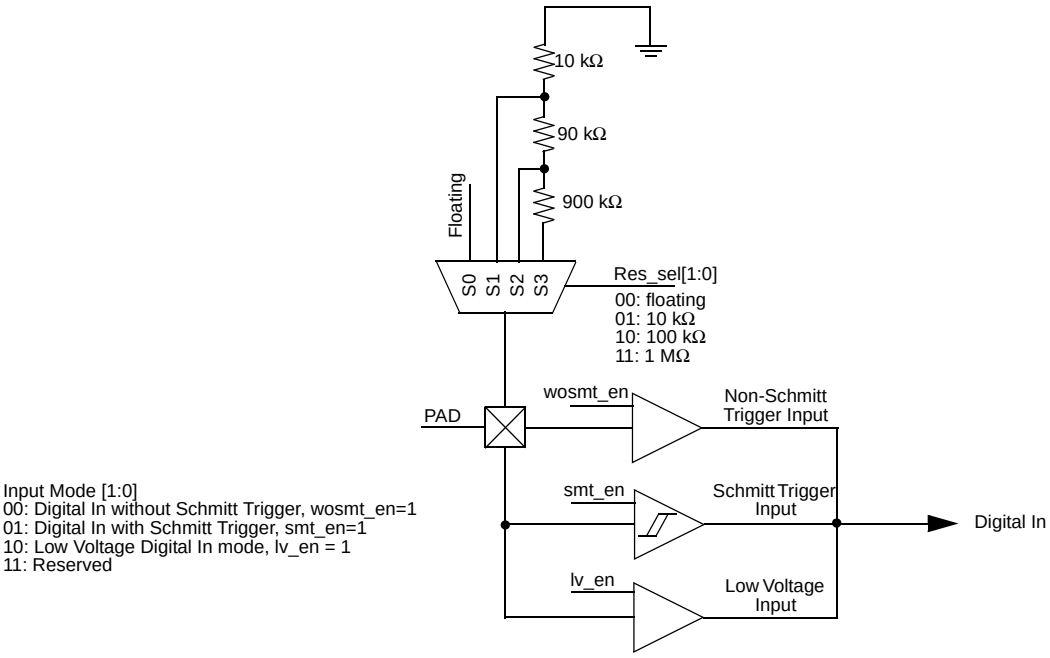


Figure 2. PIN 2 GPI IO Structure Diagram

7.6 Matrix OE IO Structure

7.6.1 Matrix OE IO Structure (for Pin 6, 10)

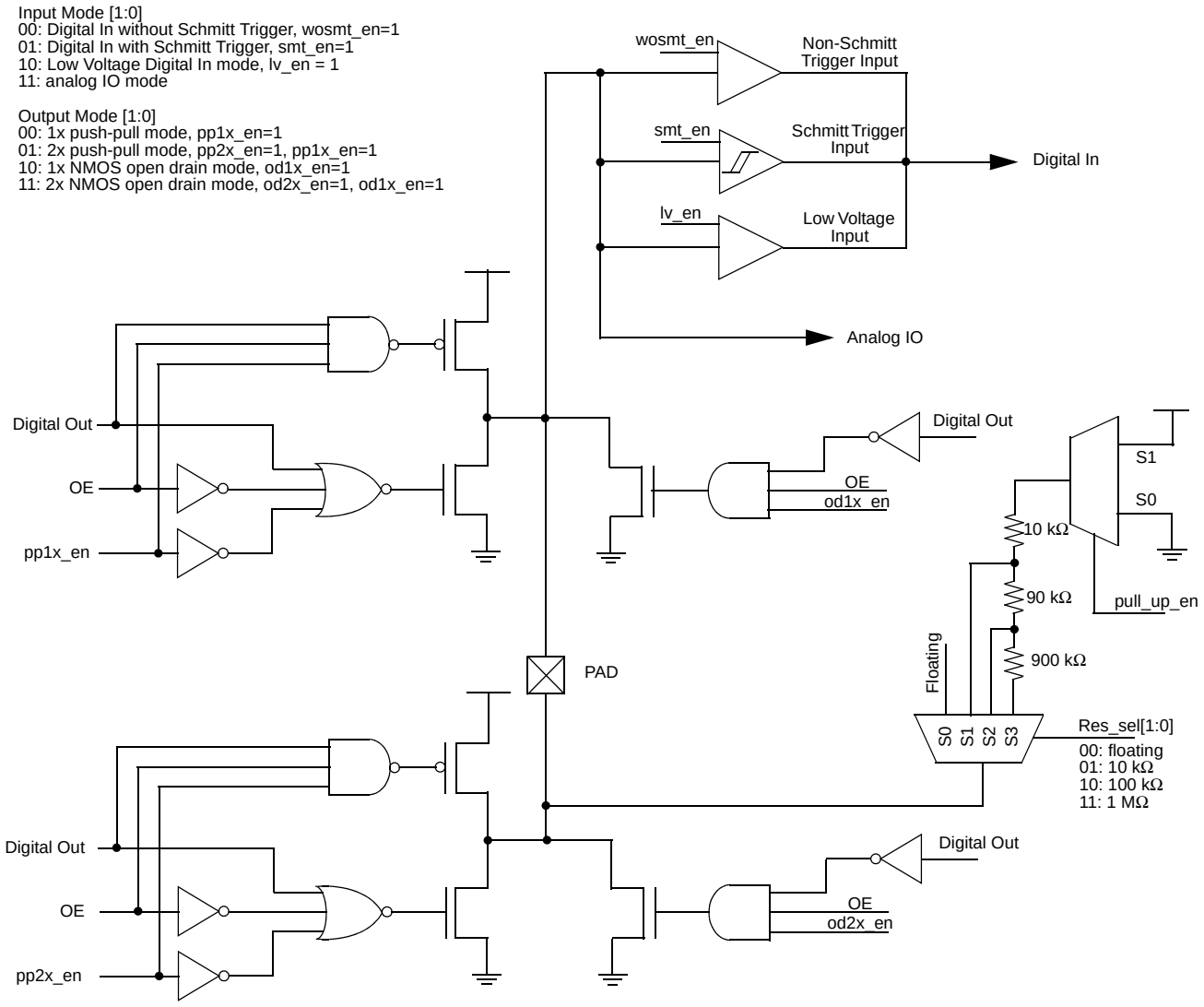


Figure 3. Matrix OE IO Structure Diagram

7.7 Register OE IO Structure

7.7.1 Register OE IO Structure (for Pins 3, 4, 8, 9, 12)

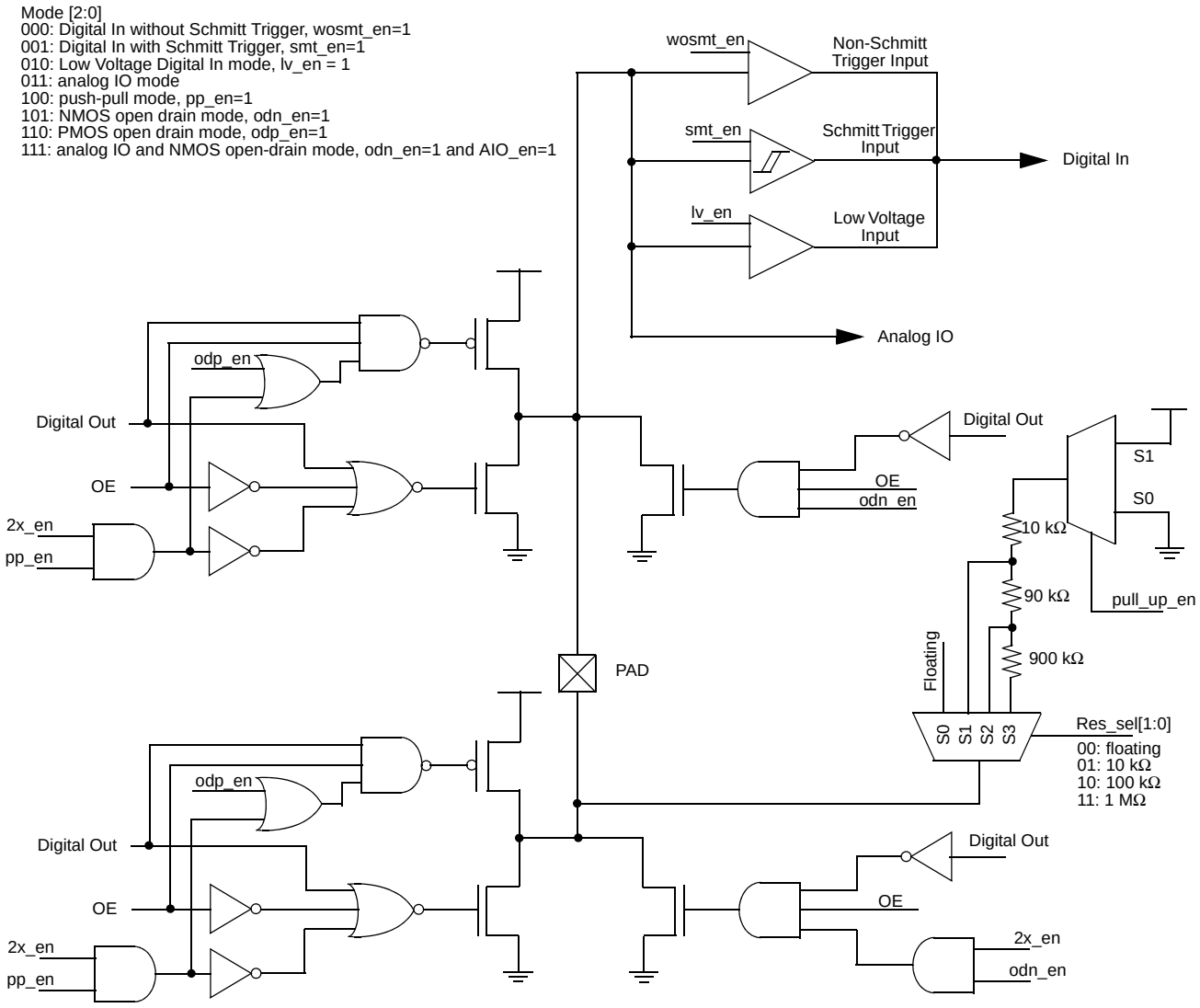


Figure 4. Register OE IO Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46110 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46110 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 512 register bits within the SLG46110 are programmed a fully custom circuit will be created.

The Connection Matrix has 32 inputs and 44 outputs. Each of the 32 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, analog comparators, other digital resources and V_{DD} and V_{SS}. The input to a digital macrocell uses a 5-bit register to select one of these 32 input lines.

For a complete list of the SLG46110’s register table, see Section 15.0 Appendix A - SLG46110 Register Definition.

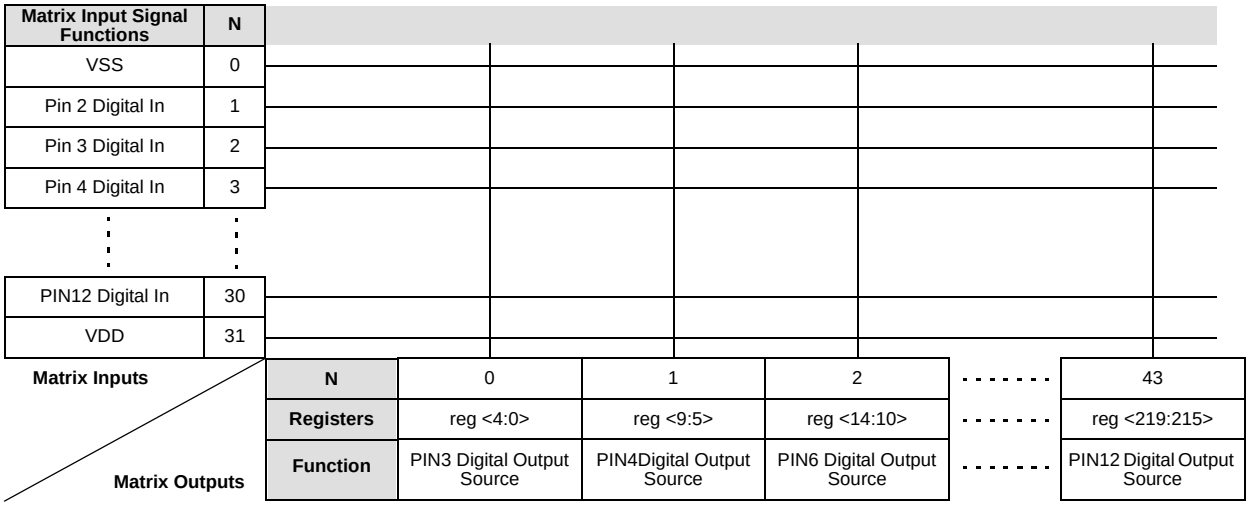


Figure 5. Connection Matrix

8.1 Matrix Input Table

Table 9. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode				
		4	3	2	1	0
0	VSS	0	0	0	0	0
1	pin2 digital Input	0	0	0	0	1
2	pin3 digital Input	0	0	0	1	0
3	pin4 digital Input	0	0	0	1	1
4	pin6 digital Input	0	0	1	0	0
5	LUT2_0 output (DFF/LATCH_0 output)	0	0	1	0	1
6	LUT2_1 output (DFF/LATCH_1 output)	0	0	1	1	0
7	LUT2_2 output	0	0	1	1	1
8	LUT2_3 output	0	1	0	0	0
9	LUT3_0 output (DFF/LATCH_2 output with resetb or seb)	0	1	0	0	1
10	LUT3_1 output (DFF/LATCH_3 output with resetb or seb)	0	1	0	1	0
11	LUT3_2 output	0	1	0	1	1
12	LUT3_3 output	0	1	1	0	0
13	LUT3_4 output(pipe delay ouput0)	0	1	1	0	1
14	pipe delay ouput1	0	1	1	1	0
15	LUT4_0 output (CNT_DLY2 output (8 bit w/ ext CK,reset))	0	1	1	1	1
16	CNT_DLY0 output (8 bit w/ ext CK (shared bottom delay/cnt),reset)	1	0	0	0	0
17	CNT_DLY1 output (8 bit w/ ext CK (from dedicated matrix output),reset)	1	0	0	0	1
18	CNT_DLY3 (8 bit) output	1	0	0	1	0
19	ACMP_0 output	1	0	0	1	1
20	ACMP_1 output	1	0	1	0	0
21	Edge detect output	1	0	1	0	1
22	Programmable delay with edge detector output (Deglitch filter output)	1	0	1	1	0
23	internal oscillator output1 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	0	1	1	1
24	internal oscillator output2 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	1	0	0	0
25	Bandgap OK signal	1	1	0	0	1
26	POR output to matrix	1	1	0	1	0
27	pin8 digital Input	1	1	0	1	1
28	pin9 digital Input	1	1	1	0	0
29	pin10 digital Input	1	1	1	0	1
30	pin12 digital Input	1	1	1	1	0
31	VDD	1	1	1	1	1

8.2 Matrix Output Table

Table 10. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <4:0>	Pin 3 digital out source	0
reg <9:5>	Pin 4 digital out source	1
reg <14:10>	Pin 6 digital out source	2
reg <19:15>	Pin 6 output enable	3
reg <24:20>	in0 of LUT2_0 (Clock Input of DFF0)	4
reg <29:25>	in1 of LUT2_0 (Data Input of DFF0)	5
reg <34:30>	in0 of LUT2_1 (Clock Input of DFF1)	6
reg <39:35>	in1 of LUT2_1 (Data Input of DFF1)	7
reg <44:40>	in0 of LUT2_2	8
reg <49:45>	in1 of LUT2_2	9
reg <54:50>	in0 of LUT2_3	10
reg <59:55>	in1 of LUT2_3	11
reg <64:60>	in0 of LUT3_0 (Clock Input of DFF2 with nReset/nSet)	12
reg <69:65>	in1 of LUT3_0 (Data input of DFF2 with nReset/nSet)	13
reg <74:70>	in2 of LUT3_0 (Resetb or Setb of DFF2 with nReset/nSet)	14
reg <79:75>	in0 of LUT3_1 (Clock Input of DFF3 with nReset/nSet)	15
reg <84:80>	in1 of LUT3_1 (Data input of DFF3 with nReset/nSet)	16
reg <89:85>	in2 of LUT3_1 (Resetb or Setb of DFF3 with nReset/nSet)	17
reg <94:90>	in0 of LUT3_2	18
reg <99:95>	in1 of LUT3_2	19
reg <104:100>	in2 of LUT3_2	20
reg <109:105>	in0 of LUT3_3	21
reg <114:110>	in1 of LUT3_3	22
reg <119:115>	in2 of LUT3_3	23
reg <124:120>	in0 of LUT3_4 (Input of pipe delay)	24
reg <129:125>	in1 of LUT3_4 (Resetb of pipe delay)	25
reg <134:130>	in2 of LUT3_4 (Clock of pipe delay)	26
reg <139:135>	in0 of LUT4_0 (Input for Delay2 ext. clock or Counter2 external Clock)	27
reg <144:140>	in1 of LUT4_0 (Input for delay2 or counter2 reset input)	28
reg <149:145>	in2 of LUT4_0	29
reg <154:150>	in3 of LUT4_0	30
reg <159:155>	Input for delay0 or counter0 reset input	31
reg <164:160>	Input for delay1 or counter1 reset input	32
reg <169:165>	Input for Delay0/1 ext. clock or Counter1 external Clock	33
reg <174:170>	Input for delay3 or counter3 reset input	34
reg <179:175>	pdb for ACMP0	35
reg <184:180>	pdb for ACMP1	36
reg <189:185>	Input for programmable delay(deglitch filter input)	37

Table 10. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <194:190>	Power down for osc. (higher priority) (high = power down).	38
reg <199:195>	Pin 8 digital out source	39
reg <204:200>	Pin 9 digital out source	40
reg <209:205>	Pin 10 digital out source	41
reg <214:210>	Pin 10 output enable	42
reg <219:215>	Pin 12 digital out source	43

9.0 Combinatorial Logic

Combinatorial logic is supported via four Lookup Tables (LUTs) within the SLG46110. There are two 2-bit LUTs and two 3-bit LUTs. The device also includes six Combination Function Macrocells that can be used as LUTs. For more details, please see Section 10.0 Combination Function Macro Cells.

Inputs/Outputs for the four LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-Bit LUT

The two 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. ..

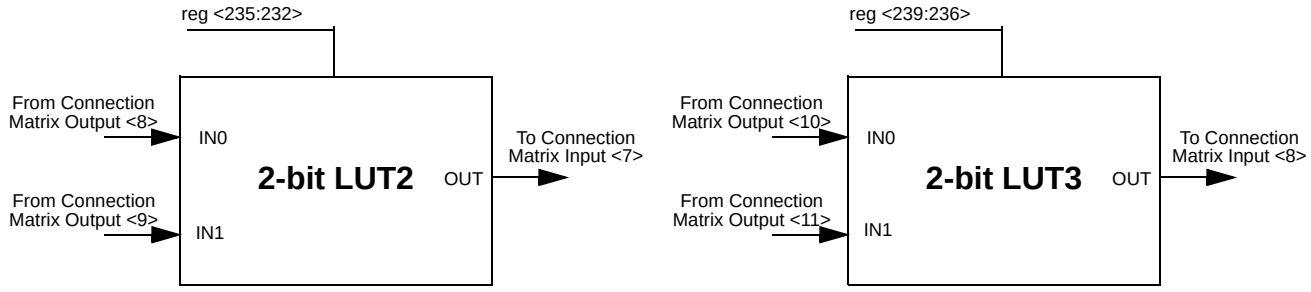


Figure 6. 2-bit LUTs

Table 11. 2-bit LUT2 Truth Table.

IN1	IN0	OUT
0	0	reg <232>
0	1	reg <233>
1	0	reg <234>
1	1	reg <235>

Table 12. 2-bit LUT3 Truth Table.

IN1	IN0	OUT
0	0	reg <236>
0	1	reg <237>
1	0	reg <238>
1	1	reg <239>

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT2 is defined by reg <235:232>

2-Bit LUT3 is defined by reg <239:236>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 13. 2-bit LUT Standard Digital Functions.

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.2 3-Bit LUT

The two 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

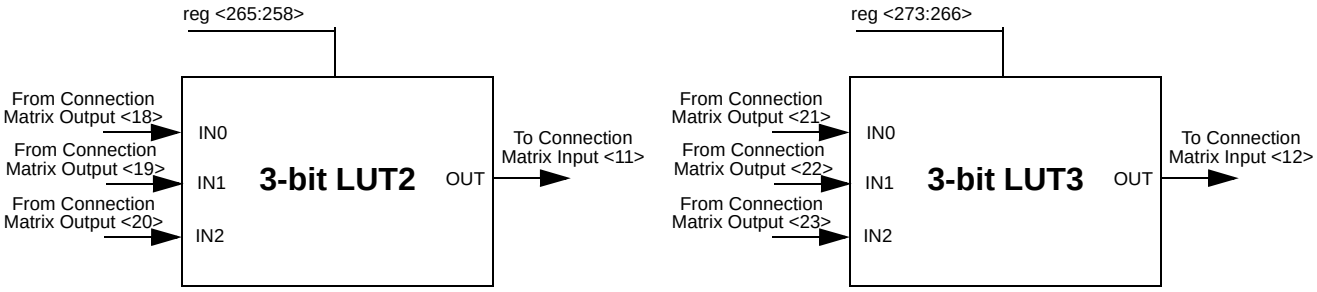


Figure 7. 3-bit LUTs

Table 14. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <258>
0	0	1	reg <259>
0	1	0	reg <260>
0	1	1	reg <261>
1	0	0	reg <262>
1	0	1	reg <263>
1	1	0	reg <264>
1	1	1	reg <265>

Table 15. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <266>
0	0	1	reg <267>
0	1	0	reg <268>
0	1	1	reg <269>
1	0	0	reg <270>
1	0	1	reg <271>
1	1	0	reg <272>
1	1	1	reg <273>

Each 3-bit LUT uses a 8-bit register signal to define their output functions;

3-Bit LUT2 is defined by reg <265:258>

3-Bit LUT3 is defined by reg <273:266>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 3-bit LUT logic cells.

Table 16. 3-bit LUT Standard Digital Functions.

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

10.0 Combination Function Macro Cells

The SLG46110 has seven combination function macrocells that can serve more than one logic or timing function. In six of these cases, they can serve as a Look Up Table (LUT), or as another logic or timing function. In the last case, it can serve as either a programmable delay or deglitch filter. See the list below for the functions that can be implemented in these macrocells;

- Two macrocells that can serve as either 2-bit LUTs or as D Flip Flops.
- Two macrocells that can serve as either 3-bit LUTs or as D Flip Flops.
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- One macrocells that can serve as either 4-bit LUTs or as 8-Bit Counter / Delays
- One macrocell that can serve as either a Programmable Delay or as a Deglitch Filter

Inputs/Outputs for the seven combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

When used as a D Flip Flop / Latch, the source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state, and all have the option to connect both the Q and Q Bar outputs to the connection matrix. The macrocells DFF2, DFF3 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CLK = 0, then Q = D

10.1 2-Bit LUT or D Flip Flop Macrocells

There are two macrocells that can serve as either 2-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (d) and clock (clk) inputs for the Flip Flop, with the output going back to the connection matrix.

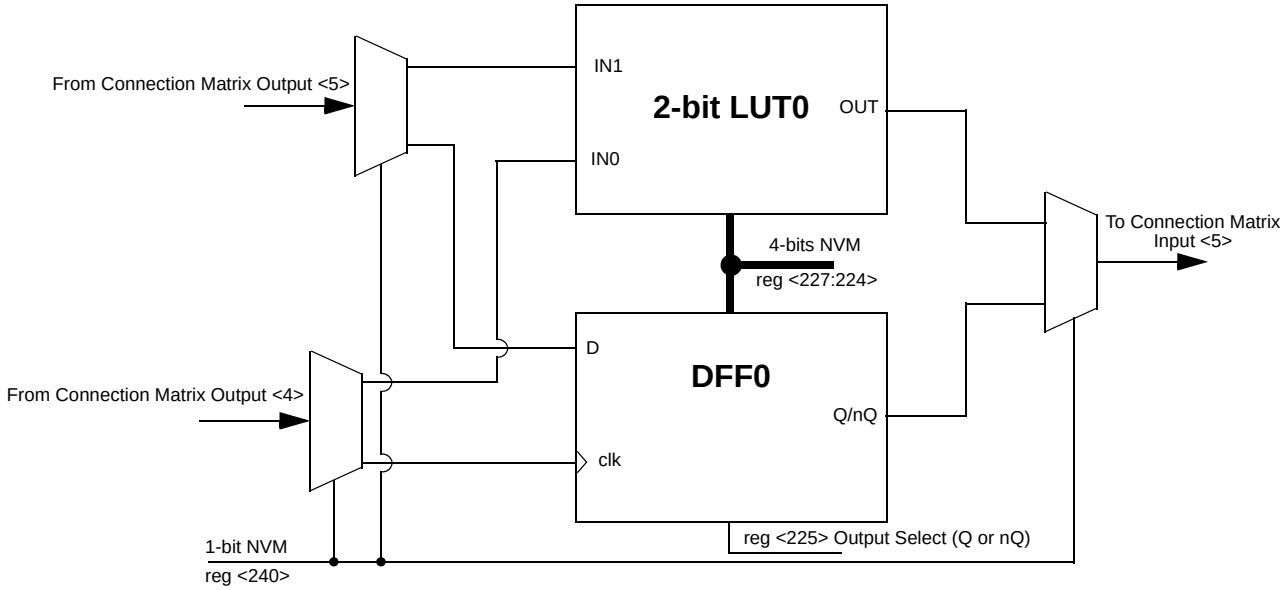


Figure 8. 2-bit LUT0 or DFF0

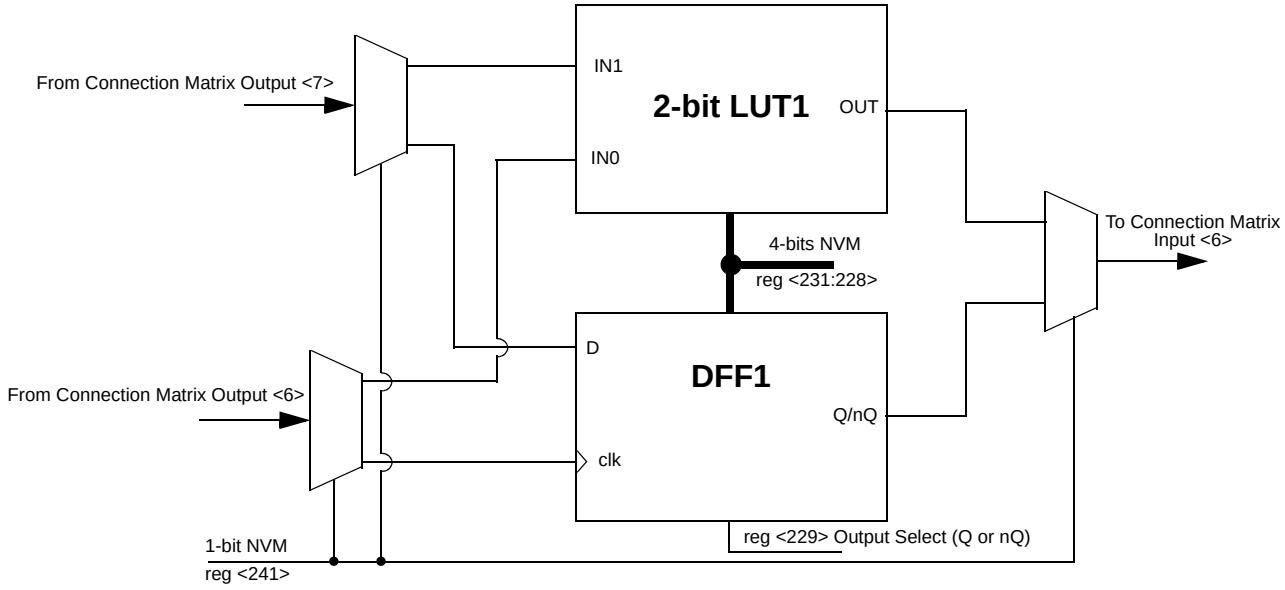


Figure 9. 2-bit LUT1 or DFF1

10.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Table 17. 2-bit LUT0 Truth Table.

IN1	IN0	OUT
0	0	reg <224>
0	1	reg <225>
1	0	reg <226>
1	1	reg <227>

Table 18. 2-bit LUT1 Truth Table.

IN1	IN0	OUT
0	0	reg <228>
0	1	reg <229>
1	0	reg <230>
1	1	reg <231>

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg <227:224>

2-Bit LUT1 is defined by reg <231:228>

10.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 19. DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF0 or Latch select	reg <224>	0: DFF function 1: Latch function
DFF0 output select	reg <225>	0: Q output 1: nQ output
DFF0 initial polarity select	reg <226>	0: Low 1: High
LUT2_0 data	reg <235:232>	LUT2_0 data
LUT2_0 or DFF0 select	reg <240>	0: LUT2_0 1: DFF0

Table 20. DFF1Register Settings

Signal Function	Register Bit Address	Register Definition
DFF1 or Latch select	reg <228>	0: DFF function 1: Latch function
DFF1 output select	reg <229>	0: Q output 1: nQ output
DFF1 initial polarity select	reg <230>	0: Low 1: High
LUT2_1 data	reg <239:236>	LUT2_1 data
LUT2_1 or DFF1 select	reg <241>	0: LUT2_1 1: DFF1

10.2 3-Bit LUT or D Flip Flop with Set/Reset Macrocells

There are two macrocells that can serve as either 3-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (d) and clock (clk) and Set/Reset (rRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix..

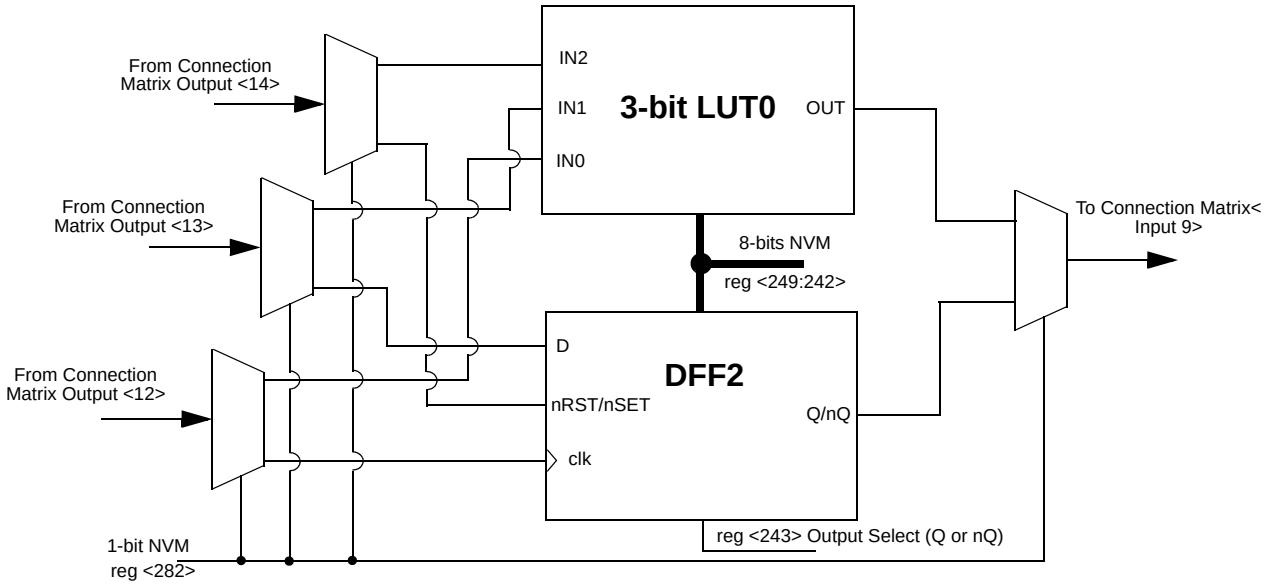


Figure 10. 3-bit LUT0 or DFF2

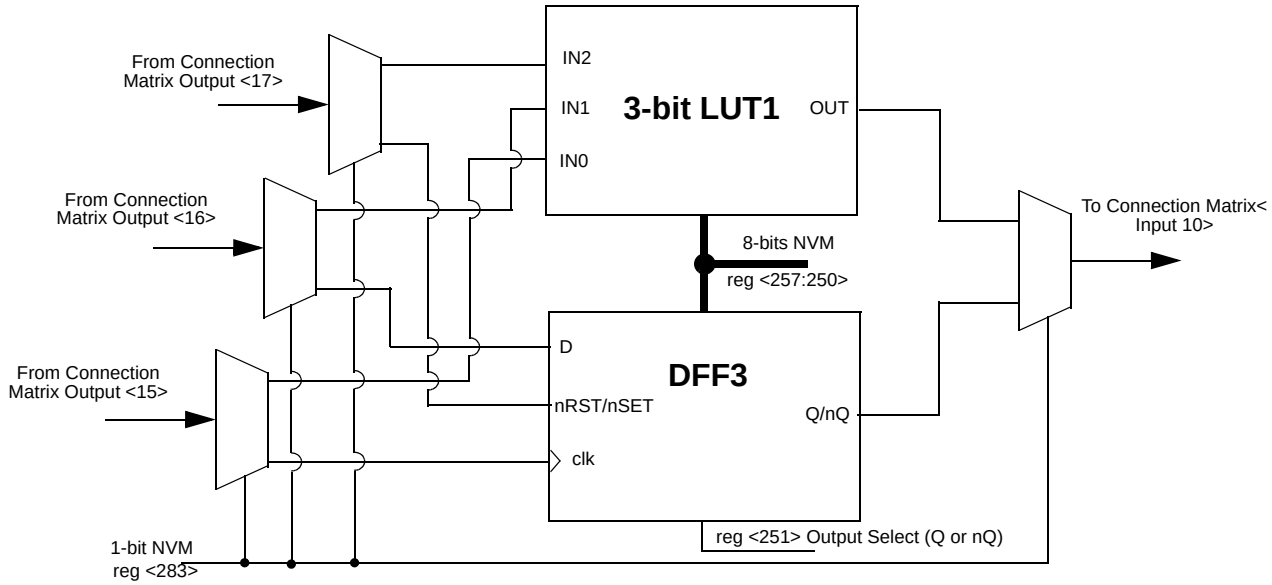


Figure 11. 3-bit LUT1 or DFF3

10.2.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

Table 21. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <242>
0	0	1	reg <243>
0	1	0	reg <244>
0	1	1	reg <245>
1	0	0	reg <246>
1	0	1	reg <247>
1	1	0	reg <248>
1	1	1	reg <249>

Table 22. 3-bit LUT1 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <250>
0	0	1	reg <251>
0	1	0	reg <252>
0	1	1	reg <253>
1	0	0	reg <254>
1	0	1	reg <255>
1	1	0	reg <256>
1	1	1	reg <257>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT2 is defined by reg <249:242>

3-Bit LUT3 is defined by reg <257:250>

10.2.2 3-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 23. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF2 or Latch select	reg <242>	0: DFF function 1: Latch function
DFF2 output select	reg <243>	0: Q output 1: nQ output
DFF2 initial polarity select	reg <244>	0: Low 1: High
DFF2 rstb/setb Select	reg <245>	1: setb from matrix out 0: resetb from matrix out
LUT3_0 data	reg <265:258>	LUT3_0 data
LUT3_0 or DFF2 select	reg <282>	0: LUT3_0 1: DFF2

Table 24. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF3 or Latch Select	reg <250>	0: DFF function 1: Latch function
DFF3 Output Select	reg <251>	0: Q output 1: nQ output
DFF3 rstb/setb Select	reg <252>	1: setb from matrix out 0: resetb from matrix out
DFF3 initial polarity select	reg <253>	0: Low 1: High
LUT3_1 data	reg <273:266>	LUT3_1 data
LUT3_1 or DFF3 select	reg <283>	0: LUT3_1 1: DFF3

10.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as an 8-stage pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CK) and Reset (nReset). The pipe delay cell is built from D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The two outputs (OUT0 and OUT1) provide user selectable options for 1 to 8 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 3-input mux that is controlled by reg <666:663> for OUT0 and reg <670:667> for OUT1. The 3-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46110 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46110). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

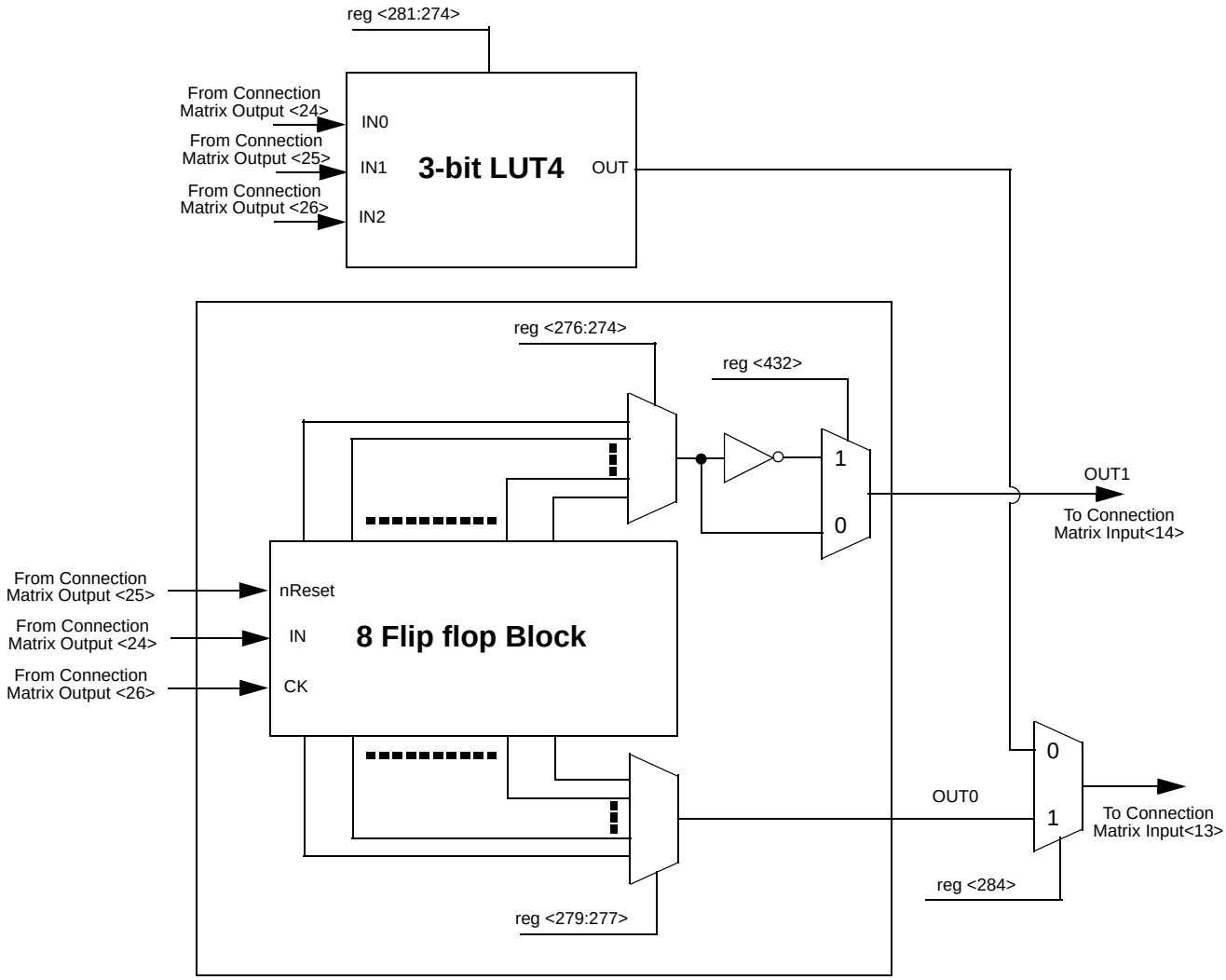


Figure 12. 3-bit LUT4 or Pipe Delay

10.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 25. 3-bit LUT4 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <274>
0	0	1	reg <275>
0	1	0	reg <276>
0	1	1	reg <277>
1	0	0	reg <278>
1	0	1	reg <279>
1	1	0	reg <280>
1	1	1	reg <281>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT4 is defined by reg <281:274>

10.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 26. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 select	reg <276:274>	data (pipe number)
OUT1 select	reg <279:277>	data (pipe number)
LUT3_4 or pipe delay output select	reg <284>	0: LUT3_4 1: pipe delay

10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells

There is one macrocell that can serve as either a 4-bit LUT or as a Counter / Delay. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delay function, two of the four input signals from the connection matrix go to the external clock (ext_clk) and reset (DLY_n/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

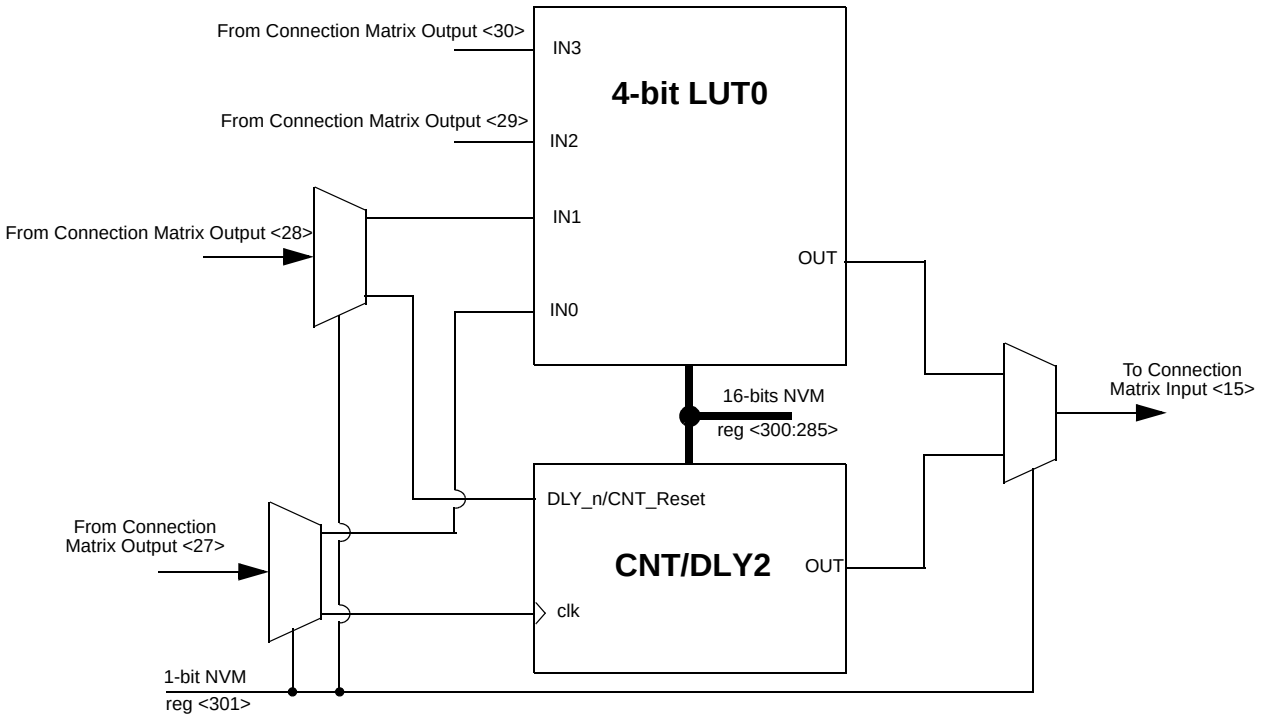


Figure 13. 4-bit LUT0 or CNT/DLY2

10.4.1 4-Bit LUT or 8-Bit Counter / Delay Macrocell Used as 4-Bit LUTs

Table 27. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <285>
0	0	0	1	reg <286>
0	0	1	0	reg <287>
0	0	1	1	reg <288>
0	1	0	0	reg <289>
0	1	0	1	reg <290>
0	1	1	0	reg <291>
0	1	1	1	reg <292>
1	0	0	0	reg <293>
1	0	0	1	reg <294>
1	0	1	0	reg <295>
1	0	1	1	reg <296>
1	1	0	0	reg <297>
1	1	0	1	reg <298>
1	1	1	0	reg <299>
1	1	1	1	reg <300>

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by reg <300:285>

Table 28. 4-bit LUT Standard Digital Functions.

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

10.4.2 4-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 8-Bit Counter / Delay Register Settings

Table 29. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay2 Mode Selection	reg <285>	0: Delay Mode 1: Counter Mode
Counter/delay2 Clock Source Select	reg <288:286>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter1 Overflow
Counter/delay2 Control Data	reg <296:289>	1 – 256 (delay time = (counter control data +1) /freq)
Delay2 Mode Select or asynchronous counter reset	reg <298:297>	00: Delay on both falling and rising edges(for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
LUT4_0 or Counter2 select	reg <301>	0: LUT4_0 1: Counter2

10.5 Programmable Delay / Edge Detector

The SLG46110 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

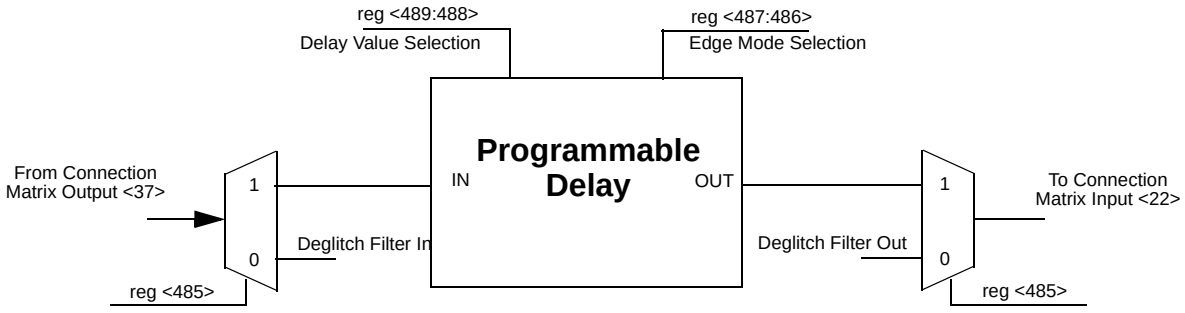


Figure 14. Programmable Delay

10.5.1 Programmable Delay Timing Diagram - Edge Detector Output

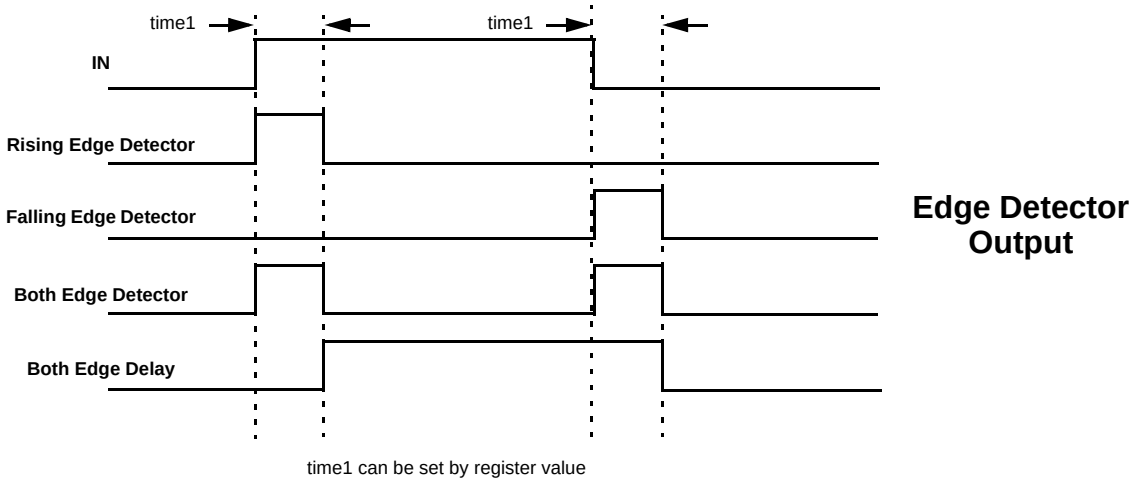


Figure 15. Edge Detector Output

10.5.2 Programmable Delay Register Settings

Table 30. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Programmable delay or filter output select	reg <485>	0: programmable delay output 1: filter output
Select the edge mode of programmable delay & edge detector	reg <487:486>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	reg <489:488>	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns

10.6 Deglitch Filter

The SLG46110 has an additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one deglitch filter.

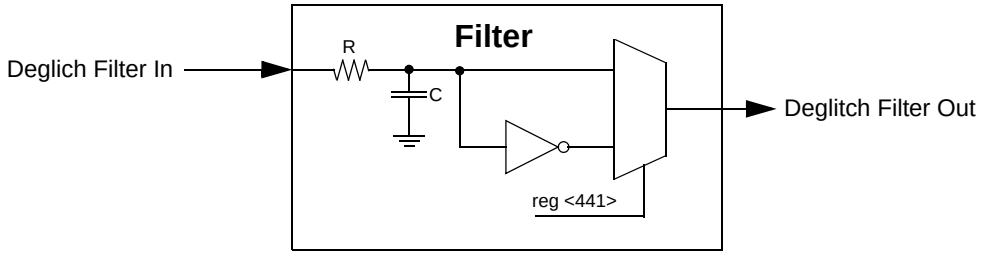


Figure 16. Deglitch Filter

11.0 Analog Comparators (ACMP)

There are two Analog Comparator (ACMP) macro cells in the SLG46110. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0_pdb and ACMP1_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by way of the external sources.

Each of the ACMP cells has a selection for the bandwidth of the input signal, which can be used to save power when low bandwidth signals are input into the analog comparator. Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV.

11.1 ACMP0 Block Diagram

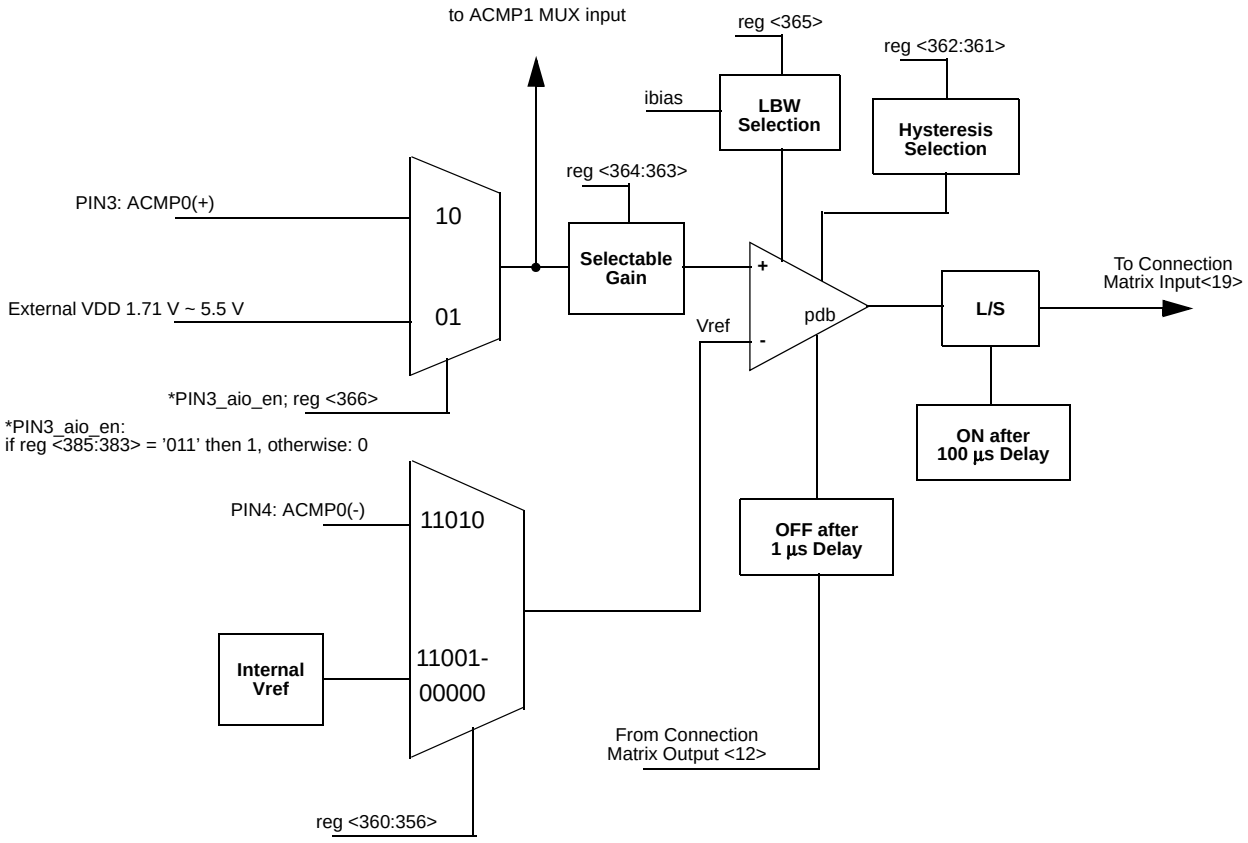


Figure 17. ACMP0 Block Diagram

11.2 ACMP0 Register Settings

Table 31. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 In Voltage Select	reg <360:356>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF (PIN4)
ACMP0 Hysteresis Enable	reg <362:361>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP0 Positive Input Divider	reg <364:363>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg <365>	0: Off 1: On
ACMP0 positive input source select PIN3 and VDD	reg <366>	0: Pin3 1: VDD

11.3 ACMP1 Block Diagram

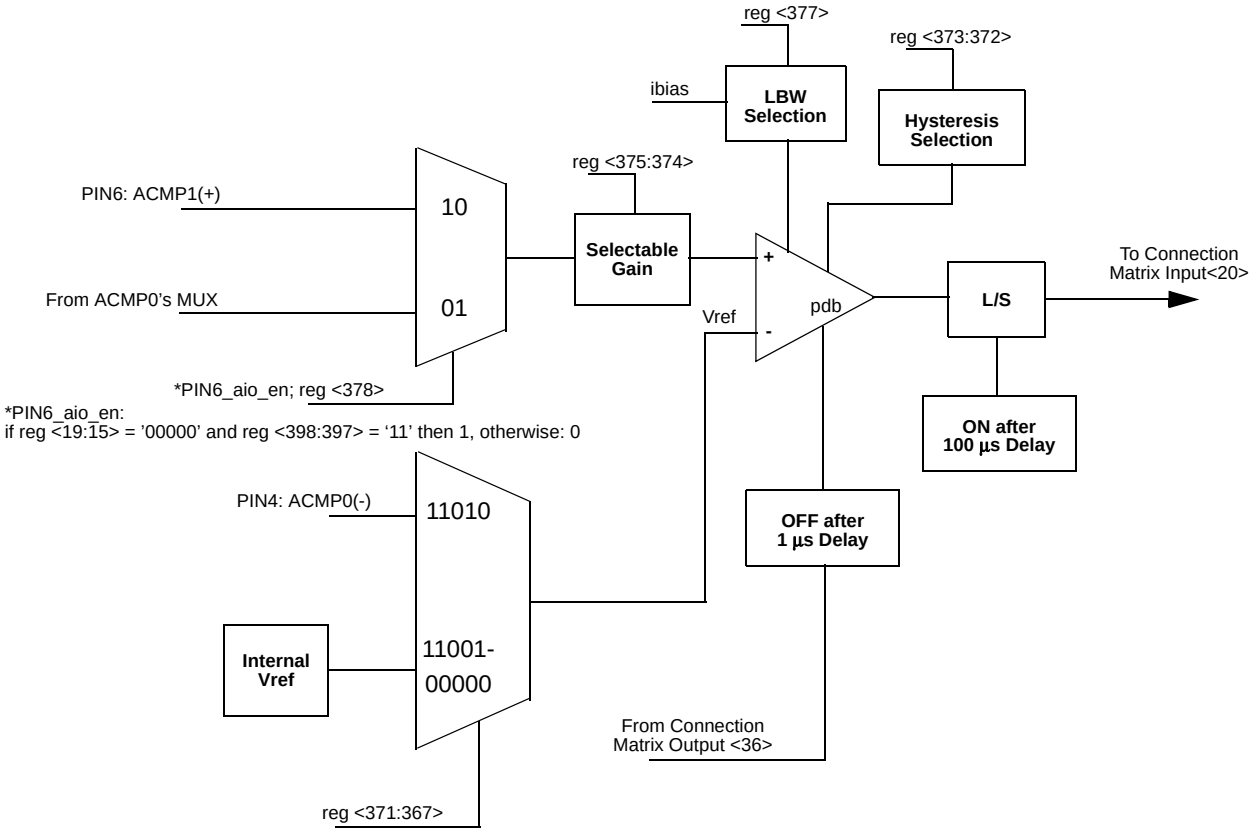


Figure 18. ACMP1 Block Diagram

11.4 ACMP1 Register Settings

Table 32. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 In Voltage Select	reg <371:367>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF (PIN4)
ACMP1 Hysteresis Enable	reg <373:372>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP1 Positive Input Divider	reg <375:374>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg <377>	1: On 0: Off
ACMP1 positive input source select PIN3 and Pin6	reg <378>	0: Pin6 1: Pin3

12.0 Counters/Delay Generators (CNT/DLY)

There are three configurable counters/delay generators in the SLG46110. The three counters/delay generators (CNT/DLY 0, 1, 3) are 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

Two of the counter/delay generator macrocells (CNT/DLY0 and CNT/DLY1) have two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. One of the counter/delay generator macrocells (CNT/DLY3) has one input from the connection matrix, which has a shared function of either a Delay Input or an external clock input.

Note that there is also one Combination Function Macrocells that can implement either 4-bit LUTs or 8-bit counter / delays, For more information please see Section 10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells.

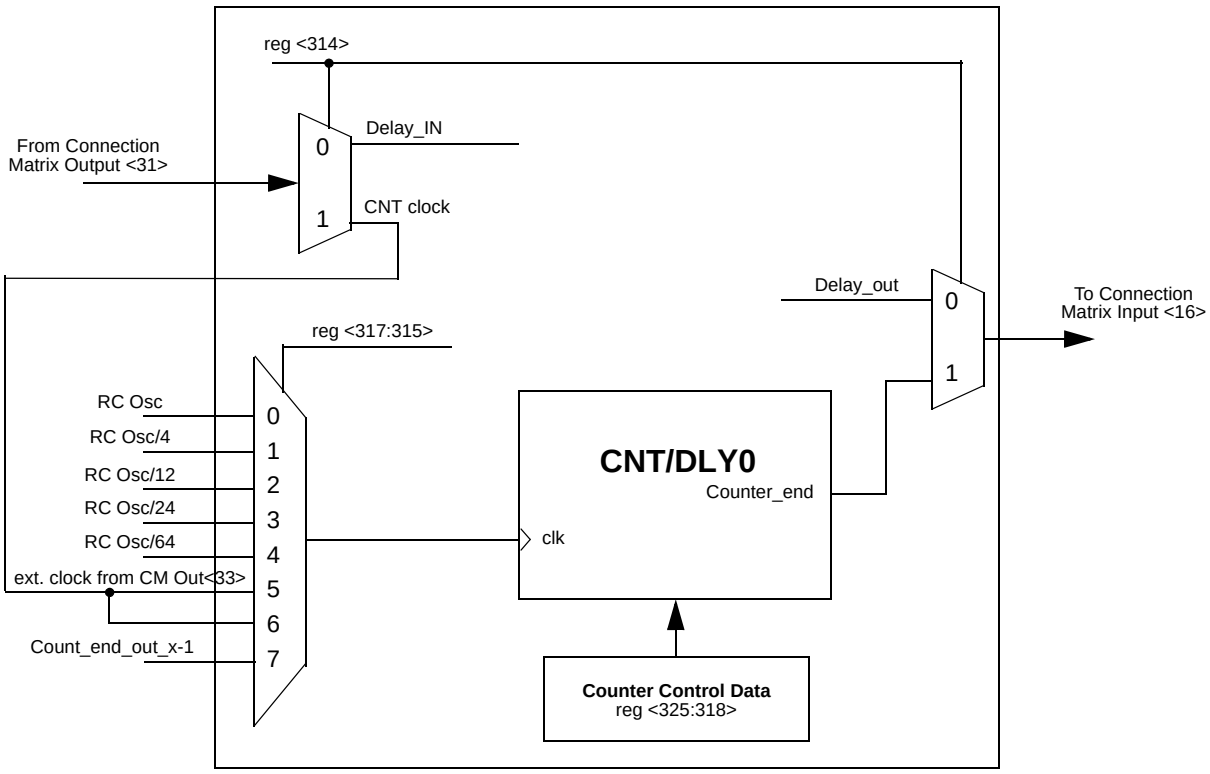


Figure 19. CNT/DLY0

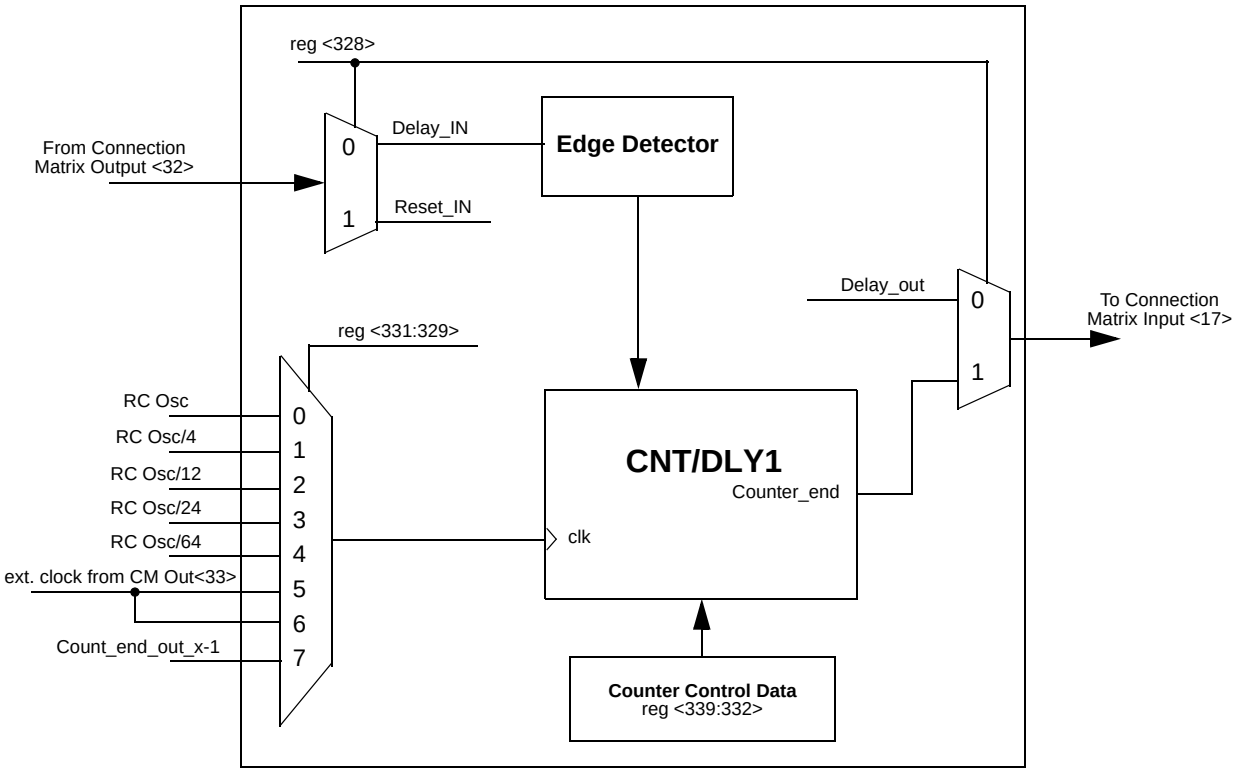


Figure 20. CNT/DLY1

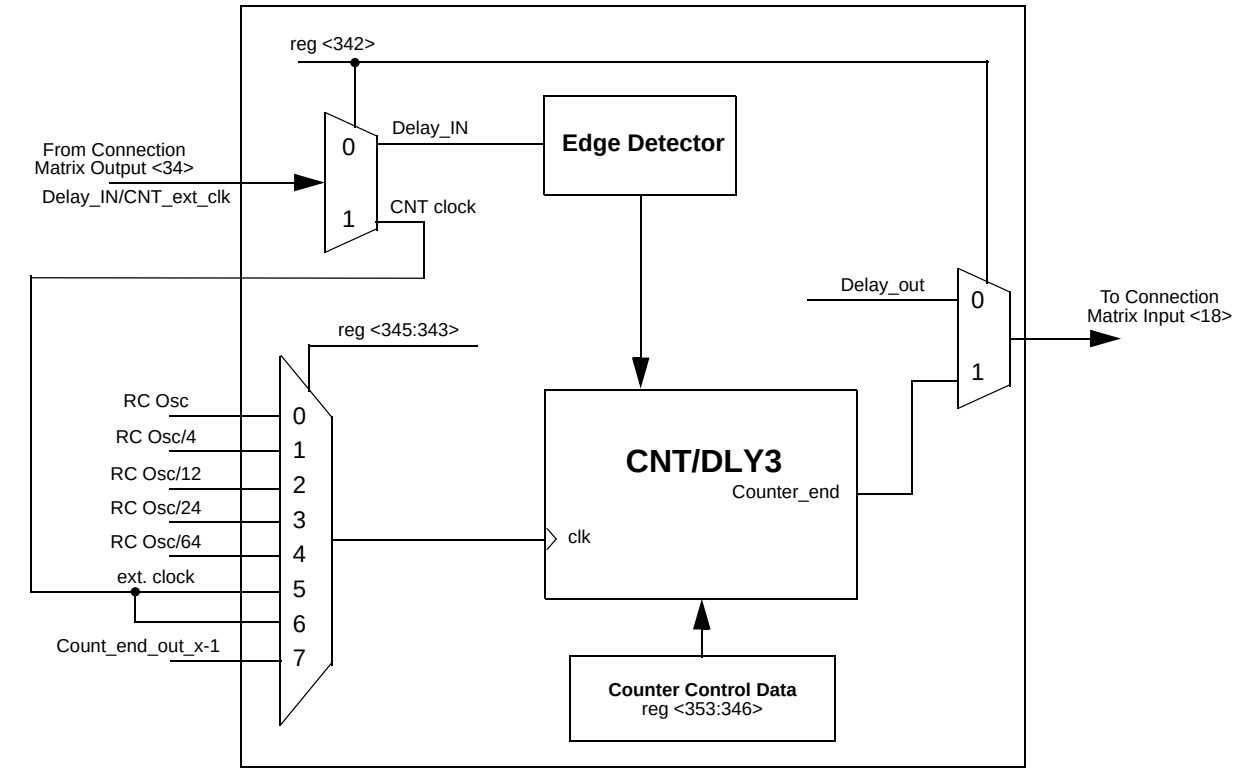


Figure 21. CNT/DLY3

12.1 CNT/DLY0 Register Settings

Table 33. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	reg <314>	0: Delay Mode 1: Counter Mode
Counter/Delay0 Clock Source Select (external clock is only for counter mode)	reg <317:315>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter3 Overflow
Counter0 Control Data/Delay0 Time Control	reg <325:318>	1-256: (delay time = (counter control data +1) /freq)
Delay0 Mode Select or asynchronous counter reset	reg <327:326>	00: Delay on both falling and rising edges(for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

12.2 CNT/DLY1 Register Settings

Table 34. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg <328>	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source Select (external clock is only for counter mode)	reg <331:329>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter0 Overflow
Counter1 Control Data/Delay1 Time Control	reg <339:332>	1-256: (delay time = (counter control data +1) /freq)
Delay1 Mode Select or asynchronous counter reset	reg <341:340>	00: Delay on both falling and rising edges(for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

12.3 CNT/DLY3 Register Settings

Table 35. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay3 Mode Select	reg <342>	0: Delay Mode 1: Counter Mode
Counter/Delay3 Clock Source Select (external clock is only for counter mode)	reg <345:343>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter2 Overflow
Counter3 Control Data/Delay3 Time Control	reg <353:346	1-256: (delay time = (counter control data +1) /freq)
Delay3 Mode Select	reg <355:354>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

13.0 Voltage Reference (VREF)

13.1 Voltage Reference Overview

The SLG46110 has a Voltage Reference Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from pin 4. The macrocell also has the option to output reference voltages on pin 10. See table below for the available selections for each analog comparator. Also see *Figure 22* below, which shows the reference output structure.

13.2 VREF Selection Table

Table 36. VREF Selection Table.

SEL<4:0>	CMP0_VREF	CMP1_VREF
11010	ext. Vref (PIN4)	ext. Vref (PIN4)
11001	VDD / 4	VDD / 4
11000	VDD / 3	VDD / 3
10111	1.20 V	1.20 V
10110	1.15 V	1.15 V
10101	1.10 V	1.10 V
10100	1.05 V	1.05 V
10011	1.00 V	1.00 V
10010	0.95 V	0.95 V
10001	0.90 V	0.90 V
10000	0.85 V	0.85 V
01111	0.80 V	0.80 V
01110	0.75 V	0.75 V
01101	0.70 V	0.70 V
01100	0.65 V	0.65 V
01011	0.60 V	0.60 V
01010	0.55 V	0.55 V
01001	0.50 V	0.50 V
01000	0.45 V	0.45 V
00111	0.40 V	0.40 V
00110	0.35 V	0.35 V
00101	0.30 V	0.30 V
00100	0.25 V	0.25 V
00011	0.20 V	0.20 V
00010	0.15 V	0.15 V
00001	0.10 V	0.10 V
00000	0.05 V	0.05 V

VDD	Practial VREF Range	Note
2.0 V - 5.5 V	50 mV ~1.2 V	
1.7 V - 2.0V	50 mV ~1.1 V	Higher than 1.1 V negative input, the comparator may show wrong result

13.3 VREF Block Diagram

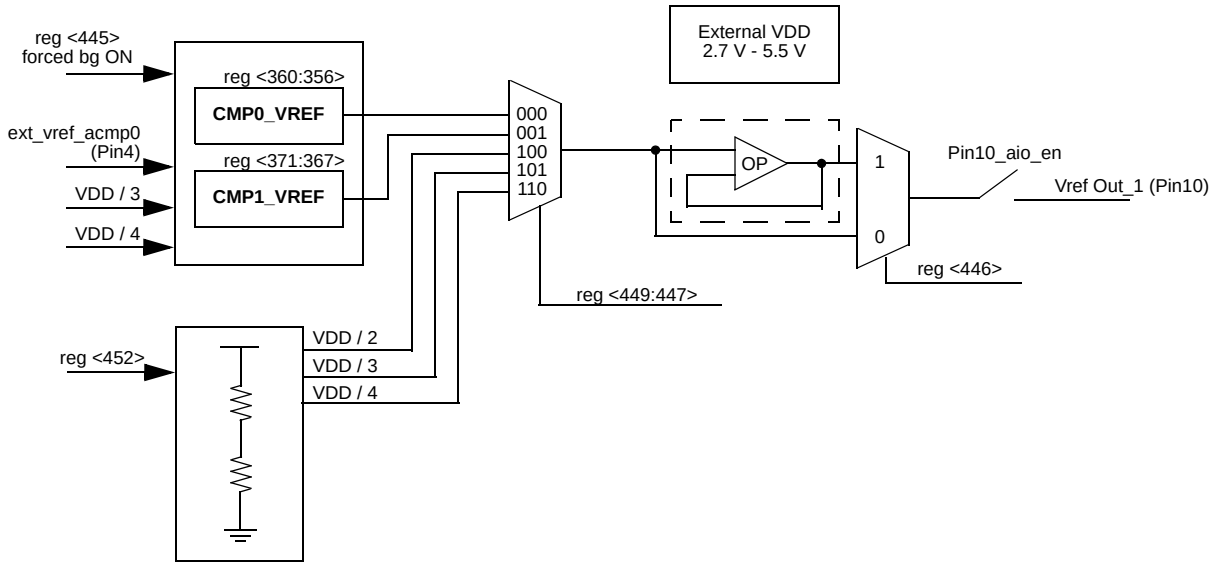


Figure 22. Voltage Reference Block Diagram

14.0 RC Oscillator (RC OSC)

14.1 RC Oscillator Overview

The SLG46110 has two internal RC oscillators, one that runs at 25 kHz and one that runs at 2 MHz. The user can select one of these fundamental frequencies for the RC OSC Macrocell, or the fundamental frequency can also come from an external clock input (Pin 12). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The first stage divider (also known as the clock pre-divider) allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. There are two second stage divider controls (OUT0 and OUT1). Each has its own input of one frequency from the first stage divider, and outputs five different frequencies on Connection Matrix Input lines <45>, <46>, <47>, <48>, and <49>. See *Figure 23* below for details of the frequencies for each of these five Connection Matrix Inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off. The PWR DOWN signal has the highest priority.

14.2 RC OSC Block Diagram

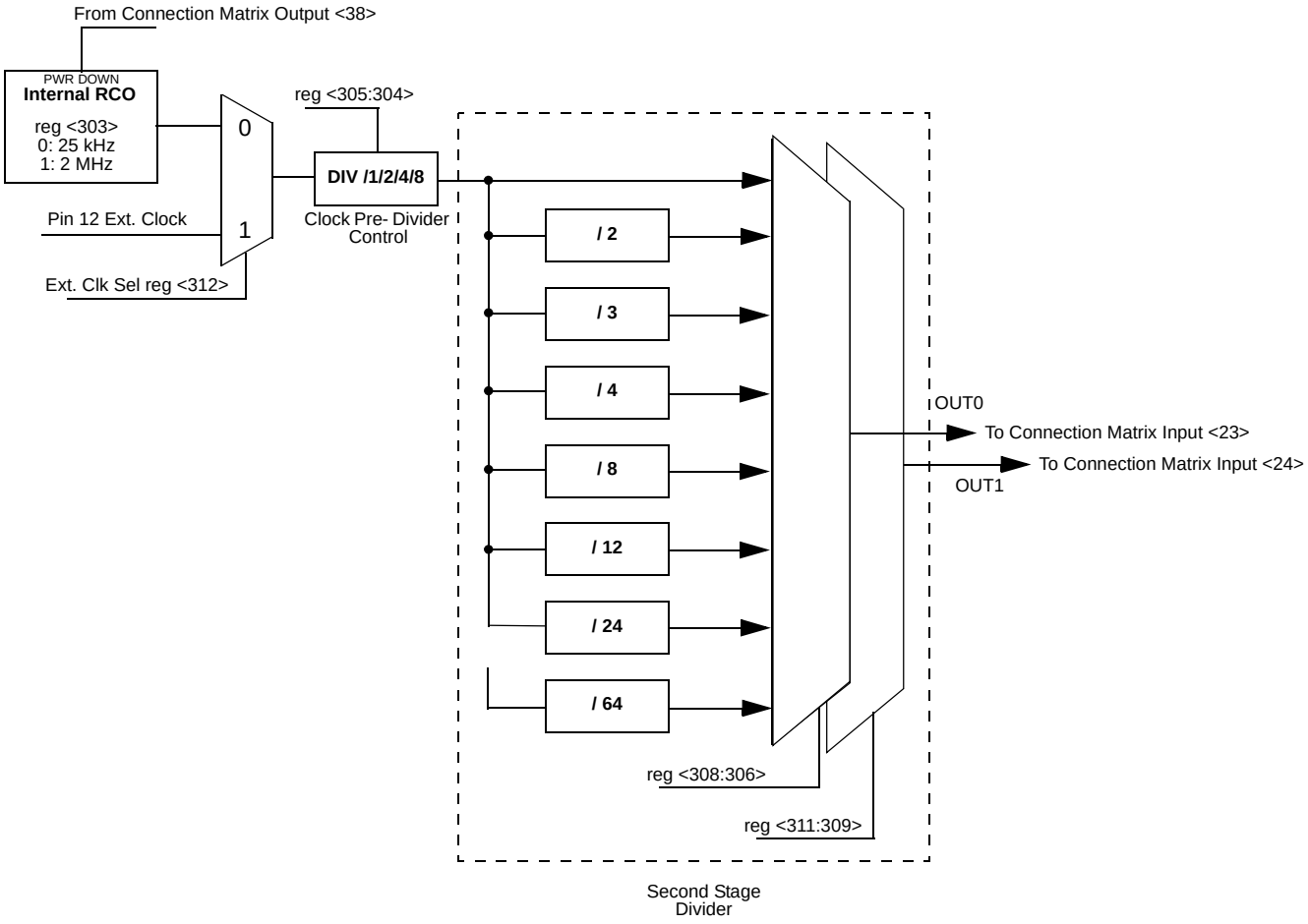


Figure 23. RC OSC Block Diagram

15.0 Appendix A - SLG46110 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg <4:0>	Matrix Out: PIN3 Digital Output Source	
reg <9:5>	Matrix Out: PIN4 Digital Output Source	
reg <14:10>	Matrix Out: PIN6 Digital Output Source	
reg <19:15>	Matrix Out: Output Enable of PIN6	
reg <24:20>	Matrix Out: In0 of LUT2_0 or Clock Input of DFF0	
reg <29:25>	Matrix Out: In1 of LUT2_0 or Data Input of DFF0	
reg <34:30>	Matrix Out: In0 of LUT2_1 or Clock Input of DFF1	
reg <39:35>	Matrix Out: In1 of LUT2_1 or Data Input of DFF1	
reg <44:40>	Matrix Out: In0 of LUT2_2	
reg <49:45>	Matrix Out: In1 of LUT2_2	
reg <54:50>	Matrix Out: In0 of LUT2_3	
reg <59:55>	Matrix Out: In1 of LUT2_3	
reg <64:60>	Matrix Out: In0 of LUT3_0 or Clock Input of DFF2	
reg <69:65>	Matrix Out: In1 of LUT3_0 or Data Input of DFF2	
reg <74:70>	Matrix Out: In2 of LUT3_0 or Resetb Input of DFF2	
reg <79:75>	Matrix Out: In0 of LUT3_1 or Clock Input of DFF3	
reg <84:80>	Matrix Out: In1 of LUT3_1 or Data Input of DFF3	
reg <89:85>	Matrix Out: In2 of LUT3_1 or Resetb(Setb) of DFF3	
reg <94:90>	Matrix Out: In0 of LUT3_2	
reg <99:95>	Matrix Out: In1 of LUT3_2	
reg <104:100>	Matrix Out: In2 of LUT3_2	
reg <109:105>	Matrix Out: In0 of LUT3_3	
reg <114:110>	Matrix Out: In1 of LUT3_3	
reg <119:115>	Matrix Out: In2 of LUT3_3	
reg <124:120>	Matrix Out: In0 of LUT3_4 or Input of Pipe delay	
reg <129:125>	Matrix Out: In1 of LUT3_4 or Resetb of Pipe delay	
reg <134:130>	Matrix Out: In2 of LUT3_4 or Clock of Pipe delay	
reg <139:135>	Matrix Out: In0 of LUT4_0 or Input for delay2 (Counter2) external clock	
reg <144:140>	Matrix Out: In1 of LUT4_0 or Input for delay2 data (counter2 reset)	
reg <149:145>	Matrix Out: In2 of LUT4_0	
reg <154:150>	Matrix Out: In3 of LUT4_0	
reg <159:155>	Matrix Out: Input for delay0 data (counter0 reset)	
reg <164:160>	Matrix Out: Input for delay1 data (counter1 reset)	
reg <169:165>	Matrix Out: Input for delay0/1 (Counter0/1) external clock	
reg <174:170>	Matrix Out: Input for delay3 (Counter3) external clock	
reg <179:175>	Matrix Out: pdb(power down) for ACMP0	
reg <184:180>	Matrix Out: pdb(power down) for ACMP1	
reg <189:185>	Matrix Out: Input for programmable delay (deglitch filter input)	

Register Bit Address	Signal Function	Register Bit Definition
reg <194:190>	Matrix Out: Power down for osc	
reg <199:195>	Matrix Out: PIN8 Digital Output Source	
reg <204:200>	Matrix Out: PIN9 Digital Output Source	
reg <209:205>	Matrix Out: PIN10 Digital Output Source	
reg <214:210>	Matrix Out: Output Enable of PIN10	
reg <219:215>	Matrix Out: PIN12 Digital Output Source	
reg <223:220>	Reserved	Reserved
DFF0/Latch		
reg <227:224>	reg <224> DFF0 or Latch select	0: DFF function 1: Latch function
	reg <225> DFF0 output select	0: Q output 1: nQ output
	reg <226> DFF0 initial polarity select	0: Low 1: High
	reg <227> Unused if DFF/Latch selected	Unused
DFF1/Latch		
reg <231:228>	reg <228> DFF1 or Latch select	0: DFF function 1:Latch function
	reg <229> DFF1 output select	0: Q output 1: nQ output
	reg <230> DFF1 initial polarity select	0: Low 1:High
	reg <231> Unused if DFF/Latch selected	Unused
LUT2_0 data		
reg <235:232>	LUT2_0 data	LUT2_0 data
LUT2_1 data		
reg <239:236>	LUT2_1 data	LUT2_1 data
LUT2_0/DFF0		
reg <240>	LUT2_0 or DFF0 select	0: LUT2_0 1: DFF0
LUT2_1/DFF1		
reg <241>	LUT2_1 or DFF1 select	0: LUT2_1 1: DFF1
LUT3_0 or DFF2/Latch		
reg <249:242>	reg <242> DFF2 or Latch select	0: DFF function 1: Latch function
	reg <243> DFF2 output select	0: Q output 1: nQ output
	reg <244> DFF2 rstb/setb select	0: resetb from matrix output 1: setb from matrix output
	reg <245> DFF2 initial polarity select	0: Low 1: High
	reg <249:246> Unused if DFF/Latch selected	Unused

Register Bit Address	Signal Function	Register Bit Definition
DFF3/Latch		
reg <257:250>	reg <250> DFF3 or Latch select	0: DFF function 1: Latch function
	reg <251> DFF3 output select 0: Q output 1: nQ output	0: Q output 1: nQ output
	reg <252> DFF3 rstb/setb select	0: resetb from matrix output 1: setb from matrix output
	reg <253> DFF3 initial polarity select	0: Low 1: High
	reg <257:254> Unused if DFF/Latch selected	Unused
LUT3_0 data		
reg <265:258>	LUT3_0 data	LUT3_0 data
LUT3_1 data		
reg <273:266>	LUT3_1 data	LUT3_1 data
LUT3_4 or pipe number select		
reg <281:274>	reg <276:274>: OUT0 select	data (pipe number)
	reg <279:277>: OUT1 select	data (pipe number)
	reg <281:280>: Unused if Pipe Delay selected	Unused
LUT3/DFF Select		
reg <282>	LUT3_0 or DFF2 select	0: LUT3_0 1: DFF2
reg <283>	LUT3_1 or DFF3 select	0: LUT3_1 1: DFF3
reg <284>	LUT3_4 or pipe delay output select	0: lut3_4 1: pipe delay
LUT4_0 or Counter/delay2 mode selection		
reg <300:285>	reg <285> Counter/delay2 mode selection	0: Delay Mode 1: Counter Mode
	reg <288:286> Counter/delay2 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter1 Overflow
	reg <296:289> Counter/delay2 Control Data	1 – 256 (delay time = (counter control data +1) /freq)
	reg <298:297> Delay2 Mode Select or asynchronous counter reset	00: Delayon both falling and rising edges(for delay & counter reset) 01: Delayon falling edge only (for delay & counter reseDelayt) 10: on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
	reg <300:299> Unused is Counter/Delay2 selected	Unused
reg <301>	LUT4_0 or Counter2 select 0: LUT4_0, 1: Counter2	0: LUT4_0 1: Counter2
reg <302>	Force RC oscillator on	0: Auto Power on 1: Force Power on

Register Bit Address	Signal Function	Register Bit Definition
reg <303>	RC Oscillator frequency control	0: 25k 1: 2M
reg <305:304>	Osc clock pre-divider	00: div1 01: div2 10: div4 11: div8
reg <308:306>	Internal Oscillator frequency divider control 0 for Matrix Input	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg <311:309>	Internal Oscillator frequency divider control 1 for Matrix Input	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg <312>	External Clock Source Select	0: Internal Oscillator 1: External Clock from PIN12
reg <313>	Reserved	Reserved
Counter/Delay 0		
reg <327:314>	reg <314>Counter/delay0 mode selection	0: Delay Mode 1: Counter Mode
	reg <317:315> Counter/delay0 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter3 Overflow
	reg <325:318> Counter0 Control Data/Delay0 Time Control	1-256: (delay time = (counter control data +1) /freq)
	reg <327:326> Delay0 Mode Select or asynchronous counter reset	00: Delayon both falling and rising edges(for delay & counter reset) 01: Delayon falling edge only (for delay & counter reset) 10: Delayon rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

Register Bit Address	Signal Function	Register Bit Definition
Counter/Delay 1		
reg <341:328>	reg <328> Counter/delay1 mode selection	0: Delay Mode 1: Counter Mode
	reg <331:329> Counter/delay1 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter0 Overflow
	reg <339:332> Counter1 Control Data/Delay1 Time Control	1-256: (delay time = (counter control data +1) /freq)
	reg <341:340> Delay1 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges(for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
Counter/Delay 3		
reg <355:342>	reg <342> Counter/delay3 mode selection	0: Delay Mode 1: Counter Mode
	reg <345:343> Counter/delay3 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter2 Overflow
	reg <353:346> Counter3 Control Data/Delay4 Time Control	1-256: (delay time = (counter control data +1) /freq)
	reg <355:354> Delay3 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

Register Bit Address	Signal Function	Register Bit Definition
ACMP0		
reg <366:356>	reg <360:356> ACMP0 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF(PIN4)
	reg <362:361> ACMP0 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
	reg <364:363> ACMP0 positive Input divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x
	reg <365> ACMP0 low bandwidth (typ: Max.1Mhz) enable.	0: off 1: on
	reg <366> ACMP0 positive input source select PIN3 and VDD	0: PIN3 1: VDD

Register Bit Address	Signal Function	Register Bit Definition
ACMP1		
reg <378:367>	reg <371:367> ACMP1 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF(PIN4)
	reg <373:372> ACMP1 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
	reg <375:374> ACMP1 positive Input divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x
	reg <376> ACMP1 100uA current source option	0: disable 1: enable
	reg <377> ACMP1 low bandwidth (typ: Max.1 MHz) enable.	0: off 1: on
	reg <378> ACMP1 positive input source select PIN6 and PIN3	0: PIN6 1: PIN3
PIN 2		
reg <382:379>	reg <380:379> PIN2 mode control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
	reg <382:381> PIN2 pull down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M

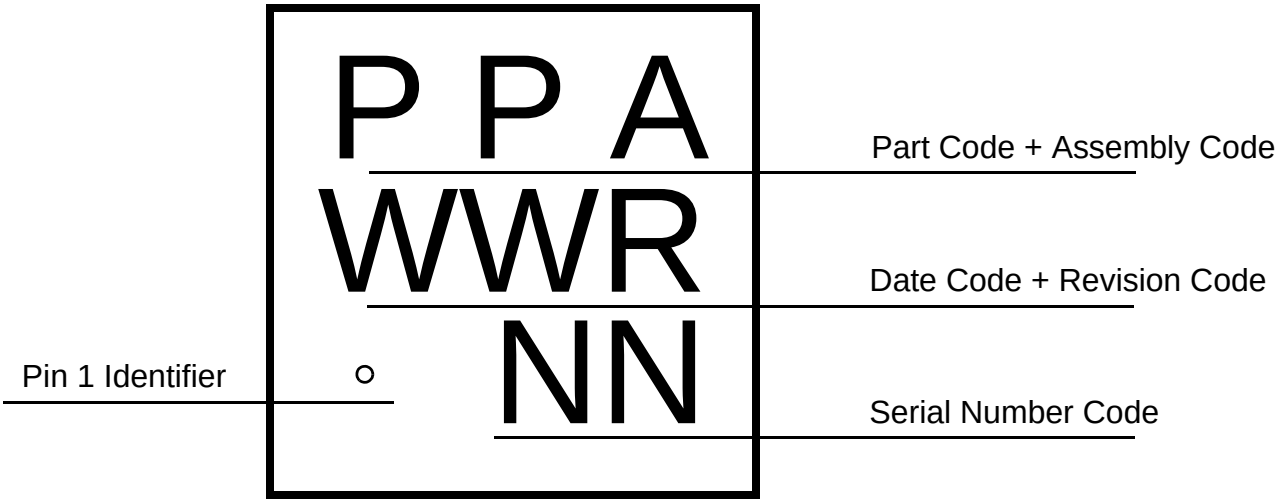
Register Bit Address	Signal Function	Register Bit Definition
PIN 3		
reg <389:383>	reg <385:383> PIN3 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
	reg <387:386> PIN3 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <388> PIN3 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <389> PIN3 driver strength selection	0: 1X 1: 2X
PIN 4		
reg <396:390>	reg <392:390> PIN4 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
	reg <394:393> PIN4 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <395> PIN4 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <396> PIN4 driver strength selection	0: 1X 1: 2X
PIN6		
reg <403:397>	reg <398:397> PIN6 mode control (sig_PIN6_oe =0)	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input / Output
	reg <400:399> PIN10 mode control (sig_PIN10_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
	reg <402:401> PIN6 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <403> PIN6 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable

Register Bit Address	Signal Function	Register Bit Definition
PIN8		
reg <410:404>	reg <406:404> PIN8 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
	reg <408:407> PIN8 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <409> PIN8 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <410> PIN8 driver strength selection	0: 1X 1: 2X
PIN9		
reg <417:411>	reg <413:411> PIN9 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
	reg <415:414> PIN9 pull down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <416> PIN9 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <417> PIN9 driver strength selection	0: 1X 1: 2X
PIN10		
reg <424:418>	reg <419:418> PIN10 mode control (sig_PIN10_oe =0)	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input / Output
	reg <421:420> PIN10 mode control (sig_PIN10_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
	reg <423:422> PIN10 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <424> PIN10 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable

Register Bit Address	Signal Function	Register Bit Definition
PIN12		
reg <431:425>	reg <427:425> PIN12 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
	reg <429:428> PIN12 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <430> PIN12 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <431> PIN12 driver strength selection	0: 1X 1: 2X
reg <432>	Pipe delay OUT1 polarity select bit	0: non-inverting 1: inverting
reg <440:433>	8-bit pattern id	8-bit pattern id
reg <441>	filter0 output polarity select	0: non-inverting 1: inverting
reg <443:442>	Reserved	Reserved
reg <444>	GPIO quick charge enable	0: Disable 1: Enable
reg <445>	Force bandgap on	0: Auto-mode 1: Enable
reg <446>	VREF1 Output Active Buffer Control	0: Disabled 1: Enabled
reg <449:447>	VREF1 Output Source Select	000: ACMP0 reference voltage 001: ACMP1 reference voltage 100: VDD/2 101: VDD/3 110: VDD/4 101: Reserved 110: Reserved 111: Reserved
reg <450>	NVM data read disable	0: Disable (read enable) 1: Enable (read disable)
reg <451>	NVM power down (or NVM data programming disable)	0: None (or programming enable) 1: Power Down (or programming disable)
reg <452>	Power Divider Power	0: Power down 1: Power On
reg <453>	POR Auto Power detect	0: Enable 1: Disable
reg <454>	Charge pump for analog block enable (when VDD <= 2.7 V turn on)	0: Disable (automatic on/off control) 1: Enable (always on)
reg <455>	VDD bypass enable	0: Regulator auto on 1: Regulator off (VDD bypass)"
reg <471:456>	Reserved	Reserved
reg <479:472>	Reserved	Reserved

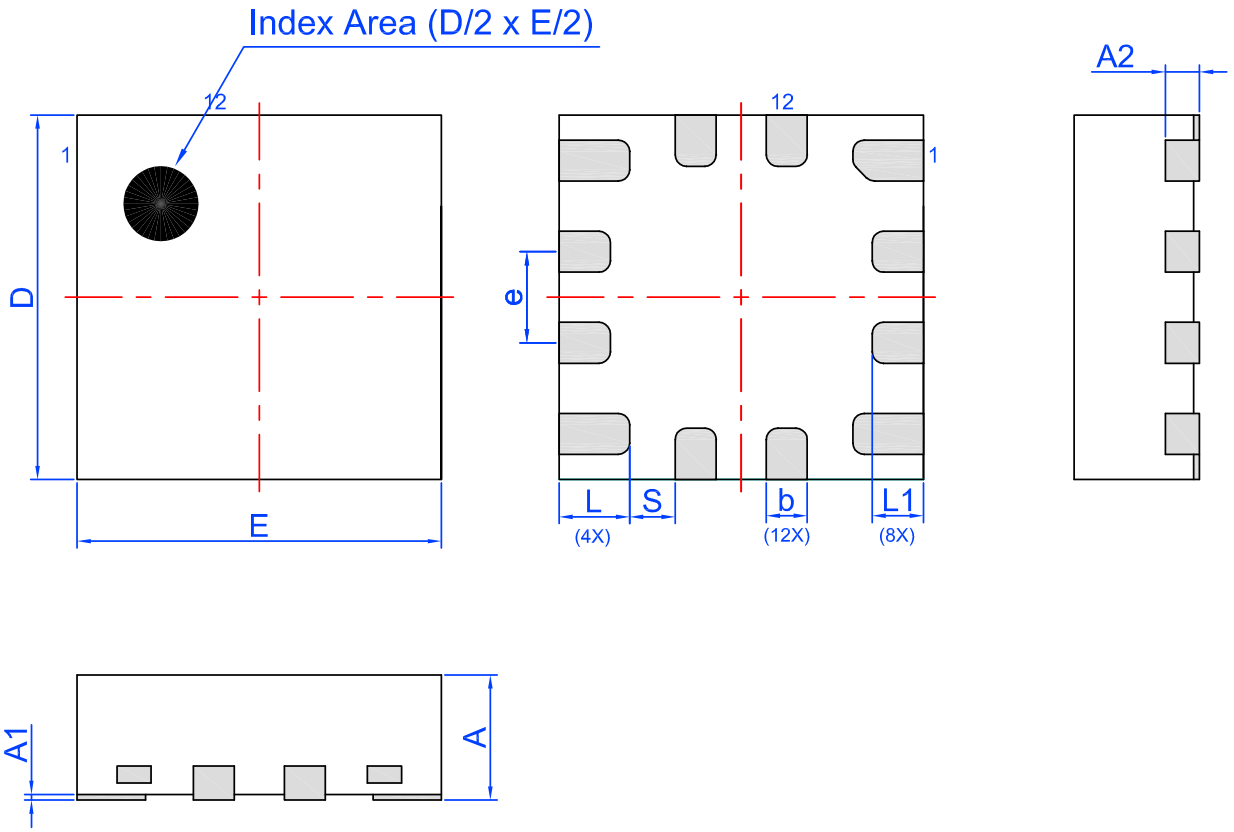
Register Bit Address	Signal Function	Register Bit Definition
reg <481:480>	Reserved	Reserved
reg <482>	PIN2 edge detect mode	0: rising edge 1: falling edge
reg <483>	Bypass the PIN2	0: PIN2 edge active 1: PIN2 high active
reg <484>	PIN2 reset enable	0: Disable 1: Enable
reg <485>	programmable delay or filter output select	0: programmable delay output 1: filter output
reg <487:486>	Select the edge mode of programmable delay & edge detector	00: rising edge detector 01: falling edge detector 10: both edge detector 11: both edge delay
reg <489:488>	Delay value select for programmable delay & edge detector (VDD = 3.3 V, typical condition)	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
reg <490>	Reserved	Reserved
reg <495:491>	Reserved	Reserved
reg <501:496>	Reserved	Reserved
reg <502>	Reserved	Reserved
reg <503>	Reserved	Reserved
reg <511:504>	Reserved	Reserved

16.0 Package Top Marking System Definition



17.0 Package Drawing and Dimensions

12 Lead STQFN FC Package 1.6 x 1.6 mm
IC net weight: 0.0028 g



Unit: mm

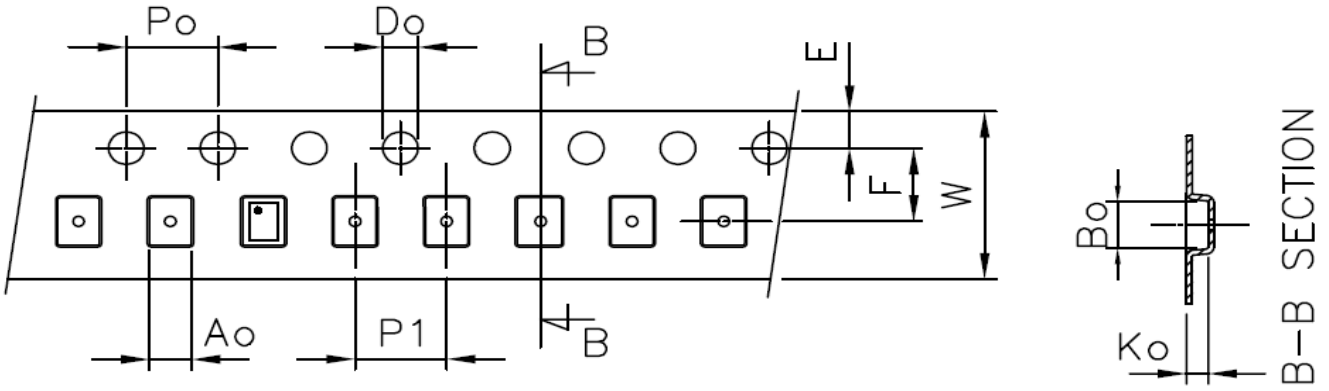
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

18.0 Tape and Reel Specifications

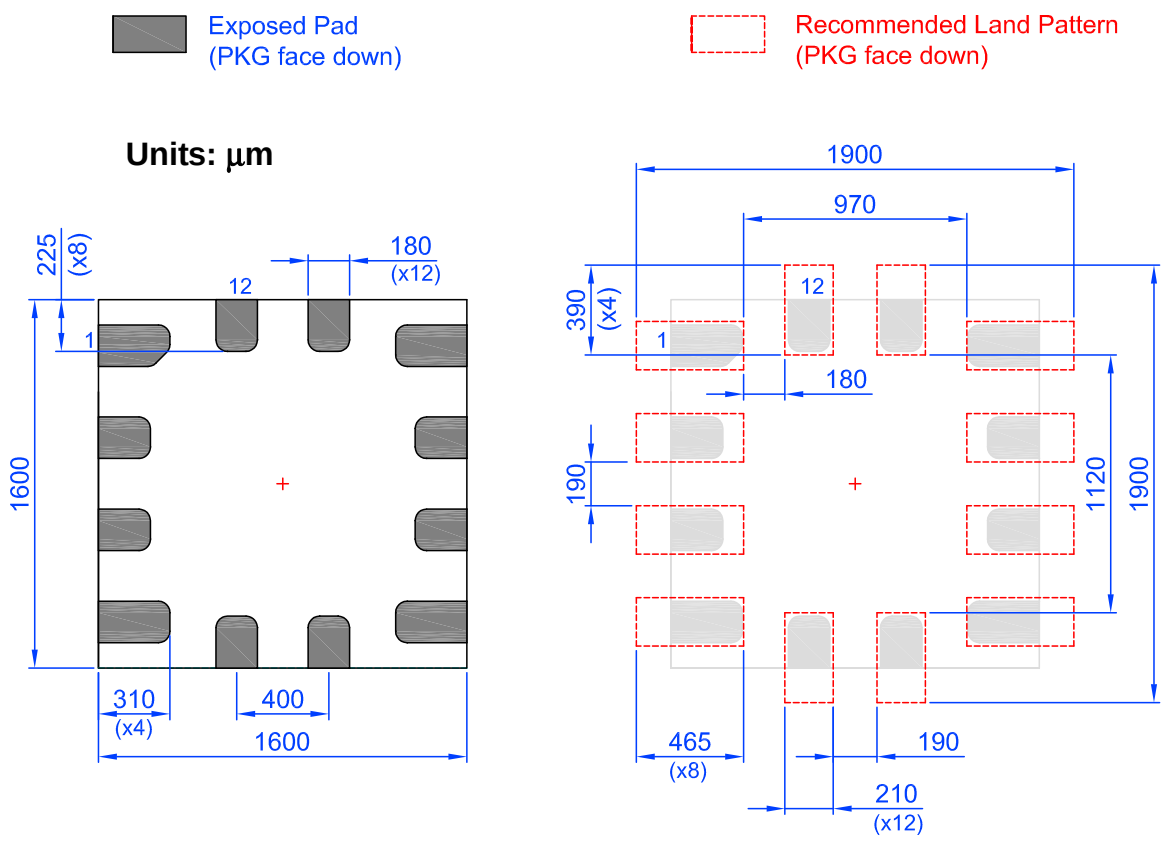
Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FC 0.4P Green	10	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

18.1 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FC 0.4P Green	1.9	1.9	0.8	4	4	1.5	1.75	3.5	8



19.0 Recommended Land Pattern



20.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

21.0 Revision History

Date	Version	Change
9/3/2014	0.57	Updated Electrical Characteristics VIH/VIL/VOH/VOL values
8/25/2014	0.56	Added Recommended Land Pattern
7/23/2014	0.55	Fixed ESD information
6/20/2014	0.54	Fixed typo on Electrical Spec
5/21/2014	0.53	Updated block diagram Fixed typos Moved Programmable Delay and Deglitch Filter to Combination Macrocells section
4/29/2014	0.52	Added ESD Ratings and MSL to Absolute Maximum Conditions
3/28/2014	0.5	Fixed typos Preliminary Release
3/18/2014	0.42	Updated block diagrams and timing diagrams for clarity
2/12/2014	0.41	Fixed typos
12/2/2013	0.4	Updated VIH/VIL in Electrical Characteristics Fixed typos Added IC net weight to Package Specification
11/25/2013	0.31	Added Block Diagram
11/11/2013	0.3	Added Diagrams
9/30/2013	0.2	Updated Electrical Characteristics Added Register Table and Descriptions
9/16/2013	0.1	Initial release

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