## /VI/IXI/VI Microprocessor-Compatible, 14-Bit DACs

#### General Description

The MX7534/MX7535 are high-performance, CMOS, monolithic, 14-bit digital-to-analog converters (DACs). Wafer-level, laser-trimmed, thin-film resistors and temperature-compensated NMOS switches assure operation over the full operating temperature range with exceptional linear and gain stability.

The MX7534 accepts right-justified data in two bytes from an 8-bit bus, while the MX7535 operates with a 14-bit data bus with separate MS-byte and LS-byte select controls. In addition, all digital inputs are compatible with both TTL and 5V CMOS-logic levels. The MX7534/MX7535 are intended for unipolar operation, but may be operated as bipolar DACs with additional external components. Both devices are protected against CMOS latchup, and neither requires the use of external Schottky protection diodes.

The MX7534 is available in 20-pin narrow (0.3") DIP, wide SO, or PLCC packages. The MX7535 is available in 28-pin, 600 mil wide DIP, wide SO, or PLCC packages.

#### Applications

Machine and Motion Control Systems Automatic Test Equipment **Digital Audio** µP-Controlled Calibration Circuitry Programmable-Gain Amplifiers **Digitally Controlled Filters** Programmable Power Supplies

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#### Pin Configurations

#### Features

- ♦ 14-Bit Monotonic Over Full Temperature Range
- Full 4-Quadrant Multiplication
- µP-Compatible, Double-Buffered Inputs
- Exceptionally Low Gain Tempco (2.5ppm/°C)
- Low Output Leakage (<20nA) Over Temp.</p> Low Power Consumption
- TTL and CMOS Compatible

#### Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
<b>MX7534</b> KN	0°C to +70°C	20 Plastic DIP	±1
MX7534JN	0°C to +70°C	20 Plastic DIP	±2
MX7534KCWP	0°C to +70°C	20 SO	±1
MX7534JCWP	0°C to +70°C	20 SO	±2
MX7534KP	0°C to +70°C	20 PLCC	±1
MX7534JP	0°C to +70°C	20 PLCC	±2
MX7534J/D	0°C to +70°C	Dice*	±2
MX7534BQ	-25°C to +85°C	20 CERDIP	±1
MX7534AQ	-25°C to +85°C	20 CERDIP	±2
MX7534BD	-25°C to +85°C	20 Ceramic SB	±1
MX7534AD	-25°C to +85°C	20 Ceramic SB	±2
MX7534KEWP	-40°C to +85°C	20 SO	±1
MX7534JEWP	-40°C to +85°C	20 SO	±2
MX7534TQ	-55°C to +125°C	20 CERDIP	±1
MX7534SQ	-55°C to +125°C	20 CERDIP	±2
MX7534TD	-55°C to +125°C	20 Ceramic SB	±1
MX7534SD	-55°C to +125°C	20 Ceramic SB	±2

Ordering Information continued at end of data sheet. \*Dice are tested at +25°C, DC parameters only.

#### Functional Diagrams

MAXIM MX7534

- RFB

<u>17</u> WR

IOUT

AGNDS 5\_ AGNOF

Maxim Integrated Products 1

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

#### **ABSOLUTE MAXIMUM RATINGS**

28-Pin PLCC (derate 10.53mW/°C above 20-Pin CERDIP (derate 11.11mW/°C abov 28-Pin CERDIP (derate 16.67mW/°C abov 20 Pin Ceramic SB	+70°C)842mW /e +70°C)889mW /e +70°C)1.33W
(derate 11.76mW/°C above +70°C)	
28-Pin Ceramic SB	
(derate 20.00mW/°C above +70°C)	1.6W
Operating Temperature Ranges	
MX753_J/K	0°C to +70°C
MX753_A/B	25°C to +85°C
MX753_EW	40°C to +85°C
MX753_S/T	55°C to +125°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{DD} = +11.4V \text{ to } +15.75V \text{ (Note 1)}, V_{REF} = 10V, V_{IOUT} = V_{AGNDS} = V_{SS} = 0V, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.})$ 

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS		
DC ACCURACY	DC ACCURACY									
Resolution					14			Bits		
Polative Accuracy	INU	MX753_K/B/T					±1	LCD		
Relative Accuracy	INL	MX753_J/A/S					±2	LSD		
Differential Nonlinearity		Guaranteed Mo	onotonic				±1	LSB		
Full Scalo Error		Measured with	internal R <sub>FB</sub> ,	MX753_K/B/T			$\pm 4$	ISP		
		current and gai	n TC	MX753_J/A/S			±8			
Gain Temperature Coefficient		MX753_K/B/T				±0.5	±2.5	nnm/°C		
(Note 2)		MX753_J/A/S				±0.5	±5	ppin/ C		
		All digital inputs at OV $T_A = +25^{\circ}C$		2			±5			
Output Leakage Current	IOUT	All digital	All digital	All digital	T <sub>A</sub> = T <sub>MIN</sub>	MX753_J/K/A/B			±25	nA
		$V_{SS} = 0V$	to T <sub>MAX</sub>	MX753_S/T			±150			
REFERENCE INPUT										
Reference Voltage Input Resistance (Note 3)	R <sub>REF</sub>				3.5	6	10	kΩ		
DIGITAL INPUTS	1									
Input High Voltage	Vinh				2.4			V		
Input Low Voltage	VINL						0.8	V		
Input Lookago Current		Digital inputs	$T_A = +25^{\circ}C$				±1			
		at 0V or V <sub>DD</sub>	TA = TMIN t	o T <sub>MAX</sub>			±10			
Input Capacitance (Note 2)	CIN						7	pF		

#### **ELECTRICAL CHARACTERISTICS (continued)**

(V<sub>DD</sub> = +11.4V to +15.75V (Note 1), V<sub>REF</sub> = 10V, V<sub>IOUT</sub> = V<sub>AGNDS</sub> = V<sub>SS</sub> = 0V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIO	MIN	TYP I	MAX	UNITS		
POWER REQUIREMENTS								
Positive Supply-Voltage Range	V <sub>DD</sub>	For specific performance	11.4	1	5.75	V		
Negative Supply-Voltage Range	V <sub>SS</sub>	For specific performance	-200		-500	mV		
Positivo Supply Current	Inn	Digital inputs at	MX7534			3	m۸	
Positive Supply Current	עטי	V <sub>INH</sub> or V <sub>INL</sub> MX7535				4	IIIA	
Negative Supply Current	ISS	Digital inputs at 0V or V <sub>DD</sub>			500	μΑ		

Note 1: Specifications are guaranteed for  $V_{DD}$  of +11.4V to +15.75V. At  $V_{DD}$  = +5V, device is still functional with degraded specifications. Note 2: Guaranteed by design, not tested.

Note 3: Resistors have a typical -300ppm/°C tempco.

#### AC PERFORMANCE CHARACTERISTICS (Note 4)

 $(V_{DD} = +11.4V \text{ to } +15.75V, V_{REF} = 10V, V_{IOUT} = V_{AGND} (V_{AGNDS} \text{ for } MX7535) = V_{SS} = 0V$ , output amplifier is AD544\*, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIC	MIN	TYP	MAX	UNITS			
Output Current Setting Time		$\begin{array}{l} T_A = +25^\circ C, \mbox{ to } 0.003\% \mbox{ of full-scale range,} \\ IOUT \mbox{ load } = 100\Omega \mbox{    13pF, DAC register} \\ alternately \mbox{ loaded with all 1s and all 0s} \end{array}$			0.8	1.5	μs		
Digital-to-Analog Glitch Impulse		$\begin{array}{l} \mbox{Measured with } V_{REF} = 0V, \\ \mbox{IOUT loads} = 100\Omega ~   ~13pF, DAC register \\ \mbox{alternately loaded with all 1s and all 0s} \end{array}$			50		nV-sec		
Multiplying Feedthrough Error		$V_{\text{REF}} = \pm 10V$ , $10kHz$	$T_A = +25^{\circ}C$		3		m\/n n		
(Note 5)		loaded with all 0s	$T_A = T_{MIN}$ to $T_{MAX}$		5		IIIVP-P		
Power Supply Pajaction		AV/DD - 15%	$T_A = +25^{\circ}C$			±0.01	0/ 10/		
Fower-Supply Rejection		$\Delta V DD = \pm 5.00$	$T_A = T_{MIN}$ to $T_{MAX}$			±0.02	/0/ /0		
	Court	DAC register loaded with a	III 1s			260	nE		
	001	DAC register loaded with all 0s		DAC register loaded with all 0s				130	
Output Noise Voltage Density (10Hz–100kHz)		Measured between RFB an		15		nV/Hz			

Note 4: These characteristics are included for design guidance only, and are not subject to test.

Note 5: Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

\* AD544 is an Analog Devices part.

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#### TIMING CHARACTERISTICS (MX7534)

 $(V_{DD} = +11.4V \text{ to } +15.75V, V_{REF} = 10V, V_{IOUT} = V_{AGND} = V_{SS} = 0V, T_A = T_{MIN} \text{ to } T_{MAX}$ , unless otherwise noted. See Figure 1a for timing diagram.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Address Valid to Write Setup Time	t <sub>1</sub>		0			ns
Address Valid to Write Hold Time	t2		0			ns
		$T_A = +25^{\circ}C$	60			
Data Setup Time	t <sub>3</sub>	$T_A = -25^{\circ}C \text{ to } +85^{\circ}C$	70			ns
		T <sub>A</sub> = -55°C to +125°C	80			1
		$T_A = +25^{\circ}C$	20			
Data Hold Time	t4	$T_A = -25^{\circ}C \text{ to } +85^{\circ}C$	20	20		ns
		T <sub>A</sub> = -55°C to +125°C	30			
Chip-Select to Write-Setup Time	t <sub>5</sub>		0			ns
Chip-Select to Write-Hold Time	t6		0			ns
			$T_{A} = +25^{\circ}C$ 170			
Write Pulse Width	t7	$T_A = -25^{\circ}C \text{ to } +85^{\circ}C$	200			ns
		T <sub>A</sub> = -55°C to +125°C	240			1

#### **TIMING CHARACTERISTICS (MX7535)**

 $(V_{DD} = +11.4V \text{ to } +15.75V, V_{REF} = 10V, V_{IOUT} = V_{AGNDS} = V_{SS} = 0V, T_A = T_{MIN} \text{ to } T_{MAX}$ , unless otherwise noted. See Figure 1b for timing diagram.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSMSB or CSLSB to WR Setup Time	t1		0			ns
CSMSB or CSLSB to WR Hold Time	t2		0			ns
		$T_A = +25^{\circ}C$	170			
LDAC Pulse Width	t3	$T_{A} = -25^{\circ}C \text{ to } +85^{\circ}C$	200			ns
		$T_A = -55^{\circ}C \text{ to } + 125^{\circ}C$	240			1
		$T_A = +25^{\circ}C$	170			
Write Pulse Width	t4	$T_A = -25^{\circ}C \text{ to } +85^{\circ}C$	200	200		ns
		T <sub>A</sub> = -55°C to +125°C	240			
		$T_A = +25^{\circ}C$	140	40 60		
Data-Setup Time	t <sub>5</sub>	$T_{A} = -25^{\circ}C \text{ to } +85^{\circ}C$	160			ns
		T <sub>A</sub> = -55°C to +125°C 180				
		$T_A = +25^{\circ}C$	20			
Data-Hold Time	t <sub>6</sub>	$T_A = -25^{\circ}C \text{ to } +85^{\circ}C$	20			ns
		$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$	30			

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PIN	NAME	FUNCTION
1	REF	Reference Input to DAC
2	RFB	Feedback Resistor. Used to close the loop around an external op amp.
3	IOUT	Current Output
4	AGNDS	Analog Ground Sense. Reference point for external circuitry. AGNDS should carry minimum current.
5	AGNDF	Analog Ground Force. Carries current from internal analog ground connec- tions. AGNDS and AGNDF are tied together internally.
6	DGND	Digital Ground
7	D7	Data Bit 7
8	D6	Data Bit 6
9	D5	Data Bit 5 or Data Bit 13 (MSB)
10	D4	Data Bit 4 or Data Bit 12
11	D3	Data Bit 3 or Data Bit 11
12	D2	Data Bit 2 or Data Bit 10
13	D1	Data Bit 1 or Data Bit 9
14	D0	Data Bit 0 (LSB) or Data Bit 8
15	A1	Address Input 1
16	A0	Address Input 0
17	WR	Write Input. Active low.
18	CS	Chip-Select Input. Active low.
19	Vdd	+12V to +15V Supply-Voltage Input
20	Vss	Bias pin for high-temperature, low-leakage configuration

## \_Pin Description (MX7534)

### Pin Description (MX7535)

PIN	NAME	FUNCTION
1	REFS	Reference Voltage Sense
2	REFF	Reference Voltage Force
3	RFB	Feedback Resistor. Used to close the loop around an external op amp.
4	IOUT	Current Output
5	AGNDS	Analog Ground Sense. Reference point for external circuitry. This pin should carry minimum current.
6	AGNDF	Analog Ground Force. Carries current from internal analog ground connections. AGNDS and AGNDF are tied together internally.
7	DGND	Digital Ground
8	D13	Data Bit 13 (MSB)
9	D12	Data Bit 12
10	D11	Data Bit 11
11	D10	Data Bit 10
12	D9	Data Bit 9
13	D8	Data Bit 8
14	D7	Data Bit 7
15	D6	Data Bit 6
16	D5	Data Bit 5
17	D4	Data Bit 4
18	D3	Data Bit 3
19	D2	Data Bit 2
20	D1	Data Bit 1
21	D0	Data Bit 0 (LSB)
22	CSMSB	Chip-Select Most Significant Byte. Active low.
23	LDAC	Asynchronous Load DAC Input. Active low.
24	CSLSB	Chip-Select Least Significant Byte. Active low.
25	WR	Write Input. Active low.
26	VDD	+12V to +15V Supply-Voltage Input
27	V <sub>SS</sub>	Bias pin for high-temperature, low-leakage configuration
28	N.C.	No Connection. Not internally connected.
	-	

MX7534/MX7535



Figure 1a. MX7534 Timing Diagram

#### \_Detailed Description

#### **Digital-to-Analog Section**

The basic MX7534/MX7535 digital-to-analog converter (DAC) circuit consists of a laser-trimmed, thin-film, 11-bit R-2R resistor array, a 3-bit segmented resistor array, and NMOS current switches, as shown in Figure 2. The three MSBs are decoded to drive switches A–G of the segmented array, and the remaining bits drive switches S0–S10 of the R-2R array.

Binary weighted currents are switched to either AGNDF or IOUT, depending on the status of each input bit. The R-2R ladder current is one-eighth of the total reference input current. The remaining seven-eighths of the current flows in the segmented resistors, dividing equally among these seven resistors. The input resistance at REF is constant; therefore, it can be driven by a voltage or current source of positive or negative polarity.

The MX7534/MX7535 are optimized for unipolar output operation (analog output from 0V to -VREF), although bipolar operation (analog output from +VREF to -VREF) is possible with some added external components.

Figure 3 shows the equivalent circuit for the two DACs.  $C_{OUT}$  varies from about 90pF to 180pF, depending on the digital code.  $R_0$  denotes the DAC'S equivalent output resistance, which varies with the input code.



Figure 1b. MX7535 Timing Diagram

 $g(V_{REF},N)$  is the Thevenin equivalent voltage generator due to the reference input voltage,  $V_{REF}$ , and the transfer function of the R-2R ladder, N.

#### **Digital Section**

All digital inputs are both TTL and 5V CMOS logic compatible. The digital inputs are protected from electrostatic discharge (ESD) with typical input currents of less than 1nA. To minimize power-supply currents, keep digital input voltages as close to 0V and 5V logic levels as possible.

#### Applications Information

#### Unipolar Operation (2-Quadrant Multiplication)

Figures 4a and 4b show the circuit diagram for unipolar binary operation. With an AC input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table 2.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high-speed op amps are used. Note that the output polarity is the inverse of the reference input.

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#### Zero-Offset Adjustment (Figures 4a and 4b)

- 1) Load the DAC register with all 0s.
- 2) Adjust the offset of amplifier A1 so that V<sub>0</sub> (see figure) is at a minimum (i.e.,  $\leq 30\mu$ V).

#### Gain Adjustment (Figures 4a and 4b)

- 1) Load the DAC register with all 1s.
- 2) Trim potentiometer R1 so that VOUT = -VIN  $\left(\frac{16383}{16384}\right)$

In fixed-reference applications, adjust full scale by omitting R1 and R2 and trimming the reference voltage magnitude. In many applications, the excellent Gain Tempco and Gain Error specifications eliminate the need for gain adjustment. However, if trims are required and the DAC is to operate over a wide temperature range, use low-tempco (>300ppm/°C) resistors.

#### **Bipolar Operation** (4-Quadrant Multiplication)

Bipolar or 4-quadrant operation is shown in Figures 5a and 5b. This configuration provides for offset binary coding. Table 4 shows DAC codes and the corresponding analog outputs for Figures 5a and 5b. With the DAC loaded to 10 0000 0000 0000, either adjust R1 for V<sub>OUT</sub> = 0V, or omit R1 and R2 and adjust the ratio of R5 and R6 for  $V_{OUT}$  = 0V. Adjust the amplitude of  $V_{IN}$ or vary the value of R7 for full-scale trimming.

Resistors R5, R6, and R7 must be matched to 0.003%. Mismatch of R5 and R6 causes both offset and fullscale errors. For wide temperature range operation, use resistors of the same material so that their temperature coefficients match and track.



Figure 3. Equivalent Analog Output Circuit

#### Table 1. MX7534 Logic States

WR	CS	A1	A2	FUNCTION
Х	1	Х	Х	Device not selected (Note 1)
1	Х	Х	Х	No data transfer
0	0	0	0	DAC loaded directly from Data Bus (Note 2)
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers

Note 1: X = Don't Care.

Note 2: When A1 = 0 and A0 = 0, all DAC registers are transparent. By placing all 0s or all 1s on the data inputs, the user can load the DAC to zero or full-scale output in one write operation. This simplifies system calibration.

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Figure 4a. Unipolar Binary Operation

14-Bit DACs

#### Grounding Considerations

Since IOUT and the output amplifier noninverting input are sensitive to offset voltages, connect nodes that must be grounded directly to a single-point ground through a separate, very-low-resistance path. Note that the output currents at IOUT and AGNDF vary with input code and create code-dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

To obtain high accuracy, it is important to use a proper grounding technique. The two AGND pins (AGNDF, AGNDS) provide flexibility in this respect. In Figures 4a and 4b, AGNDS and AGNDF are shorted together externally and an extra op amp, A2, is not used. Voltage-drops due to bond-wire resistance are not compensated for in this circuit; this could create a linearity error of approximately 0.1LSB due to bond-wire resistance alone. This can be eliminated by using the circuits shown in Figures 6a and 6b, where A2 maintains AGNDS at signal ground potential. By using force/sense techniques, all switch contacts on the DAC are kept at exactly the same potential, and any error caused by bond-wire resistance is eliminated

Figure 7 shows a remote voltage reference driving the MX7535. Op amps A2 and A3 compensate for voltage drops along the reference input line and analog ground line.

Figure 8 shows a printed circuit board (PCB) layout with a single output amplifier for the MX7534. The input to REF (Pin 1) is shielded to reduce AC feedthrough, while the digital inputs are shielded to minimize digital



Figure 4b. Unipolar Binary Operation

	BINARY DAC R	NUMBER I EGISTER	ANALOG OUTPUT (Vout)	
MSB 11	1111	1111	LSB 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10	0000	0000	0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -\frac{1}{2}V_{IN}$
00	0000	0000	0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00	0000	0000	0000	OV

Table 2. Unipolar Binary Code Table

feedthrough. The traces connecting IOUT and AGNDS

to the inverting and noninverting op amp inputs are kept as short as possible. Gain trim components, R3 and R4, are omitted.

#### Zero-Offset Adjustment (Figures 6a and 6b)

- 1) Load DAC register with all 0s.
- 2) Adjust offset of amplifier A2 for minimum potential at AGNDS. This potential should be ≤30µV with respect to signal ground.
- 3) Adjust A1's offset so that VOUT is at a minimum (i.e., ≤30µV).

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8



Figure 5a. Bipolar Operation

#### Gain Adjustment (Figures 6a and 6b)

- 1) Load DAC register with all 1s.
- 2) Trim potentiometer R3 so that VOUT =  $-\left(\frac{16383}{16384}\right)$ VIN

#### Low-Leakage Configuration

Leakage current in the DAC flowing into the IOUT line can cause gain, linearity, and offset errors. Leakage is worse at high temperatures.

Negatively bias Vss for a high-temperature, low-leakage configuration.

#### **Dynamic Considerations**

In static or DC applications, the output amplifier's AC characteristics are not critical. In higher-speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the output op amp's AC parameters must be considered.

Another error source in dynamic applications is the parasitic signal coupling from the REF terminal to IOUT. This is normally a function of board layout and lead-tolead package capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough depends on circuitboard layout and on-chip capacitive coupling. Minimize layout-induced feedthrough with guard traces between digital inputs, REF, and DAC outputs.



Figure 5b. Bipolar Operation

#### Table 3. MX7535 Logic States

CSMSB	CSLSB	LDAC	WR	FUNCTION
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load LS and MS Input Registers
1	1	0	Х	Load DAC Register from Input Register
0	0	0	0	All registers are transparent.
1	1	1	Х	No operation
Х	Х	1	1	No operation

Note: X = Don't Care.

#### Table 4. Offset Binary Bipolar Code Table

BINARY NUMBER IN DAC REGISTER				Analog Output (Vout)
MSB 11	1111	1111	LSB 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10	0000	0000	0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10	0000	0000	0000	0
01	1111	1111	1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00	0000	0000	0000	$-V_{IN}\left(\frac{8192}{8192}\right) = -V_{IN}$

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Figure 6a. Unipolar Binary Operation with Forced Ground

Table 5. Amplifier Performance Comparisons



Figure 6b. Unipolar Binary Operation with Forced Ground for Remote Load

OP AMP	INPUT OFFSET VOLTAGE (V <sub>OS</sub> )	INPUT BIAS CURRENT (I <sub>B</sub> )	OFFSET VOLTAGE DRIFT (TC V <sub>OS</sub> )	SETTLING TO 0.003% FS
MAX400	10µV	2nA	0.3µV/°C	50µs
Maxim OP07	25µV	2nA	0.6µV/°С	50µs
AD554L*	500µV	25pA	5µV/°C	5µs
HA2620*	4mV	35nA	20µV/°C	0.8µs

\* AD544L is an Analog Devices part; HA2620 is a Harris Semiconductor part.

#### Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high-speed output amplifier. The capacitor cancels the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op amp used, but typical values range from 10pF to 33pF. Too small a value causes output ringing, while excess capacitance overdamps the output. Minimize C1's size and improve output settling performance by keeping the PC board trace as short as possible and stray capacitance at IOUT as small as possible.

#### Bypassing

Place a 1 $\mu$ F bypass capacitor, in parallel with a 0.01 $\mu$ F ceramic capacitor, as close to the DAC's V<sub>DD</sub> and GND pins as possible. Use a 1 $\mu$ F tantalum bypass capacitor to optimize high-frequency noise rejection. Place a 4.7 $\mu$ F decoupling capacitor at V<sub>SS</sub> to minimize the DAC output leakage current.

The MX7534/MX7535 have high-impedance digital inputs. To minimize noise pickup, connect them to either V<sub>DD</sub> or GND terminals when not in use. Connect active inputs to V<sub>DD</sub> or GND through high-value resistors (1M $\Omega$ ) to prevent static charge accumulation if these pins are left floating, as might be the case when a circuit card is left unconnected.

#### **Op-Amp Selection**

Input offset voltage (Vos), input bias current (IB), and offset voltage drift (TC Vos) are three key parameters in determining the choice of a suitable amplifier. To maintain specified accuracy with V<sub>REF</sub> of 10V, Vos should be less than 30µV and IB should be less than 2nA. Open-loop gain should be greater than 340,000. Maxim's MAX400 has low Vos (10µV max), low IB (2nA), and low TC Vos (0.3µV/°C max). This op amp can be used without requiring any adjustments. For



Figure 7. Driving the MX7535 with a Remote Voltage Reference

medium-frequency applications, the OP27 is recommended. For higher-frequency applications, the HA-2620 is recommended. However, these op amps require external offset adjustment (Table 5).

### \_Microprocessor Interfacing

#### 8086 with MX7535

The MX7534/MX7535 interface to both 8-bit and 16-bit processors. Figure 9a shows the 8086 16-bit processor interfacing to a single MX7535. In this setup, the doublebuffering feature of the DAC is not used. ADO-AD13 of the 16-bit data bus are connected to the DAC data bus (D0-D13). The 14-bit word is written to the DAC in one MOV instruction, and the analog output responds immediately. In this example, the DAC address is D000. Table 6a shows a software routine for Figure 9a.

In a multiple DAC system, the double buffering of the DAC chips allows the user to simultaneously update all DACs. In Figure 10, a 14-bit word is loaded to each of the DAC's input registers in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., LDAC) is brought low, updating all the DACs simultaneously.

#### 8086 with MX7534

Figure 9b shows an interface circuit to a 16-bit microprocessor. The bottom 8 bits (AD0-AD7) of the 16-bit data bus are connected to the DAC data bus. The



Figure 8. Suggested Layout for MX7534 Incorporating Output Amplifier

14-bit word is loaded in two bytes, using the MOV instruction. A further MOV loads the DAC register and causes the analog data to appear at the converter output. For the example given here, the appropriate DAC register addresses are D002, D004, and D006. Table 6b shows the program for loading the DAC.

#### 8085A with MX7534

A typical interface circuit is shown in Figure 9c. The DAC is treated as four memory locations addressed by A0 and A1. In standard operation, three of these memory locations are used. Table 6c shows a sample program for loading the DAC with a 14-bit word. The MX7534 has address locations 3000–3003.

The six MSBs are written into location 3001, and eight LSBs are written to 3002. Then, with a write instruction to 3003, the full 14-bit word is loaded to the DAC register.

**MIXIM** 

#### MC68000 with MX7535

Figure 11a shows an interface diagram. The following routine writes data to the DAC input registers and then outputs the data via the DAC register:

01000	MOVE.W	#W,D0	DAC data, W, loaded into Data Register 0.
MOVE.\	N	D0,\$E000	Data W transferred between D0 and DAC Register.
	MOVE.B	#228,D7	Control returned to the System.
	TRAP	#14	Monitor Program

#### MC68000 with MX7534

Figure 11b shows the MC68000 interface diagram. The following routine writes data to the DAC input registers and then outputs the data via the DAC register:

	.A2 E003		Address Register 2 loaded with E003.
01000	MOVE.W	#W,D0	DAC data, W, loaded into Data Register 0.
	MOVEP.W	D0,\$0000(A2)	Data W transferred between D0 and the DAC's Input Register. High-ordered byte trans- ferred first. Memory address specified using the address register indirect plus displace- ment addressing mode. Address used here (E003) is odd, so data is transferred on the low- order half of the data bus (D0–D7).
	MOVE.W	D0,\$E006	This instruction provides appropriate signals to transfer data W from the DAC Input Register to the DAC Register, which controls the R-2R ladder switches.
	MOVE.B	#228,D7	Control returned to the System.
	TRAP	#14	Monitor Program
Since	this interfac	ing system us	ses only the lower half of

Since this interfacing system uses only the lower half of the data bus, it is also suitable for use with the MC68008, which provides the user with an 8-bit data bus instead of the MC68000's 16-bit bus.



Figure 9a. MX7535—8086 Interface Circuit







Figure 9c. MX7534—8085A Interface Circuit

**MIXI/N** 

#### Table 6a. Sample Program for Loading the MX7535

	ASSUME DS:D DACLOAI	ACLOAD,CS:DACLOAD D SEGMENT AT 000	
00	8CC9	MOV CX,CS	:DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOVDS,CX	:TO CODE SEGMENT REGISTER
04	BF00D0	MOVDI,#D000	:LOAD DI WITH D000
07	C705"YZWX"	MOV MEM,#YZWX	:DAC LOADED WITH WXYZ
0B	EA0000		:CONTROL IS RETURNED TO THE MONITOR PROGRAM
0E	OOFF		

#### Table 6b. Sample Program for Loading the MX7534 from 8086

ASSUME DS:DACLOAD,CS:DACLOAD		DACLOAD, CS: DACLOAD	
	DACLOAD SEGMENT AT 000		
00	8CC9	MOV CX,CS	:DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOVDS,CX	:TO CODE SEGMENT REGISTER
04	BF02D0	MOVDI.#D002	:LOAD DI WITH D002
07	C605"MS"	MOV MEM,#"MS"	:DAC LOADED WITH "MS"
0A	47	INC DI	
0B	47	INC DI	
0C	C605"LS"	MOV MEM,#"LS"	:LS INPUT REGISTER LOADED WITH "LS"
OF	47	INC DI	
10	47	INC DI	
11	C60500	MOV MEM,#00	CONTENT OF INPUT REGISTERS ARE LOADED TO THE DAC REGISTER
14	EA0000	JMP MEM	:CONTROL IS RETURNED TO THE MONITOR PROGRAM

## Table 6c. Sample Program for Loading the MX7534 from 8085A

2000	26	MVIH,#30
01	30	
02	2E	MVIL,#01
03	01	
04	3E	MVIA,#"MS"
05	"MS"	
06	77	MOV M,A
07	2C	INR L
08	3E	MVI A#"LS"
09	"LS"	
0A	77	MOV M,A
0B	2C	INR L
0C	77	MOV M,A
200D	CF	RST I

#### Z80 with MX7534/MX7535

Figure 12a is an interface circuit for the Z80, using the MX7535. This is an example of an 8-bit processor interface for these DACs. Figure 12b shows the schematic for the MX7534.

#### MC6809 with MX7534

MX7534/MX7535

Figure 13a shows an interface circuit that enables the MX7534 to be programmed using the MC6809 8-bit microprocessor. Use the 16-bit D accumulator to simplify data transfer. The two key processor instructions are:

LDD Load D accumulator from memory

STD Store D accumulator to memory

#### MC6502 with MX7534

Figure 13b shows an interface diagram for the MC6502 using the MX7534.

#### Digital Feedthrough

In the interface diagrams shown in Figures 9–13, the digital inputs of the DAC are directly connected to the microprocessor bus. Even when the device is not selected, activity on the bus can feed through on the DAC output through package capacitance and appear as noise. To minimize noise, isolate the DACs from the digital bus, as shown in Figures 14a and 14b.

**WIXIW** 

MX7534/MX7535



Figure 10. MX7535—8086 Interface: Multiple DAC Systems



Figure 11a. MX7535—MC68000 Interface





**WIXIW** 



Figure 12a. MX7535—Z80 Interface







Figure 14a. MX7534—Interface Circuit Using Latches to Minimize Digital Feedthrough





Figure 13b. MX7534—6502 Interface



Figure 14b. MX7535—Interface Circuit Using Latches to Minimize Digital Feedthrough





#### \_Ordering Information (continued)

PART	TEMP. RANGE	PIN PACKAGE	INL (LSBs)
MX7535KN	0°C to +70°C	28 Plastic DIP	±1
MX7535JN	0°C to +70°C	28 Plastic DIP	±2
MX7535KCWI	0°C to +70°C	28 Wide SO	±1
MX7535JCWI	0°C to +70°C	28 Wide SO	±2
MX7535KP	0°C to +70°C	28 PLCC	±1
MX7535JP	0°C to +70°C	28 PLCC	±2
MX7535J/D	0°C to +70°C	Dice*	±2
MX7535BQ	-25°C to +85°C	28 CERDIP	±1
MX7535AQ	-25°C to +85°C	28 CERDIP	±2
MX7535BD	-25°C to +85°C	28 Ceramic SB	±1
MX7535AD	-25°C to +85°C	28 Ceramic SB	±2
MX7535KEWI	-40°C to +85°C	28 Wide SO	±1
MX7535JEWI	-40°C to +85°C	28 Wide SO	±2
MX7535TQ	-55°C to +125°C	28 CERDIP	±1
MX7535SQ	-55°C to +125°C	28 CERDIP	±2
MX7535TD	-55°C to +125°C	28 Ceramic SB	±1
MX7535SD	-55°C to +125°C	28 Ceramic SB	±2

\*Dice are tested at +25°C, DC parameters only.

\_\_Pin Configurations (continued)



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16

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