International
IOR Rectifier

Data Sheet No. PD60213 revL

IR2114SSPbF/IR2214SSPbF

HALF-BRIDGE GATE DRIVER IC

Features

- Floating channel up to 600 V or 1200 V
- Soft over-current shutdown
- Synchronization signal to synchronize shutdown with the other phases
- Integrated desaturation detection circuit
- Two stage turn on output for di/dt control
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- Undervoltage lockout with hysteresis band
- Lead free

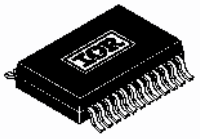
Description

The IR2114/IR2214 gate driver family is suited to drive a single half bridge in power switching applications. These drivers provide high gate driving capability (2 A source, 3 A sink) and require low quiescent current, which allows the use of bootstrap power supply techniques in medium power systems. These drivers feature full short circuit protection by means of power transistor desaturation detection and manage all half-bridge faults by smoothly turning off the desaturated transistor through the dedicated soft shutdown pin, therefore preventing over-voltages and reducing electromagnetic emissions. In multi-phase systems, the IR2114/IR2214 drivers communicate using a dedicated local network ($\overline{\text{SY\_FLT}}$ and $\overline{\text{FAULT/SD}}$ signals) to properly manage phase-to-phase short circuits. The system controller may force shutdown or read device fault state through the 3.3 V compatible CMOS I/O pin ($\overline{\text{FAULT/SD}}$). To improve the signal immunity from DC-bus noise, the control and power ground use dedicated pins enabling low-side emitter current sensing as well. Undervoltage conditions in floating and low voltage circuits are managed independently.

Product Summary

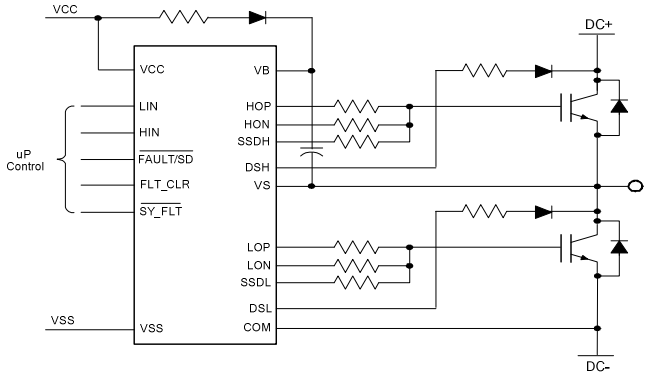
V_{OFFSET}	600 V or 1200 V max.
I_O+/- (min)	1.0 A / 1.5 A
V_{OUT}	10.4 V – 20 V
Deadtime matching (max)	75 ns
Deadtime (typ)	330 ns
Desat blanking time (typ)	3 µs
DSH, DSL input voltage threshold (typ)	8.0 V
Soft shutdown time (typ)	9.25 µs

Package



24-Lead SSOP

Typical connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}, all currents are defined positive into any lead The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		V_B - 25	V_B + 0.3	V
V_B	High side floating supply voltage	IR2114	-0.3	625	
		IR2214	-0.3	1225	
V_{HO}	High side floating output voltage (HOP, HON and SSDH)		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
COM	Power ground		V_{CC} - 25	V_{CC} + 0.3	
V_{LO}	Low side output voltage (LOP, LON and SSDL)		V_{COM} -0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN and FLT_CLR)		-0.3	V_{CC} + 0.3	
V_{FLT}	Fault input/output voltage ($\overline{\text{FAULT/SD}}$ and $\overline{\text{SY\_FLT}}$)		-0.3	V_{CC} + 0.3	
V_{DSH}	High side DS input voltage		V_S -3	V_B + 0.3	
V_{DSL}	Low side DS input voltage		V_{COM} -3	V_{CC} + 0.3	
dVs/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq 25$ °C		—	1.5	W
Rth_{JA}	Thermal resistance, junction to ambient		—	65	°C/W
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS}. The V_S offset rating is tested with all supplies biased at a 15 V differential.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage †		V_S + 11.5	V_S + 20	V
V_S	High side floating supply offset voltage ††	IR2114	V_{SS}	600	
		IR2214	V_{SS}	1200	
V_{HO}	High side output voltage (HOP, HON and SSDH)		V_S	V_S + 20	
V_{LO}	Low side output voltage (LOP, LON and SSDL)		V_{COM}	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage (Note 1)		11.5	20	
COM	Power ground		-5	5	
V_{IN}	Logic input voltage (HIN, LIN and FLT_CLR)		V_{SS}	V_{CC}	
V_{FLT}	Fault input/output voltage ($\overline{\text{FAULT/SD}}$ and $\overline{\text{SY\_FLT}}$)		V_{SS}	V_{CC}	
V_{DSH}	High side DS pin input voltage		V_S - 2.0	V_B	
V_{DSL}	Low side DS pin input voltage		V_{COM} - 2.0	V_{CC}	
t_{PWHIN}	High side pulse width for HIN input		1		µs
T_A	Ambient temperature		-40	125	°C

† While internal circuitry is operational below the indicated supply voltages, the UV lockout disables the output drivers if the UV thresholds are not reached. A minimum supply voltage of 8V is recommended for the driver to operate safely under switching conditions at VS pin (please refer to the “start-up sequence” in application section of this document)

†† Logic operational for V_S from V_{SS}-5 V to V_{SS} +600 V or 1200 V. Logic state held for V_S from V_{SS} -5 V to V_{SS}-V_{BS}. For a negative spike on V_B (referenced to V_{SS}) of less than 200ns the IC will withstand a sustained peak of -40V under normal operation and an isolated event of up to -70V peak spike (please refer to the Design Tip DT97-3 for more details).

Static Electrical Characteristics

V_{CC} = 15 V, V_{SS} = COM = 0 V, V_S = 600 V or 1200 V and T_A = 25 °C unless otherwise specified.

Pins: V_{CC}, V_{SS}, V_B, V_S (refer to Fig. 1)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	9.3	10.2	11.4	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	8.7	9.3	10.3		
V_{CCUVH}	V_{CC} supply undervoltage lockout hysteresis	—	0.9	—		
V_{BSUV+}	(V_B-V_S) supply undervoltage positive going threshold	9.3	10.2	11.4		V_S = 0 V, V_S = 600 V or 1200 V
V_{BSUV-}	(V_B-V_S) supply undervoltage negative going threshold	8.7	9.3	10.3		
V_{BSUVH}	(V_B-V_S) supply undervoltage lockout hysteresis	—	0.9	—		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V or 1200 V
I_{QBS}	Quiescent V_{BS} supply current	—	400	800		V_{IN} = 0 V or 3.3 V
I_{QCC}	Quiescent V_{CC} supply current	—	0.7	2.5	mA	no load

Pins: HIN, LIN, FLTCLR, $\overline{\text{FAULT/SD}}$, $\overline{\text{SY\_FLT}}$ (refer to Fig. 2, 3)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.0	—	—	V	V_{CC} = V_{CCUV-} to 20 V
V_{IL}	Logic "0" input voltage	—	—	0.8		
V_{IHSS}	Logic input hysteresis	0.2	0.4	—		
I_{IN+}	Logic "1" input bias current (HIN, LIN, FLTCLR)	—	330	—	µA	V_{IN} = 3.3 V
	Logic "0" input bias current ($\overline{\text{FAULT/SD}}$, $\overline{\text{SY\_FLT}}$)	0	—	1		
I_{IN-}	Logic "0" input bias current	-1	—	0		V_{IN} = 0 V
	Logic "1" input bias current ($\overline{\text{FAULT/SD}}$, $\overline{\text{SY\_FLT}}$)	-1	—	0		
$R_{ON,FLT}$	$\overline{\text{FAULT/SD}}$ open drain resistance	—	60	—	Ω	
$R_{ON,SY}$	$\overline{\text{SY\_FLT}}$ open drain resistance	—	60	—		PW≤ 7 µs

Pins: DSL, DSH (refer to Fig. 4)

V_{DESAT}, I_{DS} and I_{DSB} parameters are referenced to COM and V_S respectively for DSL and DSH.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{DESAT+}	High desat input threshold voltage	7.2	8.0	8.8	V	See Figs. 4,16
V_{DESAT-}	Low desat input threshold voltage	6.3	7.0	7.7		
V_{DSTH}	Desat input voltage hysteresis	—	1.0	—		
I_{DS+}	High DSH or DSL input bias current	—	21	—	µA	V_{DESAT} = V_{CC} or V_{BS}
I_{DS-}	Low DSH or DSL input bias current	—	-160	—		V_{DESAT} = 0 V

Pins: HOP, LOP (refer to Fig. 5)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{OH}	High level output voltage, $V_B - V_{HOP}$ or $V_{CC} - V_{LOP}$	—	40	300	mV	I_O= 20 mA
I_{O1+}	Output high first stage short circuit pulsed current	1	2	—	A	$V_{HOP/LOP}$= 0 V, H_{IN} or L_{IN} = 1, PW≤ 200 ns, resistive load, see Fig. 8
I_{O2+}	Output high second stage short circuit pulsed current	0.5	1	—		$V_{HOP/LOP}$= 0 V, H_{IN} or L_{IN}= 1, 400 ns ≤PW≤ 10 µs, resistive load, see Fig. 8

Pins: HON, LON, SSDH, SSDL (refer to Fig. 6)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{OL}	Low level output voltage, V_{HON} or V_{LON}	—	45	300	mV	I_O= 20 mA
$R_{ON,SSD}$	Soft Shutdown on resistance †	—	90	—	Ω	PW≤ 7 µs
I_{O-}	Output low short circuit pulsed current	1.5	3	—	A	$V_{HOP/LOP}$ = 15 V, H_{IN} or L_{IN} = 0, PW≤ 10 µs

† SSD operation only

AC Electrical Characteristics

V_{CC} = V_{BS} = 15 V, V_S = V_{SS} and T_A = 25 °C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn on propagation delay	220	440	660	ns	V_{IN} = 0 & 1, V_S = 0 V to 600 V or 1200 V, HOP shorted to HON, LOP shorted to LON, Fig. 7
t_{off}	Turn off propagation delay	220	440	660		
t_r	Turn on rise time (C_{LOAD}=1 nF)	—	24	—		
t_f	Turn off fall time (C_{LOAD}=1 nF)	—	7	—		
t_{on1}	Turn on first stage duration time	120	200	280		Fig. 8
t_{DESAT1}	DSH to HO soft shutdown propagation delay at HO turn on	2000	3300	4600		V_{HIN}= 1 V
t_{DESAT2}	DSH to HO soft shutdown propagation delay after blanking	1050	—	—		V_{DESAT} = 15 V, Fig. 10
t_{DESAT3}	DSL to LO soft shutdown propagation delay at LO turn on	2000	3300	4600		V_{LIN} = 1 V
t_{DESAT4}	DSL to LO soft shutdown propagation delay after blanking	1050	—	—		V_{DESAT} = 15 V, Fig. 10
t_{DS}	Soft shutdown minimum pulse width of desat	1000	—	—		Fig. 9
t_{SS}	Soft shutdown duration period	5700	9250	13500		V_{DS}=15 V, Fig. 9
$t_{SY\_FLT, DESAT1}$	DSH to $\overline{SY\_FLT}$ propagation delay at HO turn on	—	3600	—		V_{HIN} = 1 V
$t_{SY\_FLT, DESAT2}$	DSH to $\overline{SY\_FLT}$ propagation delay after blanking	1300	—	—		V_{DS} = 15 V, Fig. 10
$t_{SY\_FLT, DESAT3}$	DSL to $\overline{SY\_FLT}$ propagation delay at LO turn on	—	3050	—		V_{LIN} = 1 V
$t_{SY\_FLT, DESAT4}$	DSL to $\overline{SY\_FLT}$ propagation delay after blanking	1050	—	—		V_{DESAT}=15 V, Fig. 10
t_{BL}	DS blanking time at turn on	—	3000	—		V_{HIN} = V_{LIN} = 1 V, V_{DESAT}=15 V, Fig. 10
Deadtime/Delay Matching Characteristics						
DT	Deadtime	—	330	—		Fig. 11
MDT	Deadtime matching, MDT=DTH-DTL	—	—	75		External DT = 0 s, Fig. 11
PDM	Propagation delay matching, Max (ton, toff) – Min (ton, toff)	—	—	75		External DT > 500 ns, Fig. 7

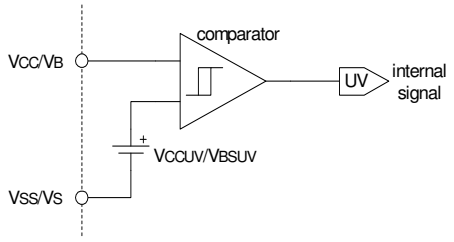


Figure 1: Undervoltage Diagram

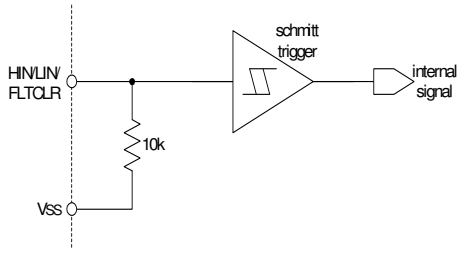


Figure 2: HIN, LIN and FLTCLR Diagram

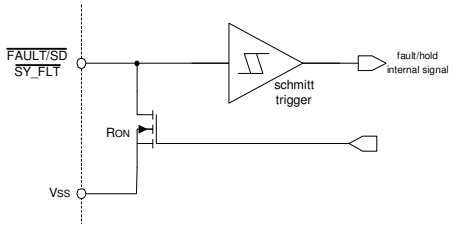


Figure 3: $\overline{\text{FAULT/SD}}$ and $\overline{\text{SY\_FLT}}$ Diagram

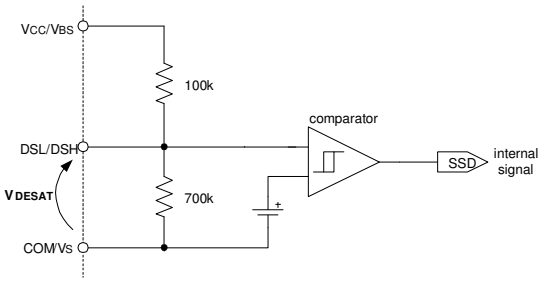


Figure 4: DSH and DSL Diagram

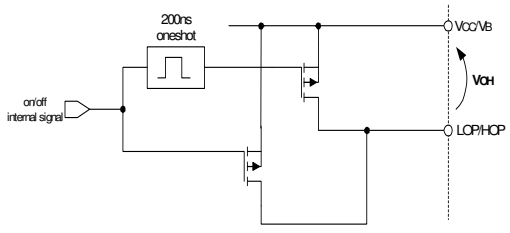


Figure 5: HOP and LOP Diagram

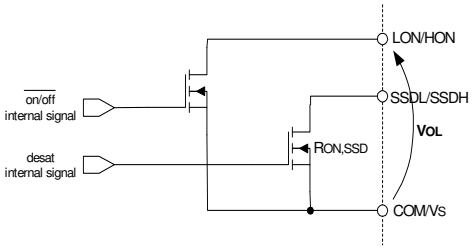


Figure 6: HON, LON, SSDH and SSDL Diagram

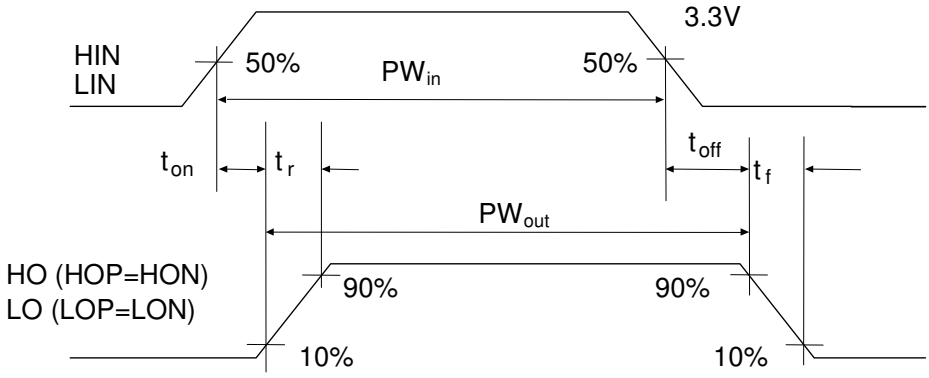


Figure 7: Switching Time Waveforms

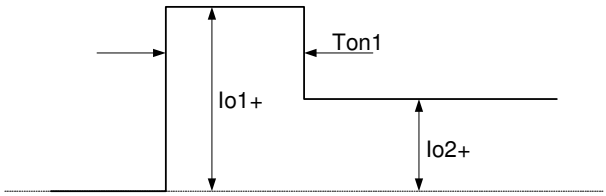


Figure 8: Output Source Current

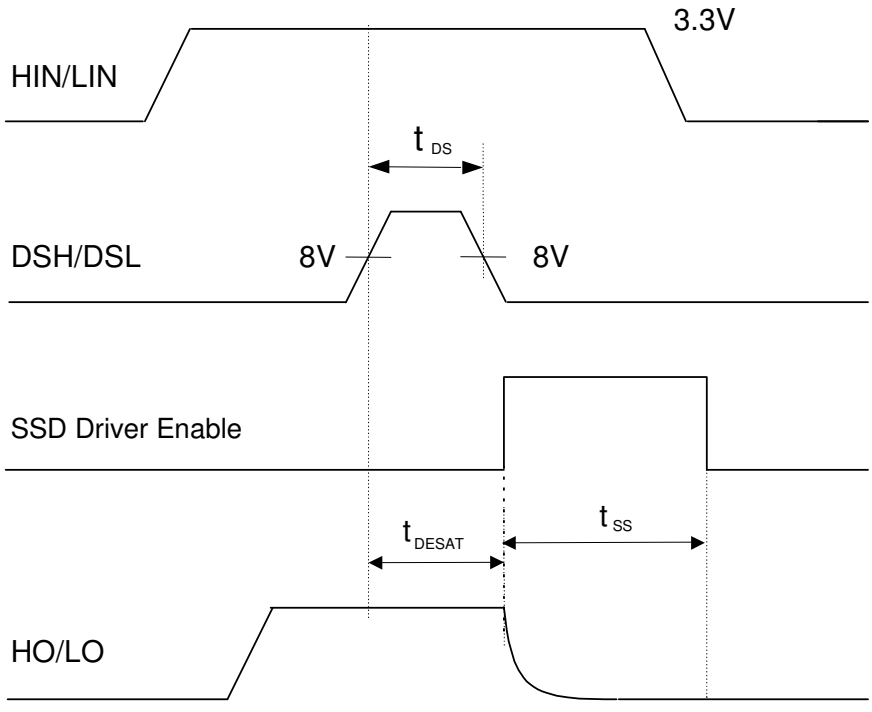


Figure 9: Soft Shutdown Timing Waveform

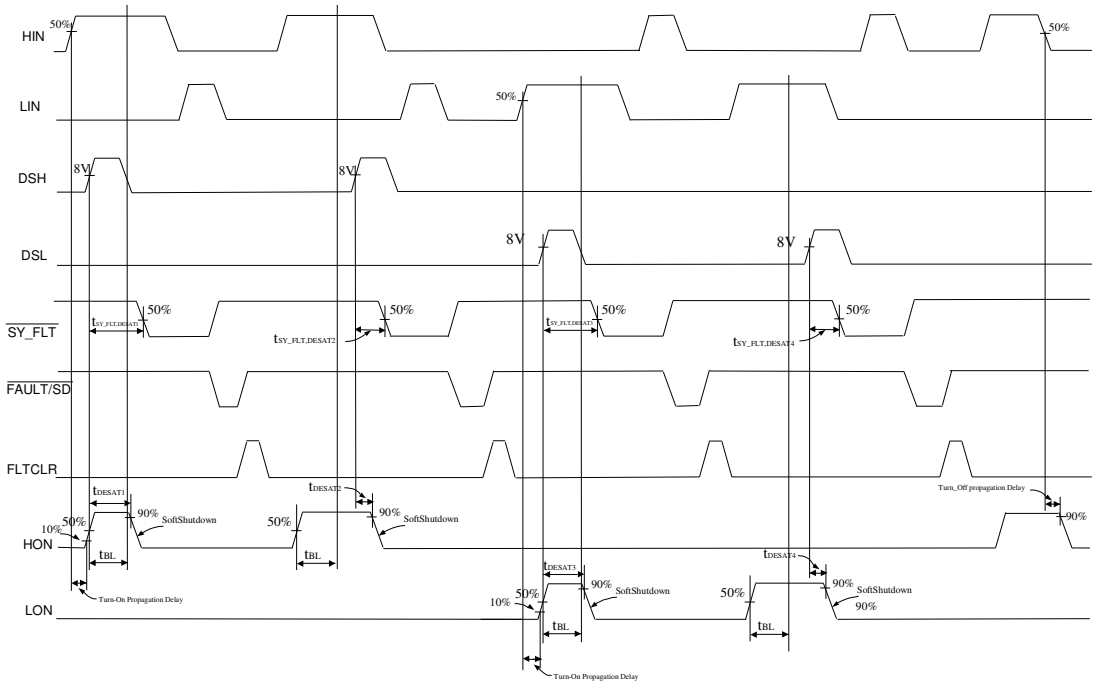


Figure 10: Desat Timing

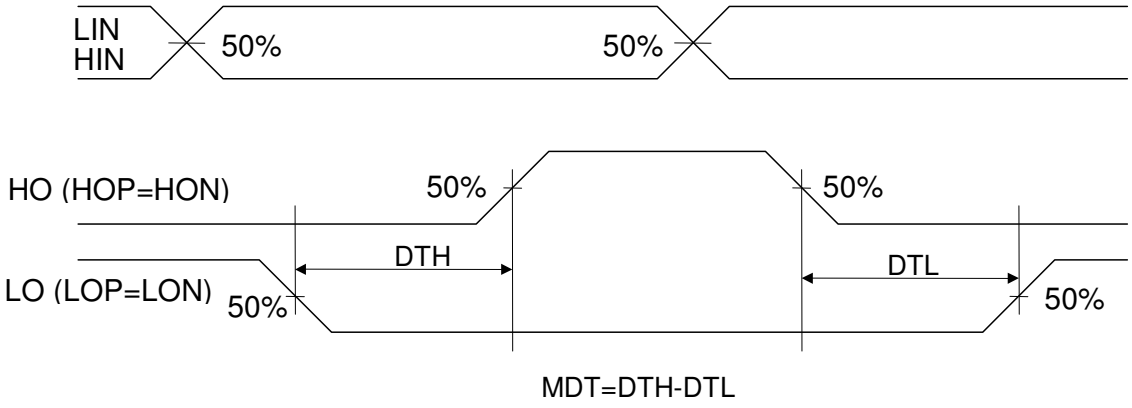
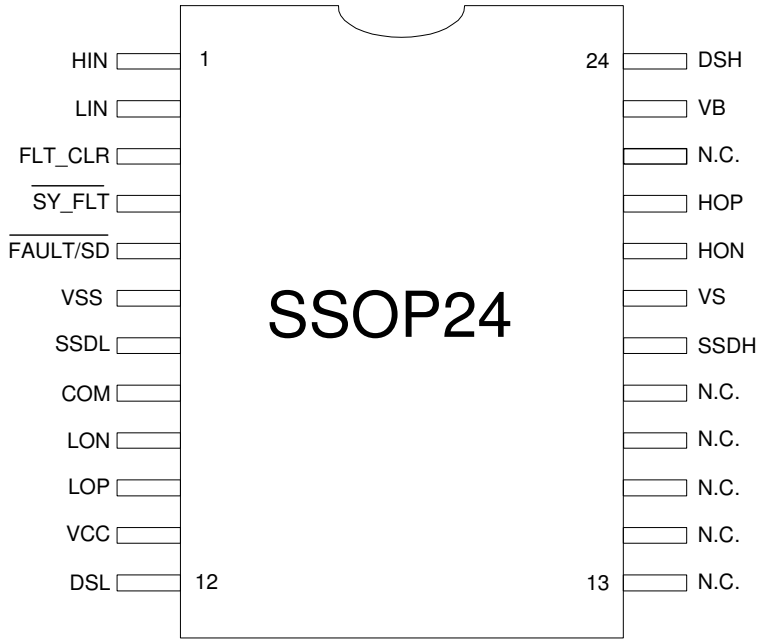


Figure 11: Internal Deadtime Timing

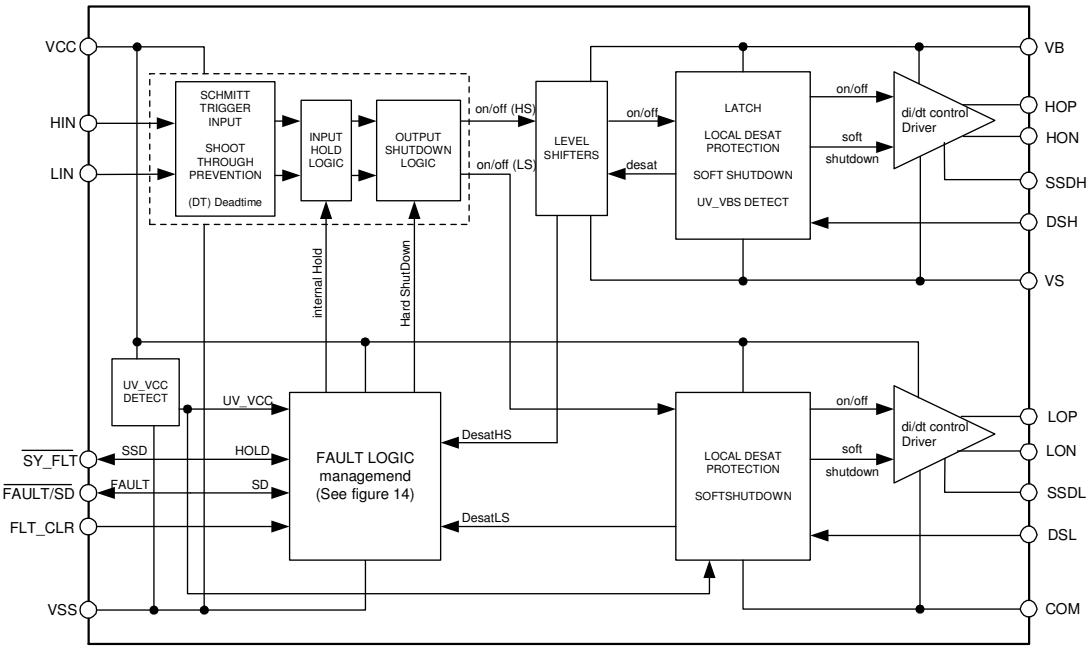
Lead Assignments

24-Lead SSOP

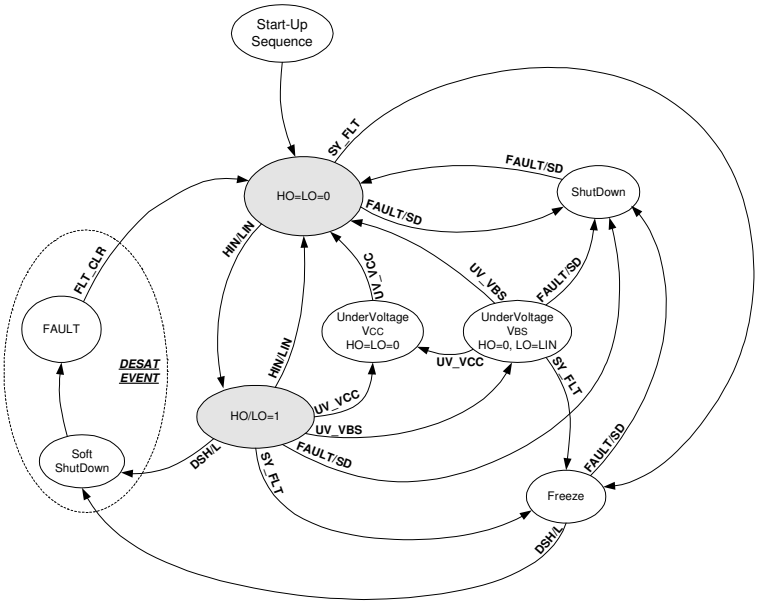


Lead Definitions

Symbol	Description
V_{CC}	Low side gate driver supply
V_{SS}	Logic ground
HIN	Logic input for high side gate driver outputs (HOP/HON)
LIN	Logic input for low side gate driver outputs (LOP/LON)
$\overline{\text{FAULT/SD}}$	Dual function (in/out) active low pin. Refer to Figs. 15, 17, and 18. As an output, indicates fault condition. As an input, shuts down the outputs of the gate driver regardless H_{IN}/L_{IN} status.
$\overline{\text{SY\_FLT}}$	Dual function (in/out) active low pin. Refer to Figs. 15, 17, and 18. As an output, indicates SSD sequence is occurring. As an input, an active low signal freezes both output status.
FLT_CLR	Fault clear active high input. Clears latched fault condition (see Fig. 17)
LOP	Low side driver sourcing output
LON	Low side driver sinking output
DSL	Low side IGBT desaturation protection input
SSDL	Low side soft shutdown
COM	Low side driver return
V_B	High side gate driver floating supply
HOP	High side driver sourcing output
HON	High side driver sinking output
DSH	High side IGBT desaturation protection input
SSDH	High side soft shutdown
V_S	High side floating supply return



FUNCTIONAL BLOCK DIAGRAM



STATE DIAGRAM

Stable State	**Temporary State**	**System Variable**
– FAULT	– SOFT SHUTDOWN	– FLT_CLR
– HO=LO=0 (Normal operation)	– START UP SEQUENCE	– HIN/LIN
– HO/LO=1 (Normal operation)		– UV_VCC
– UNDERVOLTAGE V_{CC}		– UV_VBS
– SHUTDOWN (SD)		– DSH/L
– UNDERVOLTAGE V_{BS}		– $\overline{SY\_FLT}$
– FREEZE		– $\overline{FAULT/SD}$

NOTE 1: A change of logic value of the signal labeled on lines (system variable) generates a state transition.
NOTE 2: Exiting from UNDERVOLTAGE V_{BS} state, the HO goes high only if a rising edge event happens in H_{IN}.

HO/LO Status	HOP/LOP	HON/LON	SSDH/SSDL
0	HiZ	0	HiZ
1	1	HiZ	HiZ
SSD	HiZ	HiZ	0
LO/HO	Output follows inputs (in=1->out=1, in=0->out=0)		
LO_{n-1}/HO_{n-1}	Output keeps previous status		

Logic Table: Output Drivers Status Description

	INPUTS			**INPUT/OUTPUT**		**Undervoltage** Yes: V< UV threshold No : V> UV threshold X: don't care		**OUTPUTS**	
Operation	**Hin**	**Lin**	**FLT_CLR**	**$\overline{SY\_FLT}$** SSD: desat (out) HOLD: freezing (in)	**$\overline{FAULT/SD}$** SD: shutdown (in) FAULT: diagnostic (out)	**V_{CC}**	**V_{BS}**	**HO**	**LO**
Shutdown	X	X	X	X	0 (SD)	X	X	0	0
Fault Clear	H_{IN}	L_{IN}	↓	X †	↓ (FAULT)	No	No	HO	LO
Fault Cleared	H_{IN}	L_{IN}	1	X	1 ††	No	No	HO	LO
Normal Operation	1	0	0	1	1	No	No	1	0
	0	1	0	1	1	No	No	0	1
	0	0	0	1	1	No	No	0	0
Anti Shoot Through	1	1	0	1	1	No	No	0	0
Soft Shutdown (entering)	1	0	0	↓ (SSD)	1	No	No	SSD	0
	0	1	0	↓ (SSD)	1	No	No	0	SSD
Soft Shutdown (finishing)	X	X	0	↑ (SSD)	↓ (FAULT)	No	No	0	0
	X	X	0	↑ (SSD)	↓ (FAULT)	No	No	0	0
Freeze	X	X	X	0 (HOLD)	1	No	No	HO_{n-1}	LO_{n-1}
Undervoltage	X	L_{IN}	X	1	1	No	Yes	0	LO
	X	X	X	1	0 (FAULT)	Yes	X	0	0

† $\overline{SY\_FLT}$ automatically resets after the SSD event is over, without requiring FLT_CLR to be asserted. To avoid FLT_CLR conflicting with the SSD sequence of operations, in the event of a SSD during normal operation it is recommended not to apply FLT_CLR while $\overline{SY\_FLT}$ is active. At power supply start-up instead, it is recommended to keep FLT_CLR active to prevent spurious diagnostic signals being generated, as described in section 1.1 Start-Up Sequence and in section 1.4.5 Fault Management at Start-up.

†† Holding FLT_CLR high all time will not allow the gate driver to latch the FAULT status and migth compromise power system protection.

1 Features Description

1.1 Start-Up Sequence

At power supply start-up, it is recommended to keep the FLT_CLR pin active until the supply voltages are properly established. This prevents spurious diagnostic signals being generated.

When the bootstrap supply topology is used for supplying the floating high side stage, the following start-up sequence is recommended (see also Fig. 12):

1. Set V_{CC},
2. Set FLT_CLR pin to HIGH level,
3. Set LIN pin to HIGH level and charge the bootstrap capacitor,
4. Release LIN pin to LOW level,
5. Release FLT_CLR pin to LOW level.

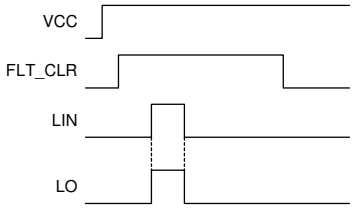


Figure 12 Start-Up Sequence

A minimum 15 µs LIN and FLT-CLR pulse is required.
A minimum supply voltage of 8V is recommended for the driver to operate safely under switching conditions at VS pin. At lower supply the gate driving capability decreases and might become not sufficient to counteract switching charge injected to the outputs.

1.2 Normal Operation Mode

After the start-up sequence has completed, the device becomes fully operative (see grey blocks in the State Diagram).

HIN and LIN produce driver outputs to switch accordingly, while the input logic monitors the input signals and deadtime (DT) prevent shoot-through events from occurring.

1.3 Shutdown

The system controller can asynchronously command the Hard Shutdown (HSD) through the 3.3 V compatible CMOS I/O $\overline{\text{FAULT/SD}}$ pin. This event is not latched.

In a multi-phase system, $\overline{\text{FAULT/SD}}$ signals are or-ed so the controller or one of the gate drivers can force the simultaneous shutdown of the other gate drivers through the same pin.

1.4 Fault Management

The IR2114/IR2214 is able to manage supply failure (undervoltage lockout) and transistor desaturation (on both the low and high side switches).

1.4.1 Undervoltage (UV)

The undervoltage protection function disables the driver's output stage which prevents the power device from being driven when the input voltage is less than the undervoltage threshold. Both the low side (V_{CC} supplied) and the floating side (V_{BS} supplied) are controlled by a dedicate undervoltage function.

An undervoltage event on the V_{CC} pin (when $V_{CC} < UV_{VCC-}$) generates a diagnostic signal by forcing the $\overline{\text{FAULT/SD}}$ pin low (see $\overline{\text{FAULT/SD}}$ section and Fig. 14). This event disables both the low side and floating drivers and the diagnostic signal holds until the undervoltage condition is over. The fault condition is not latched and the $\overline{\text{FAULT/SD}}$ pin is released once V_{CC} becomes higher than UV_{VCC+}.

The V_{BS} undervoltage protection works by disabling only the floating driver. Undervoltage on V_{BS} does not prevent the low side driver from activating its output nor does it generate diagnostic signals. The V_{BS} undervoltage condition ($V_{BS} < UV_{VBS-}$) latches the high side output stage in the low state. V_{BS} must exceed the UV_{VBS+} threshold to return the device to its normal operating mode. To turn on the floating driver, H_{IN} must be re-asserted high (rising edge event on H_{IN} is required).

1.4.2 Power Devices Desaturation

Different causes can generate a power inverter failure (phase and/or rail supply short-circuit, overload conditions induced by the load, etc.). In all of these fault conditions, a large increase in current results in the IGBT.

The IR2114/IR2214 fault detection circuit monitors the IGBT emitter to collector voltage (V_{CE}) (an external high voltage diode is connected between the IGBT's collector and the ICs DSH or DSL pins). A high current in the IGBT may cause the transistor to desaturate; this condition results in an increase of V_{CE}.

Once in desaturation, the current in the power transistor can be as high as 10 times the nominal current. Whenever the transistor is switched off, this high current generates relevant voltage transients in the power stage that need to be smoothed out in order to avoid destruction (by over-voltage). The gate driver is able to control the transient condition by smoothly turning off the desaturated transistor with its integrated soft shutdown (SSD) protection.

1.4.3 Desaturation Detection: DSH/L Function

Figure 13 shows the structure of the desaturation sensing and soft shutdown block. This configuration is the same for both the high and low side output stages.

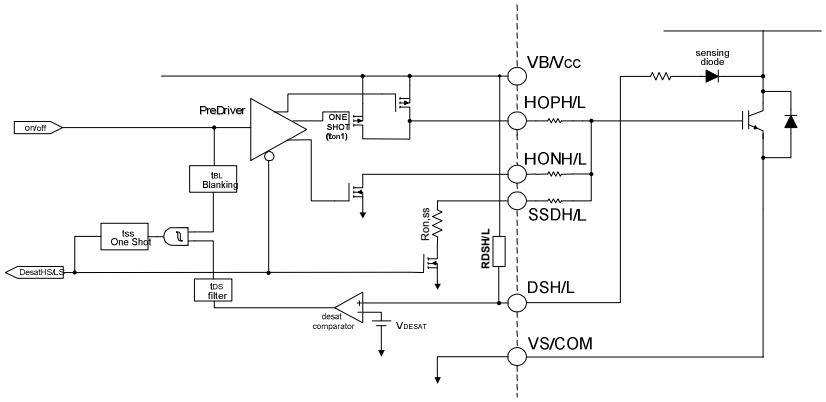


Figure 13: High and Low Side Output Stage

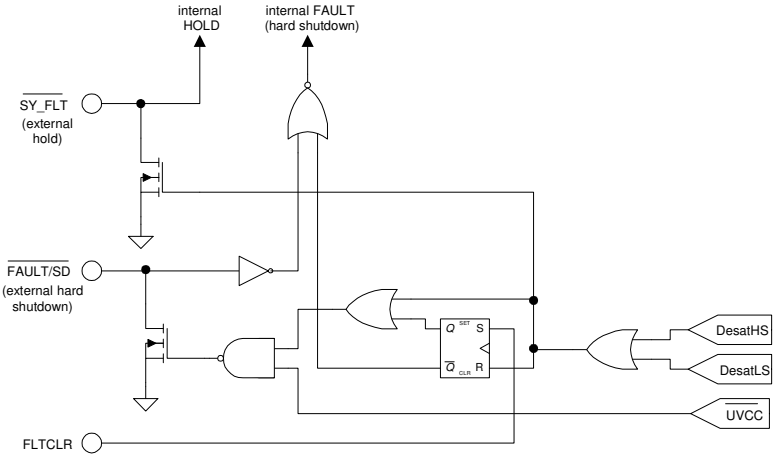


Figure 14: Fault Management Diagram

The external sensing diode should have breakdown voltage greater than 600 V (IR2114) or 1200 V (IR2214), low stray capacitance and low recovery current (in order to minimize noise coupling and switching delays). In series an external decoupling 1KΩ resistor is required in order to limit the current flowing in and out of DSH and DSL pins because of switching noise coupled through the external de-saturation sensing diode. The diode is biased by an internal pull-up resistor $R_{DSH/L}$ (equal to V_{CC}/I_{DS-} or V_{BS}/I_{DS-}). When V_{CE} increases, the voltage at the DSH or DSL pin increases too. Being internally biased to the local supply, the DSH/DSL voltage is automatically clamped. When DSH/DSL exceeds the V_{DESAT+} threshold, the comparator triggers (see Fig. 13). The comparator's output is filtered in order to avoid false desaturation detection by externally induced noise; pulses shorter than t_{DS} are filtered out. To avoid detecting a false desaturation event during IGBT turn on, the desaturation circuit is disabled by a blanking signal (T_{BL}, see blanking block in Fig. 13). This time is the estimated maximum IGBT turn on time and must be not exceeded by proper gate resistance sizing. When the IGBT is not completely saturated after T_{BL}, desaturation is detected and the driver will turn off.

Eligible desaturation signals initiate the SSD sequence. While in SSD, the driver's output goes to a high impedance state and the SSD pull-down is activated to turn off the IGBT through the SSDH/SSDL pin. The $\overline{SY\_FLT}$ output pin (active low, see Fig. 14) reports the gate driver status during the SSD sequence (t_{SS}). Once the SSD has finished, $\overline{SY\_FLT}$ releases, and the gate driver generates a FAULT signal (see the $\overline{FAULT/SD}$ section) by activating the $\overline{FAULT/SD}$ pin. This generates a hard shutdown for both the high and low output stages (HO=LO=low). Each driver is latched low until the fault is cleared (see FLT_CLR).

Figure 14 shows the fault management circuit. In this diagram DesatHS and DesatLS are two internal signals that come from the output stages (see Fig. 13).

It must be noted that while in SSD, both the undervoltage fault and external SD are masked until the end of SSD. Desaturation protection is working independently by the other control pin and it is disabled only when the output status is off.

For the purpose of sensing the power transistor desaturation, the collector voltage is monitored (an external high voltage diode is connected between the IGBT's collector and the IC's DSH or DSL pin). The diode is normally biased by an internal pull up resistor connected to the local supply line (V_B or V_{CC}). When the transistor is "on" the diode is conducting and the amount

of current flowing in the circuit is determined by the internal pull up resistor value.

In the high side circuit, the desaturation biasing current may become relevant for dimensioning the bootstrap capacitor (see Fig. 19). In fact, a pull up resistor with a low resistance may result in a high current the significantly discharges the bootstrap capacitor. For that reason, the internal pull up resistor typical value is of the order of 100 kΩ.

While the impedance of the DSH/DSL pins is very low when the transistor is on (low impedance path through the external diode down to the power transistor), the impedance is only controlled by the pull up resistor when the transistor is off. In that case, relevant dV/dt generated at VS node might push the DSH/DSL pins outside the recommended operating conditions.

1.4.4 Fault Management in Multi-Phase Systems

In a system with two or more gate drivers the IR2114/IR2214 devices must be connected as shown in Fig. 15.

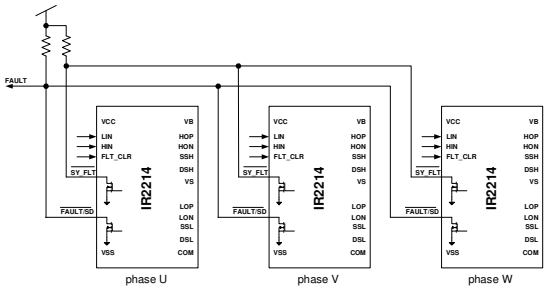


Figure 15: IR2214 used in a 3 phase application

SY_FLT: The bi-directional SY_FLT pins communicate each other through a local network. The logic signal is active low. The device that detects the IGBT desaturation activates the SY_FLT, which is then read by the other gate drivers. When SY_FLT is active all the drivers hold their output state regardless of the input signals (H_{IN}, L_{IN}) they receive from the controller (freeze state). This feature is particularly important in phase-to-phase short circuit where two IGBTs are involved; in fact, while one is softly shutting-down, the other must be prevented from hard shutdown to avoid exiting SSD. In the freeze state, the frozen drivers are not completely inactive because desaturation detection still takes the highest priority. SY_FLT communication has been designed for creating a local network between the drivers. There is no need to wire SY_FLT to the controller.

FAULT/SD: The bi-directional FAULT/SD pins communicate with each other and with the system controller. The logic signal is active low. When low, the FAULT/SD signal commands the outputs to go off by hard shutdown. There are three events that can force FAULT/SD low:

1. Desaturation detection event: the FAULT/SD pin is *latched* low when SSD is over, and only a FLT_CLR signal can reset it;
2. Undervoltage on V_{CC}: the FAULT/SD pin is forced low and held until the undervoltage is active. This event is not latched;
3. FAULT/SD is externally driven low either from the controller or from another IR2114/IR2214 device. This event is not latched; therefore the FLT_CLR cannot disable it. Only when FAULT/SD becomes high the device returns to its normal operating mode.

1.4.5 Fault Management at Start-up

When the bootstrap supply topology is used for supplying the floating high side and the recommended power supply start-up sequence is followed, FLT_CLR pin must be kept active to prevent spurious diagnostic signals being generated.
In the event of power inverter failure already present or occurring during start-up (phase and/or rail supply short-circuit, overload conditions induced by the load, etc.), keeping the FLT_CLR pin active will also prevent the real fault condition to be detected with the FAULT/SD pin. In such a condition a large current increase in the IGBT will desaturate the transistor, allowing the gate driver to detect and turn-off the desaturated transistor with the integrated soft shutdown (SSD) protection.
As with a normal SSD sequence, during SSD the SY_FLT output pin (active low, see Fig. 14) will report the gate driver status. But now, being the FLT_CLR pin already active, the gate driver will not generate a FAULT signal by activating the FAULT/SD pin and it will not enter hard shutdown.
To prevent the driver to resume charging the bootstrap capacitor, therefore re-establishing the condition that will determine again the occurrence of the large current increase in the IGBT, it is recommended to monitor the SY_FLT output pin. Should the SY_FLT output pin go low during the start-up sequence, the controller must interpret a power inverter failure is present, and stop the start-up sequence.

1.6 Output Stage

The structure is shown in Fig. 13 and consists of two turn on stages and one turn off stage. When the driver turns on the IGBT (see Fig. 8), a first stage is activated while an additional stage is maintained in the active state for a limited time (t_{on1}). This feature boosts the total driving capability in order to accommodate both a fast gate charge to the plateau voltage and dV/dt control in switching.

At turn off, a single n-channel sinks up to 3 A (I_{O-}) and offers a low impedance path to prevent the self-turn on due to the parasitic Miller capacitance in the power switch.

1.7 Timing and Logic State Diagrams Description

The following figures show the input/output logic diagram. Figure 17 shows the SY_FLT and FAULT/SD signals as outputs, whereas Fig. 18 shows them as inputs.

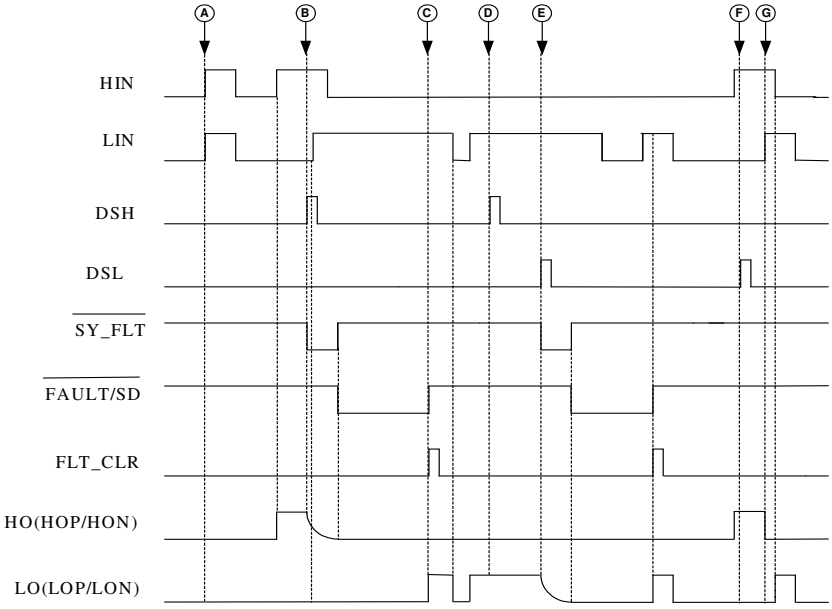


Figure 17: I/O Timing Diagram with $\overline{\text{SY\_FLT}}$ and $\overline{\text{FAULT/SD}}$ as Output

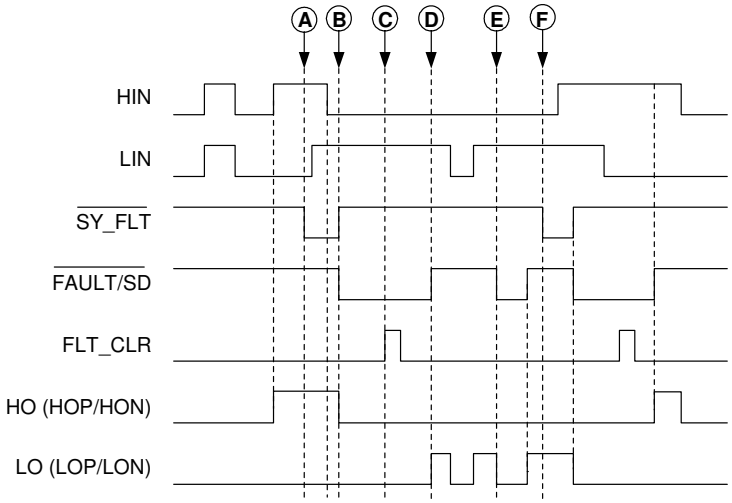


Figure 18: I/O Logic Diagram with $\overline{\text{SY\_FLT}}$ and $\overline{\text{FAULT/SD}}$ as Input

Referred to the timing diagram of Fig. 17:

A. When the input signals are on together the outputs go off (anti-shoot through),
B. The HO signal is on and the high side IGBT desaturates, the HO turn off softly while the $\overline{\text{SY\_FLT}}$ stays low. When $\overline{\text{SY\_FLT}}$ goes high the $\overline{\text{FAULT/SD}}$ goes low. While in SSD, if LIN goes up, LO does not change (freeze),
C. When $\overline{\text{FAULT/SD}}$ is latched low (see $\overline{\text{FAULT/SD}}$ section) FLT_CLR can disable it and the outputs go back to follow the inputs,
D. The DSH goes high but this is not read because HO is off,
E. The LO signal is on and the low side IGBT desaturates, the low side behaviour is the same as described in point B,
F. The DSL goes high but this is not read as LO is off,
G. As point A (anti-shoot through).

Referred to the timing diagram Fig. 18:

A. The device is in the hold state, regardless of input variations. The hold state results as $\overline{\text{SY\_FLT}}$ is forced low externally,
B. The device outputs go off by hard shutdown, externally commanded. A through B is the same sequence adopted by another IR2x14x device in SSD procedure.
C. Externally driven low $\overline{\text{FAULT/SD}}$ (shutdown state) cannot be disabled by forcing FLT_CLR (see $\overline{\text{FAULT/SD}}$ section),
D. The $\overline{\text{FAULT/SD}}$ is released and the outputs go back to follow the inputs,
E. Externally driven low $\overline{\text{FAULT/SD}}$: outputs go off by hard shutdown (like point B),
F. As point A and B but for the low side output.

2 Sizing Tips

2.1 Bootstrap Supply

The V_{BS} voltage provides the supply to the high side driver circuitry of the gate driver. This supply sits on top of the V_S voltage and so it must be floating. The bootstrap method is used to generate the V_{BS} supply and can be used with any of the IR211(4,41)/ IR221(4,41) drivers. The bootstrap supply is formed by a diode and a capacitor as connected in Fig. 19.

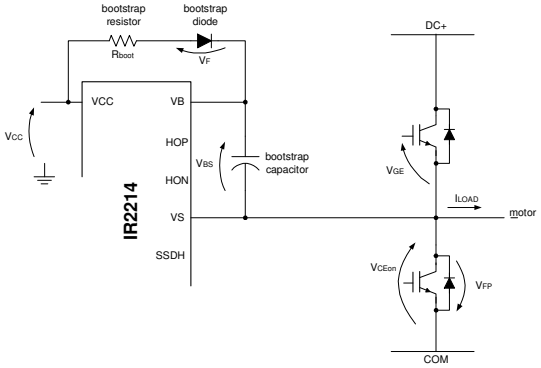


Figure 19: Bootstrap Supply Schematic

This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

2.2 Bootstrap Capacitor Sizing

To size the bootstrap capacitor, the first step is to establish the minimum voltage drop (ΔV_{BS}) that we have to guarantee when the high side IGBT is on.

If V_{GEmin} is the minimum gate emitter voltage we want to maintain, the voltage drop must be:

$$\Delta V_{BS} \le V_{CC} - V_F - V_{GE\min} - V_{CEon}$$

under the condition,

$$V_{GE\min} > V_{BSUV-}$$

where V_{CC} is the IC voltage supply, V_F is bootstrap diode forward voltage, V_{CEon} is emitter-collector voltage of low side IGBT, and V_{BSUV-} is the high-side supply undervoltage negative going threshold.

Now we must consider the influencing factors contributing V_{BS} to decrease:

- IGBT turn on required gate charge (Q_G),
- IGBT gate-source leakage current (I_{LK_GE}),
- Floating section quiescent current (I_{QBS}),
- Floating section leakage current (I_{LK}),
- Bootstrap diode leakage current (I_{LK_DIODE}),
- Desat diode bias when on (I_{DS}),
- Charge required by the internal level shifters (Q_{LS}); typical 20 nC,
- Bootstrap capacitor leakage current (I_{LK_CAP}),
- High side on time (T_{HON}).

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

Then we have:

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + \\ + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP} + I_{DS-}) \cdot T_{HON}$$

The minimum size of bootstrap capacitor is:

$$C_{BOOT\min} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

An example follows using IR2214SS or IR22141SS:

a) using a 25 A @ 125 °C 1200 V IGBT (IRGP30B120KD):

- I_{QBS} = 800 µA (datasheet IR2214);
- I_{LK} = 50 µA (see Static Electrical Characteristics);
- Q_{LS} = 20 nC
- Q_G = 160 nC (datasheet IRGP30B120KD);
- I_{LK_GE} = 100 nA (datasheet IRGP30B120KD);
- I_{LK_DIODE} = 100 µA (reverse recovery <100 ns);
- I_{LK_CAP} = 0 (neglected for ceramic capacitor);
- I_{DS-} = 150 µA (see Static Electrical Characteristics);
- T_{HON} = 100 µs.

And:

- V_{CC} = 15 V
- V_F = 1 V
- $V_{CEonmax}$ = 3.1 V
- V_{GEmin} = 10.5 V

the maximum voltage drop ΔV_{BS} becomes

$$\Delta V_{BS} \le V_{CC} - V_F - V_{GE\min} - V_{CEon} = \\ = 15\,V - 1\,V - 10.5\,V - 3.1\,V = 0.4\,V$$

And the bootstrap capacitor is:

$$C_{BOOT} \ge \frac{290\,nC}{0.4\,V} = 725\,nF$$

NOTICE: V_{CC} has been chosen to be 15 V. Some IGBTs may require a higher supply to work correctly with the bootstrap technique. Also V_{CC} variations must be accounted in the above formulas.

2.3 Some Important Considerations

Voltage Ripple: There are three different cases to consider (refer to Fig. 19).

- I_{LOAD} < 0 A; the load current flows in the low side IGBT (resulting in V_{CEon}).

$$V_{BS} = V_{CC} - V_F - V_{CEon}$$

In this case we have the lowest value for V_{BS}. This represents the worst case for the bootstrap capacitor sizing. When the IGBT is turned off, the V_s node is pushed up by the load current until the high side freewheeling diode is forwarded biased.

- I_{LOAD} = 0 A; the IGBT is not loaded while being on and V_{CE} can be neglected

$$V_{BS} = V_{CC} - V_F$$

- I_{LOAD} > 0 A; the load current flows through the freewheeling diode

$$V_{BS} = V_{CC} - V_F + V_{FP}$$

In this case we have the highest value for V_{BS}. Turning on the high side IGBT, I_{LOAD} flows into it and V_S is pulled up. To minimize the risk of undervoltage, the bootstrap capacitor should be sized according to the I_{LOAD}< 0 A case.

Bootstrap Resistor: A resistor (R_{boot}) is placed in series with the bootstrap diode (see Fig. 19) in order to limit the current when the bootstrap capacitor is initially charged. We suggest not exceeding 10 Ω to avoid increasing the V_{BS} time-constant. The minimum on time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time-constant.

Bootstrap Capacitor: For high t_{HON} designs where an electrolytic capacitor is used, its ESR must be considered. This parasitic resistance forms a voltage divider with R_{boot}, which generats a voltage step on V_{BS} at the first charge of bootstrap capacitor. The voltage step and the related speed (dV_{BS}/dt) should be limited. As a general rule, ESR should meet the following constraint.

$$\frac{ESR}{ESR + R_{BOOT}} \cdot V_{CC} \le 3V$$

A parallel combination of a small ceramic capacitor and a large electrolytic capacitor is normally the best compromise, the first capacitor posses a fast time constant and limits the dV_{BS}/dt by reducing the equivalent resistance. The second capacitor provides a large capacitance to maintain the V_{BS} voltage drop within the desired ΔV_{BS}.

Bootstrap Diode: The diode must have a BV > 600 V or 1200 V and a fast recovery time (t_{rr} < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor to V_{CC} supply.

2.4 Gate Resistances

The switching speed of the output transistor can be controlled by properly sizing the resistors controlling the turn-on and turn-off gate currents. The following section provides some basic rules for sizing the resistors to obtain the desired switching time and speed by introducing the equivalent output resistance of the gate driver (R_{DRp} and R_{DRn}).

The example shown uses IGBT power transistors and Figure 20 shows the nomenclature used in the following paragraphs. In addition, V_{ge}^* indicates the plateau voltage, Q_{gc} and Q_{ge} indicate the gate to collector and gate to emitter charge respectively.

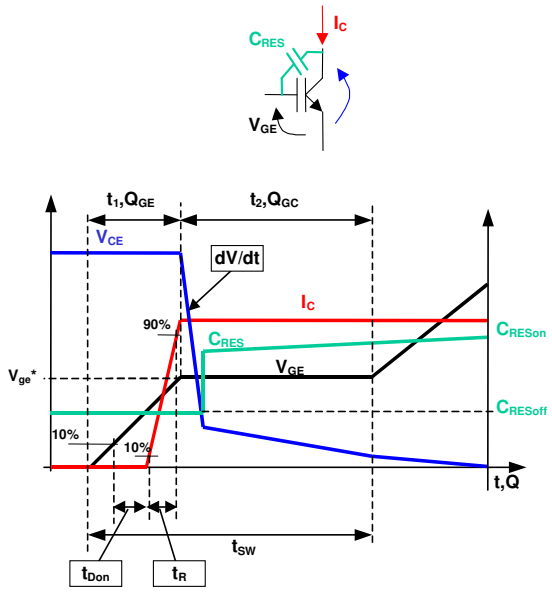


Figure 20: Nomenclature

2.5 Sizing The Turn-On Gate Resistor

Switching-Time: For the matters of the calculation included hereafter, the switching time t_{sw} is defined as the time spent to reach the end of the plateau voltage (a total Q_{gc}+Q_{ge} has been provided to the IGBT gate). To obtain the desired switching time the gate resistance can be sized starting from Q_{ge} and Q_{gc}, Vcc, V_{ge}^* (see Fig. 21):

$$I_{avg} = \frac{Q_{gc} + Q_{ge}}{t_{sw}}$$

and

$$R_{TOT} = \frac{Vcc - V_{ge}^*}{I_{avg}}$$

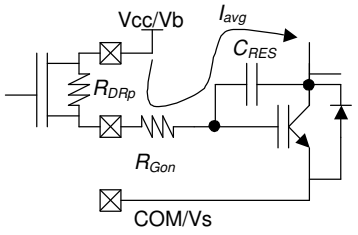


Figure 21: R_{Gon} Sizing

where $R_{TOT} = R_{DRp} + R_{Gon}$

R_{Gon} = gate on-resistor
R_{DRp} = driver equivalent on-resistance

R_{DRp} is approximately given by

$$R_{DRp} = \begin{cases} \dfrac{Vcc}{I_{o1+}} \dfrac{t_{SW}}{t_{on1}} + \dfrac{Vcc}{I_{o2+}} \dfrac{t_{SW} - t_{on1}}{t_{SW}} & for \quad t_{SW} > t_{on1} \\ \dfrac{Vcc}{I_{o1+}} & for \quad t_{SW} \le t_{on1} \end{cases}$$

(I_{O1+} ,I_{O2+} and t_{on1} from "Static Electrical Characteristics").

Table 1 reports the gate resistance size for two commonly used IGBTs (calculation made using typical datasheet values and assuming V_{CC}= 15 V).

Output Voltage Slope: The turn-on gate resistor R_{Gon} can be sized to control the output slope (dV_{OUT}/dt). While the output voltage has a non-linear behaviour, the maximum output slope can be approximated by:

$$\frac{dV_{out}}{dt} = \frac{I_{avg}}{C_{RESoff}}$$

inserting the expression yielding I_{avg} and rearranging:

$$R_{TOT} = \frac{Vcc - V_{ge}^{*}}{C_{RESoff} \cdot \dfrac{dV_{out}}{dt}}$$

As an example, table 2 shows the sizing of gate resistance to get dV_{out}/dt= *5 V/ns* when using two popular IGBTs (typical datasheet values are used and V_{CC}= *15 V* is assumed).

NOTICE: Turn on time must be lower than T_{BL} to avoid improper desaturation detection and SSD triggering.

2.6 Sizing the Turn-Off Gate Resistor

The worst case in sizing the turn-off resistor R_{Goff} is when the collector of the IGBT in the off state is forced to commutate by an external event (e.g., the turn-on of the companion IGBT). In this case the dV/dt of the output node induces a parasitic current through C_{RESoff} flowing in R_{Goff} and R_{DRn} (see Fig. 22). If the voltage drop at the gate exceeds the threshold voltage of the IGBT, the device may self turn on, causing large oscillation and relevant cross conduction.

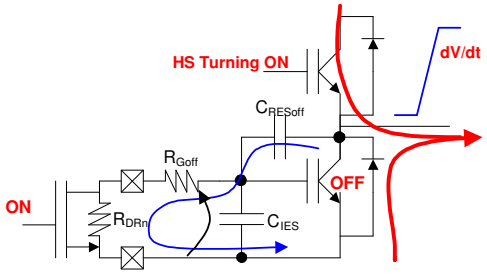


Figure 22: R_{Goff} Sizing: Current Path When Low Side is Off and High Side Turns On

The transfer function between the IGBT collector and the IGBT gate then becomes:

$$\frac{V_{ge}}{V_{de}} = \frac{s \cdot (R_{Goff} + R_{DRn}) \cdot C_{RESoff}}{1 + s \cdot (R_{Goff} + R_{DRn}) \cdot (C_{RESoff} + C_{IES})}$$

which yields to a high pass filter with a pole at:

$$1/\tau = \frac{1}{(R_{Goff} + R_{DRn}) \cdot (C_{RESoff} + C_{IES})}$$

As a result, when τ is faster than the collector rise time (to be verified after calculation) the transfer function can be approximated by:

$$\frac{V_{ge}}{V_{de}} = s \cdot (R_{Goff} + R_{DRn}) \cdot C_{RESoff}$$

so that

$$V_{ge} = (R_{Goff} + R_{DRn}) \cdot C_{RESoff} \cdot \frac{dV_{de}}{dt}$$

in the time domain. Then the condition:

$$V_{th} > V_{ge} = \left(R_{Goff} + R_{DRn}\right) \cdot C_{RESoff} \frac{dV_{out}}{dt}$$

must be verified to avoid spurious turn on. Rearranging the equation yields:

$$R_{Goff} < \frac{V_{th}}{C_{RESoff} \cdot \dfrac{dV}{dt}} - R_{DRn}$$

R_{DRn} is approximately given by

$$R_{DRn} = \frac{Vcc}{I_{o-}}$$

In any case, the worst condition for unwanted turn on is with very fast steps on the IGBT collector.

In that case, the collector to gate transfer function can be approximated with the capacitor divider:

$$V_{ge} = V_{de} \cdot \frac{C_{RESoff}}{(C_{RESoff} + C_{IES})}$$

which is driven only by IGBT characteristics.

As an example, table 3 reports R_{Goff} (calculated with the above mentioned disequation) for two popular IGBTs to withstand $dV_{out}/dt = 5$ *V/ns*.

NOTICE: The above-described equations are intended to approximate a way to size the gate resistance. A more accurate sizing may provide more precise device and PCB (parasitic) modelling.

IGBT	Qge	Qgc	Vge*	tsw	Iavg	Rtot	RGon → std commercial value	Tsw
IRGP30B120K(D)	19 nC	82 nC	9 V	400 ns	0.25 A	24 Ω	RTOT - RDRp = 12.7 Ω → 10 Ω	→420 ns
IRG4PH30K(D)	10 nC	20 nC	9 V	200 ns	0.15 A	40 Ω	RTOT - RDRp = 32.5 Ω → 33 Ω	→202 ns

Table 1: t_{sw} Driven R_{Gon} Sizing

IGBT	Qge	Qgc	Vge*	CRESoff	Rtot	RGon → std commercial value	dVout/dt
IRGP30B120K(D)	19 nC	82 nC	9 V	85 pF	14 Ω	RTOT - RDRp = 6.5 Ω → 8.2 Ω	→4.5 V/ns
IRG4PH30K(D)	10 nc	20 nC	9 V	14 pF	85 Ω	RTOT - RDRp = 78 Ω → 82 Ω	→5 V/ns

Table 2: dV_{OUT}/dt Driven R_{Gon} Sizing

IGBT	Vth(min)	CRESoff	RGoff
IRGP30B120K(D)	4	85 pF	RGoff ≤ 4 Ω
IRG4PH30K(D)	3	14 pF	RGoff ≤ 35 Ω

Table 3: R_{Goff} Sizing

3 PCB Layout Tips

3.1 Distance from High to Low Voltage

The IR2x14x pinout maximizes the distance between floating (from DC- to DC+) and low voltage pins. It's strongly recommended to place components tied to floating voltage on the high voltage side of device (V_B, V_S side) while the other components are placed on the opposite side.

3.2 Ground Plane

To minimize noise coupling, the ground plane must not be placed under or near the high voltage floating side.

3.3 Gate Drive Loops

Current loops behave like antennas and are able to receive and transmit EM noise. In order to reduce the EM coupling and improve the power switch turn on/off performances, gate drive loops must be reduced as much as possible. Figure 23 shows the high and low side gate loops.

Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, increasing the possibility of self turn-on. For this reason, it is strongly recommended to place the three gate resistances close together and to minimize the loop area (see Fig. 23).

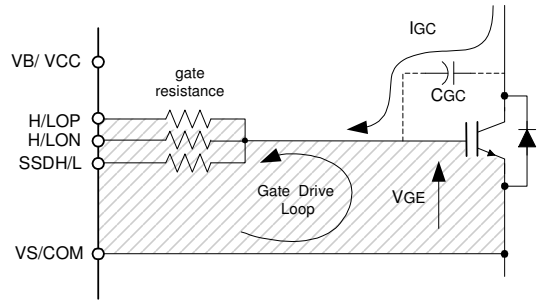


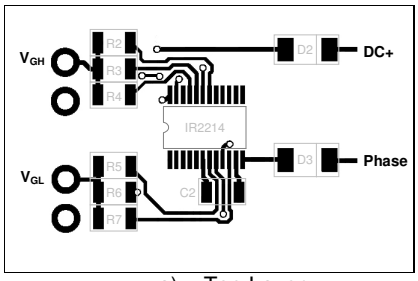
Figure 23: gate drive loop

3.4 Supply Capacitors

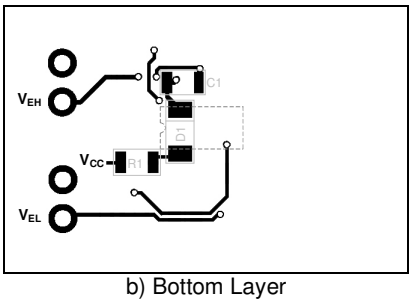
The IR2x14x output stages are able to quickly turn on an IGBT, with up to 2 A of output current. The supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) in order to minimize parasitic inductance/resistance.

3.5 Routing and Placement Example

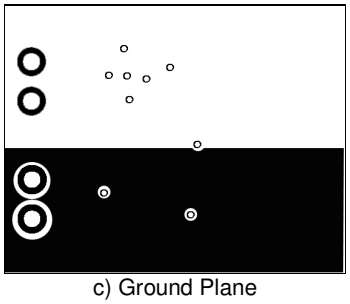
Figure 24 shows one of the possible layout solutions using a 3 layer PCB. This example takes into account all the previous considerations. Placement and routing for supply capacitors and gate resistances in the high and low voltage side minimize the supply path loop and the gate drive loop. The bootstrap diode is placed under the device to have the cathode as close as possible to the bootstrap capacitor and the anode far from high voltage and close to V_{CC}.



a) Top Layer



b) Bottom Layer



c) Ground Plane

Figure 24: layout example

Information below refers to Fig. 24:
Bootstrap section: R1, C1, D1
High side gate: R2, R3, R4
High side Desat: D2
Low side supply: C2
Low side gate: R5, R6, R7
Low side Desat: D3

Figures 25-83 provide information on the experimental performance of the IR2114/IR2214SSPbF HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples from multiple wafer lots were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

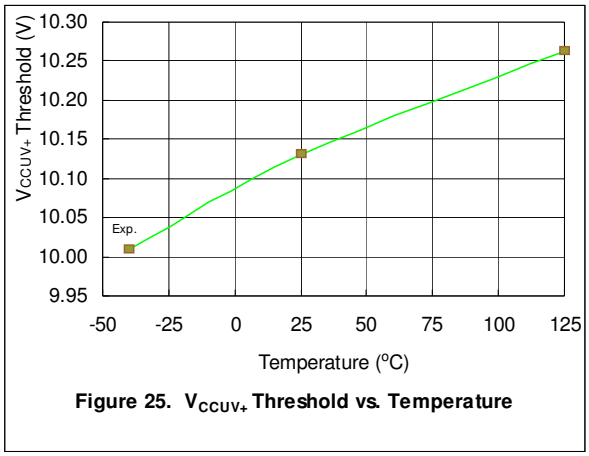


Figure 25. V_{CCUV+} Threshold vs. Temperature

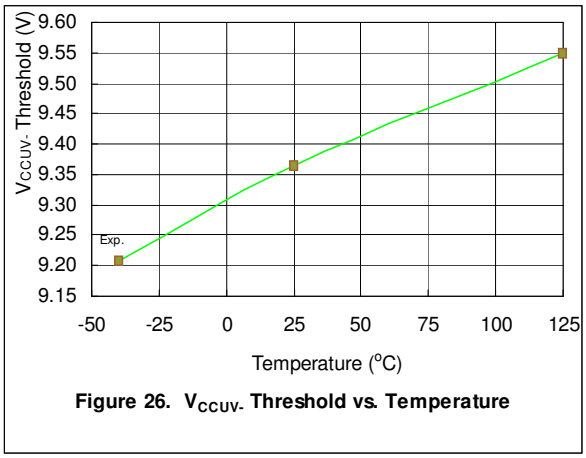


Figure 26. V_{CCUV-} Threshold vs. Temperature

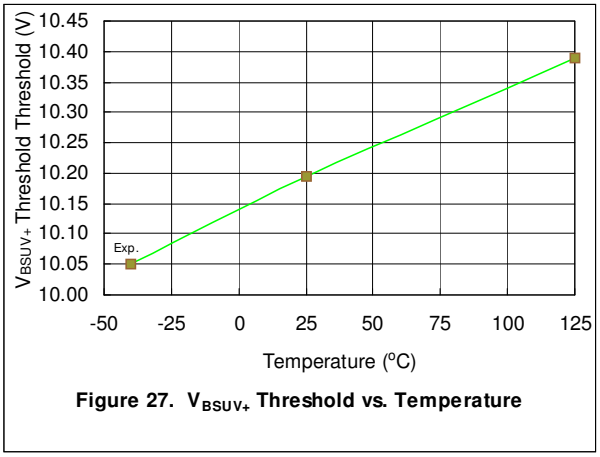


Figure 27. V_{BSUV+} Threshold vs. Temperature

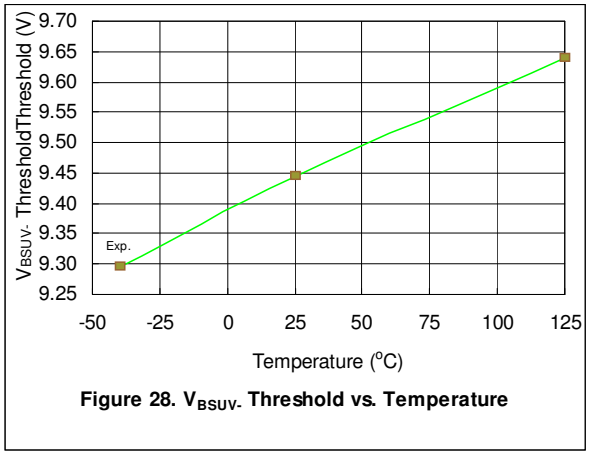


Figure 28. V_{BSUV-} Threshold vs. Temperature

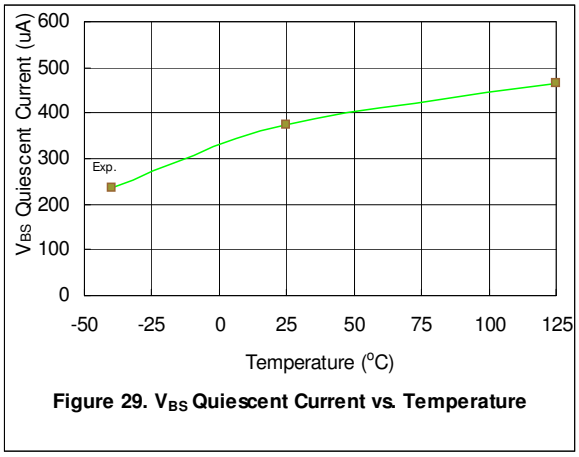


Figure 29. V_{BS} Quiescent Current vs. Temperature

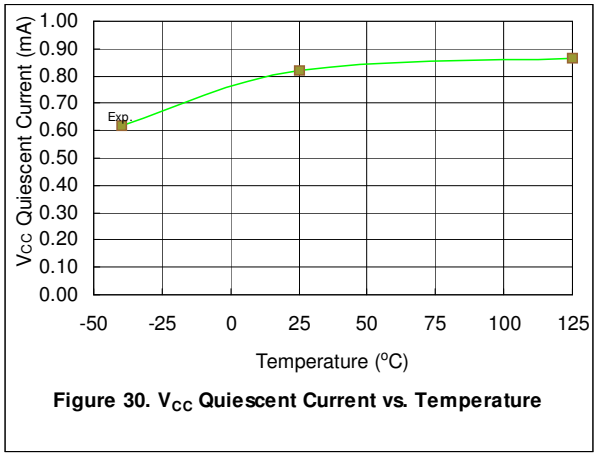


Figure 30. V_{CC} Quiescent Current vs. Temperature

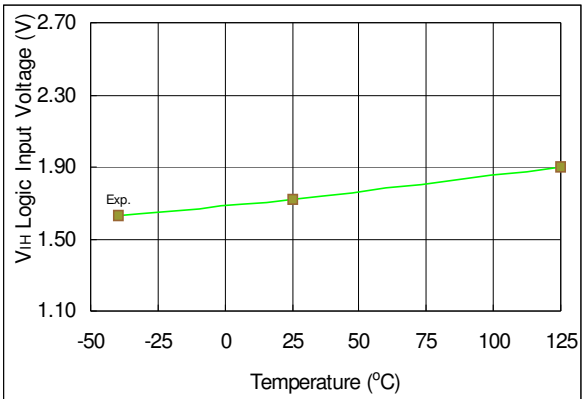


Figure 31. V_{IH} Logic Input Voltage vs. Temperature

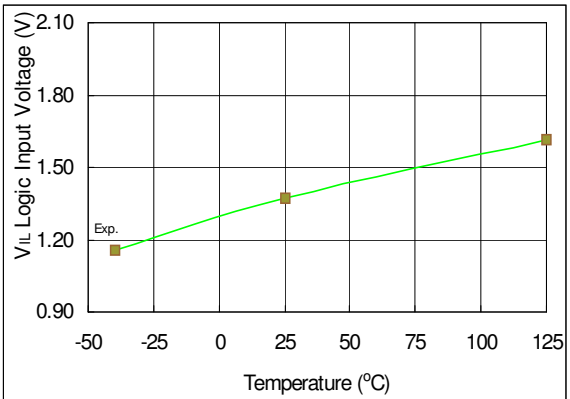


Figure 32. V_{IL} Logic Input Voltage vs. Temperature

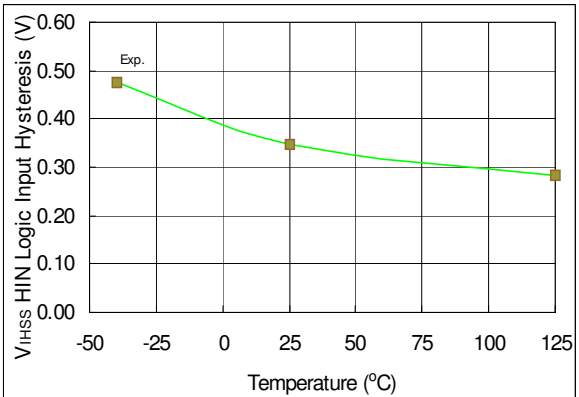


Figure 33. V_{IHSS} HIN Logic Input Hysteresis vs. Temperature

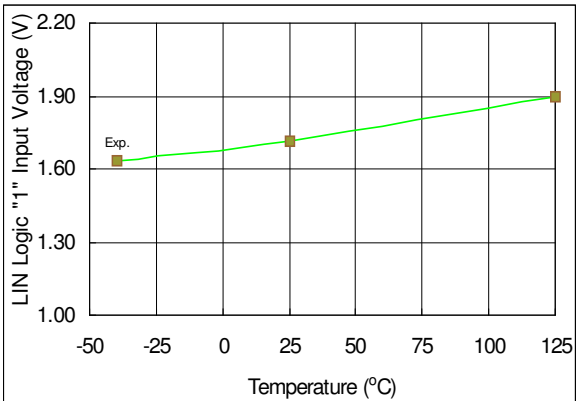


Figure 34. LIN Logic "1" Input Voltage vs. Temperature

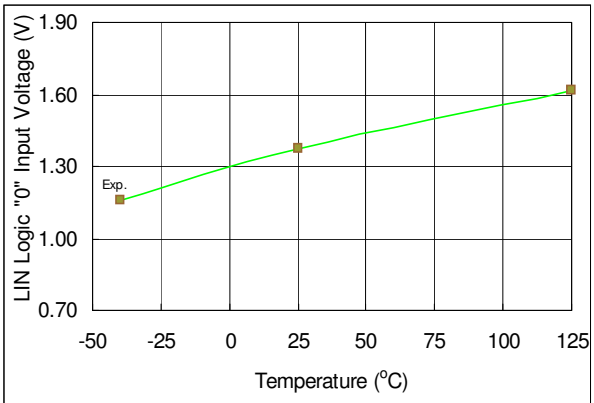


Figure 35. LIN Logic "0" Input Voltage vs. Temperature

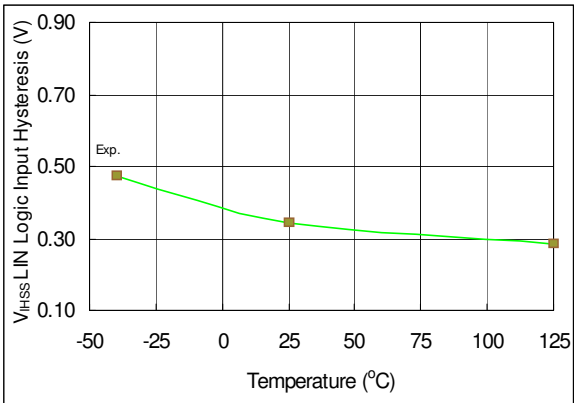


Figure 36. V_{IHSS} LIN Logic Input Hysteresis vs. Temperature

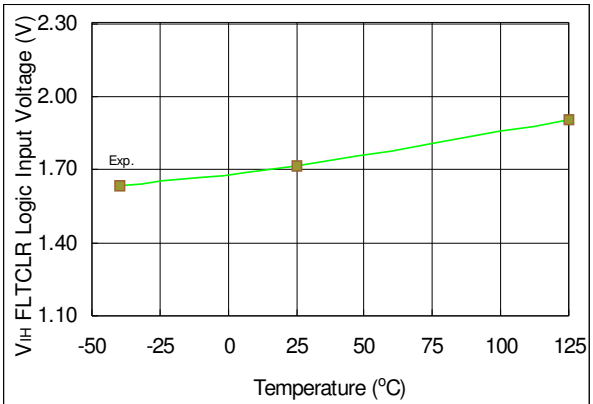


Figure 37. V_{IH} FLTCLR Logic Input Voltage vs. Temperature

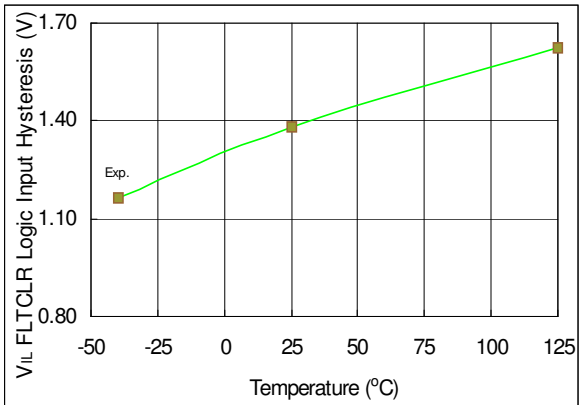


Figure 38. V_{IL} FLTCLR Logic Input Voltage vs. Temperature

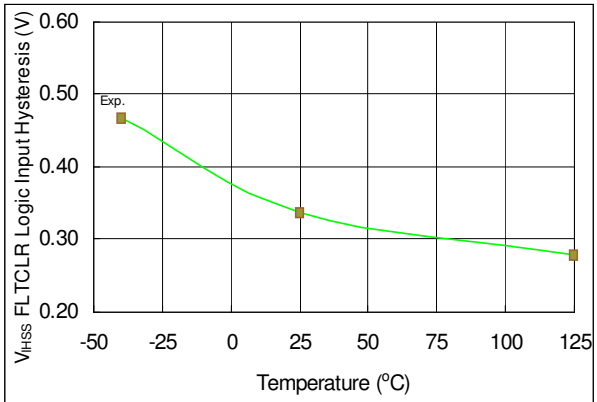


Figure 39. V_{IHSS} FLTCLR Logic Input Hysteresis vs. Temperature

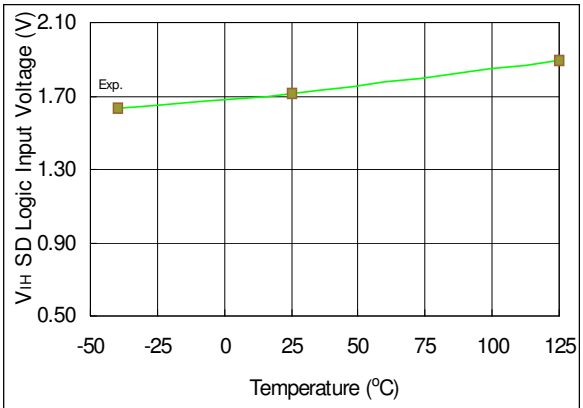


Figure 40. V_{IH} SD Logic Input Voltage vs. Temperature

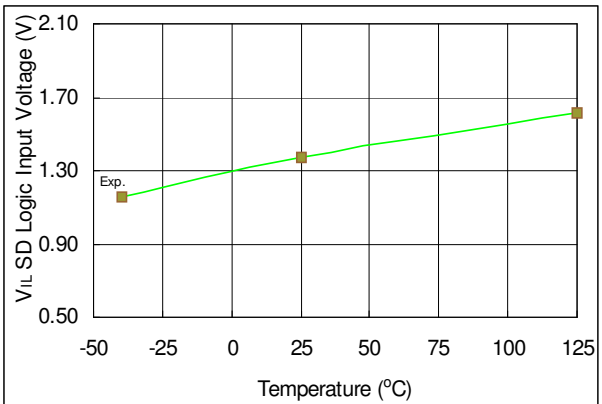


Figure 41. V_{IL} SD Logic Input Voltage vs. Temperature

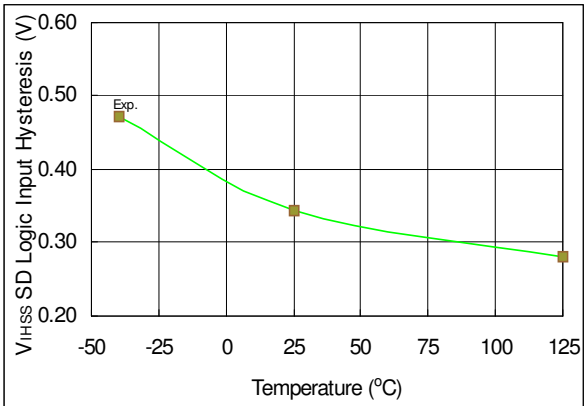


Figure 42. V_{IHSS} SD Logic Input Hysteresis vs. Temperature

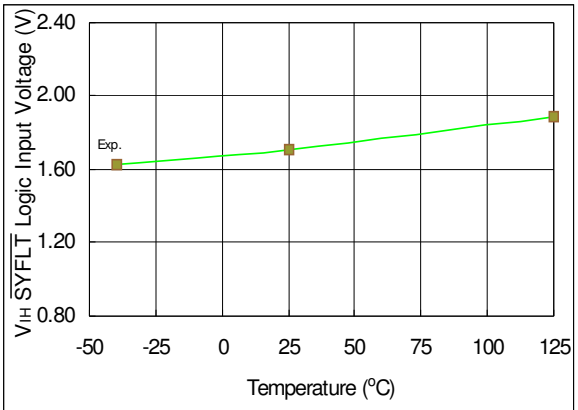


Figure 43. V_{IH} $\overline{SYFLT}$ Logic Input Voltage vs. Temperature

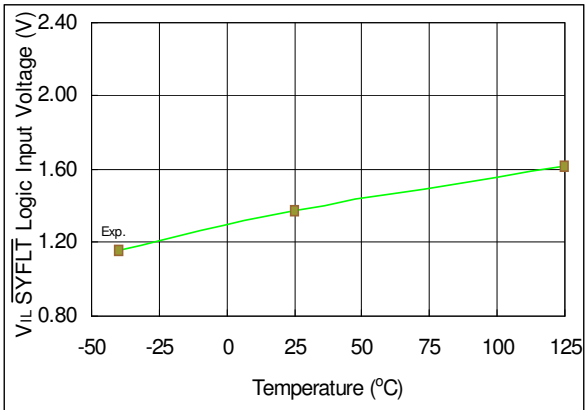


Figure 44. V_{IL} $\overline{SYFLT}$ Logic Input Voltage vs. Temperature

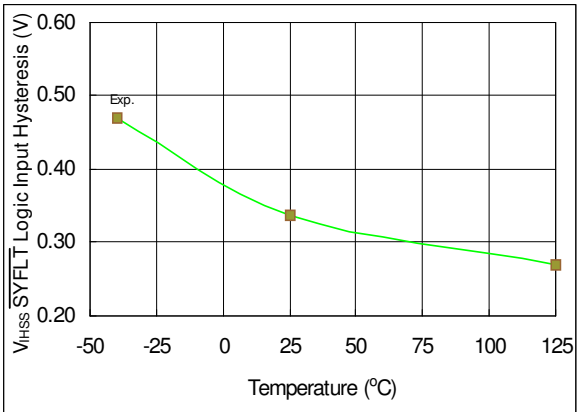


Figure 45. V_{IHSS} $\overline{SYFLT}$ Logic Input Hysteresis vs. Temperature

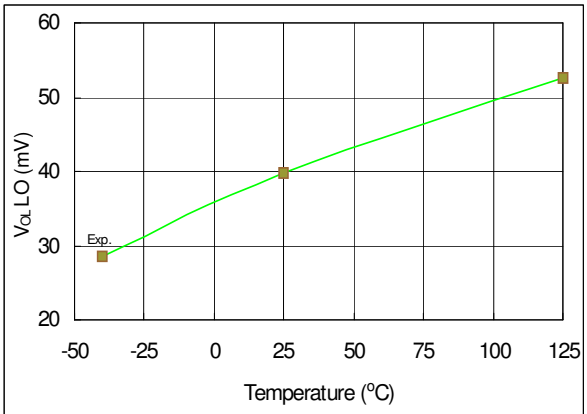


Figure 46. V_{OL} LO vs. Temperature

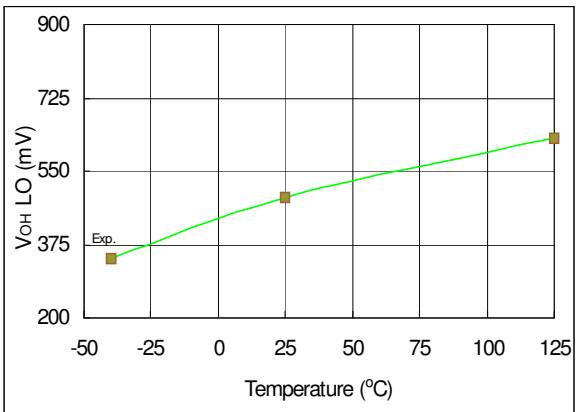


Figure 47. V_{OH} LO vs. Temperature

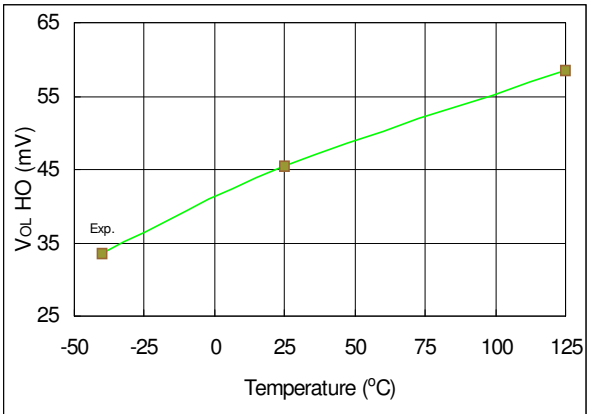


Figure 48. V_{OL} HO vs. Temperature

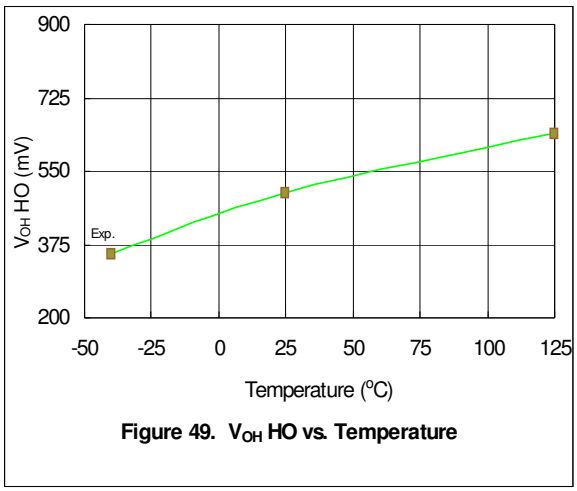


Figure 49. V_{OH} HO vs. Temperature

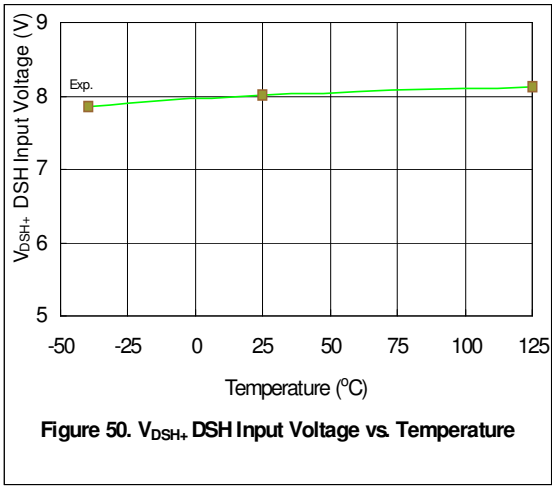


Figure 50. V_{DSH+} DSH Input Voltage vs. Temperature

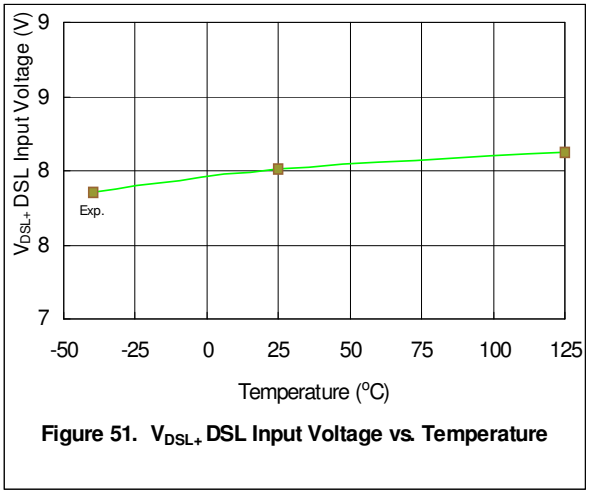


Figure 51. V_{DSL+} DSL Input Voltage vs. Temperature

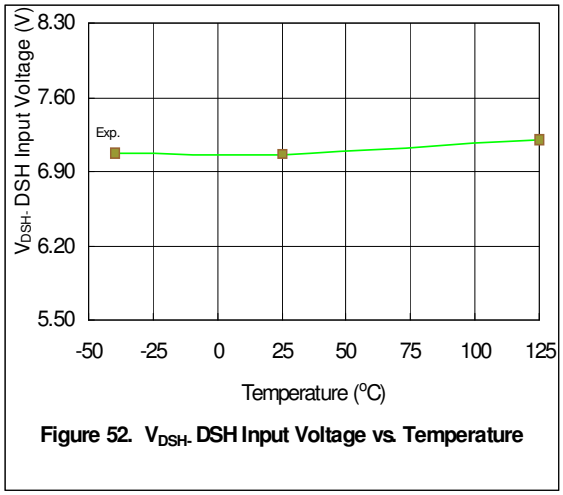


Figure 52. V_{DSH-} DSH Input Voltage vs. Temperature

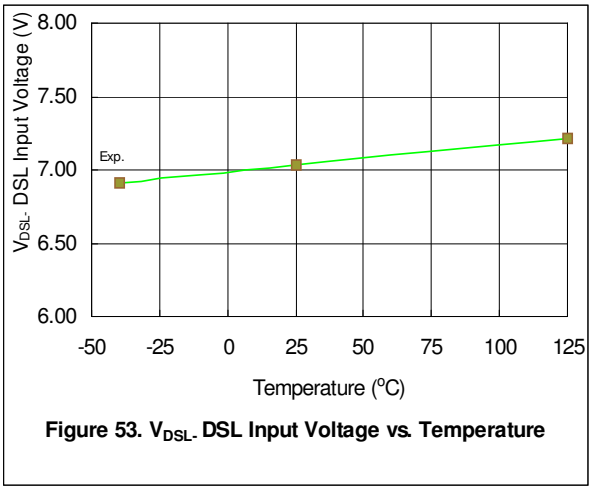


Figure 53. V_{DSL-} DSL Input Voltage vs. Temperature

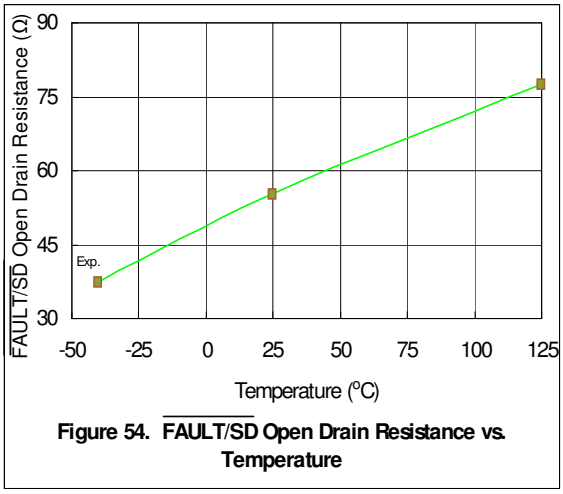


Figure 54. $\overline{FAULT/SD}$ Open Drain Resistance vs. Temperature

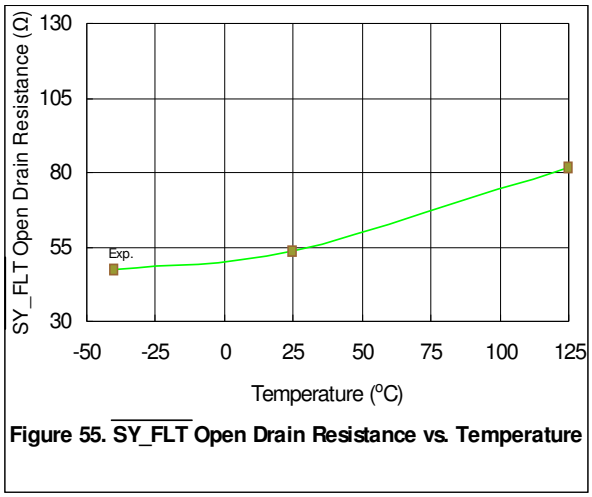


Figure 55. $\overline{\text{SY\_FLT}}$ Open Drain Resistance vs. Temperature

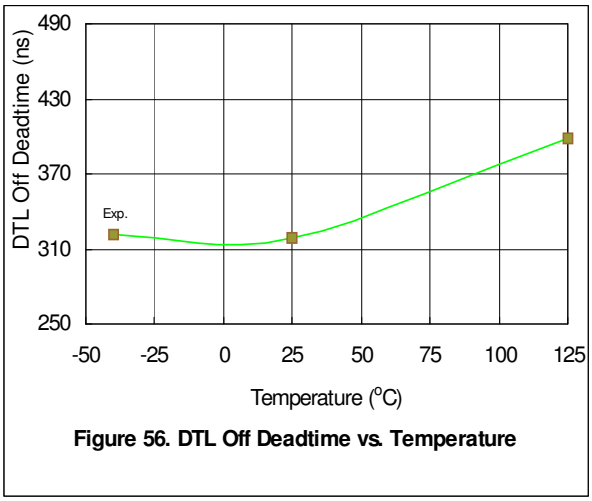


Figure 56. DTL Off Deadtime vs. Temperature

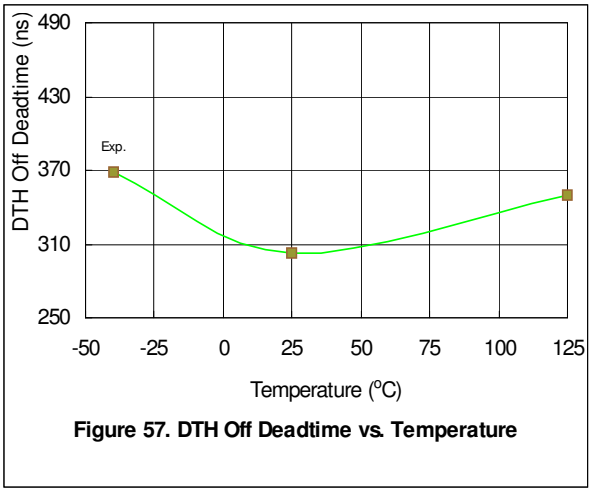


Figure 57. DTH Off Deadtime vs. Temperature

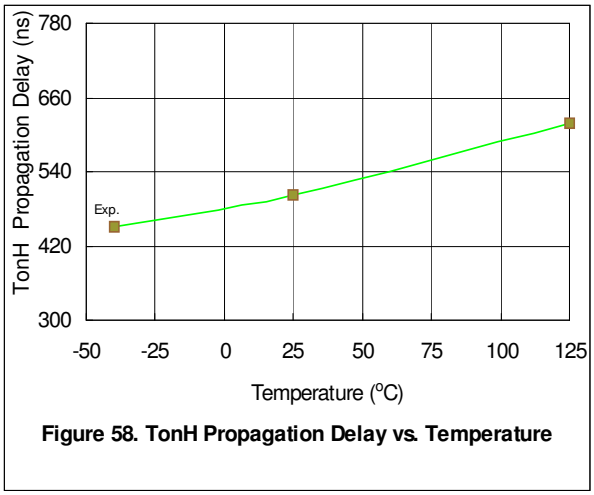


Figure 58. TonH Propagation Delay vs. Temperature

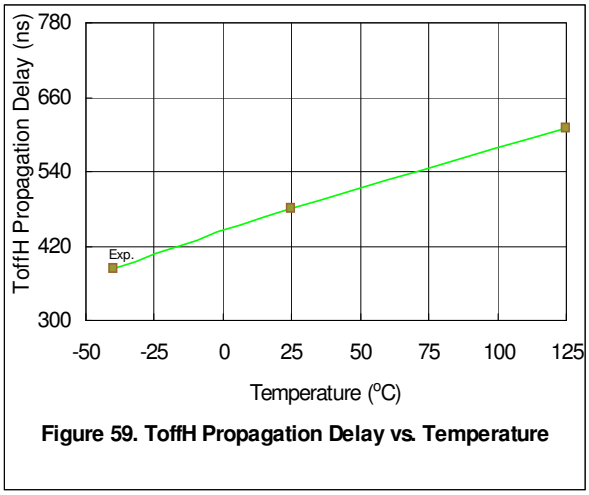


Figure 59. ToffH Propagation Delay vs. Temperature

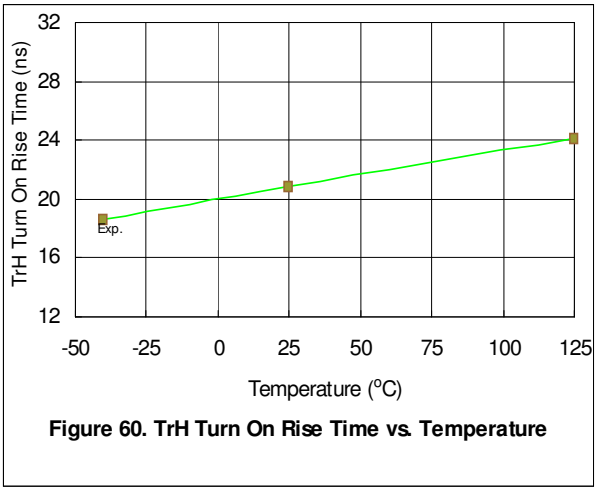


Figure 60. TrH Turn On Rise Time vs. Temperature

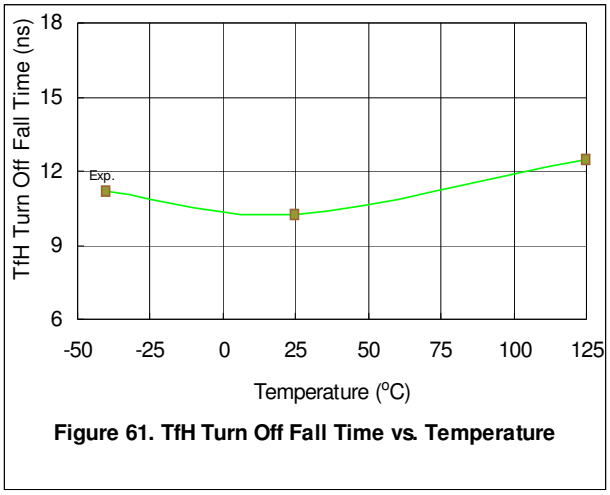


Figure 61. TfH Turn Off Fall Time vs. Temperature

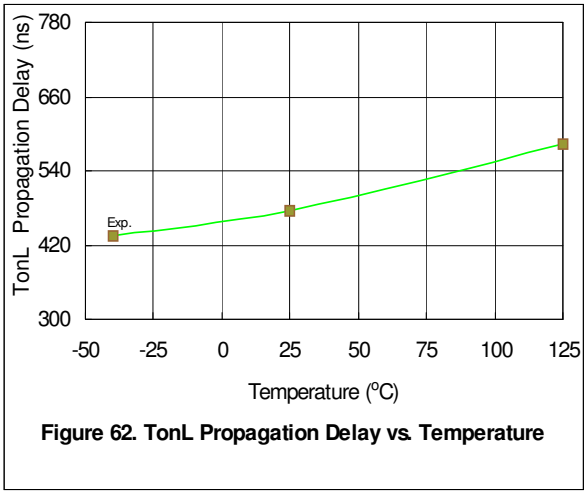


Figure 62. TonL Propagation Delay vs. Temperature

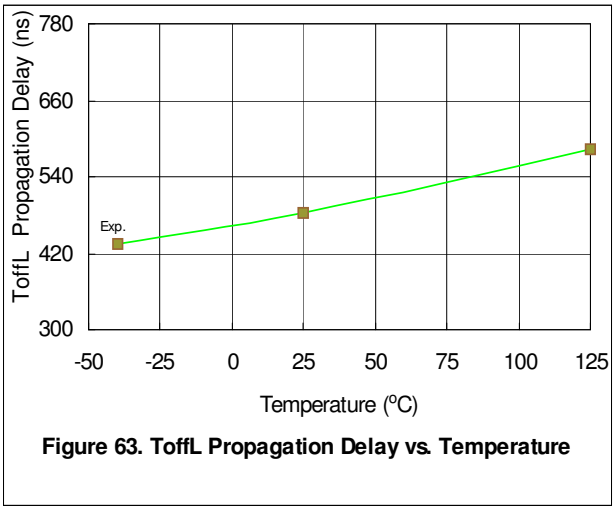


Figure 63. ToffL Propagation Delay vs. Temperature

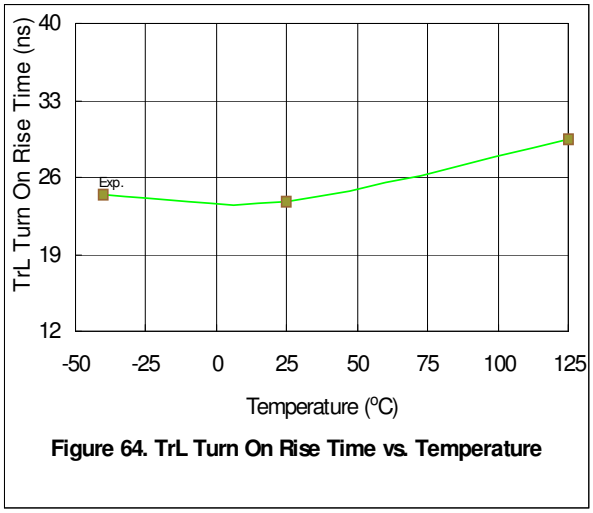


Figure 64. TrL Turn On Rise Time vs. Temperature

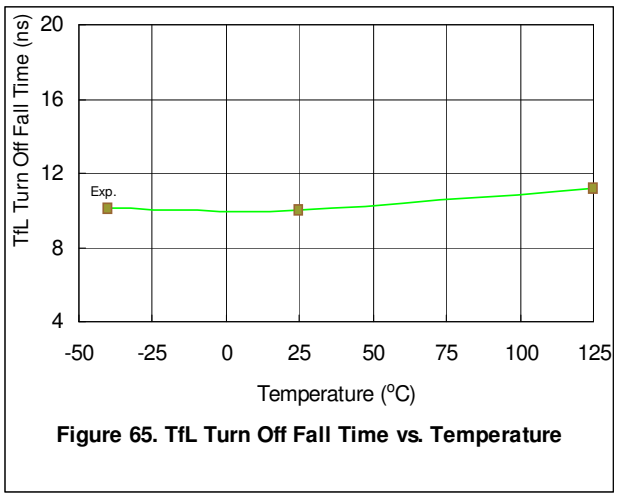


Figure 65. TfL Turn Off Fall Time vs. Temperature

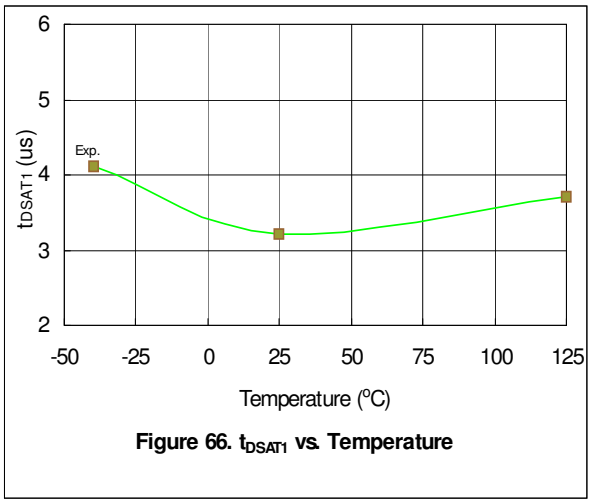


Figure 66. t_{DSAT1} vs. Temperature

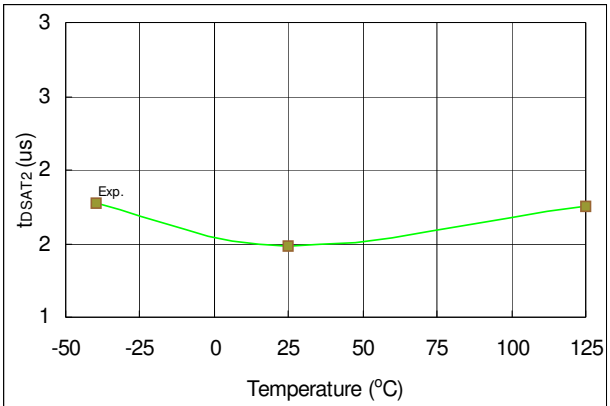


Figure 67. t_{DSAT2} vs. Temperature

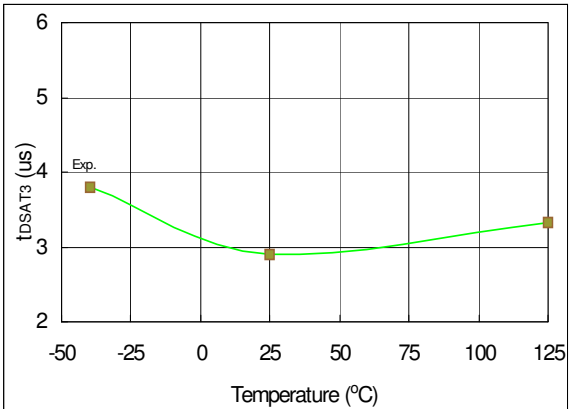


Figure 68. t_{DSAT3} vs. Temperature

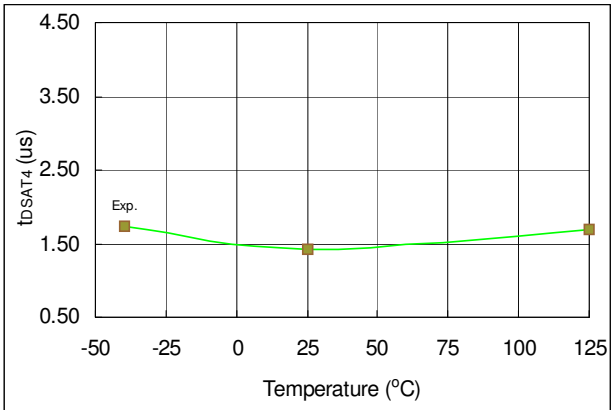


Figure 69. t_{DSAT4} vs. Temperature

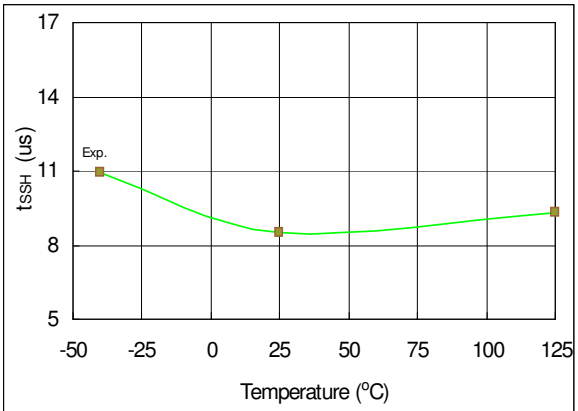


Figure 70. t_{SSH} vs. Temperature

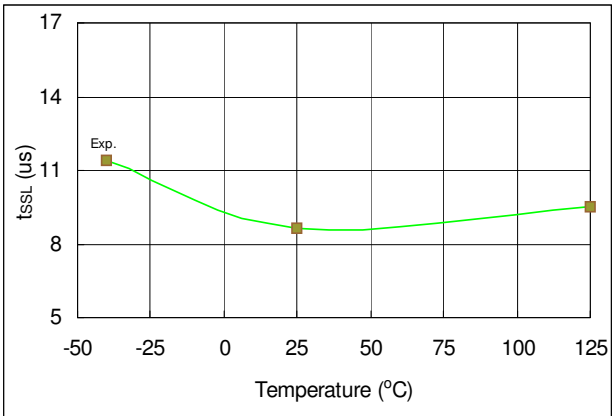


Figure 71. t_{SSL} vs. Temperature

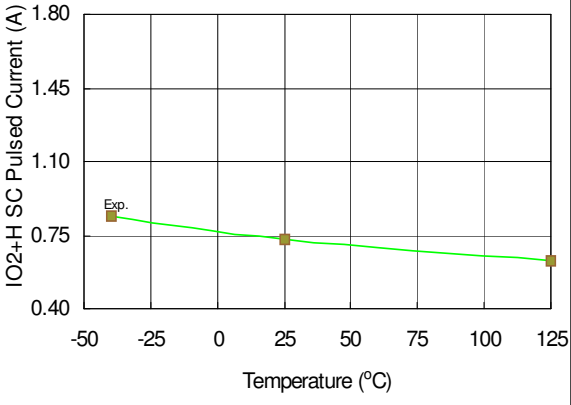


Figure 72. IO2+H SC Pulsed Current vs. Temperature

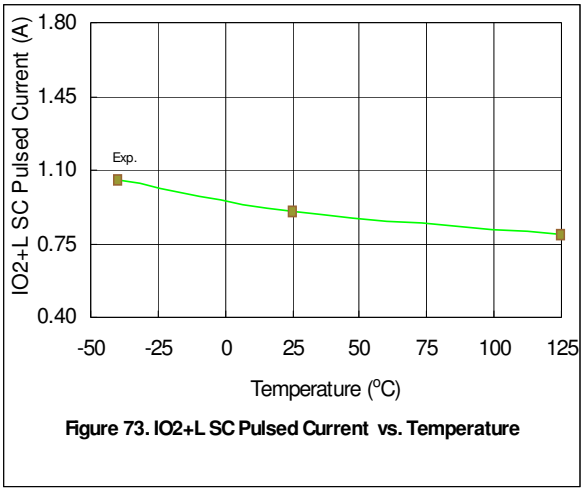


Figure 73. IO2+L SC Pulsed Current vs. Temperature

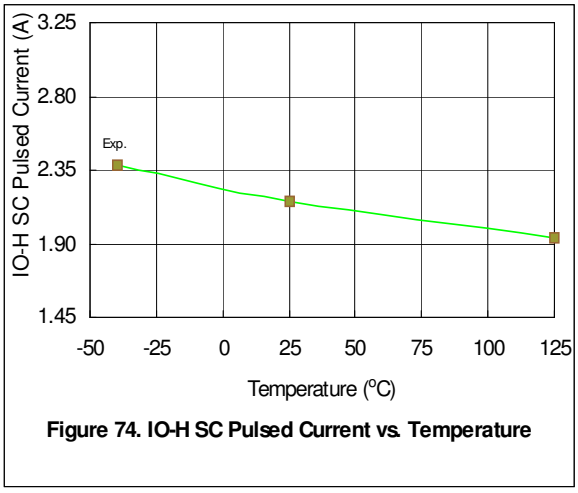


Figure 74. IO-H SC Pulsed Current vs. Temperature

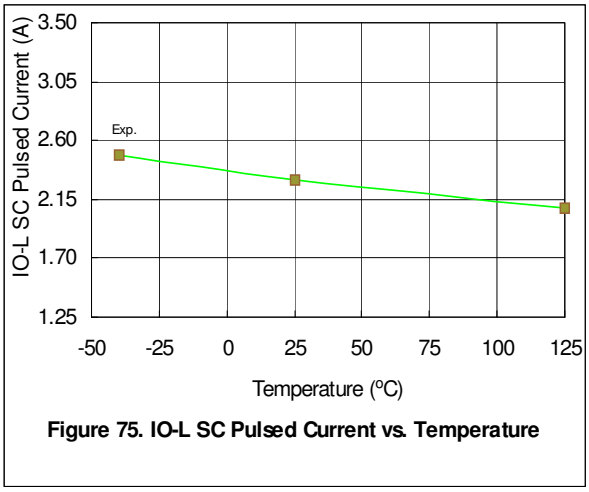


Figure 75. IO-L SC Pulsed Current vs. Temperature

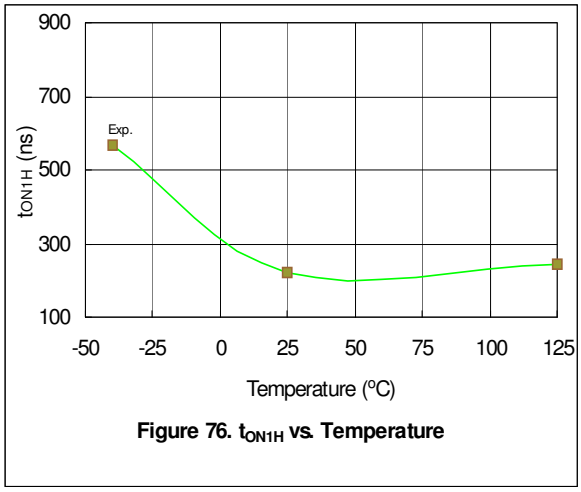


Figure 76. t_{ON1H} vs. Temperature

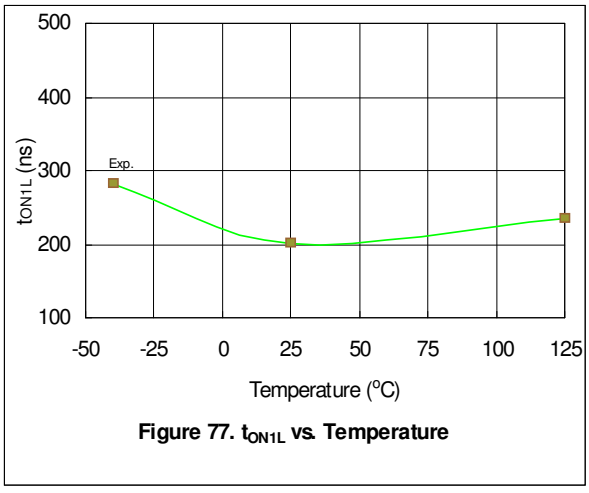


Figure 77. t_{ON1L} vs. Temperature

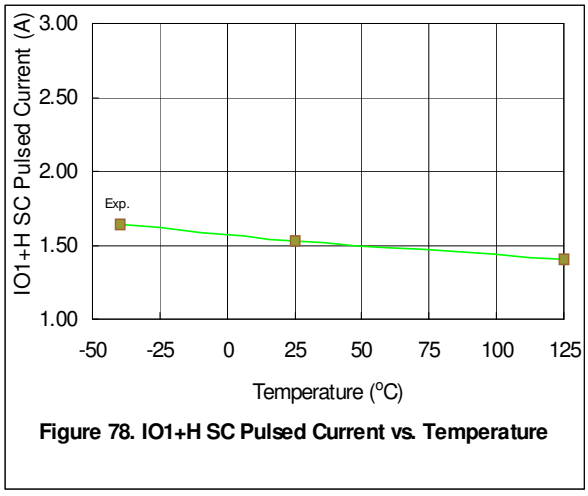


Figure 78. IO1+H SC Pulsed Current vs. Temperature

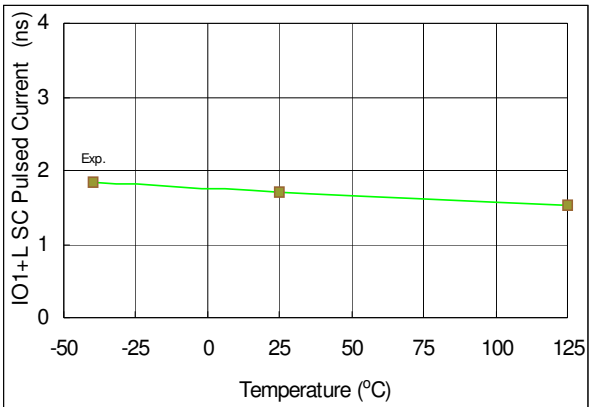


Figure 79. IO1+L SC Pulsed Current vs. Temperature

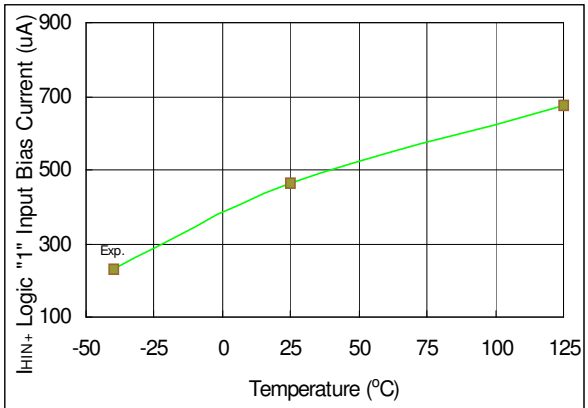


Figure 80. I_{HIN+} Logic "1" Input Bias Current vs. Temperature

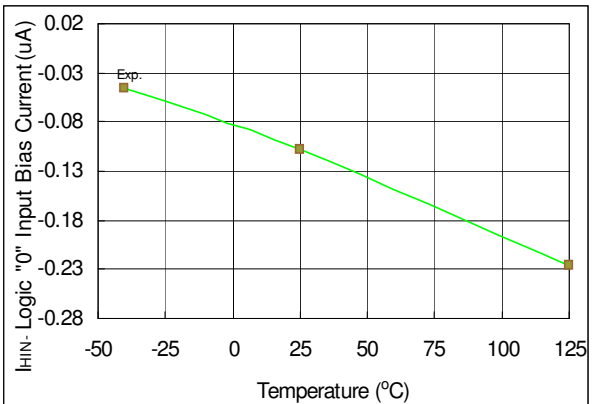


Figure 81. I_{HIN-} Logic "0" Input Bias Currentvs. Temperature

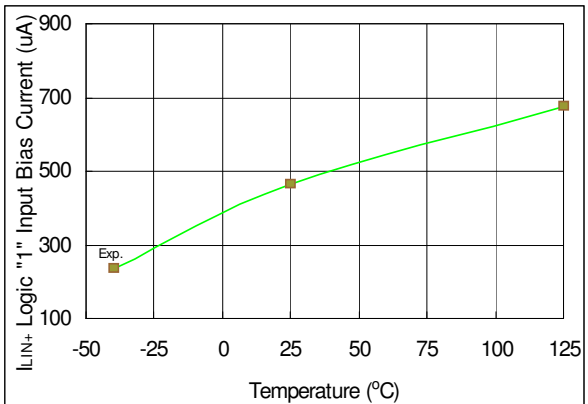


Figure 82. I_{LIN+} Logic "1" Input Bias Current vs. Temperature

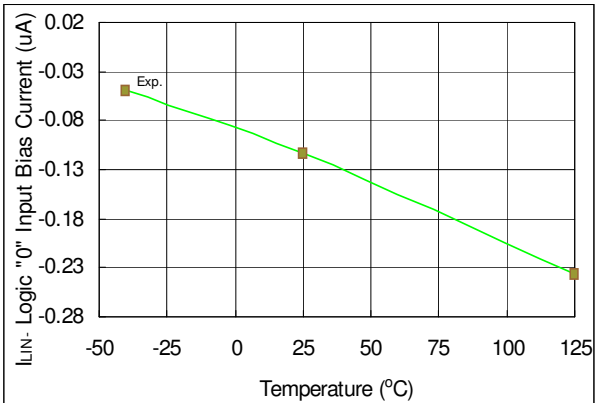
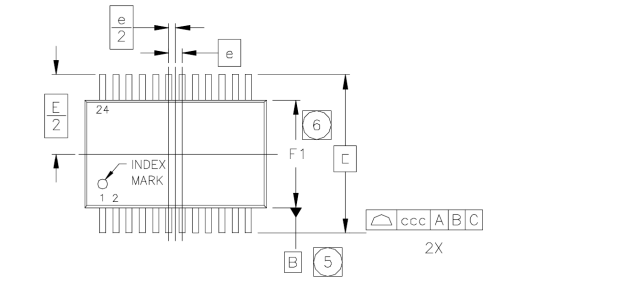
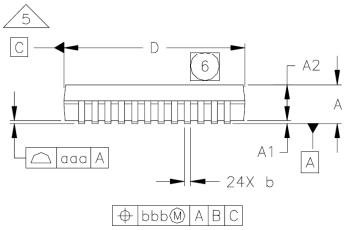
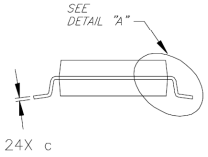


Figure 83. I_{LIN-} Logic "0" Input Bias Current vs. Temperature

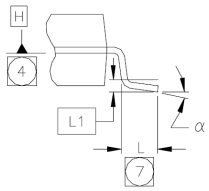
Case Outline





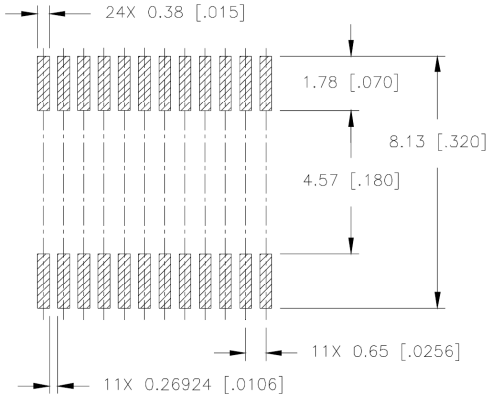


SYMBOL	DIMENSIONS					
	MILLIMETERS			INCHES		
	MO-150AH			MO-150AH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	2.00	.068	.073	.078
A1	0.05	0.13	0.20	.002	.005	.008
A2	1.65	1.75	1.85	.065	.069	.073
b	0.22	0.30	0.38	.009	.012	.015
c	0.09	0.15	0.25	.004	.006	.010
D	7.90	8.20	8.50	.311	.323	.334
E	7.80 BSC			.307		
E1	5.00	5.30	5.60	.197	.209	.221
e	0.65 BSC			.026 BSC		
L	0.55	0.75	0.95	.022	.030	.037
L1	0.25 BSC			.010 BSC		
α	0°	4°	8°	0°	4°	8°
aaa	0.10			.004		
bbb	0.15			.006		
ccc	0.20			.008		



DETAIL "A"

MINIMUM RECOMMENDED FOOTPRINT

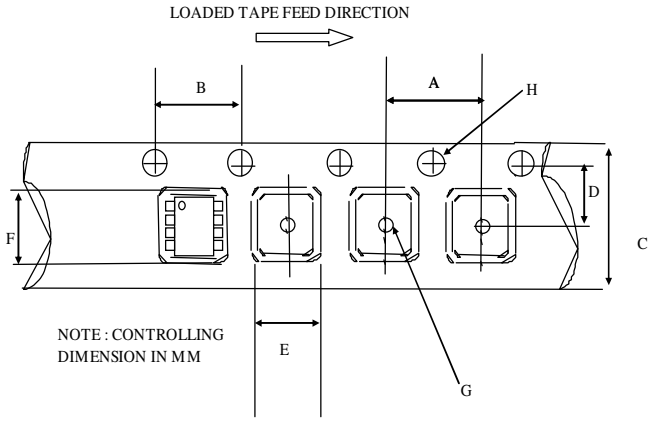


NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
5. DATUM B AND C TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM PLANE H.
7. L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE MO-150AH.

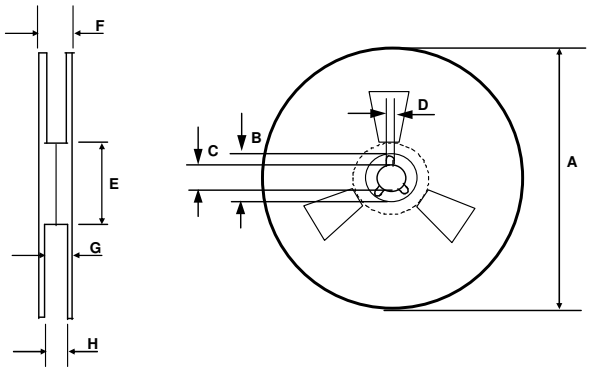
24-Lead SSOP

01 6076 01
01 5537 01 MO-150AH



CARRIER TAPE DIMENSION FOR 24SSOP:2000 units per reel

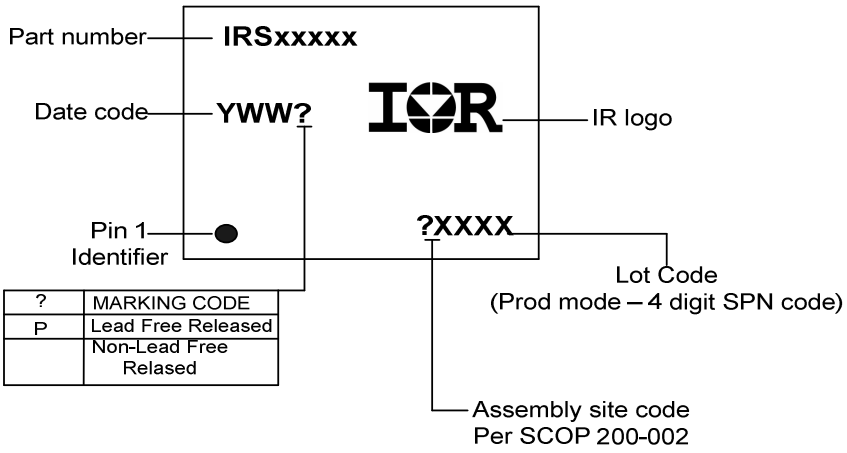
	Metric		Imperial	
Code	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	8.30	8.50	0.326	0.334
F	8.50	8.70	0.334	0.342
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 24SSOP

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

ORDER INFORMATION

24-Lead SSOP IR2114SSPbF
24-Lead SSOP IR2214SSPbF

24-Lead SSOP Tape & Reel IR2114SSPbF
24-Lead SSOP Tape & Reel IR2214SSPbF

International
IOR Rectifier

WORLDWIDE HEADQUARTERS: 233 Kansas Street, El Segundo, CA 90245 Tel: (310) 252-7105
This part has been qualified per industrial level
http://www.irf.com Data and specifications subject to change without notice. 5/18/2006

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