

## FEATURES

**Low noise, low input bias current FET input amplifier**

**Very low input bias current:  $\pm 0.25$  pA typical at 25°C**

**Low input voltage noise**

**92 nV/ $\sqrt{\text{Hz}}$  typical at 10 Hz at 5 V**

**5 nV/ $\sqrt{\text{Hz}}$  typical at 100 kHz at  $\pm 5$  V**

**Gain bandwidth product: 175 MHz**

**Input capacitance**

**3 pF typical, differential mode**

**2 pF typical, common mode**

**Integrated gain switching**

**Sampling and feedback switch off leakage:  $\pm 0.5$  pA typical**

**Worst case  $t_{\text{ON}}/t_{\text{OFF}}$  times: 105 ns typical/65 ns typical**

**Integrated analog-to-digital converter (ADC) driver**

**Differential mode and single-ended mode**

**Adjustable output common-mode voltage**

**$-5$  V to  $+3.8$  V typical for  $\pm 5$  V supply**

**Wide output voltage swing:  $\pm 4.8$  V minimum for  $\pm 5$  V supply**

**Linear output current: 18 mA rms typical for  $\pm 5$  V supply**

**SPI or parallel switch control of all functions**

**Wide operating range: 3.3 V to 12 V**

**Quiescent current: 8.5 mA typical ( $\pm 5$  V full system)**

## APPLICATIONS

**Current to voltage (I to V) conversions**

**Photodiode preamplifiers**

**Chemical analyzers**

**Mass spectrometry**

**Molecular spectroscopy**

**Laser/LED receivers**

**Data acquisition systems**

## GENERAL DESCRIPTION

The [ADA4350](#) is an analog front end for photodetectors or other sensors whose output produces a current proportional to the sensed parameter or voltage input applications where the system requires the user to select between very precise gain levels to maximize the dynamic range.

The [ADA4350](#) integrates a FET input amplifier, a switching network, and an ADC driver with all functions controllable via a serial peripheral interface (SPI) or parallel control logic into a single IC. The FET input amplifier has very low voltage noise and current noise making it an excellent choice to work with a wide range of photodetectors, sensors, or precision data acquisition systems.

Its switching network allows the user individual selection of up to six different, externally configurable feedback networks; by using external components for the feedback network, the user can more easily match the system to their desired photodetector or sensor capacitance. This feature also allows the use of low thermal drift resistors, if required.

The design of the switches minimizes error sources so that they add virtually no error in the signal path. The output driver can be used in either single-ended or a differential mode and is ideal for driving the input of an ADC.

The [ADA4350](#) can operate from a single  $+3.3$  V supply or a dual  $\pm 5$  V supply, offering user flexibility when choosing the polarity of the detector. It is available in a Pb-free, 28-lead TSSOP package and is specified to operate over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.

Multifunction pin names may be referenced by their relevant function only.

## FUNCTIONAL BLOCK DIAGRAM

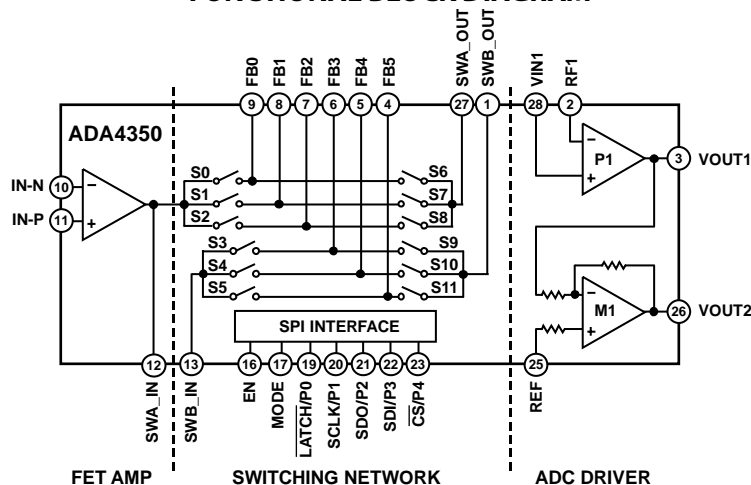


Figure 1.

Rev. B

[Document Feedback](#)

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## REVISION HISTORY

### 3/16—Rev. A to Rev. B

Change to Table 15 .....	29
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### 12/15—Rev. 0 to Rev. A

Changes to Table 1 .....	3
Changes to Table 5 .....	8
Deleted Figure 4; Renumbered Sequentially .....	14
Changes to Table 10 .....	15
Changes to Table 14 .....	29

### 4/15—Revision 0: Initial Version

## SPECIFICATIONS

## ±5 V FULL SYSTEM

$T_A = 25^\circ\text{C}$ ,  $+V_S = +5\text{ V}$ ,  $-V_S = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$  differential, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	Gain (G) = –5, $V_{OUT} = 200\text{ mV p-p}$		20		MHz
	G = –5, $V_{OUT} = 2\text{ V p-p}$		12		MHz
Slew Rate	$V_{OUT} = 2\text{ V step}$ , 10% to 90%		60		V/ $\mu\text{s}$
HARMONIC PERFORMANCE					
Harmonic Distortion (HD2/HD3)	G = –5, $f_C = 100\text{ kHz}$		–95/–104		dBc
	G = –5, $f_C = 1\text{ MHz}$		–77/–78		dBc
DC PERFORMANCE					
Input Bias Current	At $25^\circ\text{C}$		$\pm 0.25$	$\pm 1$	pA
	At $85^\circ\text{C}$		$\pm 8$	$\pm 25$	pA
INPUT CHARACTERISTICS					
Input Resistance	Common mode		100		G $\Omega$
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	Common-mode rejection ratio (CMRR) > 80 dB	–4.5		+3.8	V
	CMRR > 68 dB	–5		+3.9	V
Common-Mode Rejection	$V_{CM} = \pm 3.0\text{ V}$	92	104		dB
OUTPUT CHARACTERISTICS					
Linear Output Current	$V_{OUT} = 4\text{ V p-p}$ , 60 dB spurious-free dynamic range (SFDR)		18		mA rms
Short-Circuit Current	Sinking/sourcing		43/76		mA
Settling Time to 0.1%	G = –5, $V_{OUT} = 2\text{ V step}$		100		ns
ANALOG POWER SUPPLY ( $+V_S$ , $-V_S$ )					
Operating Range		3.3		12	V
Quiescent Current	Enabled		8.5	10	mA
	M1 disabled (see Figure 1)		7		mA
	All disabled		2		$\mu\text{A}$
Positive Power Supply Rejection Ratio			90		dB
Negative Power Supply Rejection Ratio			85		dB
DIGITAL SUPPLIES					
Digital Supply Range	DVDD, DGND	3.3		5.5	V
Quiescent Current	Enabled		50		$\mu\text{A}$
	Disabled		0.6		$\mu\text{A}$
$+V_S$ to DGND Head Room			$\geq 3.3$		V

**±5 V FET INPUT AMPLIFIER**

$T_A = 25^\circ\text{C}$ ,  $+V_S = +5\text{ V}$ ,  $-V_S = -5\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
–3 dB Bandwidth	$G = -5$ , $V_{OUT} = 100\text{ mV p-p}$		26		MHz
	$G = -5$ , $V_{OUT} = 2\text{ V p-p}$		24		MHz
Gain Bandwidth Product			175		MHz
Slew Rate	$V_{OUT} = 2\text{ V step}$ , 10% to 90%		100		V/ $\mu\text{s}$
Settling Time to 0.1%	$G = -5$ , $V_{OUT} = 2\text{ V step}$		28		ns
<b>NOISE/HARMONIC PERFORMANCE</b>					
Harmonic Distortion (HD2/HD3)	$f = 100\text{ kHz}$ , $V_{OUT} = 2\text{ V p-p}$ , $G = -5$		–106/–114		dBc
	$f = 1\text{ MHz}$ , $V_{OUT} = 2\text{ V p-p}$ , $G = -5$		–83/–93		dBc
Input Voltage Noise	$f = 10\text{ Hz}$		85		nV/ $\sqrt{\text{Hz}}$
	$f = 100\text{ kHz}$		5		nV/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>					
Input Offset Voltage			15	80	$\mu\text{V}$
Input Offset Voltage Drift	From $-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.1	1.6	$\mu\text{V}/^\circ\text{C}$
	From $25^\circ\text{C}$ to $85^\circ\text{C}$		0.1	1.0	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	At $25^\circ\text{C}$		$\pm 0.25$	$\pm 1$	pA
	At $85^\circ\text{C}$		$\pm 8$	$\pm 25$	pA
Input Bias Offset Current	At $25^\circ\text{C}$		$\pm 0.1$	$\pm 0.8$	pA
	At $85^\circ\text{C}$		$\pm 0.5$		pA
Open-Loop Gain	$V_{OUT} = \pm 2\text{ V}$	106	115		dB
<b>INPUT CHARACTERISTICS</b>					
Input Resistance	Common mode		100		G $\Omega$
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	CMRR > 80 dB	–4.5		+3.8	V
	CMRR > 68 dB	–5		+3.9	V
Common-Mode Rejection Ratio	$V_{CM} = \pm 3\text{ V}$	92	115		V
<b>OUTPUT CHARACTERISTICS</b>					
Output Overdrive Recovery Time	$V_{OUT} = V_S \pm 10\%$		60		ns
Output Voltage Swing	$G = +21$ , $R_F = 1\text{ k}\Omega$ , $R_L$ open measured at FBx	–3.6 to +3.9	–4.05 to +4.07		V
	$G = +21$ , $R_F = 100\text{ k}\Omega$ , $R_L$ open measured at FBx	–4.7 to +4.8	–4.9 to +4.86		V
Linear Output Current	$V_{OUT} = 2\text{ V p-p}$ , 60 dB SFDR		18		mA rms
Short-Circuit Current	Sinking/sourcing		41/45		mA
<b>POWER SUPPLY</b>					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio		90	109		dB
Negative Power Supply Rejection Ratio		90	109		dB

**±5 V INTERNAL SWITCHING NETWORK AND DIGITAL PINS**

$T_A = 25^\circ\text{C}$ ,  $+V_S = +5\text{ V}$ ,  $-V_S = -5\text{ V}$ , unless otherwise specified. See Figure 1 for feedback and sampling switches notation.

**Table 3.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>FEEDBACK/SAMPLE ANALOG SWITCH</b>						
Analog Signal Range			-5		+5	V
Switch On-Resistance						
Feedback	$R_{ON, FB}$	For S0 to S2, $V_{CM} = 0\text{ V}$ $T_A = 85^\circ\text{C}$		149 195	196	$\Omega$ $\Omega$
		For S3 to S5, $V_{CM} = 0\text{ V}$ $T_A = 85^\circ\text{C}$		149 195	196	$\Omega$ $\Omega$
Sampling	$R_{ON, S}$	For S6 to S8, $V_{CM} = 0\text{ V}$ $T_A = 85^\circ\text{C}$		297 390	356	$\Omega$ $\Omega$
		For S9 to S11, $V_{CM} = 0\text{ V}$ $T_A = 85^\circ\text{C}$		297 388	356	$\Omega$ $\Omega$
On-Resistance Match Between Channels						
Feedback Resistance	$\Delta R_{ON, FB}$	$V_{CM} = 0\text{ V}$		2	15	$\Omega$
Sampling Resistance	$\Delta R_{ON, S}$	$V_{CM} = 0\text{ V}$		2	14	$\Omega$
<b>SWITCH LEAKAGE CURRENTS</b>						
Sampling and Feedback Switch Off Leakage	$I_{S(OFF)}$	$T_A = 85^\circ\text{C}$		$\pm 0.5$ $\pm 40$	$\pm 1.7$ $\pm 120$	pA pA
<b>DYNAMIC CHARACTERISTICS</b>						
Power-On Time	$t_{ON}$	DVDD = 5 V DVDD = 3.3 V		76 80		ns ns
Power-Off Time	$t_{OFF}$	DVDD = 5 V DVDD = 3.3 V		86 90		ns ns
Off Isolation		$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$				
Feedback Switches				-92		dB
Sampling Switches				-118		dB
Channel to Channel Crosstalk		$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$		-86		dB
Worst Case Switch Feedback Capacitance (Switch Off)	$C_{FB(OFF)}$			0.1		pF
<b>THRESHOLD VOLTAGES FOR DIGITAL INPUT PINS</b>						
Input High Voltage	$V_{IH}$	EN, MODE, DGND, $\overline{\text{LATCH}}/\text{P0}$ , SCLK/P1, SDO/P2, SDI/P3, $\overline{\text{CS}}/\text{P4}^1$ DVDD = 5 V DVDD = 3.3 V	2.0 1.5			V V
Input Low Voltage	$V_{IL}$	DVDD = 5 V DVDD = 3.3 V			1.4 1.0	V V
<b>DIGITAL SUPPLIES</b>						
Digital Supply Range		DVDD, DGND	3.3		5.5	V
Quiescent Current		Enabled Disabled		50 0.6		$\mu\text{A}$ $\mu\text{A}$
+Vs to DGND Head Room				$\geq 3.3$		V

<sup>1</sup> When referring to a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

**±5 V ADC DRIVER**

$T_A = 25^\circ\text{C}$ ,  $+V_S = +5\text{ V}$ ,  $-V_S = -5\text{ V}$ , unless otherwise specified. See Figure 1 for the P1 and M1 amplifiers.  $R_L = 1\text{ k}\Omega$  when differential, and  $R_L = 500\text{ }\Omega$  when single-ended.

**Table 4.**

Parameter	Test Conditions/Comments <sup>1</sup>	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
–3 dB Bandwidth	When used differentially, $V_{OUT} = 0.1\text{ V p-p}$		38		MHz
	When used differentially, $V_{OUT} = 2.0\text{ V p-p}$		16		MHz
	When P1 is used, $V_{OUT} = 50\text{ mV p-p}$		55		MHz
	When P1 is used, $V_{OUT} = 1.0\text{ V p-p}$		17		MHz
	When M1 is used, $V_{OUT} = 50\text{ mV p-p}$		45		MHz
	When M1 is used, $V_{OUT} = 1.0\text{ V p-p}$		21		MHz
Overdrive Recovery Time	Positive recovery/negative recovery for P1		200/180		ns
	Positive recovery/negative recovery for M1		100/100		ns
Slew Rate	When differentially used, $V_{OUT} = 2\text{ V step}$		57		V/ $\mu\text{s}$
	When P1 or M1 is single-ended, $V_{OUT} = 1\text{ V step}$		30		V/ $\mu\text{s}$
Settling Time 0.1%	When used differentially, $V_{OUT} = 2\text{ V step}$		95		ns
	When P1 is used, $V_{OUT} = 1\text{ V step}$		80		ns
	When M1 is used, $V_{OUT} = 1\text{ V step}$		80		ns
<b>NOISE/DISTORTION PERFORMANCE</b>					
Harmonic Distortion (HD2/HD3)	When used differentially, $f_c = 100\text{ kHz}$ , $V_{OUT} = 4\text{ V p-p}$		–105/–109		dBc
	When used differentially, $f_c = 1\text{ MHz}$ , $V_{OUT} = 4\text{ V p-p}$		–75/–73		dBc
	When P1 is used, $f_c = 100\text{ kHz}$ , $V_{OUT} = 2\text{ V p-p}$		–112/–108		dBc
	When P1 is used, $f_c = 1\text{ MHz}$ , $V_{OUT} = 2\text{ V p-p}$		–75/–73		dBc
	When M1 is used, $f_c = 100\text{ kHz}$ , $V_{OUT} = 2\text{ V p-p}$		–98/–103		dBc
	When M1 is used, $f_c = 1\text{ MHz}$ , $V_{OUT} = 2\text{ V p-p}$		–70/–69		dBc
Referred to Input (RTI) Voltage Noise	For P1, $f = 10\text{ Hz}$		55		nV/ $\sqrt{\text{Hz}}$
	For P1, $f = 100\text{ kHz}$		5		nV/ $\sqrt{\text{Hz}}$
Referred to Output (RTO) Voltage Noise	For P1 and M1, $f = 10\text{ Hz}$ , measured at VOUT2		95		nV/ $\sqrt{\text{Hz}}$
	For P1 and M1, $f = 100\text{ kHz}$ , measured at VOUT2		16		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$ , referred to P1		1.1		pA/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>					
Output Offset Voltage	Differential		0.125	0.5	mV
Output Offset Voltage Drift	Differential		0.7	13	$\mu\text{V}/^\circ\text{C}$
Input Offset Voltage	Single-ended, P1 only		50	180	$\mu\text{V}$
	Single-ended, M1 only		40	180	$\mu\text{V}$
Input Offset Voltage Drift	Single-ended, P1 only		0.2	4.75	$\mu\text{V}/^\circ\text{C}$
	Single-ended, M1 only		0.4	3.6	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	P1 only at VIN1 pin		60	220	nA
	P1 only at RF1 pin		60	325	nA
	M1 at REF pin		60	200	nA
Input Offset Current	P1 only		60	260	nA
Open-Loop Gain	P1 only, $V_{OUT} = \pm 2\text{ V}$	102	112		dB
Gain	M1 only	1.99	1.9996	2.01	V/V
Gain Error		–0.5		+0.5	%
Gain Error Drift			0.6	1.9	ppm/ $^\circ\text{C}$
<b>INPUT CHARACTERISTICS</b>					
Input Resistance	VIN1 and REF		200		M $\Omega$
Input Capacitance	VIN1 and REF		1.4		pF
Input Common-Mode Voltage Range		–5		+3.8	V
Common-Mode Rejection Ratio	For P1, $V_{CM} = \pm 3.0\text{ V}$	82	100		dB

Parameter	Test Conditions/Comments <sup>1</sup>	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L = \text{no load, single-ended}$	$\pm 4.8$	$\pm 4.83$		V
	$R_L = 500\ \Omega$ , single-ended	$\pm 4.55$	$\pm 4.6$		V
Output Common-Mode Voltage Range		-5		+3.8	V
Linear Output Current	P1 or M1, $V_{OUT} = 2\text{ V p-p}$ , 60 dB SFDR		18		mA rms
	Differential output, $V_{OUT} = 4\text{ V p-p}$ , 60 dB SFDR		18		mA rms
Short Circuit Current	P1 or M1, sinking/sourcing		43/76		mA
Capacitive Load Drive	When used differentially at each $V_{OUTx}$ , 30% overshoot, $V_{OUT} = 200\text{ mV p-p}$		33		pF
	When P1/M1 is used, 30% overshoot, $V_{OUT} = 100\text{ mV p-p}$		47		pF
POWER SUPPLY					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio	For P1	90	106		dB
	For M1	86	100		dB
Negative Power Supply Rejection Ratio	For P1	80	100		dB
	For M1	78	90		dB

<sup>1</sup> P1 and M1 within this table refer to the amplifiers shown in Figure 1.

**5 V FULL SYSTEM**

$T_A = 25^\circ\text{C}$ ,  $+V_S = 5\text{ V}$ ,  $-V_S = 0\text{ V}$ ,  $R_F = 1\text{ k}\Omega$  differential, unless otherwise specified.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
–3 dB Bandwidth	$G = -5$ , $V_{OUT} = 200\text{ mV p-p}$		15		MHz
	$G = -5$ , $V_{OUT} = 1\text{ V p-p}$		14		MHz
Slew Rate	$V_{OUT} = 2\text{ V step}$ , 10% to 90%		30		V/ $\mu\text{s}$
<b>HARMONIC PERFORMANCE</b>					
Harmonic Distortion (HD2/HD3)	$G = -5$ , $f_c = 100\text{ kHz}$		–85/–94		dBc
	$G = -5$ , $f_c = 1\text{ MHz}$		–66/–75		dBc
Input Voltage Noise	$f = 10\text{ Hz}$		92		nV/ $\sqrt{\text{Hz}}$
	$f = 100\text{ kHz}$		4.4		nV/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>					
Input Bias Current	At $25^\circ\text{C}$		$\pm 0.35$	$\pm 1.6$	pA
	At $85^\circ\text{C}$		$\pm 8.5$	$\pm 30$	pA
<b>INPUT CHARACTERISTICS</b>					
Input Resistance	Common mode		100		G $\Omega$
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	CMRR > 80 dB	0.5		3.8	V
	CMRR > 68 dB	0		3.9	V
Common-Mode Rejection	$V_{CM} = \pm 0.5\text{ V}$	88	94		dB
<b>OUTPUT CHARACTERISTICS</b>					
Linear Output Current	$V_{OUT} = 1\text{ V p-p}$ , 60 dB SFDR		9		mA rms
Short-Circuit Current	Sinking/sourcing, $R_L < 1\text{ }\Omega$		41/63		mA
Settling Time to 0.1%	$G = -5$ , $V_{OUT} = 2\text{ V step}$		130		ns
<b>POWER SUPPLY</b>					
Operating Range		3.3		12	V
Quiescent Current	Enabled		8	9	mA
	M1 disabled (see Figure 1)		6.5		mA
	All disabled		2		$\mu\text{A}$
Positive Power Supply Rejection Ratio			86		dB
Negative Power Supply Rejection Ratio			80		dB
<b>DIGITAL SUPPLIES (DVDD, DGND)</b>					
Digital Supply Range	DVDD, DGND	3.3		5.5	V
Quiescent Current	Enabled		50		$\mu\text{A}$
	Disabled		0.6		$\mu\text{A}$
$+V_S$ to DGND Head Room			$\geq 3.3$		V



**5 V FET INPUT AMPLIFIER**

$T_A = 25^\circ\text{C}$ ,  $+V_S = 5\text{ V}$ ,  $-V_S = 0\text{ V}$ ,  $R_L = 1\text{ k}\Omega$ , unless otherwise specified.

**Table 6.**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
–3 dB Bandwidth	$G = -5$ , $V_{OUT} = 100\text{ mV p-p}$		25		MHz
	$G = -5$ , $V_{OUT} = 1\text{ V p-p}$		24		MHz
Gain Bandwidth Product			175		MHz
Slew Rate	$V_{OUT} = 2\text{ V step}$ , 10% to 90%		56		V/ $\mu\text{s}$
Settling Time to 0.1%	$G = -5$ , $V_{OUT} = 2\text{ V step}$		60		ns
<b>NOISE/HARMONIC PERFORMANCE</b>					
Harmonic Distortion (HD2/HD3)	$f = 100\text{ kHz}$ , $V_{OUT} = 1\text{ V p-p}$ , $G = -5$		–113/–117		dBc
	$f = 1\text{ MHz}$ , $V_{OUT} = 1\text{ V p-p}$ , $G = -5$		–82/–83		dBc
Input Voltage Noise	$f = 10\text{ Hz}$		92		nV/ $\sqrt{\text{Hz}}$
	$f = 100\text{ kHz}$		4.4		nV/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>					
Input Offset Voltage			25	80	$\mu\text{V}$
Input Offset Voltage Drift	From $-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.1	1.5	$\mu\text{V}/^\circ\text{C}$
	From $25^\circ\text{C}$ to $85^\circ\text{C}$		0.05	1	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	At $25^\circ\text{C}$		$\pm 0.35$	$\pm 1.6$	pA
	At $85^\circ\text{C}$		$\pm 8.5$	$\pm 30$	pA
Input Bias Offset Current	At $25^\circ\text{C}$		$\pm 0.25$	$\pm 1.25$	pA
	At $85^\circ\text{C}$		$\pm 0.4$		pA
Open-Loop Gain	$V_{OUT} = 1.5\text{ V to }3.5\text{ V}$	98	102		dB
<b>INPUT CHARACTERISTICS</b>					
Input Resistance	Common mode		100		G $\Omega$
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	CMRR > 80 dB	0.5		3.8	V
	CMRR > 68 dB	0		3.9	V
Common-Mode Rejection Ratio	$V_{CM} = \pm 0.5\text{ V}$	88	94		dB
<b>OUTPUT CHARACTERISTICS</b>					
Output Overdrive Recovery Time	$V_{OUT} = V_S \pm 10\%$ , positive/negative		60/50		ns
Output Voltage Swing	$G = +21$ , $R_F = 1\text{ k}\Omega$ , $R_L$ open measured at FBx	1.15 to 3.46	0.86 to 3.66		V
	$G = +21$ , $R_F = 100\text{ k}\Omega$ , $R_L$ open measured at FBx	0.27 to 4.80	0.08 to 4.87		V
Linear Output Current	$V_{OUT} = 1\text{ V p-p}$ , 60 dB SFDR		10		mA rms
Short-Circuit Current	Sinking/sourcing		32/38		mA
<b>POWER SUPPLY</b>					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio		90	100		dB
Negative Power Supply Rejection Ratio		86	100		dB

**5 V INTERNAL SWITCHING NETWORK AND DIGITAL PINS**

$T_A = 25^\circ\text{C}$ ,  $+V_S = 5\text{ V}$ ,  $-V_S = 0\text{ V}$ , unless otherwise specified. See Figure 1 for sampling and feedback switches position.

**Table 7.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>FEEDBACK/SAMPLE ANALOG SWITCH</b>						
Analogue Signal Range			0		5	V
Switch On Resistance						
Feedback	$R_{ON, FB}$	$S0\text{ to }S2, V_{CM} = 2.5\text{ V}$ $T_A = 85^\circ\text{C}$		308 382	390	$\Omega$ $\Omega$
		$S3\text{ to }S5, V_{CM} = 2.5\text{ V}$ $T_A = 85^\circ\text{C}$		308 384	390	$\Omega$ $\Omega$
Sampling	$R_{ON, S}$	$S6\text{ to }S8, V_{CM} = 2.5\text{ V}$ $T_A = 85^\circ\text{C}$		610 762	770	$\Omega$ $\Omega$
		$S9\text{ to }S11, V_{CM} = 2.5\text{ V}$ $T_A = 85^\circ\text{C}$		612 764	770	$\Omega$ $\Omega$
On-Resistance Match Between Channels						
Feedback Resistance	$\Delta R_{ON, FB}$	$V_{CM} = 2.5\text{ V}$		3	21	$\Omega$
Sampling Resistance	$\Delta R_{ON, S}$	$V_{CM} = 2.5\text{ V}$		3	23	$\Omega$
<b>SWITCH LEAKAGE CURRENTS</b>						
Sampling and Feedback Switch Off Leakage	$I_{S(OFF)}$	$T_A = 85^\circ\text{C}$		$\pm 0.4$ $\pm 30$	$\pm 1.2$ $\pm 80$	pA pA
<b>DYNAMIC CHARACTERISTICS</b>						
Power-On Time	$t_{ON}$	$DVDD = 3.3\text{ V}$		105		ns
Power-Off Time	$t_{OFF}$	$DVDD = 3.3\text{ V}$		65		ns
Off Isolation		$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$				
Feedback Switches				-93		dB
Sampling Switches				-116		dB
Channel to Channel Crosstalk		$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$		-83		dB
Worst Case Switch Feedback Capacitance (Switch Off)	$C_{FB(OFF)}$			0.1		pF
<b>THRESHOLD VOLTAGES FOR DIGITAL INPUT PINS</b>						
Input High Voltage	$V_{IH}$	EN, MODE, DGND, <u>LATCH/P0</u> , SCLK/P1, SDO/P2, SDI/P3, <u>CS/P4</u> <sup>1</sup> $DVDD = 5\text{ V}$	2.0			V
		$DVDD = 3.3\text{ V}$	1.5			V
Input Low Voltage	$V_{IL}$	$DVDD = 5\text{ V}$			1.4	V
		$DVDD = 3.3\text{ V}$			1.0	V
<b>DIGITAL SUPPLIES</b>						
Digital Supply Range		DVDD, DGND	3.3		5.5	V
Quiescent Current		Enabled		50		$\mu\text{A}$
		Disabled		0.6		$\mu\text{A}$
$+V_S$ to DGND Head Room				$\geq 3.3$		V

<sup>1</sup> When referring to a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

**5 V ADC DRIVER**

$T_A = 25^\circ\text{C}$ ,  $+V_S = 5\text{ V}$ ,  $-V_S = 0\text{ V}$ , unless otherwise specified. See Figure 1 for the P1 and M1 amplifiers,  $R_L = 1\text{ k}\Omega$  when differential, and  $R_L = 500\text{ }\Omega$  when single-ended.

**Table 8.**

Parameter	Test Conditions/Comments <sup>1</sup>	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
–3 dB Bandwidth	When used differentially, $V_{OUT} = 0.1\text{ V p-p}$		33		MHz
	When used differentially, $V_{OUT} = 2.0\text{ V p-p}$		16		MHz
	When P1 is used, $V_{OUT} = 50\text{ mV p-p}$		47		MHz
	When P1 is used, $V_{OUT} = 1.0\text{ V p-p}$		16		MHz
	When M1 is used, $V_{OUT} = 50\text{ mV p-p}$		37		MHz
	When M1 is used, $V_{OUT} = 1.0\text{ V p-p}$		18		MHz
Overdrive Recovery Time	For P1, positive recovery/negative recovery		200/200		ns
	For M1, positive recovery/negative recovery		140/120		ns
Slew Rate	When differentially used, $V_{OUT} = 2\text{ V step}$		37		V/ $\mu\text{s}$
	When P1 or M1 is single-ended, $V_{OUT} = 1\text{ V step}$		20		V/ $\mu\text{s}$
Settling Time 0.1%	When used differentially, $V_{OUT} = 2\text{ V step}$		75		ns
	When P1 is used, $V_{OUT} = 1\text{ V step}$		60		ns
	When M1 is used, $V_{OUT} = 1\text{ V step}$		60		ns
<b>NOISE/DISTORTION PERFORMANCE</b>					
Harmonic Distortion (HD2/HD3)	When used differentially, $f_C = 100\text{ kHz}$ , $V_{OUT} = 1\text{ V p-p}$		–117/–116		dBc
	When used differentially, $f_C = 1\text{ MHz}$ , $V_{OUT} = 1\text{ V p-p}$		–80/–85		dBc
	When P1 is used, $f_C = 100\text{ kHz}$ , $V_{OUT} = 500\text{ mV p-p}$		–108/–115		dBc
	When P1 is used, $f_C = 1\text{ MHz}$ , $V_{OUT} = 500\text{ mV p-p}$		–80/–83		dBc
	When M1 is used, $f_C = 100\text{ kHz}$ , $V_{OUT} = 500\text{ mV p-p}$		–103/–107		dBc
	When M1 is used, $f_C = 1\text{ MHz}$ , $V_{OUT} = 500\text{ mV p-p}$		–75/–78		dBc
Referred to Input (RTI) Voltage Noise	For P1, $f = 10\text{ Hz}$		60		nV/ $\sqrt{\text{Hz}}$
	For P1, $f = 100\text{ kHz}$		5.2		nV/ $\sqrt{\text{Hz}}$
Referred to Output (RTO) Voltage Noise	For P1 and M1, $f = 10\text{ Hz}$ , measured at VOUT2		140		nV/ $\sqrt{\text{Hz}}$
	For P1 and M1, $f = 100\text{ kHz}$ , measured at VOUT2		18		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$ , referred to P1		1.1		pA/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>					
Output Offset Voltage	Differential		0.15	0.75	mV
Input Offset Voltage Drift	Differential		0.6	16	$\mu\text{V}/^\circ\text{C}$
Output Offset Voltage	Single-ended, P1 only		60	275	$\mu\text{V}$
	Single-ended, M1 only		70	250	$\mu\text{V}$
Input Offset Voltage Drift	Single-ended, P1 only		0.1	5.9	$\mu\text{V}/^\circ\text{C}$
	Single-ended, M1 only		0.3	4.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	P1 only at VIN1 pin		60	230	nA
	P1 only at RF1 pin		60	350	nA
	M1 only at REF pin		60	200	nA
Input Offset Current	P1 only		60	270	nA
Open-Loop Gain	P1 only, $V_{OUT} = 1.5\text{ V to }3.5\text{ V}$	94	100		dB
Gain	M1 only	1.99	1.9995	2.01	V/V
Gain Error		–0.5		+0.5	%
Gain Error Drift			0.6	3.4	ppm/ $^\circ\text{C}$

Parameter	Test Conditions/Comments <sup>1</sup>	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>					
Input Resistance	VIN1 and REF		200		MΩ
Input Capacitance	VIN1 and REF		1.4		pF
Input Common-Mode Voltage Range		0		3.9	V
Common-Mode Rejection Ratio	For P1, $V_{CM} = \pm 0.5$ V	84	94		dB
<b>OUTPUT CHARACTERISTICS</b>					
Output Voltage Swing	$R_L =$ no load, single-ended	0.15 to 4.85	0.125 to 4.875		V
	$R_L = 500 \Omega$ , single-ended	0.28 to 4.72	0.24 to 4.76		V
Output Common-Mode Voltage Range		0		3.9	V
Linear Output Current	For P1 or M1, $V_{OUT} = 1$ V p-p, 60 dB SFDR		4		mA rms
	Differential output, $V_{OUT} = 1$ V p-p, 60 dB SFDR		10		mA rms
Short-Circuit Current	For P1 or M1, sinking/sourcing		41/63		mA
Capacitive Load Drive	When used differentially at each $V_{OUTx}$ , 30% overshoot, $V_{OUT} = 100$ mV p-p		33		pF
	When P1/M1 is used, 30% overshoot, $V_{OUT} = 50$ mV p-p		47		pF
<b>POWER SUPPLY</b>					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio	For P1	86	104		dB
	For M1	80	94		dB
Negative Power Supply Rejection Ratio	For P1	80	92		dB
	For M1	76	88		dB

<sup>1</sup> P1 and M1 within this table refer to the amplifiers shown in Figure 1.

## TIMING SPECIFICATIONS

All input signals are specified with  $t_R = t_F = 2$  ns (10% to 90% of DVDD) and timed from a voltage threshold level of  $V_{TH} = 1.3$  V at DVDD = 3.3 V or  $V_{TH} = 1.7$  V at DVDD = 5 V. Guaranteed by characterization; not production tested. See Figure 2 and Figure 3.

Table 9.

Parameter	Description <sup>1</sup>	DVDD = 3.3 V		DVDD = 5 V		Unit
		Min	Max	Min	Max	
$t_1$	SCLK period.	20		20		ns
$t_2$	SCLK positive pulse width.	10		10		ns
$t_3$	SCLK negative pulse width.	10		10		ns
$t_4$	$\overline{CS}$ setup time. The time required to begin sampling data after $\overline{CS}$ goes low.	1		1		ns
$t_5$	$\overline{CS}$ hold time. The amount of time required for $\overline{CS}$ to be held low after the last data bit is sampled before bringing $\overline{CS}$ high. Data is latched on the $\overline{CS}$ rising edge. If LATCH is held low, data is also applied on the $\overline{CS}$ rising edge.	7		5		ns
$t_6$	$\overline{CS}$ positive pulse width. The amount of time required between consecutive words.	2		1		ns
$t_7$	Data setup time. The amount of time the data bit (SDI) must be set before sampling on the falling edge of SCLK.	1		1		ns
$t_8$	Data hold time. The amount of time SDI must be held after the falling edge of SCLK for valid data to be sampled.	2		2		ns
$t_9$	Data latched to the internal switches updated. The amount of time it takes from the latched data being applied until the internal switches are updated.		145		140	ns
	$\overline{LATCH}$ disabled referenced from the rising edge of $\overline{CS}$ .					
	$\overline{LATCH}$ enabled referenced from the falling edge of $\overline{LATCH}$ .					
$t_{10}$	$\overline{LATCH}$ negative pulse width.	3		3		ns
$t_{11}^2$	SCLK rising edge to SDO valid. The amount of time between the SCLK rising edge and the valid SDO transitions ( $CL_{SDO}^3 = 20$ pF).		15		10	ns
$t_{12}$	$\overline{CS}$ rising edge to the SCLK falling edge. The amount of time required to prevent a 25 <sup>th</sup> SCLK edge from being recognized (only 24 bits allowed for valid word).	1		1		ns

<sup>1</sup> When referring to a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

<sup>2</sup> This is while in daisy-chain mode and in readback mode.

<sup>3</sup>  $CL_{SDO}$  is the capacitive load on the SDO output.

## Timing Diagrams for Serial Mode

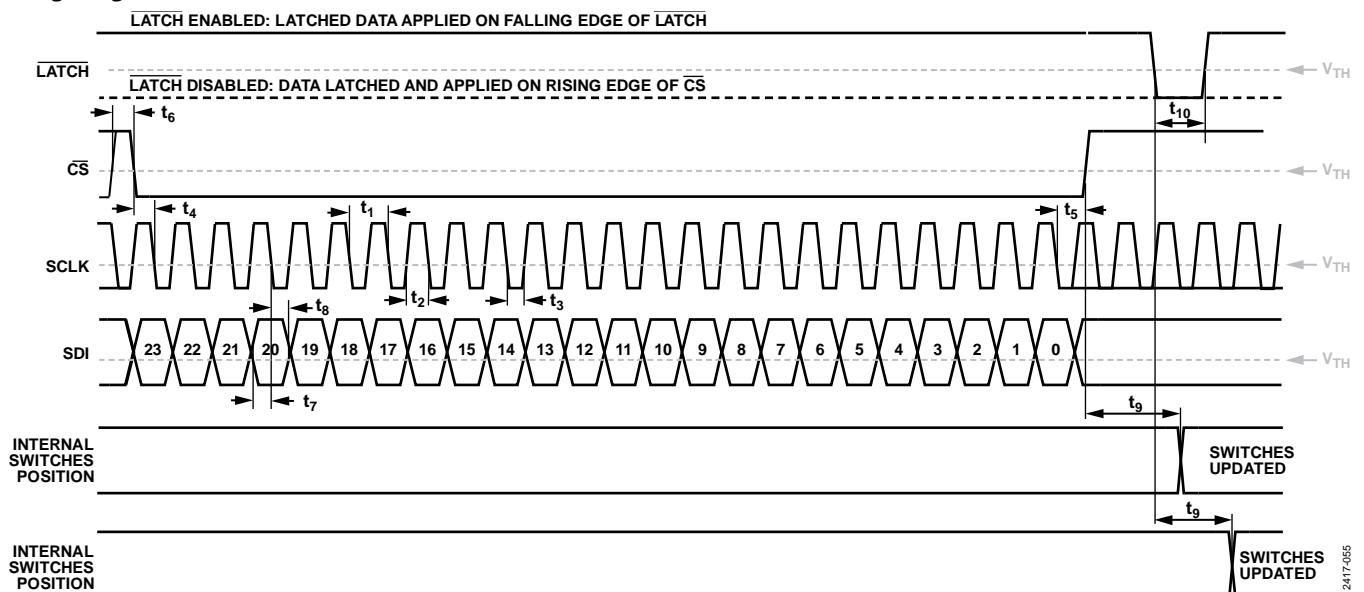


Figure 2. Write Operation

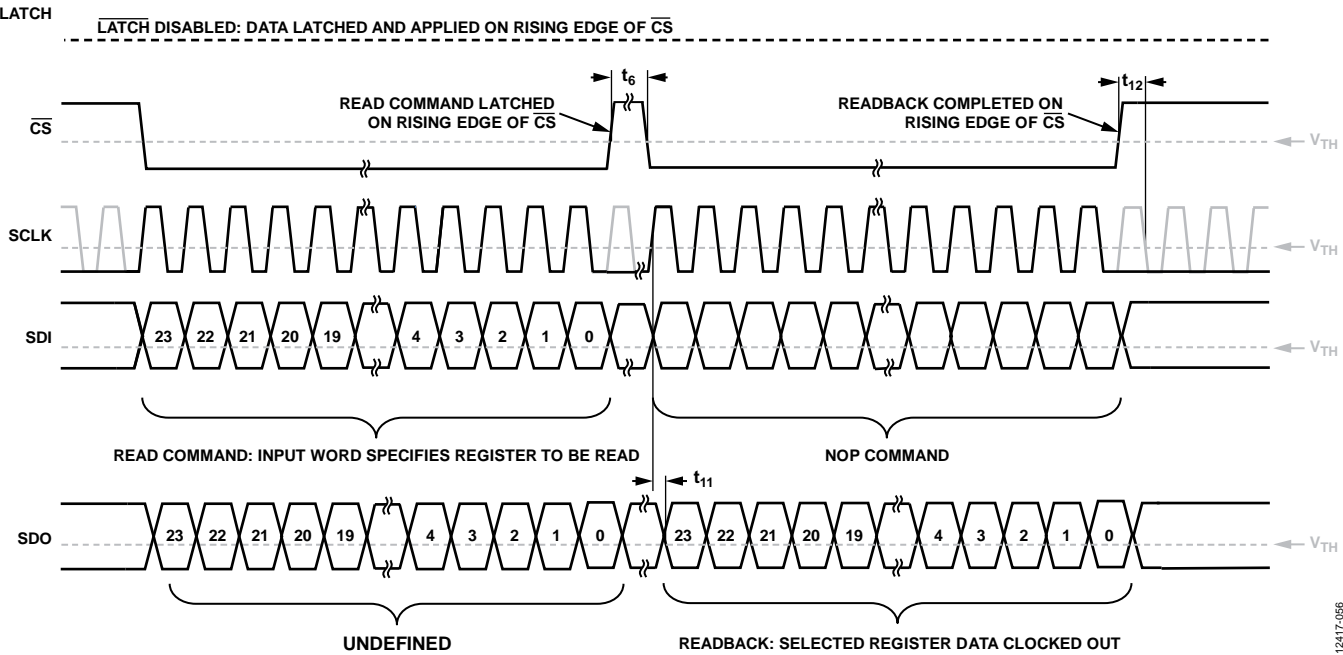


Figure 3. Read Operation

## ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
Analog Supply Voltage	14 V
Digital Supply Voltage	5.5 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage	$\pm V_S \pm 0.3V$
Differential Input Voltage	$\pm 0.7V$
Input Current (IN-N, IN-P, VIN1, RF1, and REF)	20 mA
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst case conditions, that is,  $\theta_{JA}$  is specified for a device soldered in a circuit board for surface-mount packages. Table 11 lists the  $\theta_{JA}$  for the ADA4350.

Table 11. Thermal Resistance

Package Type	$\theta_{JA}$	Unit
28-Lead TSSOP	72.4	°C/W

### MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4350 is limited by the associated rise in junction temperature ( $T_J$ ) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4350. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package ( $P_D$ ) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4350 output load drive.

The quiescent power dissipation is the voltage between the supply pins ( $\pm V_S$ ) multiplied by the quiescent current ( $I_S$ ).

$$P_D = \text{Quiescent Power} + (\text{Total Drive Power} - \text{Load Power})$$

$$P_D = (\pm V_S \times I_S) + \left( \frac{\pm V_S}{2} \times \frac{V_{OUT}}{R_L} \right) - \frac{V_{OUT}^2}{R_L}$$

Consider rms output voltages. If  $R_L$  is referenced to  $-V_S$ , as in single-supply operation, the total drive power is  $+V_S \times I_{OUT}$ . If the rms signal levels are indeterminate, consider the worst case, when  $V_{OUT} = +V_S/4$  for  $R_L$  to midsupply for dual supplies and  $V_{OUT} = +V_S/2$  for single supply.

$$P_D = (+V_S \times I_S) + \frac{(V_{OUT})^2}{R_L}$$

Airflow increases heat dissipation, effectively reducing  $\theta_{JA}$ . In addition, more metal directly in contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes reduces  $\theta_{JA}$ .

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard 4-layer board.  $\theta_{JA}$  values are approximations.

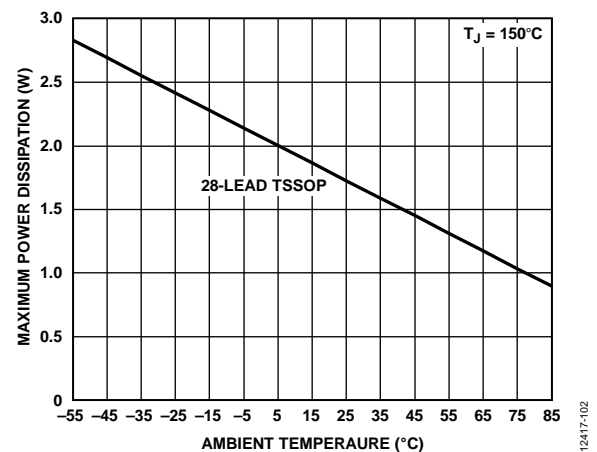


Figure 4. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

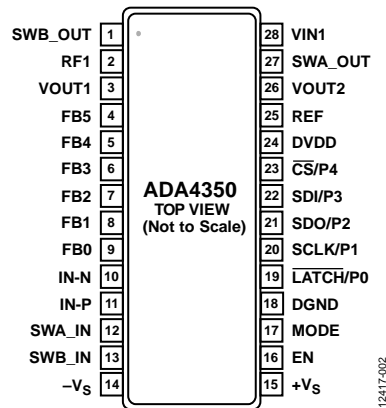


Figure 5. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SWB_OUT	Switch Group B (S3 to S5 and S9 to S11) Output.
2	RF1	Feedback Resistor for Output Differential Amplifier.
3	VOUT1	Differential Amplifier Output 1.
4	FB5	Feedback Pin 5 for FET Input Amplifier.
5	FB4	Feedback Pin 4 for FET Input Amplifier.
6	FB3	Feedback Pin 3 for FET Input Amplifier.
7	FB2	Feedback Pin 2 for FET Input Amplifier.
8	FB1	Feedback Pin 1 for FET Input Amplifier.
9	FB0	Feedback Pin 0 for FET Input Amplifier.
10	IN-N	FET Input Amplifier Inverting Input.
11	IN-P	FET Input Amplifier Noninverting Input.
12	SWA_IN	Switch Group A (S0 to S2 and S6 to S8) Input.
13	SWB_IN	Switch Group B (S3 to S5 and S9 to S11) Input.
14	-Vs	Analog Negative Supply.
15	+Vs	Analog Positive Supply.
16	EN	Enable Pin.
17	MODE	Mode Pin. Use this pin to switch between the SPI interface and the parallel interface.
18	DGND	Digital Ground.
19	LATCH/P0	Latch Bit in the Serial Mode ( $\overline{\text{LATCH}}$ ). Parallel Data Bit 0 in parallel mode (P0).
20	SCLK/P1	Digital Clock in Serial Mode (SCLK). Parallel Data Bit 1 in parallel mode (P1).
21	SDO/P2	Serial Data Out in Serial Mode (SDO). Parallel Data Bit 2 in parallel mode (P2).
22	SDI/P3	Serial Data In in Serial Mode (SDI). Parallel Data Bit 3 in parallel mode (P3).
23	$\overline{\text{CS}}$ /P4	Select Bit in Serial Mode ( $\overline{\text{CS}}$ ). Parallel Data Bit 4 in parallel mode (P4).
24	DVDD	Digital Positive Supply.
25	REF	Reference for the ADC Driver at M1.
26	VOUT2	Differential Amplifier Output 2.
27	SWA_OUT	Switch Group A (S0 to S2 and S6 to S8) Output.
28	VIN1	Differential Amplifier Noninverting Input.



## TYPICAL PERFORMANCE CHARACTERISTICS

### FULL SYSTEM

These plots are for the full system, which includes the FET input amplifier, the switching network, and the ADC driver. Unless otherwise stated,  $R_L = 1\text{ k}\Omega$  differential. For  $V_S = \pm 5\text{ V}$ ,  $DVDD = +5\text{ V}$ , and for  $V_S = +5\text{ V}$  (or  $\pm 2.5\text{ V}$ ),  $DVDD = +3.3\text{ V}$ .

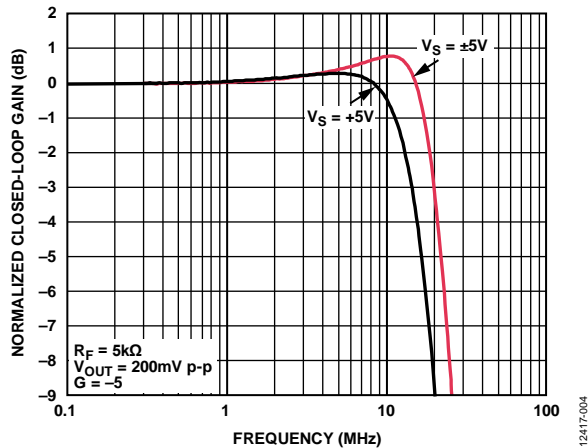


Figure 6. Small Signal Frequency Response for Various Supplies, See Test Circuit in Figure 49

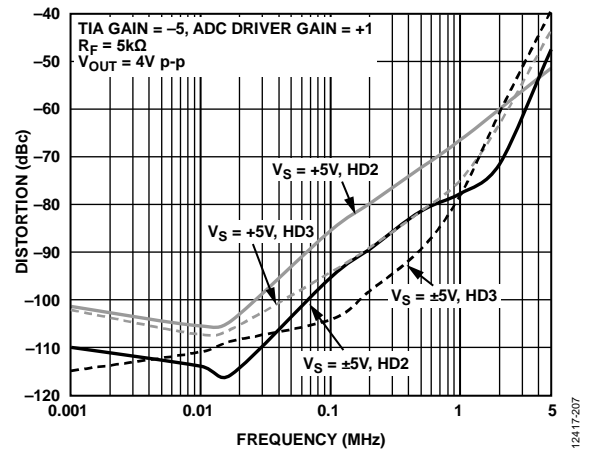


Figure 9. Harmonic Distortion vs. Frequency for Various Supplies, See Test Circuit in Figure 48

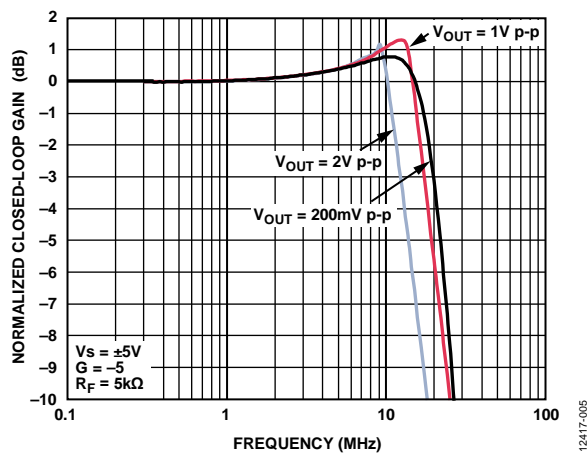


Figure 7. Frequency Response for Various Voltage Outputs, See Test Circuit in Figure 49

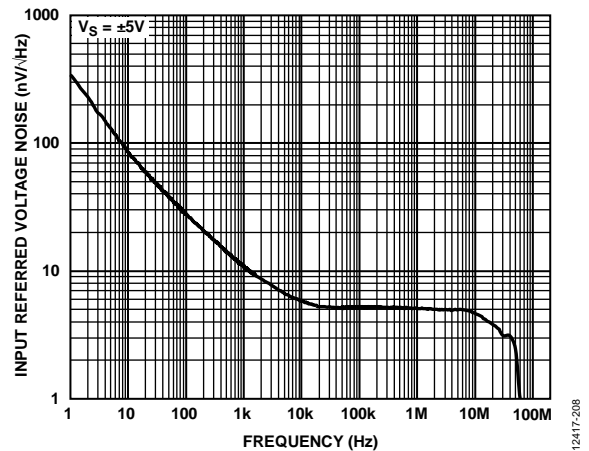


Figure 10. Input Referred Voltage Noise vs. Frequency

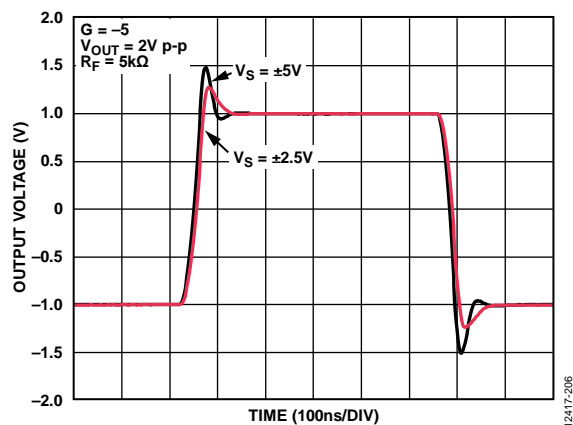


Figure 8. Large Signal Step Response,  $G = -5$  for Various Supplies

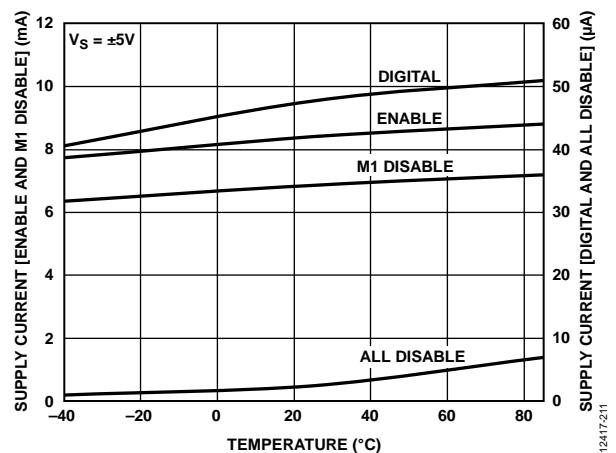


Figure 11. Supply Current vs. Temperature at Different Modes

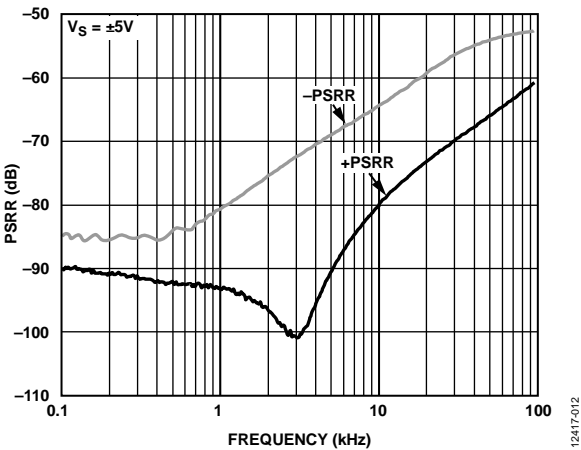


Figure 12. PSRR vs. Frequency

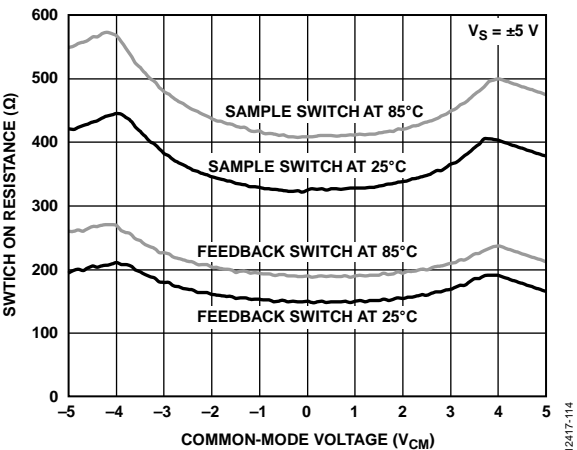


Figure 14. Switch On-Resistance vs. Common-Mode Voltage at Switches for Various Temperature

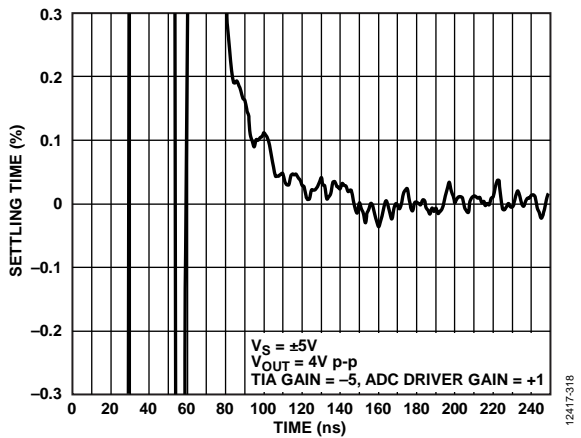


Figure 13. 0.1% Settling Time, See Test Circuit in Figure 49

## FET INPUT AMPLIFIER

Unless otherwise stated,  $R_L = 1\text{ k}\Omega$ . For  $V_S = \pm 5\text{ V}$ ,  $DVDD = +5\text{ V}$ , and for  $V_S = \pm 2.5\text{ V}$ ,  $DVDD = +3.3\text{ V}$ .

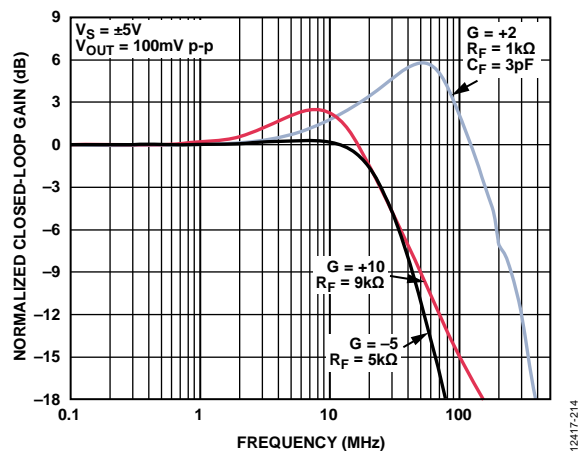


Figure 15. Small Signal Frequency Response for Various Gains,  $V_S = \pm 5\text{ V}$ , See Test Circuit Diagrams in Figure 50 and Figure 51

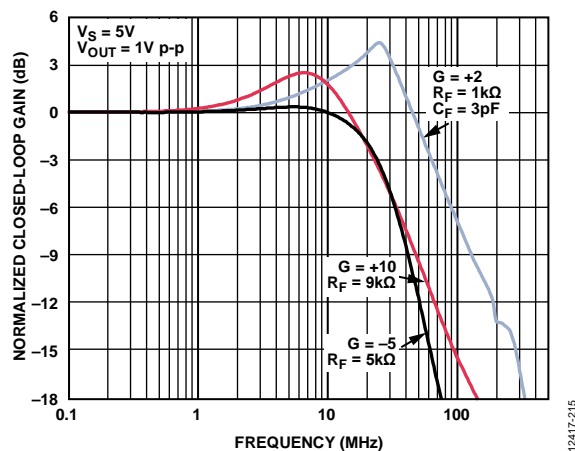


Figure 18. Large Signal Frequency Response for Various Gains,  $V_S = 5\text{ V}$ , See Test Circuit Diagrams in Figure 50 and Figure 51

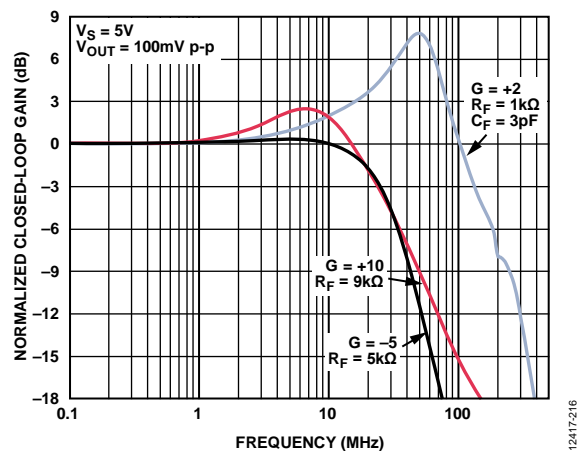


Figure 16. Small Signal Frequency Response for Various Gains,  $V_S = 5\text{ V}$ , See Test Circuit Diagrams in Figure 50 and Figure 51

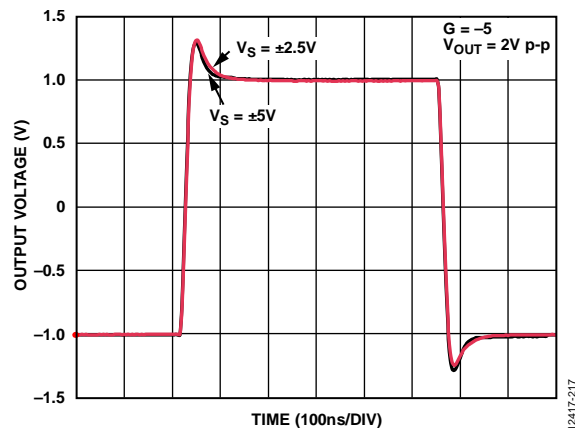


Figure 19. Large Signal Step Response for Various Supplies,  $G = -5$

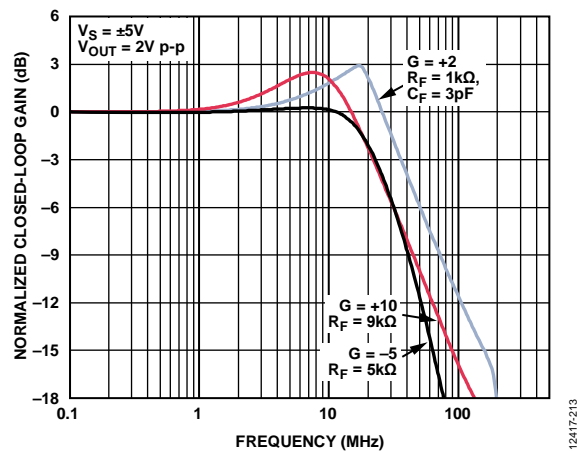


Figure 17. Large Signal Frequency Response for Various Gains,  $V_S = \pm 5\text{ V}$ , See Test Circuit Diagrams in Figure 50 and Figure 51

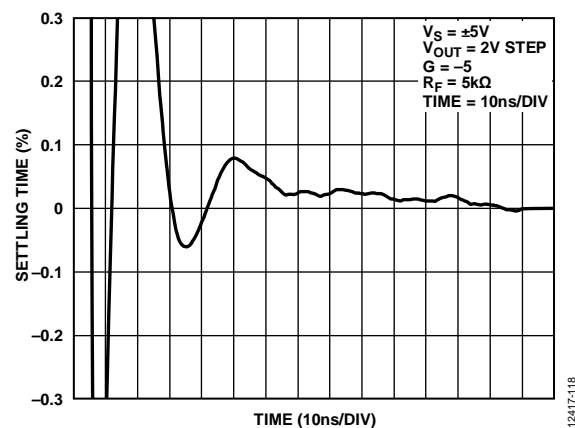


Figure 20. 0.1% Settling Time

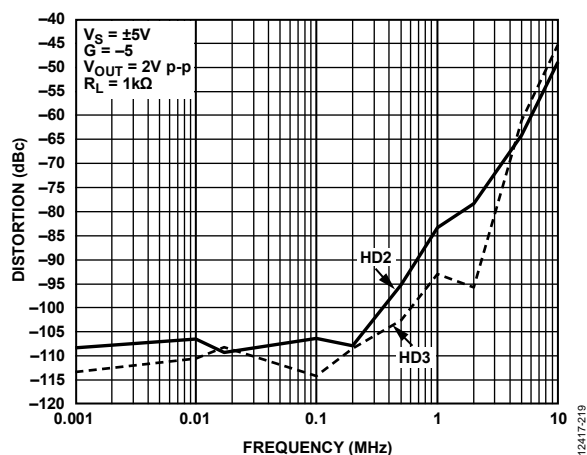


Figure 21. Distortion (HD2/HD3) vs. Frequency,  $G = -5$

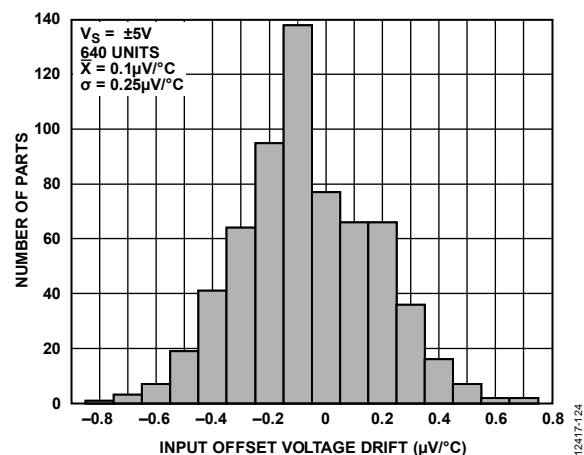


Figure 24. Input Offset Voltage Drift

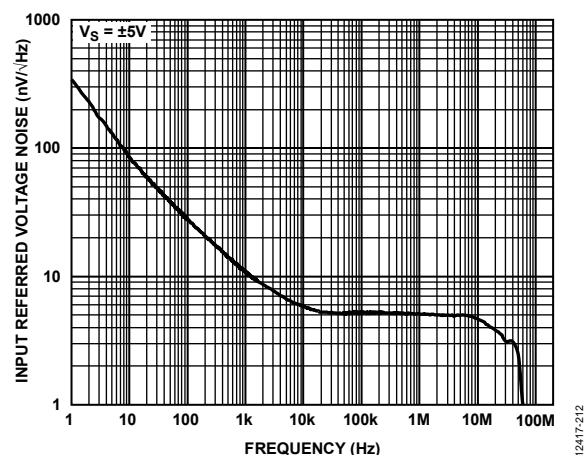


Figure 22. Input Voltage Noise

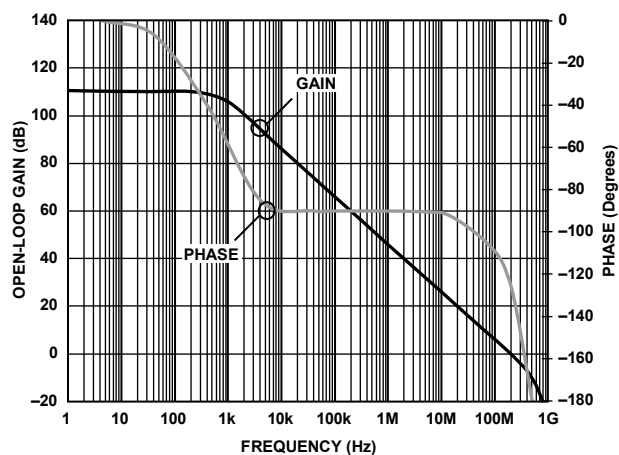


Figure 25. Open-Loop Gain and Phase vs. Frequency

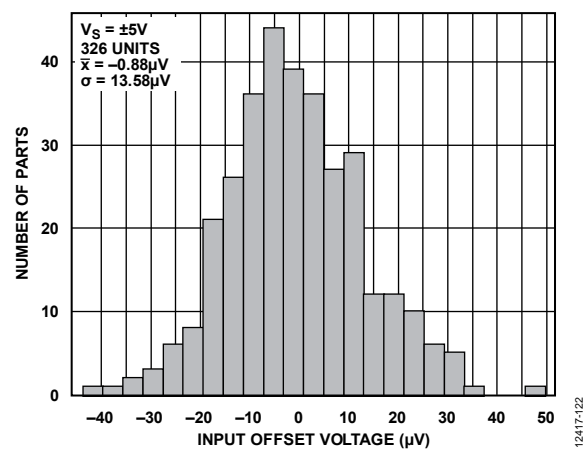


Figure 23. Input Offset Voltage

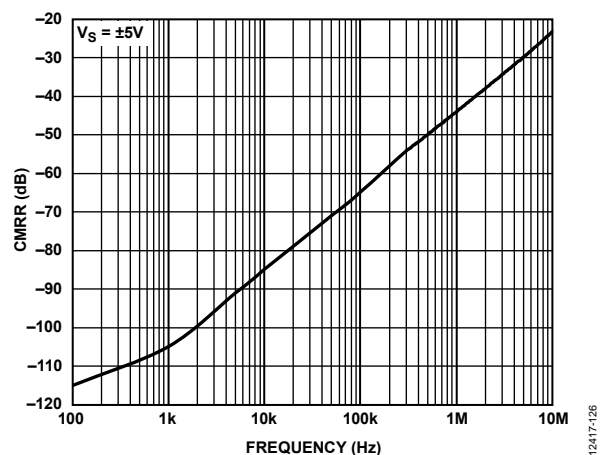


Figure 26. CMRR vs Frequency

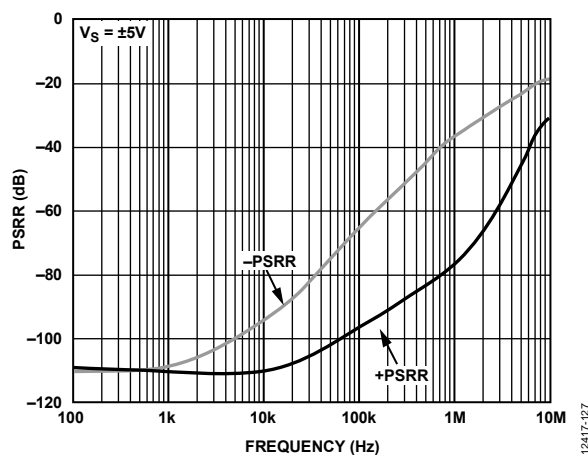


Figure 27. PSRR vs Frequency

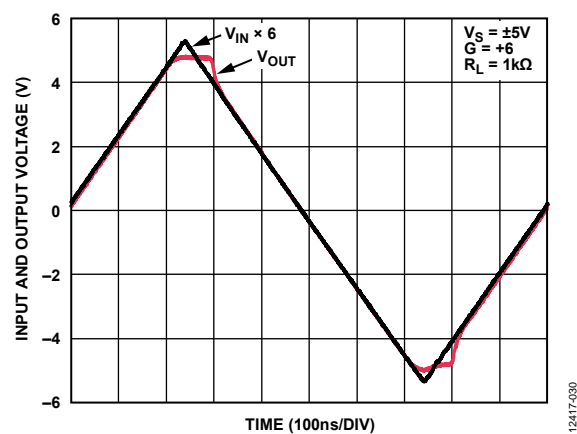


Figure 28. Output Overdrive Recovery when Used as an Amplifier

## ADC DRIVER

Unless stated otherwise,  $R_L = 1\text{ k}\Omega$  differential, and  $R_L = 500\ \Omega$  when single-ended. For  $V_S = \pm 5\text{ V}$ ,  $DVDD = +5\text{ V}$ , and for  $V_S = +5\text{ V}$  (or  $\pm 2.5\text{ V}$ ),  $DVDD = +3.3\text{ V}$ .

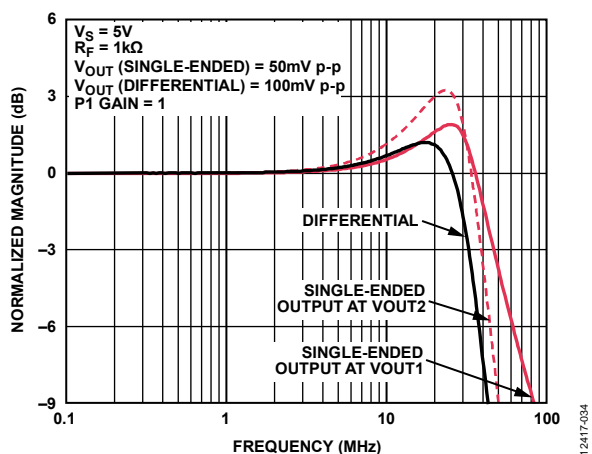


Figure 29. Small Signal Frequency Response,  $V_S = 5\text{ V}$

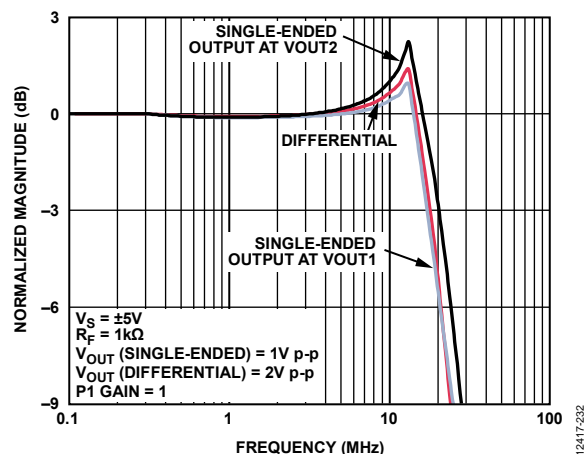


Figure 32. Large Signal Frequency Response,  $V_S = \pm 5\text{ V}$

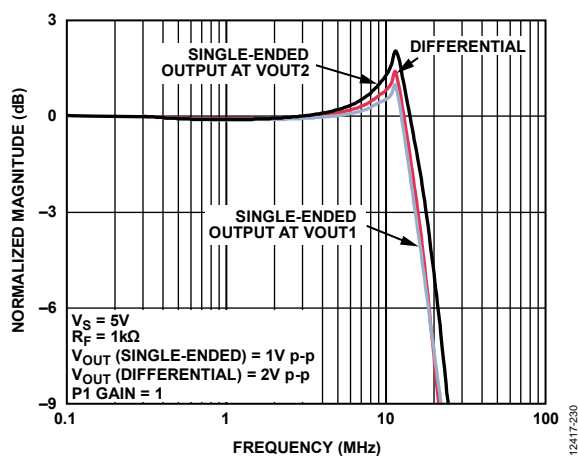


Figure 30. Large Signal Frequency Response,  $V_S = 5\text{ V}$

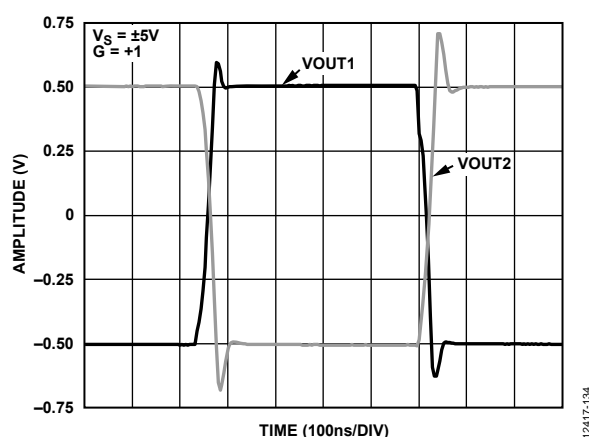


Figure 33. Large Signal Step Response (Single-Ended Output),  $V_S = \pm 5\text{ V}$

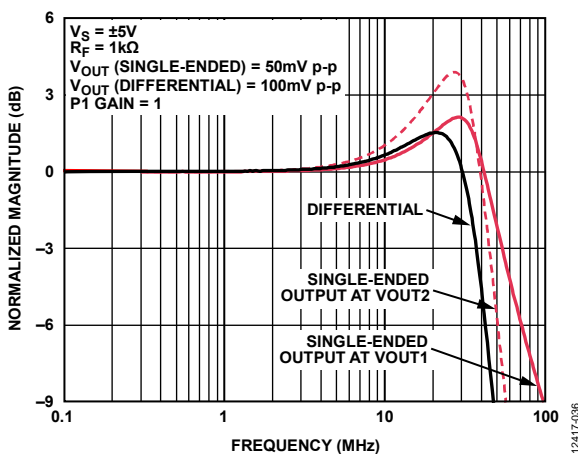


Figure 31. Small Signal Frequency Response,  $V_S = \pm 5\text{ V}$

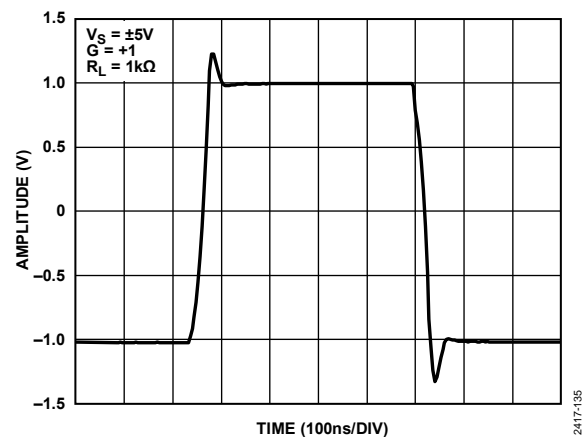


Figure 34. Large Signal Step Response (Differential Output),  $V_S = \pm 5\text{ V}$

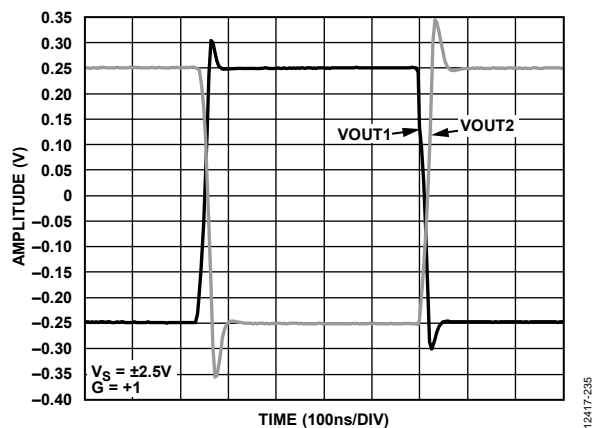
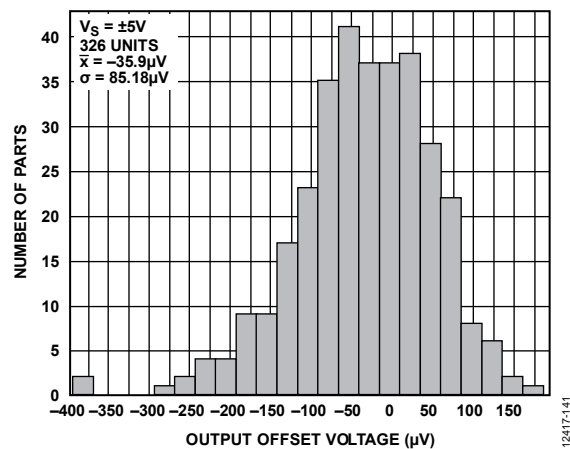
Figure 35. Large Signal Step Response (Single-Ended Output),  $V_S = \pm 2.5\text{ V}$ 

Figure 38. Differential Output Offset Voltage

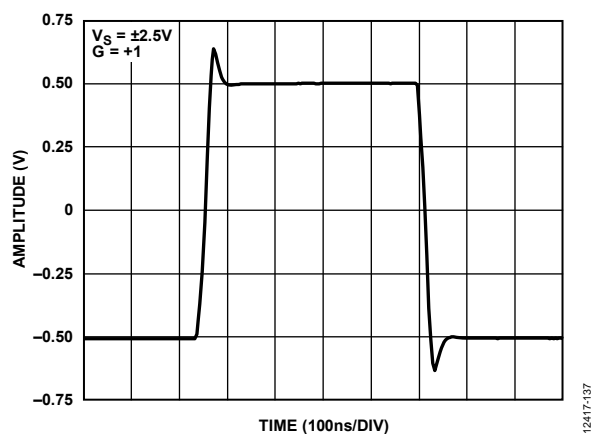
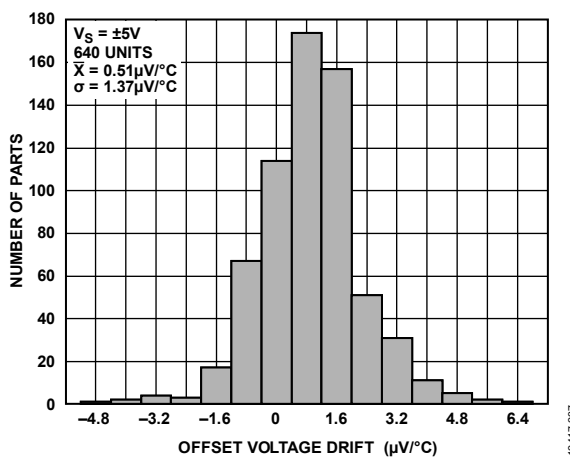
Figure 36. Large Signal Step Response (Differential Output),  $V_S = \pm 2.5\text{ V}$ 

Figure 39. Differential Output Offset Voltage Drift

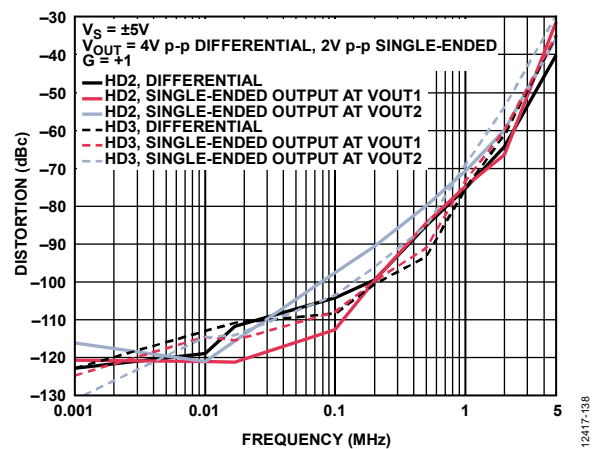


Figure 37. Harmonic Distortion vs. Frequency

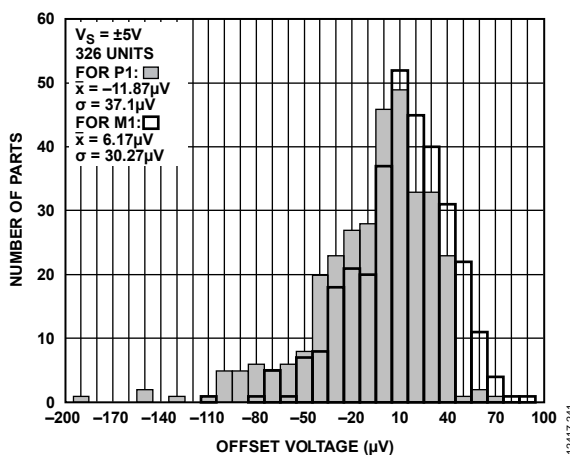
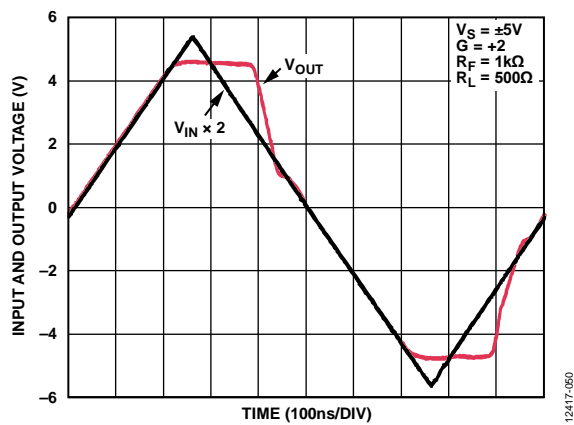
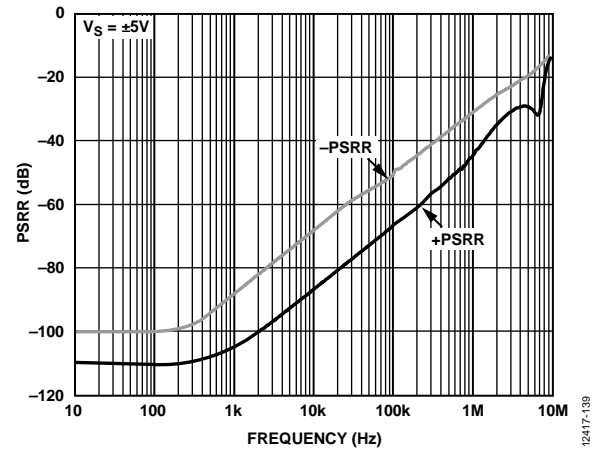
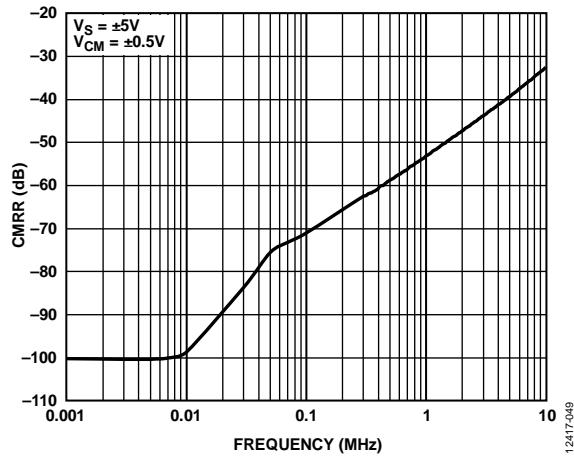
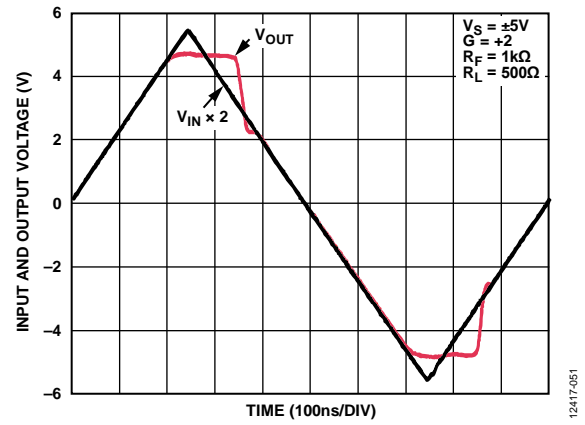
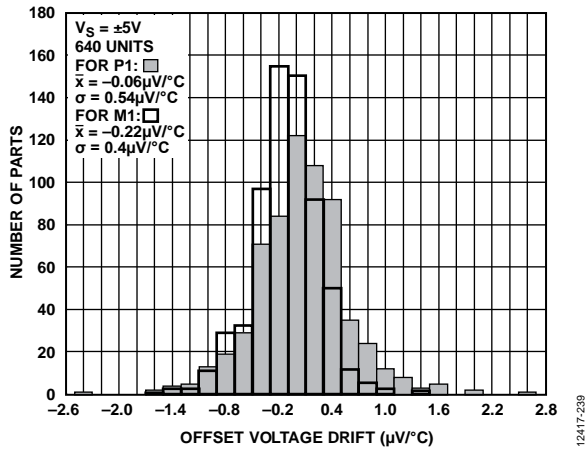


Figure 40. Single-Ended Output Offset Voltage





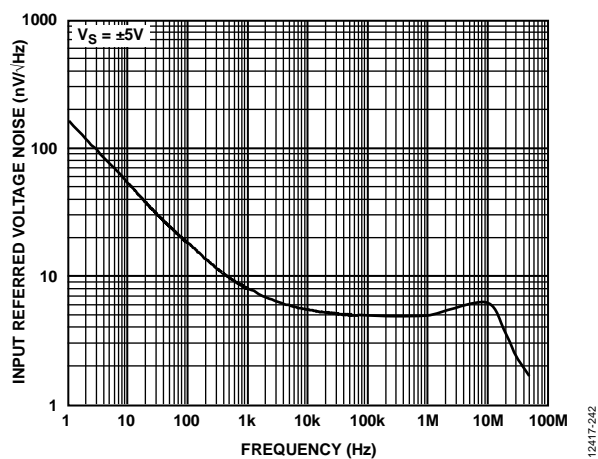


Figure 46. Input Referred Voltage Noise vs. Frequency, P1 Only,  
See Test Circuit Diagram in Figure 52

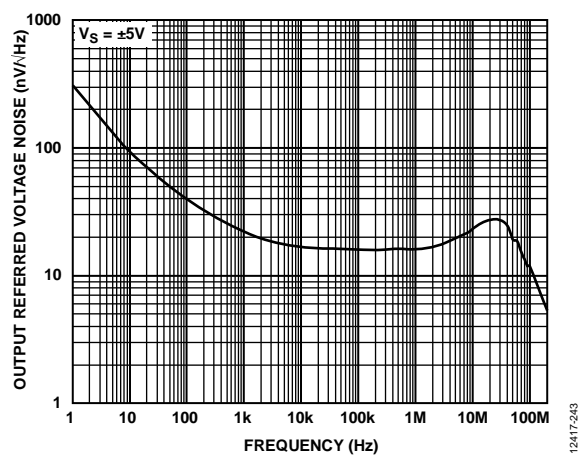


Figure 47. Output Referred Voltage Noise vs. Frequency, P1 and M1,  
See Test Circuit Diagram in Figure 53

# TEST CIRCUITS

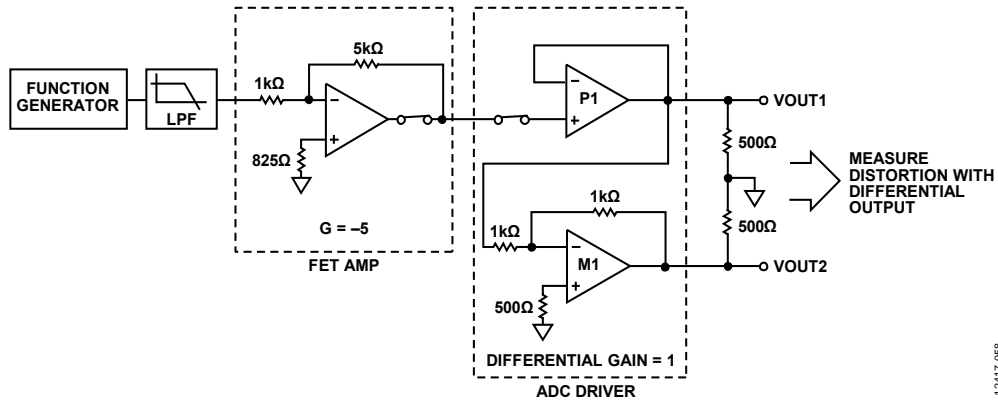


Figure 48. Harmonic Distortion for Full System

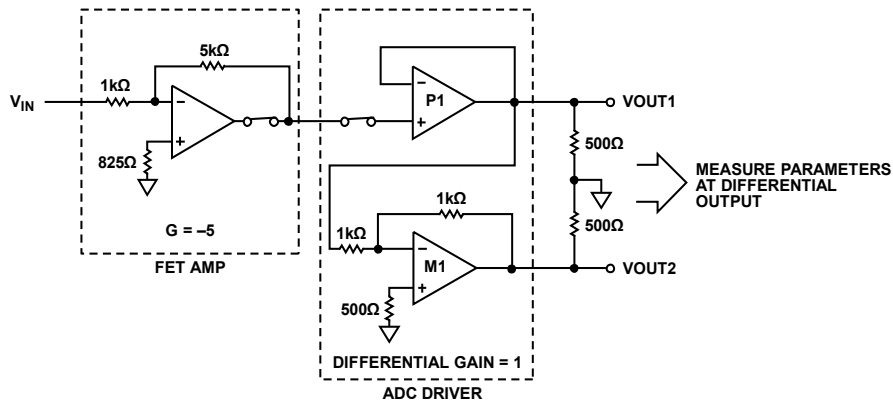


Figure 49. Full System Measurement for Other Parameters

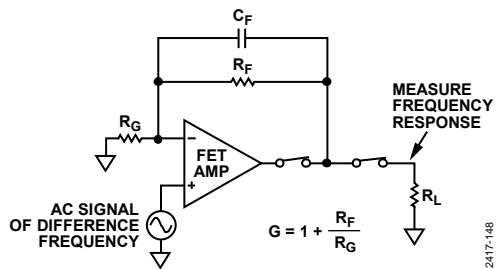


Figure 50. Frequency Response for FET Input Amplifier, Noninverting Gain Configuration

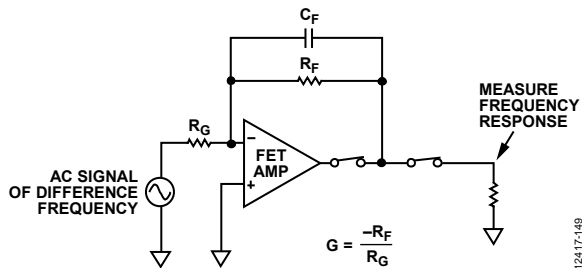


Figure 51. Frequency Response for FET Input Amplifier, Inverting Gain Configuration

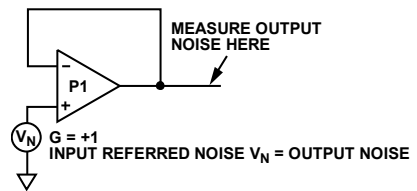


Figure 52. Input Referred Voltage Noise for P1

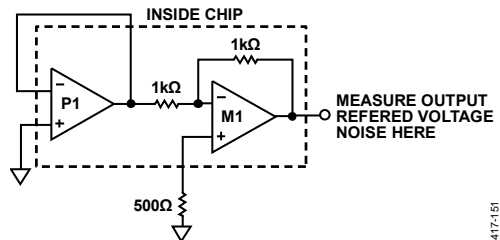
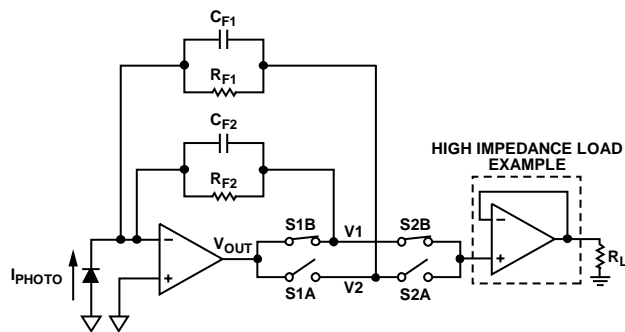


Figure 53. Output Referred Voltage Noise for P1 and M1

## THEORY OF OPERATION

### KELVIN SWITCHING TECHNIQUES

Traditional gain selectable amplifiers use analog switches in a feedback loop to connect discrete external resistors and capacitors to the inverting input by selecting the appropriate feedback path. This approach introduces several errors due to the nonideal nature of the analog switches in the loop. For example, the on-resistance of the analog switch causes voltage and temperature dependent gain errors, while the leakage current causes offset errors, especially at high temperature. The Kelvin switching technique solves this problem by introducing two switches in each gain selection loop, one to connect the transimpedance/op amp output to the feedback network, and the other to connect the feedback network output to the downstream components. Figure 54 shows a programmable gain transimpedance amplifier with Kelvin switching.



#### NOTES

1. S1A, S1B, S2A, AND S2B ARE THE ANALOG SWITCHES.  
R<sub>Fx</sub> ARE THE FEEDBACK RESISTORS SPECIFIC TO EACH TRANSIMPEDANCE PATH. C<sub>Fx</sub> ARE THE FEEDBACK CAPACITORS SPECIFIC TO EACH TRANSIMPEDANCE PATH.

12417-103

Figure 54. Programmable Gain Transimpedance Amplifier with Kelvin Switching

Although this technique requires using twice as many switches, the voltage (V<sub>x</sub>) in the center node is no longer switch dependent; it is only dependent on the current across the selected resistor (see Equation 1 through Equation 3).

$$V_{OUT} = -I_{PHOTO} \times (R_{F2} + R_{S1B}) \quad (1)$$

$$V1 = V_{OUT} \times (R_{F2} / (R_{F2} + R_{S1B})) \quad (2)$$

Substituting Equation 1 into Equation 2,

$$V1 = -I_{PHOTO} \times R_{F2} \quad (3)$$

where:

V<sub>OUT</sub> is the output of the first amplifier.

I<sub>PHOTO</sub> is the current from the photodiode.

R<sub>F2</sub> is the feedback resistor of Transimpedance Path 2.

R<sub>S1B</sub> is the switch resistance of the S1B switch.

The switches shown on the right (S2A and S2B) in Figure 54 only have a small output impedance and contribute negligible error if the amplifier drives a high impedance load. In the case of the [ADA4350](#), the high impedance load is the integrated ADC driver.

APPLICATIONS INFORMATION

CONFIGURING THE ADA4350

See the [EVAL-ADA4350RUZ-P](#) user guide for details on the basic configuration of the [ADA4350](#), and how to use the evaluation board. For more details on configuring the ADC driver in a different gain setting, see the [ADA4941-1](#) data sheet.

The gain settings of the [ADA4350](#) can be chosen via the SPI interface or manually through a 5-lead DIP switch.

SELECTING THE TRANSIMPEDANCE GAIN PATHS MANUALLY OR THROUGH THE PARALLEL INTERFACE

In the manual mode (or parallel mode), only five out of the six transimpedance paths can be accessed (FB0 to FB4). Figure 55 shows the simplified schematics of the [ADA4350](#) and the positions of FB0 to FB4. In this example, the first two feedback paths (FB0 and FB1) are configured as two different transimpedance gain paths.

To operate in manual mode or in parallel mode, set the EN pin (Pin 16) and the MODE pin (Pin 17) to Logic 1. In this mode, Pin 19 to Pin 23 represent P0 through P4, respectively. To select one gain, set the corresponding Px pin to Logic 1, and set all other Px pins to Logic 0. Table 13 shows the relationship between the gain select switches (P0 through P4) and the gain path selected.

Setting more than one Px pin to Logic 1 results in connecting the selected gain paths in parallel.

Table 13. Manual Mode or Parallel Mode Operation

Bit On	Switch Closed	Gain Path Selected
P0	S0 and S6	FB0
P1	S1 and S7	FB1
P2	S2 and S8	FB2
P3	S3 and S9	FB3
P4	S4 and S10	FB4

SELECTING THE TRANSIMPEDANCE GAIN PATHS THROUGH THE SPI INTERFACE (SERIAL MODE)

For serial mode operation, set the EN pin (Pin 16) to Logic 1 and the MODE pin (Pin 17) to Logic 0. In serial mode, Pin 19 is  $\overline{\text{LATCH}}$ , Pin 20 is SCLK, Pin 21 is SDO, Pin 22 is SDI, and Pin 23 is  $\overline{\text{CS}}$ . Serial mode operation uses a 24-bit command to configure each individual switch, S0 through S11, as well as additional options. Table 14 shows the 24-bit map used in serial mode operation. Table 15 shows the example codes that select the various transimpedance gain paths.

Multifunction pin names may be referenced by their relevant function only.

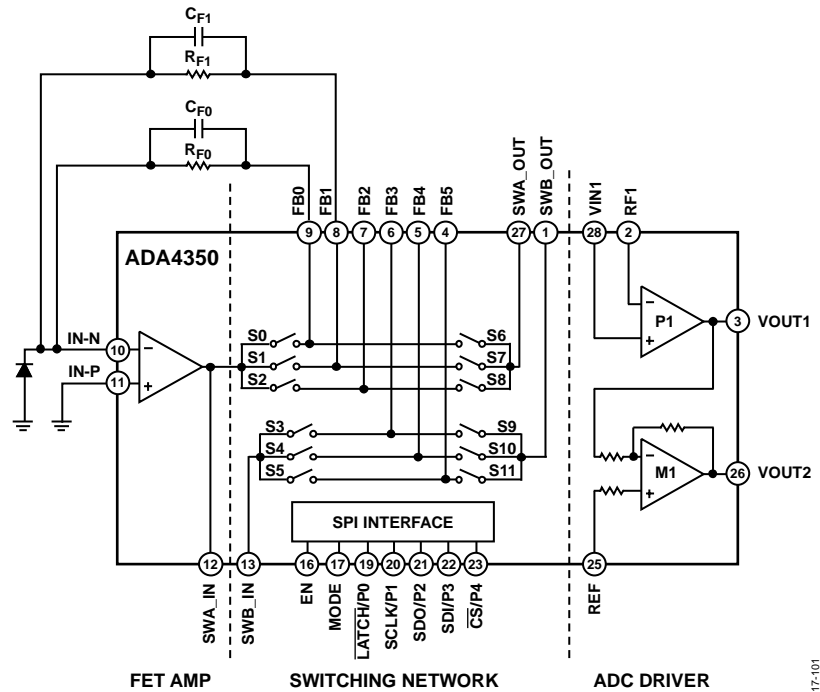


Figure 55. Simplified Schematic

Table 14. 24-Bit Map Used in Serial Mode Operation

Bit No.	Function	Default Setting
0	S0 on/off control. Write 1 to this bit to close Switch S0.	0
1	S1 on/off control. Write 1 to this bit to close Switch S1.	0
2	S2 on/off control. Write 1 to this bit to close Switch S2.	0
3	S3 on/off control. Write 1 to this bit to close Switch S3.	0
4	S4 on/off control. Write 1 to this bit to close Switch S4.	0
5	S5 on/off control. Write 1 to this bit to close Switch S5.	0
6	S6 on/off control. Write 1 to this bit to close Switch S6.	0
7	S7 on/off control. Write 1 to this bit to close Switch S7.	0
8	S8 on/off control. Write 1 to this bit to close Switch S8.	0
9	S9 on/off control. Write 1 to this bit to close Switch S9.	0
10	S10 on/off control. Write 1 to this bit to close Switch S10.	0
11	S11 on/off control. Write 1 to this bit to close Switch S11.	0
12	Reserved. Set to logic low.	0
13 <sup>1</sup>	Optional internal 1 pF feedback capacitor between the inverting input and the output of the amplifier. Write 1 to this bit to turn the capacitor on.	0
14	Disable the SDO pin. Write 1 to this bit to disable the SDO pin.	0
15	Disable the M1 amplifier. Write 1 to this bit to disable the M1 amplifier.	0
16	Reserved. Set to logic low.	0
17	Reserved. Set to logic low.	0
18	Reserved. Set to logic low.	0
19	Reserved. Set to logic low.	0
20	Reserved. Set to logic low.	0
21	Reserved. Set to logic low.	0
22	Reserved. Set to logic low.	0
23	Read/write bit. Set to 1 to read and set to 0 to write.	0

<sup>1</sup> The optional internal 1 pF feedback capacitor provides a quick and convenient way to compensate the TIA when using a high value feedback resistor (>1 MΩ).

Table 15. Serial Mode Operation

Command (Hex Code Format, B23...B0)	Switch Closed	Gain Path Selected
00 00 41 (MSB Side)	S0 and S6	FB0
00 20 41	S0 and S6	FB0, optional internal feedback capacitor on
00 00 82	S1 and S7	FB1
00 01 04	S2 and S8	FB2
00 02 08	S3 and S9	FB3
00 04 10	S4 and S10	FB4
00 08 20	S5 and S11	FB5

**SPICE MODEL**

The SPICE model only supports parallel mode operation.

Pin P5 enables parallel mode and allows full switching network functionality.

The EN and MODE inputs are internally set to high and low, respectively, and are not accessible in this model. Figure 56 shows the recommended symbol pins when creating the [ADA4350](#) symbol in the SPICE simulator.

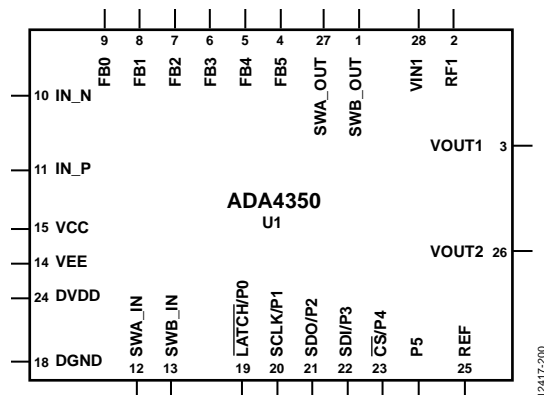


Figure 56. Recommended Symbol Layout

Table 16. Model Pin Descriptions

Symbol Pin	Model Node	Pin No.	Mnemonic
1	N10	10	IN_N
2	N11	11	IN_P
3	VCC	15	VCC
4	VEE	14	VEE
5	VDD	24	DVDD
6	DGND	18	DGND
7	N12	12	SWA_IN
8	N13	13	SWB_IN
9	PO	19	LATCH/P0
10	P1	20	SCLK/P1
11	P2	21	SDO/P2
12	P3	22	SDI/P3
13	P4	23	CS/P4
14	P5	Not applicable	P5
15	N25	25	REF
16	N26	26	VOUT2
17	N3	3	VOUT1
18	N2	2	RF1
19	N28	28	VIN1
20	27	27	SWA_OUT
21	1	1	SWB_OUT
22	4	4	FB5
23	5	5	FB4
24	6	6	FB3
25	7	7	FB2
26	8	8	FB1
27	9	9	FB0

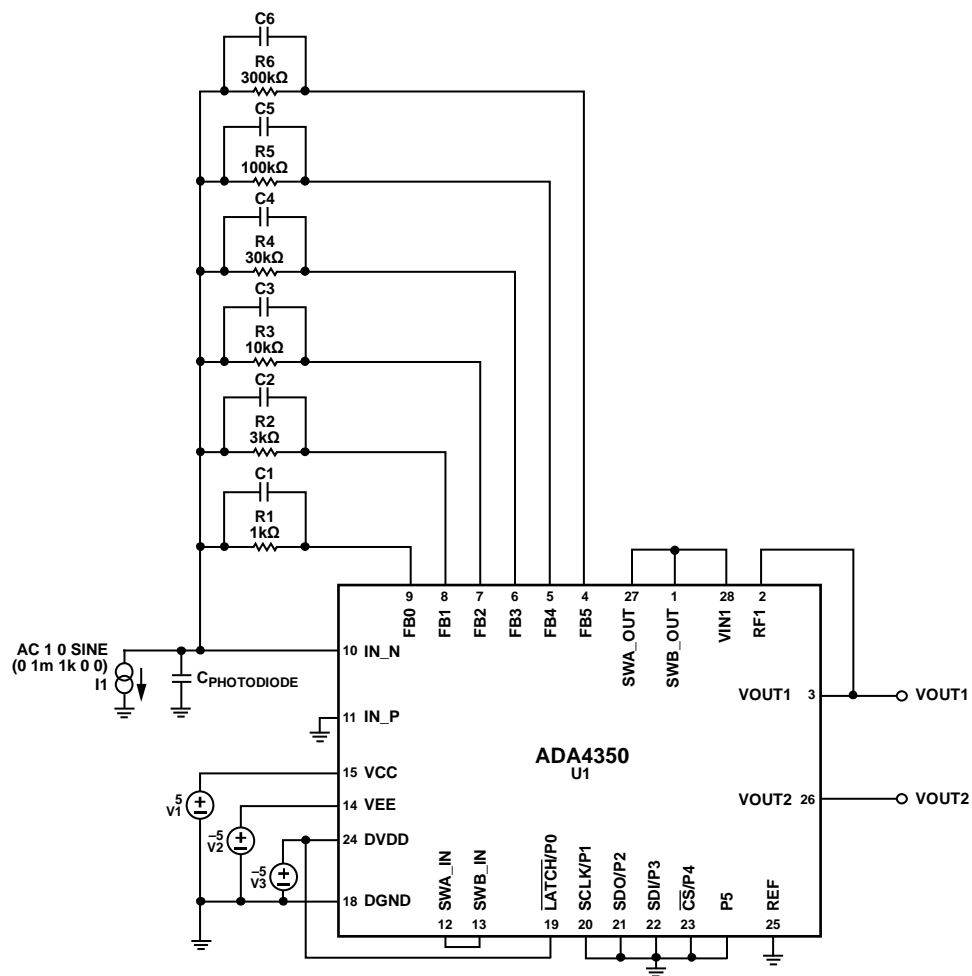


Figure 57. SPICE Schematic Example to Test Basic Functionality

## TRANSIMPEDANCE AMPLIFIER DESIGN THEORY

Because its low input bias current minimizes the dc error at the preamp output, the ADA4350 works well in photodiode preamp applications. In addition, its high gain bandwidth product and low input capacitance maximizes the signal bandwidth of the photodiode preamp. Figure 58 shows the transimpedance amplifier model of the ADA4350.

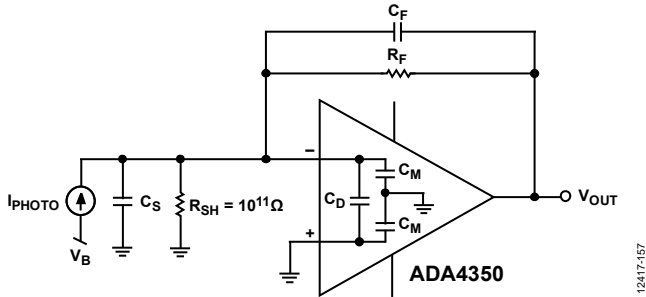


Figure 58. Transimpedance Amplifier Model of the ADA4350

The basic transfer function in Equation 4 describes the transimpedance gain of the photodiode preamp.

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F} \quad (4)$$

where:

$I_{PHOTO}$  is the output current of the photodiode.

$R_F$  is the feedback resistor.

$C_F$  is the feedback capacitance.

The signal bandwidth is  $1/(R_F \times C_F)$ , as determined by Equation 4. In general, set  $R_F$  such that the maximum attainable output voltage corresponds to the maximum diode current,  $I_{PHOTO}$ , allowing the use of the full output swing.

The signal bandwidth attainable with this preamp is a function of  $R_F$ , the gain bandwidth product ( $f_{GBW}$ ) of the amplifier, and the total capacitance at the amplifier summing junction, including  $C_S$  and the amplifier input capacitance of  $C_D$  and  $C_M$ .  $R_F$  and the total capacitance produce a pole with the loop frequency ( $f_P$ ).

$$f_P = 1/2\pi R_F C_S \quad (5)$$

With the additional pole from the open-loop response of the amplifier, the two-pole system results in peaking and instability due to an insufficient phase margin (see gray lines for the noise gain and phase in Figure 59).

Adding  $C_F$  to the feedback loop creates a zero in the loop transmission that compensates for the effect of the input pole, which stabilizes the photodiode preamp design because of the increased phase margin (see the gray lines for the noise gain and phase in Figure 60). It also sets the signal bandwidth,  $f_z$  (see the I to V gain line for the signal gain in Figure 60). The signal bandwidth and the zero frequency,  $f_z$ , are determined by

$$f_z = \frac{1}{2\pi R_F C_F} \quad (6)$$

Equating the zero frequency,  $f_z$ , with the  $f_x$  frequency maximizes the signal bandwidth with a 45° phase margin. Calculate  $f_x$  as follows because  $f_x$  is the geometric mean of  $f_P$  and  $f_{GBW}$ :

$$f_x = \sqrt{f_P \times f_{GBW}} \quad (7)$$

By combining Equation 5, Equation 6, and Equation 7, the  $C_F$  value that produces  $f_x$  is defined by

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times f_{GBW}}} \quad (8)$$

The frequency response in this case shows approximately 2 dB peaking and 15% overshoot. Doubling  $C_F$  and cutting the bandwidth in half results in a flat frequency response with approximately 5% transient overshoot.

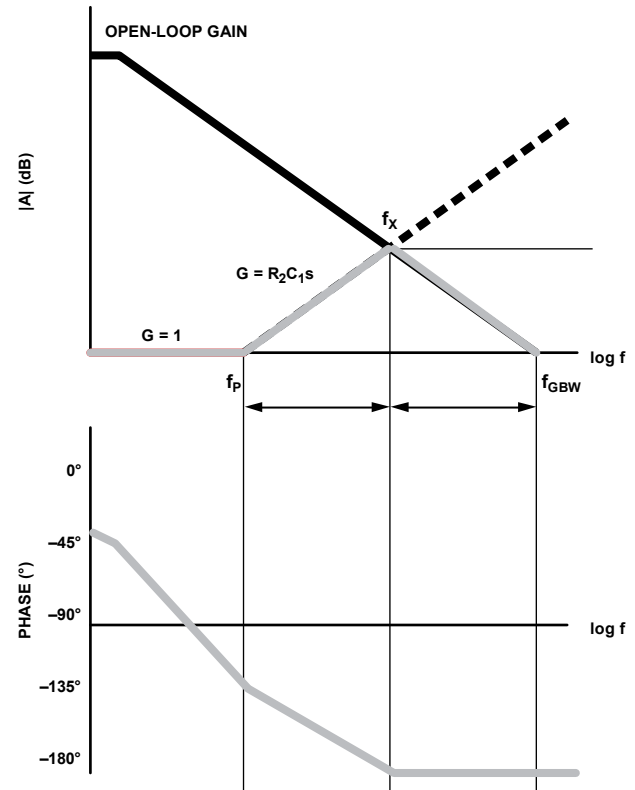


Figure 59. Noise Gain and Phase Bode Plot of the Transimpedance Amplifier Design Without Compensation



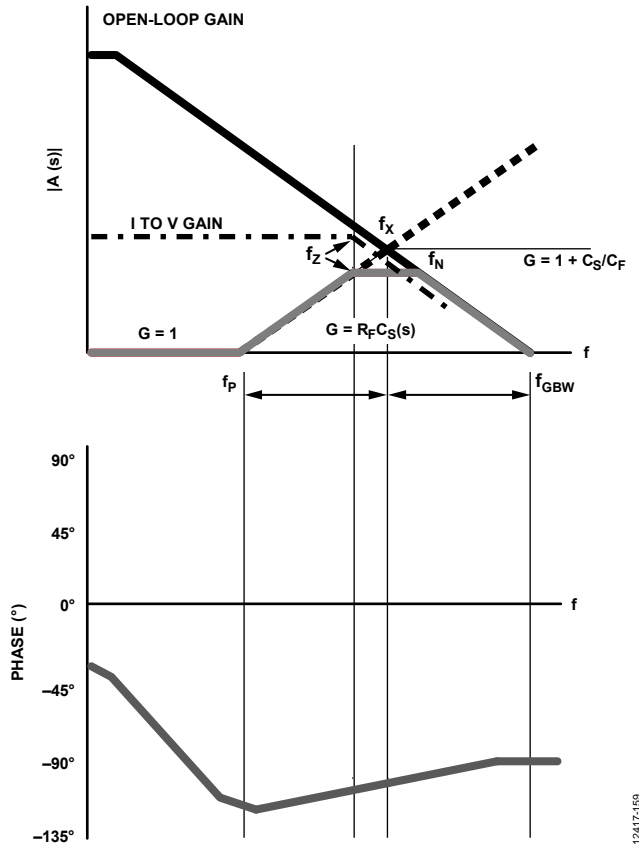


Figure 60. Signal and Noise Gain and Phase of the Transimpedance Amplifier Design with Compensation

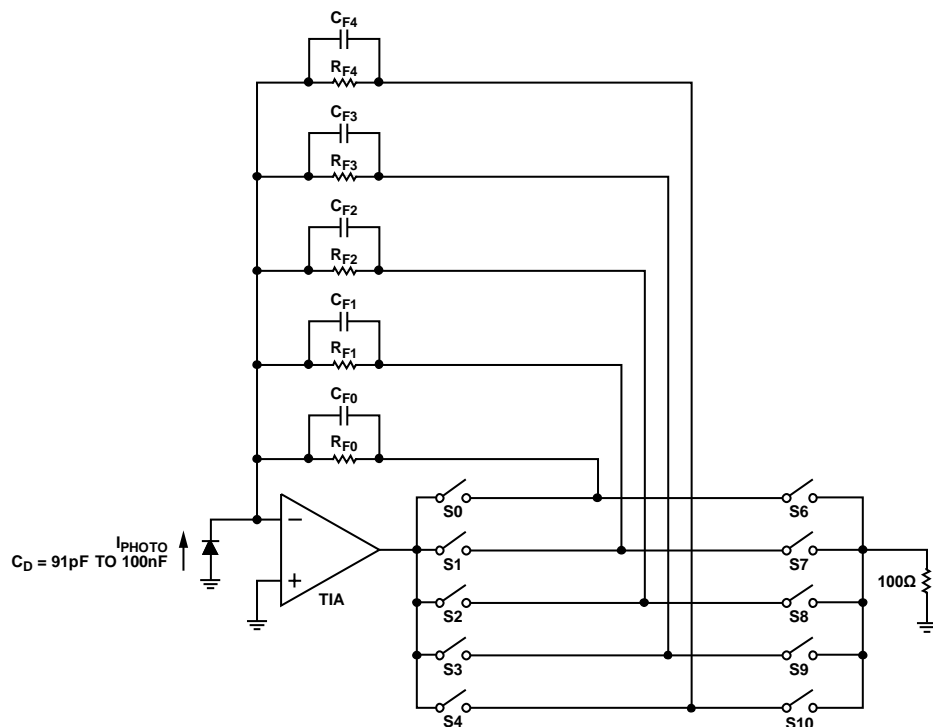
The dominant output noise sources in the transimpedance amplifier design are the input voltage noise of the amplifier,  $V_{\text{NOISE}}$ , and the resistor noise due to  $R_F$ . The effect due to the current noise is negligible in comparison. The gray line in Figure 60 shows the noise gain and phase over frequencies for the transimpedance amplifier. The noise bandwidth is at the  $f_N$  frequency, and is calculated by

$$f_N = \frac{f_{\text{GBW}}}{(C_S + C_F)/C_F} \quad (9)$$

Table 17 shows the dominant noise sources ( $R_F$  and  $V_{\text{NOISE}}$ ) for the transimpedance amplifier when it has a 45° phase margin for the maximum bandwidth, and in this case,  $f_Z = f_X = f_N$ .

Table 17. RMS Noise Contributions of Transimpedance Amplifier

Contributor	Expression
$R_F$	$\sqrt{4kT \times R_F \times f_N \times \frac{\pi}{2}}$
$V_{\text{NOISE}}$	$V_{\text{NOISE}} \times \frac{(C_S + C_M + C_F + 2C_D)}{C_F} \times \sqrt{\frac{\pi}{2} \times f_N}$



## NOTES

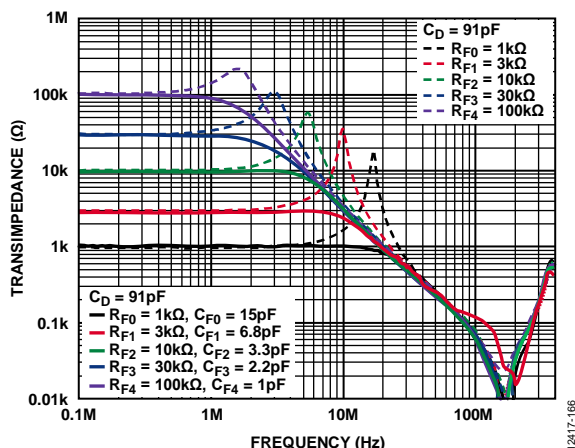
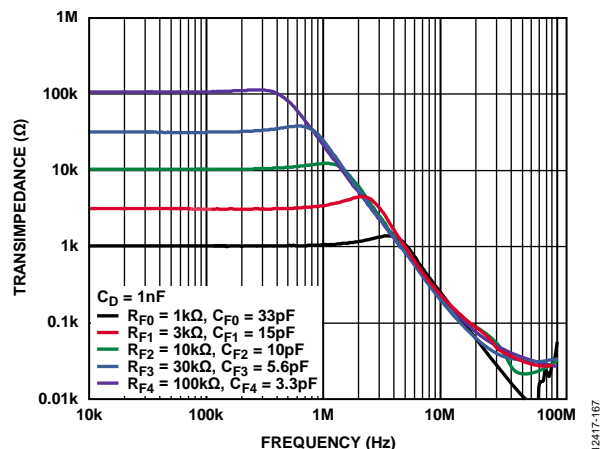
1.  $R_{Fx}$  ARE THE FEEDBACK RESISTORS SPECIFIC TO EACH TRANSIMPEDANCE PATH.  $C_{Fx}$  ARE THE FEEDBACK CAPACITORS SPECIFIC TO EACH TRANSIMPEDANCE PATH.

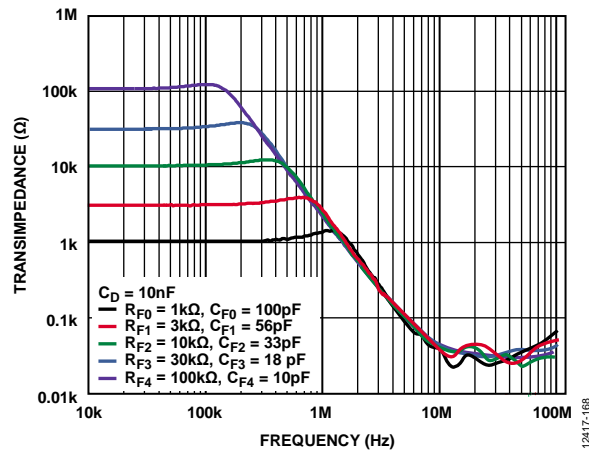
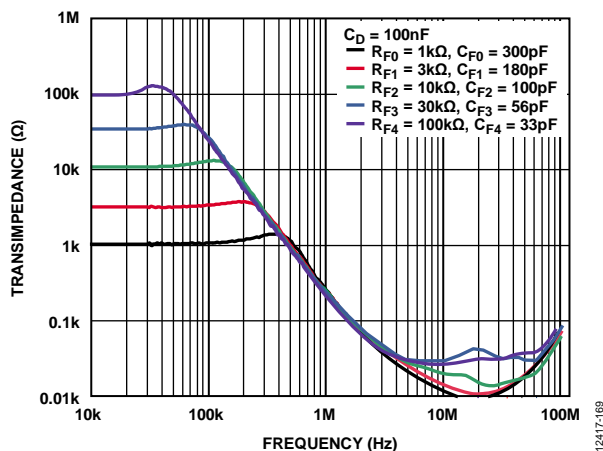
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Figure 61. ADA4350 Configured as a Transimpedance Amplifier with Five Different Gains

## TRANSIMPEDANCE GAIN AMPLIFIER PERFORMANCE

Figure 61 shows the ADA4350 configured as a transimpedance amplifier with five different gains. The photodiode sensor capacitance,  $C_D$ , varies from 91 pF to 100 nF to showcase the transimpedance gain performance at various frequency. Figure 62 to Figure 65 shows the transimpedance vs. frequency at different  $C_D$  settings. Note that the compensation capacitors,  $C_{F0}$  to  $C_{F4}$ , correct for the inherent instability of the transimpedance configuration. Capacitors chosen were such that the transimpedance gain response compensates for the maximum bandwidth and is close to having a 45° phase margin.

Figure 62. Transimpedance vs. Frequency,  $C_D = 91$  pFFigure 63. Transimpedance vs. Frequency,  $C_D = 1$  nF

Figure 64. Transimpedance vs. Frequency,  $C_D = 10$  nFFigure 65. Transimpedance vs. Frequency,  $C_D = 100$  nF

### THE EFFECT OF LOW FEEDBACK RESISTOR $R_{Fx}$

As the load of the transimpedance amplifier increases, excessive peaking in the frequency response can be observed when the  $R_{Fx}$  value is too small. This peaking can persist even when excessive  $C_{Fx}$  overcompensates for it. Figure 66 shows the ADA4350 configured with a photodiode capacitance value of 91 pF and a 1 kΩ transimpedance load. Figure 67 shows the normalized frequency response of this configuration. By decreasing  $R_F$  from 500 Ω to 68 Ω, the peaking in the frequency response increases progressively. The large peaking translates to a huge overshoot in the pulse response, which is an undesirable result.

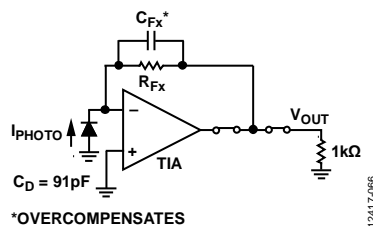
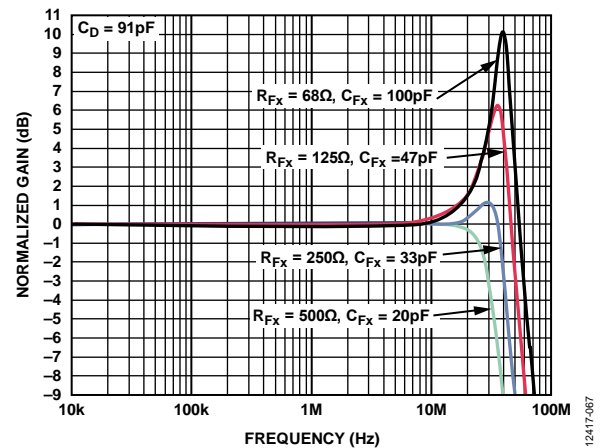


Figure 66. Transimpedance Amplifier Circuit

Figure 67. Normalized Frequency Response with Decreasing  $R_F$  (See Figure 66)

To mitigate this effect, use an additional snubber circuit at the output of the FET input amplifier, as shown in Figure 68. In this configuration, the feedback resistor ( $R_{Fx}$ ) is 68 Ω, and the capacitance of the photodiode is 40 pF.

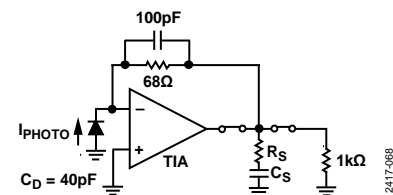


Figure 68. Snubber Circuit Added to Mitigate Peaking

Figure 69 shows the effect of various snubber circuits clamping down the peaking. Without the snubber circuit, there is 6 dB of peaking when an overcompensated  $C_{Fx}$  of 100 pF is used. With the snubber circuits, the bandwidth is restricted to approximately 10 MHz. To compromise between the peaking and the bandwidth, adjust the values of the snubber circuit.

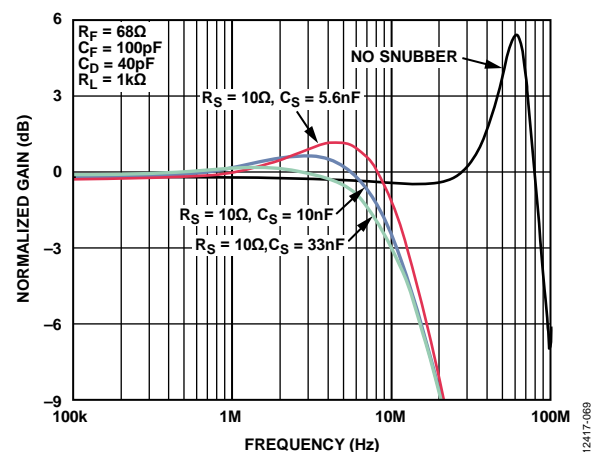


Figure 69. Effect of Snubber Circuits on the Transimpedance Frequency Response (See Figure 68)

## USING THE T NETWORK TO IMPLEMENT LARGE FEEDBACK RESISTOR VALUES

Large feedback resistors (>1 MΩ) can cause the two following issues in the transimpedance amplifier design:

- If the parasitic capacitance of the feedback resistor exceeds the optimal compensation value, it can significantly reduce the TIA signal bandwidth.
- If the required compensation capacitance is too low (<1 pF), it is not practical to choose a feedback capacitor.

The T network (the  $R_{Fx}$ ,  $R2$ , and  $R1$  resistors) maintains the transimpedance gain and signal bandwidth with a lower feedback resistor and a resistive gain network, as shown in Figure 70.

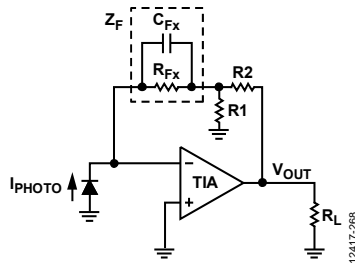


Figure 70. T Network

The relationship between the transimpedance  $V_{OUT}/I_{PHOTO}$  and the T network resistors ( $R_{Fx}$ ,  $R1$ , and  $R2$ ) can be expressed as

$$\frac{V_{OUT}}{I_{PHOTO}} = -Z_F \times \left( 1 + \frac{R2}{R1} + \frac{R2}{Z_F} \right) \quad (10)$$

where:

$V_{OUT}$  is the output voltage of the TIA.

$I_{PHOTO}$  is the input photodiode current.

$Z_F = R_{Fx} / ((R_{Fx} \times C_{Fx})s + 1)$ , where  $R_{Fx}$  and  $C_{Fx}$  are the feedback resistor and capacitor, respectively, of any of the chosen transimpedance gain paths.

$R1$  and  $R2$  are the T network gain resistors.

If  $Z_F \gg R2$ , the transimpedance equation is simplified to

$$\frac{V_{OUT}}{I_{PHOTO}} = -\frac{R_{Fx}}{(R_{Fx} \times C_{Fx})s + 1} \times \left( 1 + \frac{R2}{R1} \right)$$

Therefore, as compared to the standard TIA design, the T network uses a feedback resistor value that is  $1/(1 + R1/R2)$  smaller to obtain the same transimpedance. This eliminates the concern of the high parasitic capacitance associated with the large feedback resistor. To maintain the same signal bandwidth (or same pole), increase  $C_F$  by a factor of  $1 + R2/R1$  to eliminate concerns of an impractical small compensation capacitor.

As compared to a standard TIA design, the T network is noisier because the dominant voltage noise density is amplified by the gain factor  $1 + R2/R1$ .

Figure 71 shows the ADA4350 configured as a 1 MΩ transimpedance path and its T network equivalent. Figure 72 compares the performance of the 1 MΩ path and the equivalent T network with and without compensation capacitors.

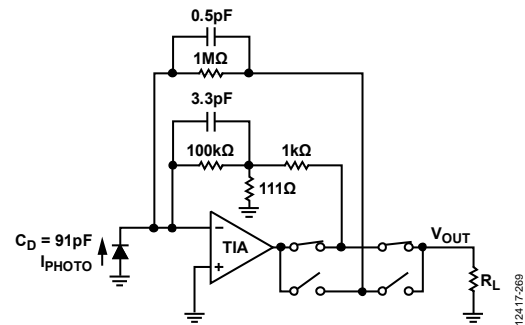


Figure 71. 1 MΩ Transimpedance Path and its Equivalent T Network

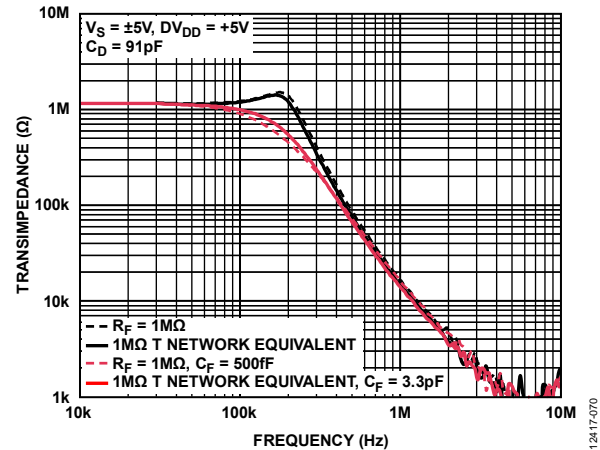
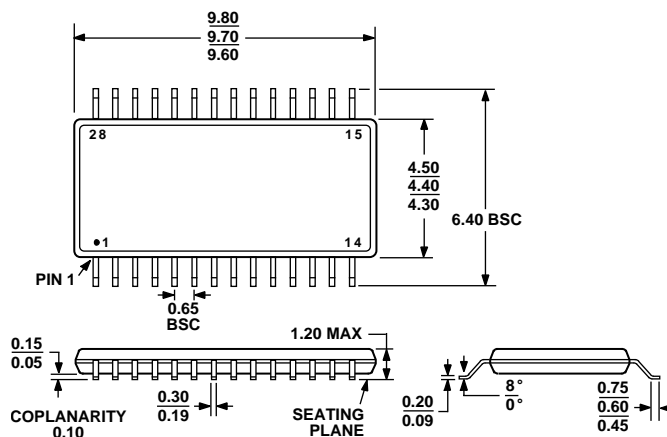


Figure 72. Comparing the 1 MΩ Transimpedance Path and T Network Performance

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 73. 28-Lead Thin Shrink Small Outline Package [TSSOP],  
(RU-28)

Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADA4350ARUZ	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADA4350ARUZ-R7	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
EVAL-ADA4350RUZ-P		Evaluation Board for 28-Lead TSSOP, Precision Version with Guard Rings	

<sup>1</sup> Z = RoHS Compliant Part.



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