

74HC193; 74HCT193

Presettable synchronous 4-bit binary up/down counter

Rev. 03 — 23 May 2007

Product data sheet

1. General description

The 74HC193 and 74HCT193 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC193 and 74HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (\overline{PL}).

The 74HC193 and 74HCT193 each contain four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CPD input will decrease the count by one, while a similar transition on the CPU input will advance the count by one.

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up (\overline{TCU}) and terminal count down (\overline{TCD}) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause \overline{TCU} to go LOW.

\overline{TCU} will stay LOW until CPU goes HIGH again, duplicating the count up clock.

Likewise, the \overline{TCD} output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load (\overline{PL}) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to

Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

2. Features

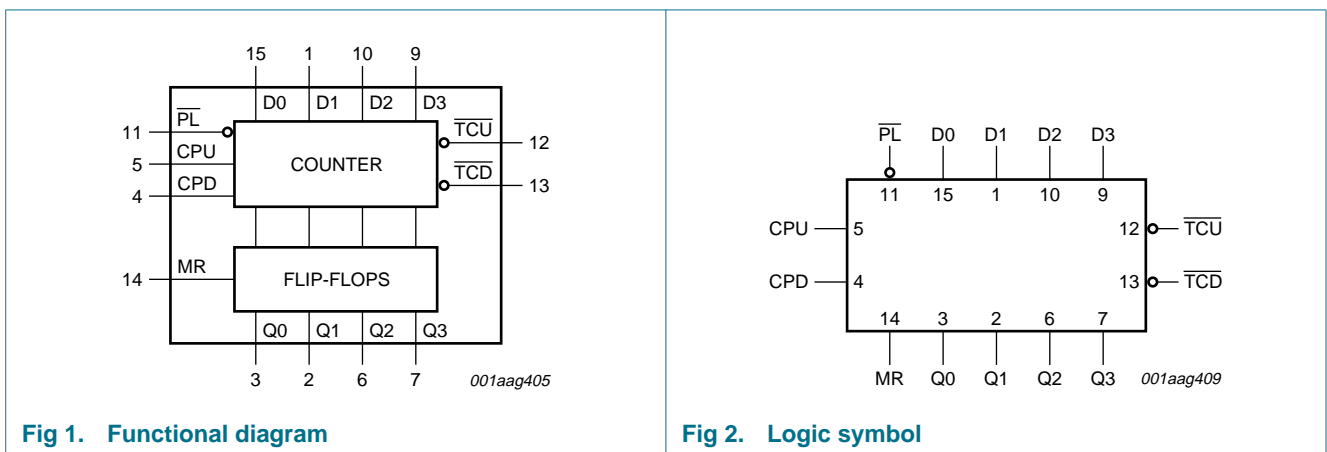
- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | |
| 74HC193D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HC193DB | -40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HC193N | -40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HC193PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT193D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT193DB | -40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT193N | -40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HCT193PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

4. Functional diagram



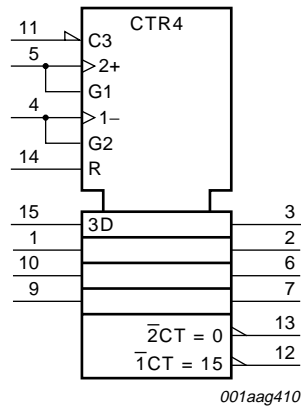
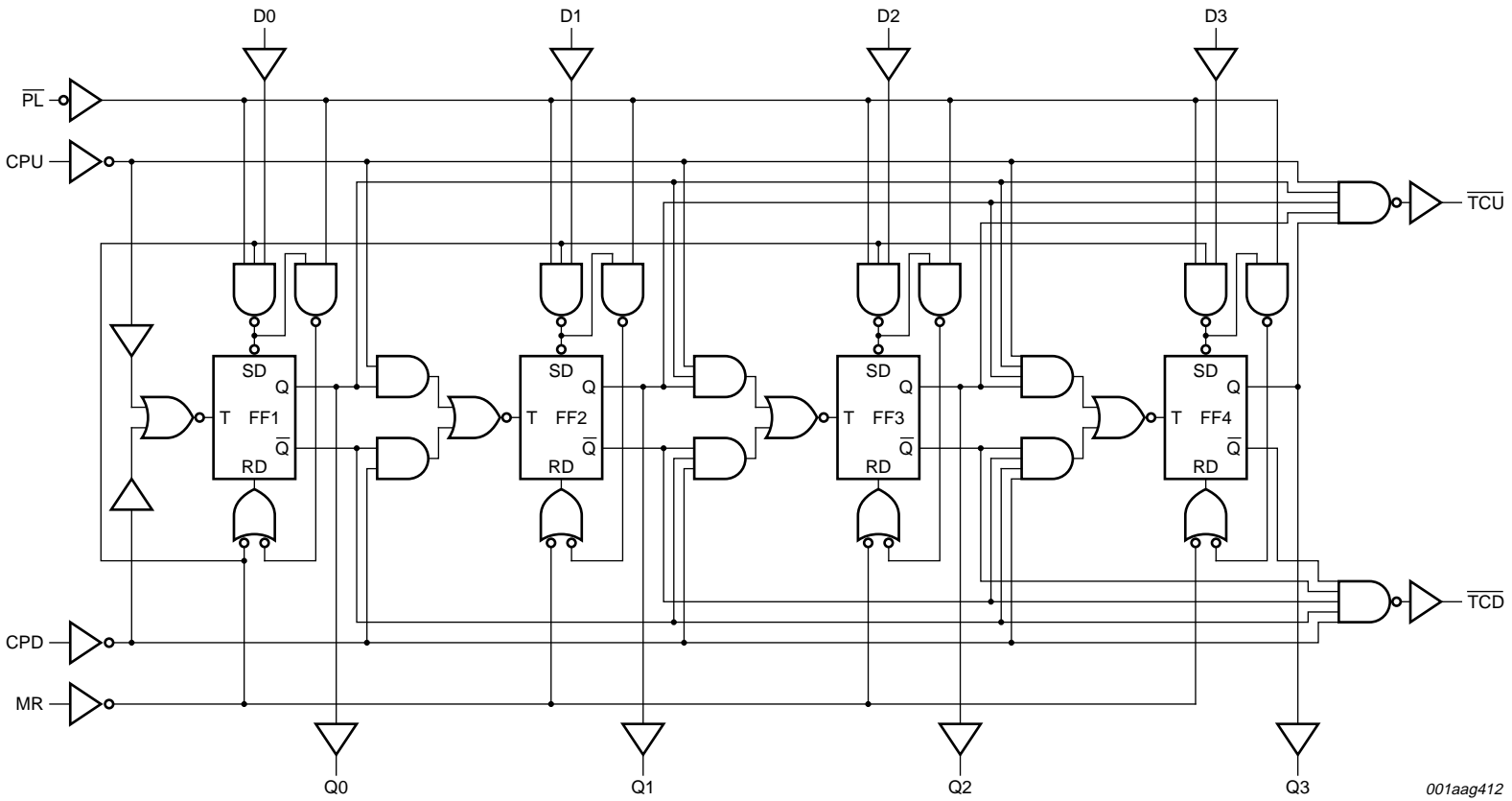


Fig 3. IEC logic symbol

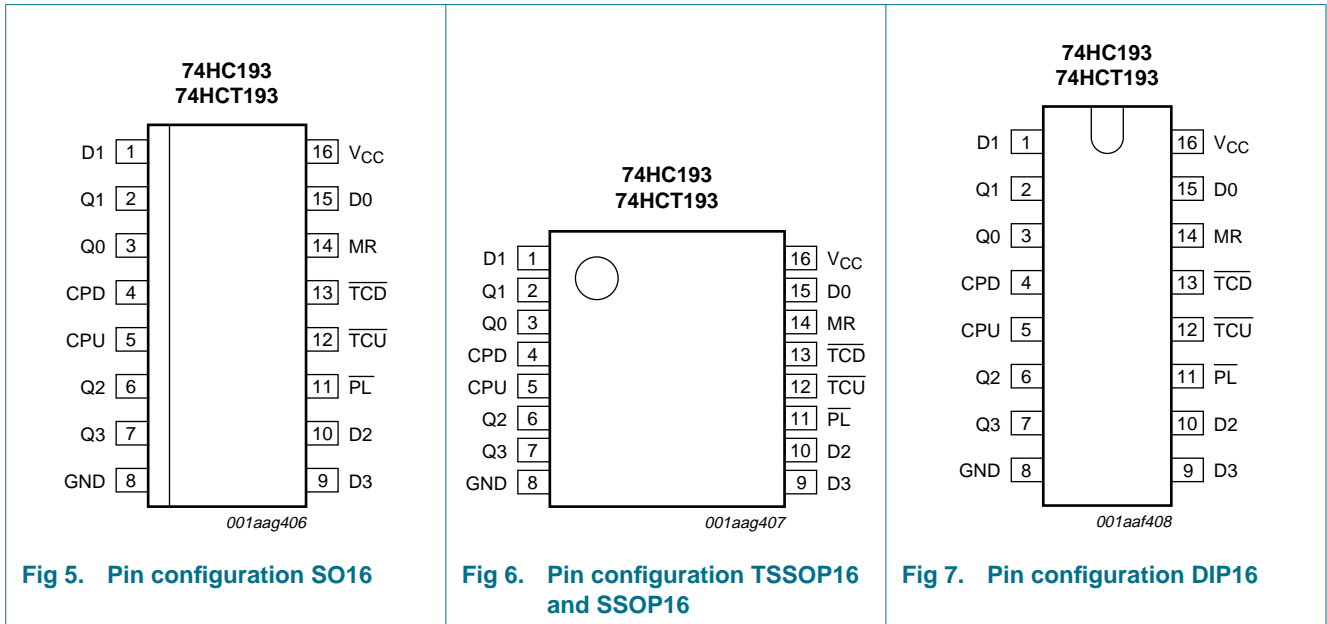


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Fig 4. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|-----|--|
| D0 | 15 | data input 0 |
| D1 | 1 | data input 1 |
| D2 | 10 | data input 2 |
| D3 | 9 | data input 3 |
| Q0 | 3 | flip-flop output 0 |
| Q1 | 2 | flip-flop output 1 |
| Q2 | 6 | flip-flop output 2 |
| Q3 | 7 | flip-flop output 3 |
| CPD | 4 | count down clock input ^[1] |
| CPU | 5 | count up clock input ^[1] |
| GND | 8 | ground (0 V) |
| PL | 11 | asynchronous parallel load input (active LOW) |
| TCU | 12 | terminal count up (carry) output (active LOW) |
| TCD | 13 | terminal count down (borrow) output (active LOW) |
| MR | 14 | asynchronous master reset input (active HIGH) |
| V _{CC} | 16 | supply voltage |

[1] LOW-to-HIGH, edge triggered.

6. Functional description

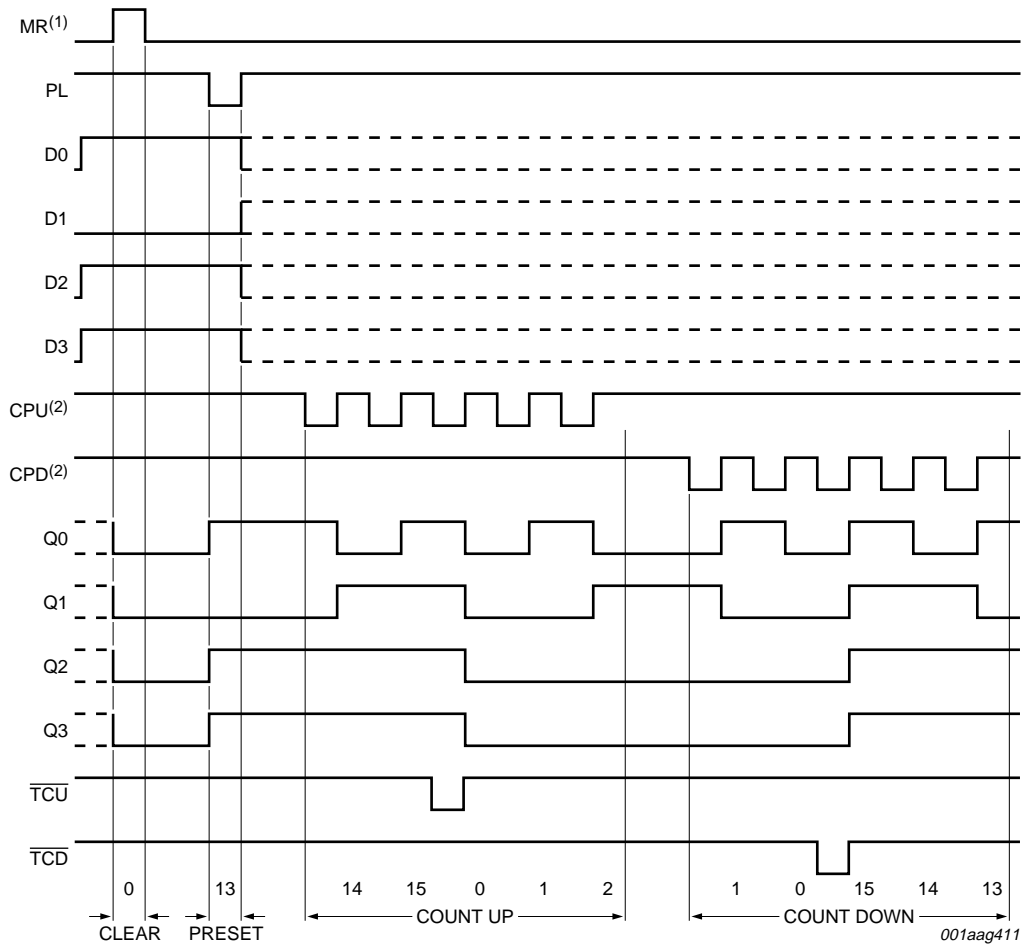
Table 3. Function table^[1]

| Operating mode | Inputs | | | | | | | | Outputs | | | | | |
|----------------|--------|-----------------|-----|-----|----|----|----|----|------------|----|----|----|------------------|------------------|
| | MR | \overline{PL} | CPU | CPD | D0 | D1 | D2 | D3 | Q0 | Q1 | Q2 | Q3 | \overline{TCU} | \overline{TCD} |
| Reset (clear) | H | X | X | L | X | X | X | X | L | L | L | L | H | L |
| | H | X | X | H | X | X | X | X | L | L | L | L | H | H |
| Parallel load | L | L | X | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | X | H | L | L | L | L | L | L | L | L | H | H |
| | L | L | L | X | H | H | H | H | H | H | H | H | L | H |
| | L | L | H | X | H | H | H | H | H | H | H | H | H | H |
| Count up | L | H | ↑ | H | X | X | X | X | count up | | | | H ^[2] | H |
| Count down | L | H | H | ↑ | X | X | X | X | count down | | | | H | H ^[3] |

[1] H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 ↑ = LOW-to-HIGH clock transition.

[2] \overline{TCU} = CPU at terminal count up (HHHH)

[3] \overline{TCD} = CPD at terminal count down (LLLL).



- (1) Clear overrides load, data and count inputs.
- (2) When counting up, the count down clock input (CPD) must be HIGH, when counting down the count up clock input (CPU) must be HIGH.

Sequence

Clear (reset outputs to zero);
 load (preset) to binary thirteen;
 count up to fourteen, fifteen, terminal count up, zero, one and two;
 count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Fig 8. Typical clear, load and count sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|-------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | [1] - | ±20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | [1] - | ±20 | mA |
| I_O | output current | $V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$ | - | ±25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | - | -50 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | DIP16 package | [2] - | 750 | mW |
| | | SO16 package | [2] - | 500 | mW |
| | | SSOP16 package | [2] - | 500 | mW |
| | | TSSOP16 package | [2] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly at 12 mW/K.

For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.

For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---------------------|-------------------------|-----|-----|----------|------|
| 74HC193 | | | | | | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| t_r | rise time | inputs | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | - | - | 1000 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | - | 6.0 | 500 | ns |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 400 | ns |
| t_f | fall time | inputs | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | - | - | 1000 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | - | 6.0 | 500 | ns |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 400 | ns |

Table 5. Recommended operating conditions ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------|---------------------------------|-----|-----|-----------------|------|
| 74HCT193 | | | | | | |
| V _{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| t _r | rise time | inputs; V _{CC} = 4.5 V | - | 6.0 | 500 | ns |
| t _f | fall time | inputs; V _{CC} = 4.5 V | - | 6.0 | 500 | ns |

9. Static characteristics

Table 6. Static characteristics type 74HC193

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---------------------------|--|------|------|------|------|
| T_{amb} = 25 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | - | - | - | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | - | - | - | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | μA |
| | | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | μA |
| C _i | input capacitance | | - | 3.5 | - | pF |
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | V |
| | | V _{CC} = 4.5 V | 3.15 | - | - | V |
| | | V _{CC} = 6.0 V | 4.2 | - | - | V |

Table 6. Static characteristics type 74HC193 ...continued
 At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|--|------|-----|------|------|
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | - | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.84 | - | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.34 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | - | 0.33 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | - | 0.33 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 80 | μA |
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | V |
| | | V _{CC} = 4.5 V | 3.15 | - | - | V |
| | | V _{CC} = 6.0 V | 4.2 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | - | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.7 | - | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.2 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 160 | μA |

Table 7. Static characteristics type 74HCT193

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|--|------|------|-------|------|
| T_{amb} = 25 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | |
| | | I _O = -20 µA | 4.4 | 4.5 | - | V |
| | | I _O = -4.0 mA | 3.98 | 4.32 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | |
| | | I _O = 20 µA | - | 0 | 0.1 | V |
| | | I _O = 4.0 mA | - | 0.15 | 0.26 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V and other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V | | | | |
| | | pin Dn | - | 35 | 126 | µA |
| | | pins CPU, CPD | - | 140 | 504 | µA |
| | | pin \overline{PL} | - | 65 | 234 | µA |
| | | pin MR | - | 105 | 378 | µA |
| C _i | input capacitance | | - | 3.5 | - | pF |
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | |
| | | I _O = -20 µA | 4.4 | - | - | V |
| | | I _O = -4.0 mA | 3.84 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | |
| | | I _O = 20 µA | - | - | 0.1 | V |
| | | I _O = 4.0 mA | - | - | 0.33 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±1.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 80 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V and other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V | | | | |
| | | pin Dn | - | - | 157.5 | µA |
| | | pins CPU, CPD | - | - | 630 | µA |
| | | pin \overline{PL} | - | - | 292.5 | µA |
| | | pin MR | - | - | 472.5 | µA |
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | V |

Table 7. Static characteristics type 74HCT193 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------------|--|-----|-----|-------|------|
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | |
| | | I _O = -20 μA | 4.4 | - | - | V |
| | | I _O = -4.0 mA | 3.7 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | |
| | | I _O = 20 μA | - | - | 0.1 | V |
| | | I _O = 4.0 mA | - | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 160 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V and other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V | | | | |
| | | pin Dn | - | - | 171.5 | μA |
| | | pins CPU, CPD | - | - | 686 | μA |
| | | pin \overline{PL} | - | - | 318.5 | μA |
| | | pin MR | - | - | 514.5 | μA |

10. Dynamic characteristics

Table 8. Dynamic characteristics type 74HC193

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit | | |
|---|-------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|--|--|
| | | | Min | Typ | Max | Min | Max | Min | Max | | | |
| t _{pd} | propagation delay | CPU, CPD to Qn; see Figure 9 ^[1] | - | | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 63 | 215 | - | 270 | - | 325 | ns | | |
| | | V _{CC} = 4.5 V | - | 23 | 43 | - | 54 | - | 65 | ns | | |
| | | V _{CC} = 6.0 V | - | 18 | 37 | - | 46 | - | 55 | ns | | |
| | | CPU to \overline{TCU} ; see Figure 10 | | | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 39 | 125 | - | 155 | - | 190 | ns | | |
| | | V _{CC} = 4.5 V | - | 14 | 25 | - | 31 | - | 38 | ns | | |
| | | V _{CC} = 6.0 V | - | 11 | 21 | - | 26 | - | 32 | ns | | |
| | | CPD to \overline{TCD} ; see Figure 10 | | | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 39 | 125 | - | 155 | - | 190 | ns | | |
| | | V _{CC} = 4.5 V | - | 14 | 25 | - | 31 | - | 38 | ns | | |
| | | V _{CC} = 6.0 V | - | 11 | 21 | - | 26 | - | 32 | ns | | |
| | | \overline{PL} to Qn; see Figure 11 | | | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 69 | 220 | - | 275 | - | 330 | ns | | |
| | | V _{CC} = 4.5 V | - | 25 | 44 | - | 55 | - | 66 | ns | | |
| | | V _{CC} = 6.0 V | - | 20 | 37 | - | 47 | - | 56 | ns | | |
| | | MR to Qn; see Figure 12 | | | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 58 | 200 | - | 250 | - | 300 | ns | | |
| | | V _{CC} = 4.5 V | - | 21 | 40 | - | 50 | - | 60 | ns | | |
| | | V _{CC} = 6.0 V | - | 17 | 34 | - | 43 | - | 51 | ns | | |
| | | Dn to Qn; see Figure 11 | | | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 69 | 210 | - | 265 | - | 315 | ns | | |
| | | V _{CC} = 4.5 V | - | 25 | 42 | - | 53 | - | 63 | ns | | |
| | | V _{CC} = 6.0 V | - | 20 | 36 | - | 45 | - | 54 | ns | | |
| | | \overline{PL} to \overline{TCU} , \overline{PL} to \overline{TCD} ; see Figure 14 | | | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 80 | 290 | - | 365 | - | 435 | ns | | |
| | | V _{CC} = 4.5 V | - | 29 | 58 | - | 73 | - | 87 | ns | | |
| | | V _{CC} = 6.0 V | - | 23 | 49 | - | 62 | - | 74 | ns | | |
| MR to \overline{TCU} , MR to \overline{TCD} ; see Figure 14 | | | | | | | | | | | | |
| V _{CC} = 2.0 V | - | 74 | 285 | - | 355 | - | 430 | ns | | | | |
| V _{CC} = 4.5 V | - | 27 | 57 | - | 71 | - | 86 | ns | | | | |
| V _{CC} = 6.0 V | - | 22 | 48 | - | 60 | - | 73 | ns | | | | |

Table 8. Dynamic characteristics type 74HC193 ...continued

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|------------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{pd} | propagation delay | Dn to $\overline{\text{TCU}}$, Dn to $\overline{\text{TCD}}$; see Figure 14 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 80 | 290 | - | 365 | - | 435 | ns |
| | | V _{CC} = 4.5 V | - | 29 | 58 | - | 73 | - | 87 | ns |
| | | V _{CC} = 6.0 V | - | 23 | 49 | - | 62 | - | 74 | ns |
| t _{THL} | HIGH to LOW output transition time | see Figure 12 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | V _{CC} = 6.0 V | - | 6 | 13 | - | 16 | - | 19 | ns |
| t _{TLH} | LOW to HIGH output transition time | see Figure 12 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | V _{CC} = 6.0 V | - | 6 | 13 | - | 16 | - | 19 | ns |
| t _w | pulse width | CPU, CPD (HIGH or LOW); see Figure 9 | | | | | | | | |
| | | V _{CC} = 2.0 V | 100 | 22 | - | 125 | - | 150 | - | ns |
| | | V _{CC} = 4.5 V | 20 | 8 | - | 25 | - | 30 | - | ns |
| | | V _{CC} = 6.0 V | 17 | 6 | - | 21 | - | 26 | - | ns |
| | | MR (HIGH); see Figure 12 | | | | | | | | |
| | | V _{CC} = 2.0 V | 100 | 25 | - | 125 | - | 150 | - | ns |
| | | V _{CC} = 4.5 V | 20 | 9 | - | 25 | - | 30 | - | ns |
| | | V _{CC} = 6.0 V | 17 | 7 | - | 21 | - | 26 | - | ns |
| | | $\overline{\text{PL}}$ (LOW); see Figure 11 | | | | | | | | |
| | | V _{CC} = 2.0 V | 100 | 19 | - | 125 | - | 150 | - | ns |
| | | V _{CC} = 4.5 V | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | V _{CC} = 6.0 V | 17 | 6 | - | 21 | - | 26 | - | ns |
| t _{rec} | recovery time | $\overline{\text{PL}}$ to CPU, CPD; see Figure 11 | | | | | | | | |
| | | V _{CC} = 2.0 V | 50 | 8 | - | 65 | - | 75 | - | ns |
| | | V _{CC} = 4.5 V | 10 | 3 | - | 13 | - | 15 | - | ns |
| | | V _{CC} = 6.0 V | 9 | 2 | - | 11 | - | 13 | - | ns |
| | | MR to CPU, CPD; see Figure 12 | | | | | | | | |
| | | V _{CC} = 2.0 V | 50 | 0 | - | 65 | - | 75 | - | ns |
| | | V _{CC} = 4.5 V | 10 | 0 | - | 13 | - | 15 | - | ns |
| | | V _{CC} = 6.0 V | 9 | 0 | - | 11 | - | 13 | - | ns |

Table 8. Dynamic characteristics type 74HC193 ...continued

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|-------|------|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{su} | set-up time | Dn to \overline{PL} ; see Figure 13 ; note: CPU = CPD = HIGH | | | | | | | | |
| | | V _{CC} = 2.0 V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | V _{CC} = 4.5 V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | V _{CC} = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |
| t _h | hold time | Dn to \overline{PL} ; see Figure 13 | | | | | | | | |
| | | V _{CC} = 2.0 V | 0 | -14 | - | 0 | - | 0 | - | ns |
| | | V _{CC} = 4.5 V | 0 | -5 | - | 0 | - | 0 | - | ns |
| | | V _{CC} = 6.0 V | 0 | -4 | - | 0 | - | 0 | - | ns |
| | | CPU to CPD, CPD to CPU; see Figure 15 | | | | | | | | |
| | | V _{CC} = 2.0 V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | V _{CC} = 6.0 V | 8 | 6 | - | 17 | - | 20 | - | ns |
| f _{max} | maximum frequency | CPU, CPD; see Figure 9 | | | | | | | | |
| | | V _{CC} = 2.0 V | 4.0 | 13.5 | - | 3.2 | - | 2.6 | - | MHz |
| | | V _{CC} = 4.5 V | 20 | 41 | - | 16 | - | 13 | - | MHz |
| | | V _{CC} = 6.0 V | 24 | 49 | - | 19 | - | 15 | - | MHz |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} ; [2] V _{CC} = 5 V; f _i = 1 MHz | - | 24 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 9. Dynamic characteristics type 74HCT193

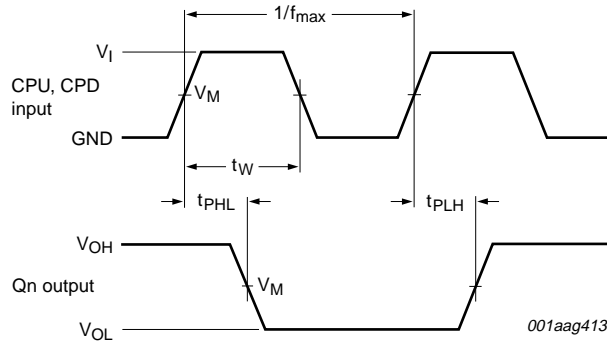
| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit | |
|--|------------------------------------|---|------------------------------------|--|-----|------------------|-----|-------------------|-----|------|----|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| t _{pd} | propagation delay | CPU, CPD to Qn; see Figure 9 ^[1] | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 23 | 43 | - | 54 | - | 65 | ns | |
| | | CPU to $\overline{\text{TCU}}$; see Figure 10 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 15 | 27 | - | 34 | - | 41 | ns | |
| | | CPD to $\overline{\text{TCD}}$; see Figure 10 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 15 | 27 | - | 34 | - | 41 | ns | |
| | | $\overline{\text{PL}}$ to Qn; see Figure 11 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 26 | 46 | - | 58 | - | 69 | ns | |
| | | MR to Qn; see Figure 12 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 22 | 40 | - | 50 | - | 60 | ns | |
| | | Dn to Qn; see Figure 11 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 27 | 46 | - | 58 | - | 69 | ns | |
| t _{THL} | HIGH to LOW output transition time | $\overline{\text{PL}}$ to $\overline{\text{TCU}}$, $\overline{\text{PL}}$ to $\overline{\text{TCD}}$; see Figure 14 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 31 | 55 | - | 69 | - | 83 | ns | |
| | | MR to $\overline{\text{TCU}}$, MR to $\overline{\text{TCD}}$; see Figure 14 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 29 | 55 | - | 69 | - | 83 | ns | |
| | | Dn to $\overline{\text{TCU}}$, Dn to $\overline{\text{TCD}}$; see Figure 14 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 32 | 58 | - | 73 | - | 87 | ns | |
| | | see Figure 12 | | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns | |
| | | t _{TLH} | LOW to HIGH output transition time | see Figure 12 | | | | | | | |
| | | | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 |
| | | t _w | pulse width | CPU, CPD (HIGH or LOW); see Figure 9 | | | | | | | |
| | | | | V _{CC} = 4.5 V | 25 | 11 | - | 31 | - | 38 | - |
| MR (HIGH); see Figure 12 | | | | | | | | | | | |
| V _{CC} = 4.5 V | 20 | | | 7 | - | 25 | - | 30 | - | ns | |
| t _w | pulse width | $\overline{\text{PL}}$ (LOW); see Figure 11 | | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 8 | - | 25 | - | 30 | - | ns | |

Table 9. Dynamic characteristics type 74HCT193 ...continued

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{rec} | recovery time | \overline{PL} to CPU, CPD; see Figure 11 $V_{CC} = 4.5\text{ V}$ | 10 | 2 | - | 13 | - | 15 | - | ns |
| | | MR to CPU, CPD; see Figure 12 $V_{CC} = 4.5\text{ V}$ | 10 | 0 | - | 13 | - | 15 | - | ns |
| t _{su} | set-up time | Dn to \overline{PL} ; see Figure 13 ; note: CPU = CPD = HIGH $V_{CC} = 4.5\text{ V}$ | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | Dn to \overline{PL} ; see Figure 13 $V_{CC} = 4.5\text{ V}$ | 0 | -6 | - | 0 | - | 0 | - | ns |
| t _h | hold time | CPU to CPD, CPD to CPU; see Figure 15 $V_{CC} = 4.5\text{ V}$ | 16 | 7 | - | 20 | - | 24 | - | ns |
| | | CPU, CPD; see Figure 9 $V_{CC} = 4.5\text{ V}$ | 20 | 43 | - | 16 | - | 13 | - | MHz |
| C _{PD} | power dissipation capacitance | $V_I = \text{GND to } V_{CC} - [2]$ $1.5\text{ V}; V_{CC} = 5\text{ V};$ $f_i = 1\text{ MHz}$ | - | 26 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
 [2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

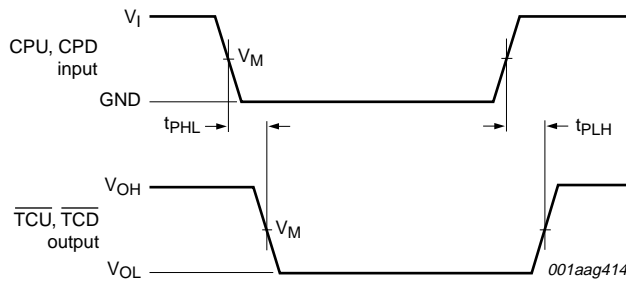


Measurement points are given in [Table 10](#).

t_{PLH} and t_{PHL} are the same as t_{pd} .

Logic levels V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 9. The clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width, and the maximum clock pulse frequency

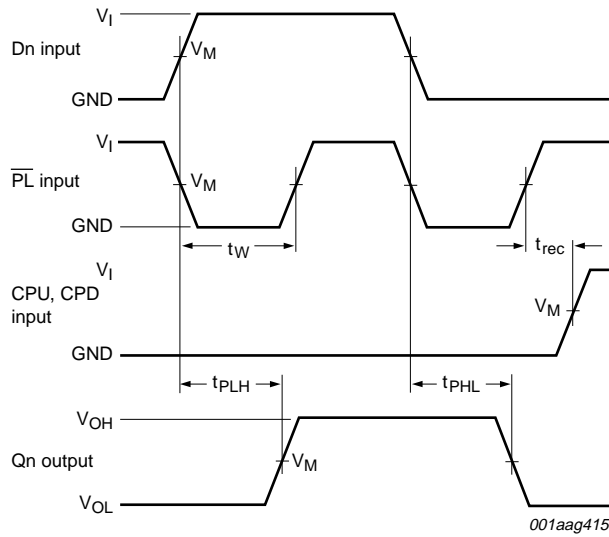


Measurement points are given in [Table 10](#).

t_{PLH} and t_{PHL} are the same as t_{pd} .

Logic levels V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 10. The clock (CPU, CPD) to terminal count output (TCU, TCD) propagation delays

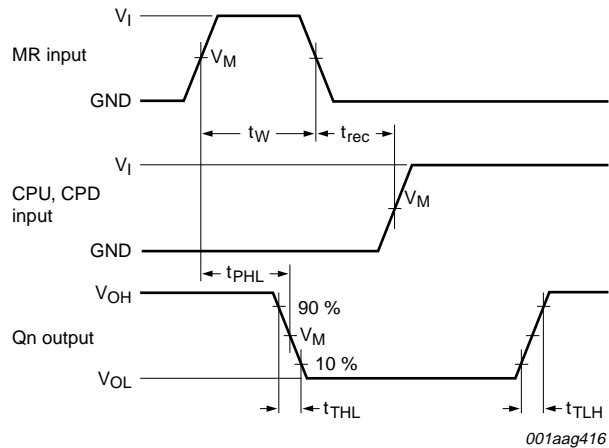


Measurement points are given in [Table 10](#).

t_{PLH} and t_{PHL} are the same as t_{pd} .

Logic levels V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 11. The parallel load input (PL) and data (Dn) to Qn output propagation delays and PL removal time to clock input (CPU, CPD)

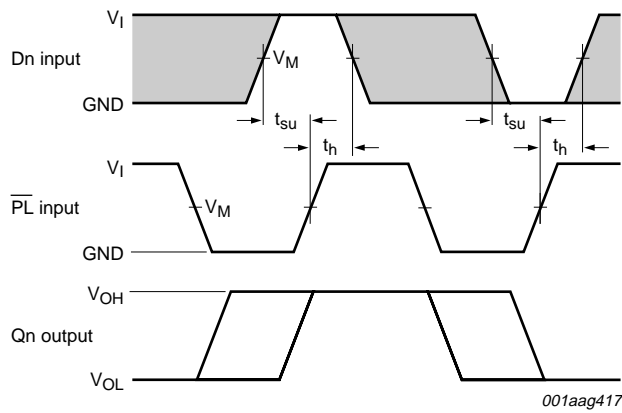


Measurement points are given in [Table 10](#).

t_{PLH} and t_{PHL} are the same as t_{pd} .

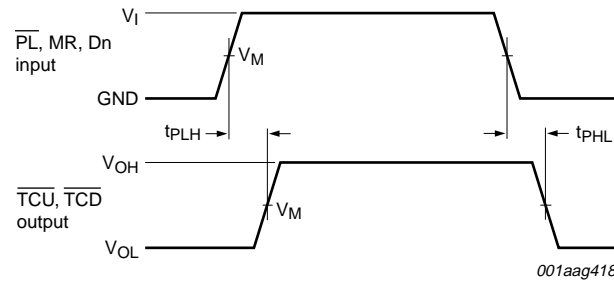
Logic levels V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 12. The master reset input (MR) pulse width, MR to Qn propagation delays, MR to CPU, CPD removal time and output transition times



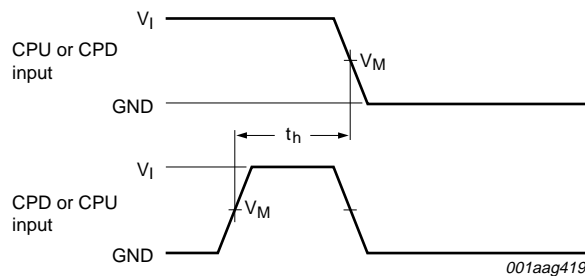
The shaded areas indicate when the input is permitted to change for predictable output performance. Measurement points are given in [Table 10](#). Logic levels V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 13. The data input (Dn) to parallel load input (PL) set-up and hold times



Measurement points are given in [Table 10](#). t_{PLH} and t_{PHL} are the same as t_{pd} . Logic levels V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 14. The data input (Dn), parallel load input (PL) and the master reset input (MR) to the terminal count outputs (TCU, TCD) propagation delays

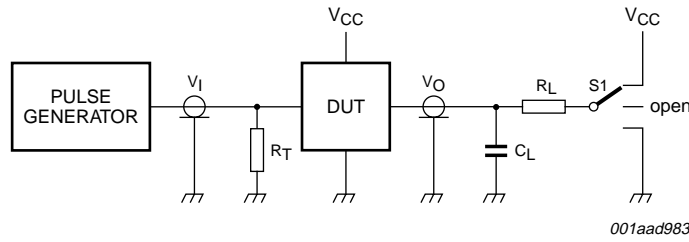
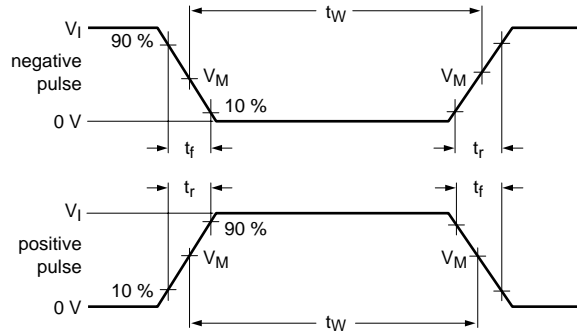


Measurement points are given in [Table 10](#).

Fig 15. The CPU to CPD or CPD to CPU hold times

Table 10. Measurement points

| Type | Input | | Output |
|----------|---------------------|-----------------|---------------------|
| | V_M | V_I | V_M |
| 74HC193 | $0.5 \times V_{CC}$ | GND to V_{CC} | $0.5 \times V_{CC}$ |
| 74HCT193 | 1.3 V | GND to 3 V | 1.3 V |



Test data is given in [Table 11](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

S1 = Test selection switch

Fig 16. Load circuitry for measuring switching times

Table 11. Test data

| Type | Input | | Load | | S1 position |
|----------|----------|------------|--------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} |
| 74HC193 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open |
| 74HCT193 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open |

12. Application information

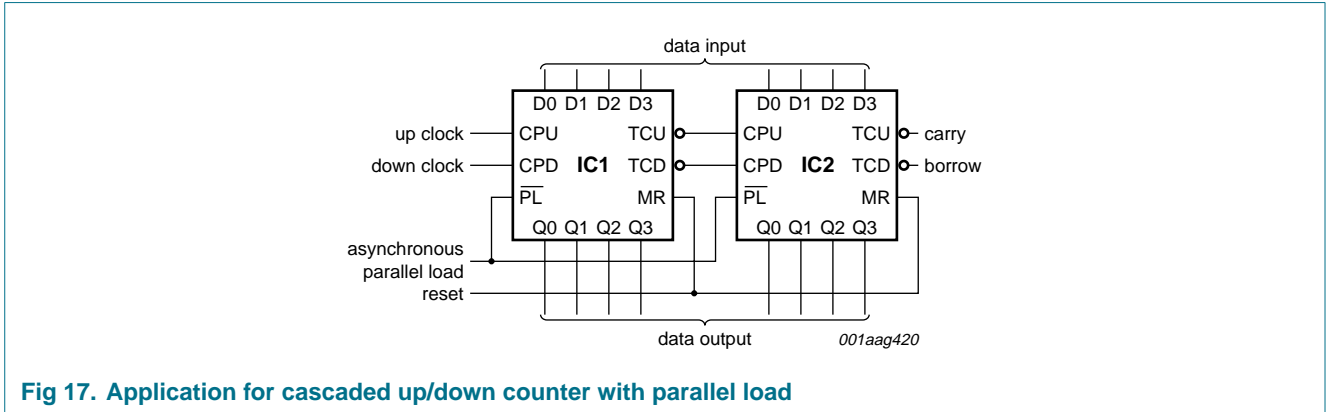


Fig 17. Application for cascaded up/down counter with parallel load

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

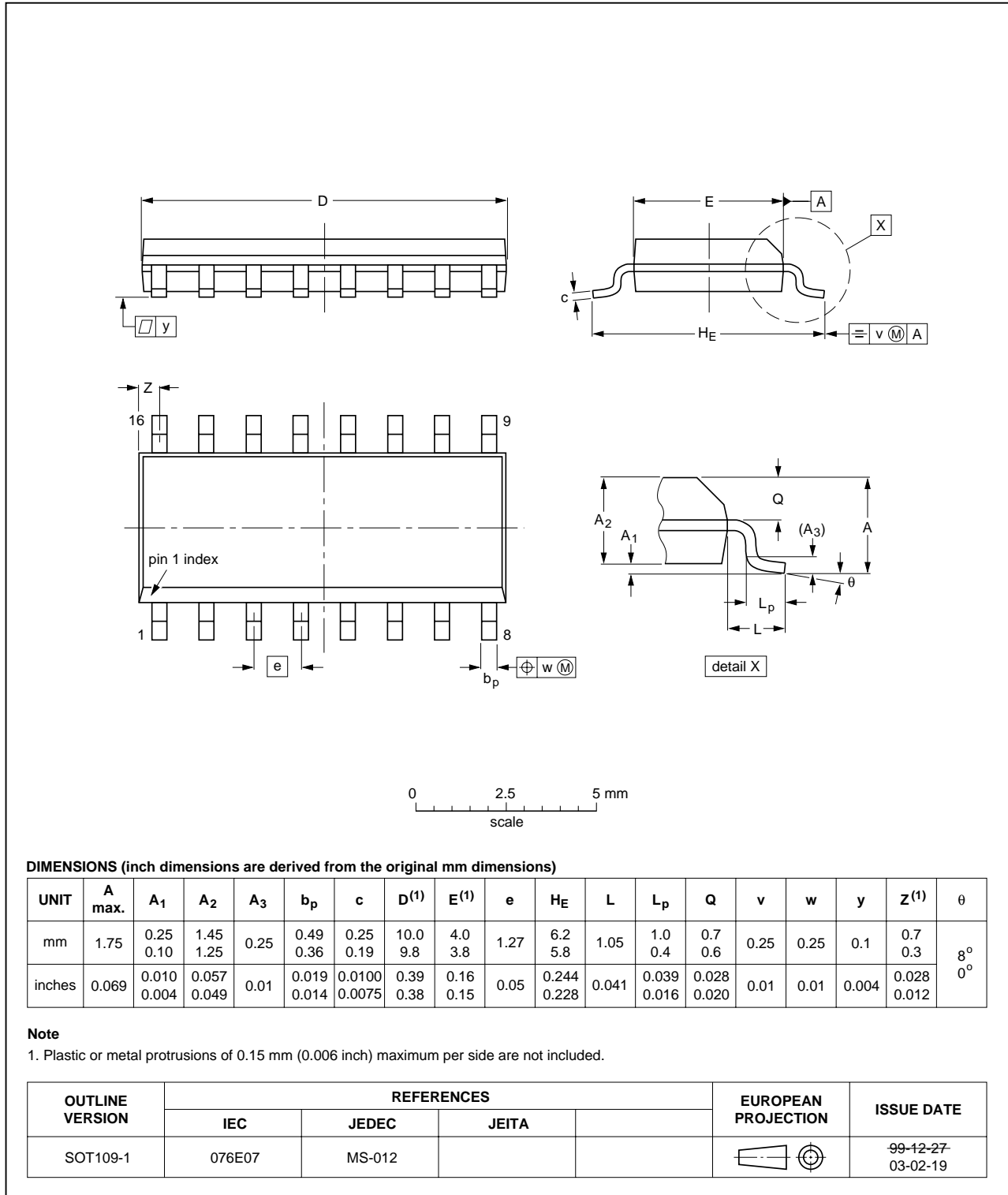


Fig 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

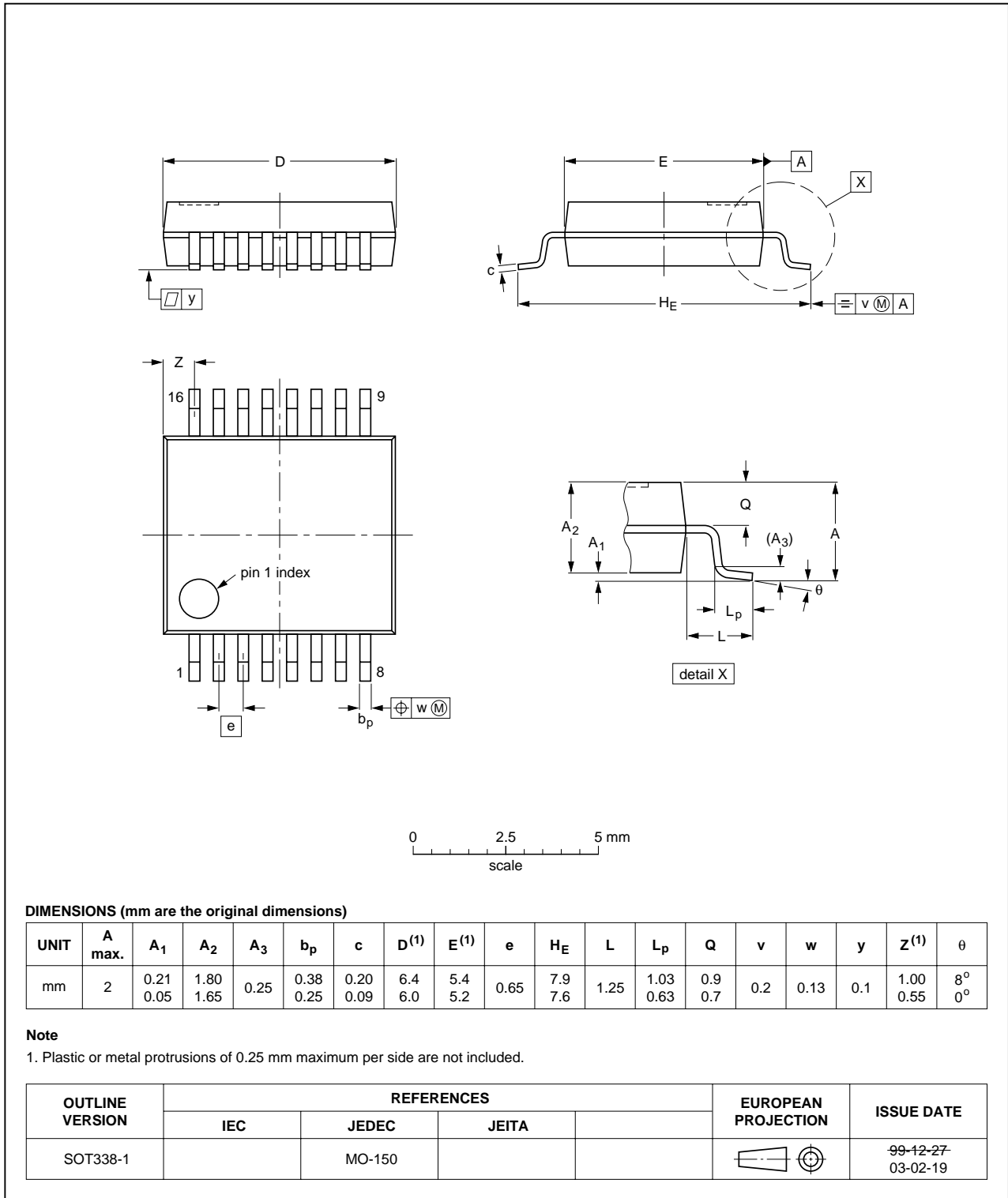


Fig 19. Package outline SOT338-1 (SSOP16)

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

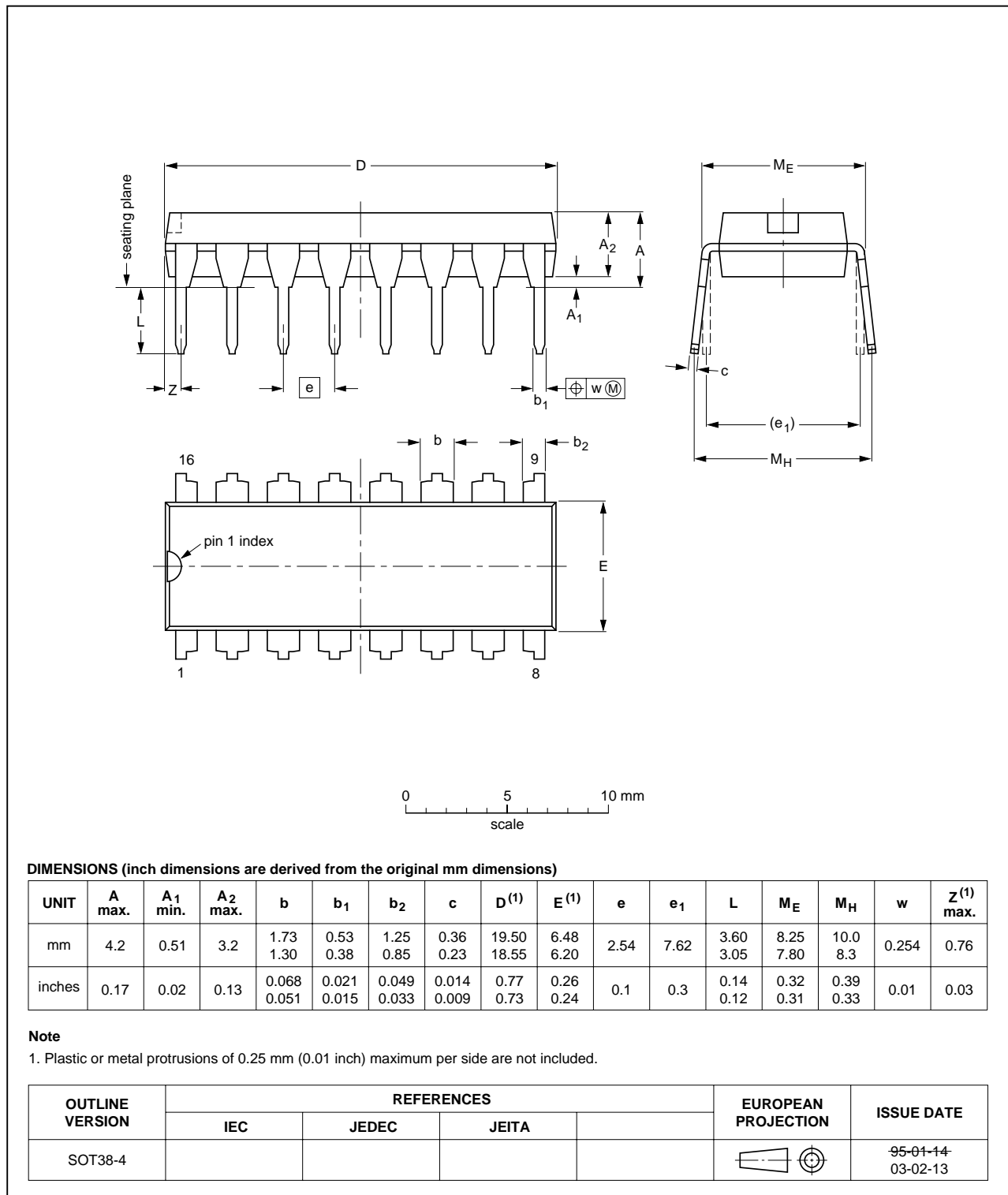


Fig 20. Package outline SOT38-4 (DIP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

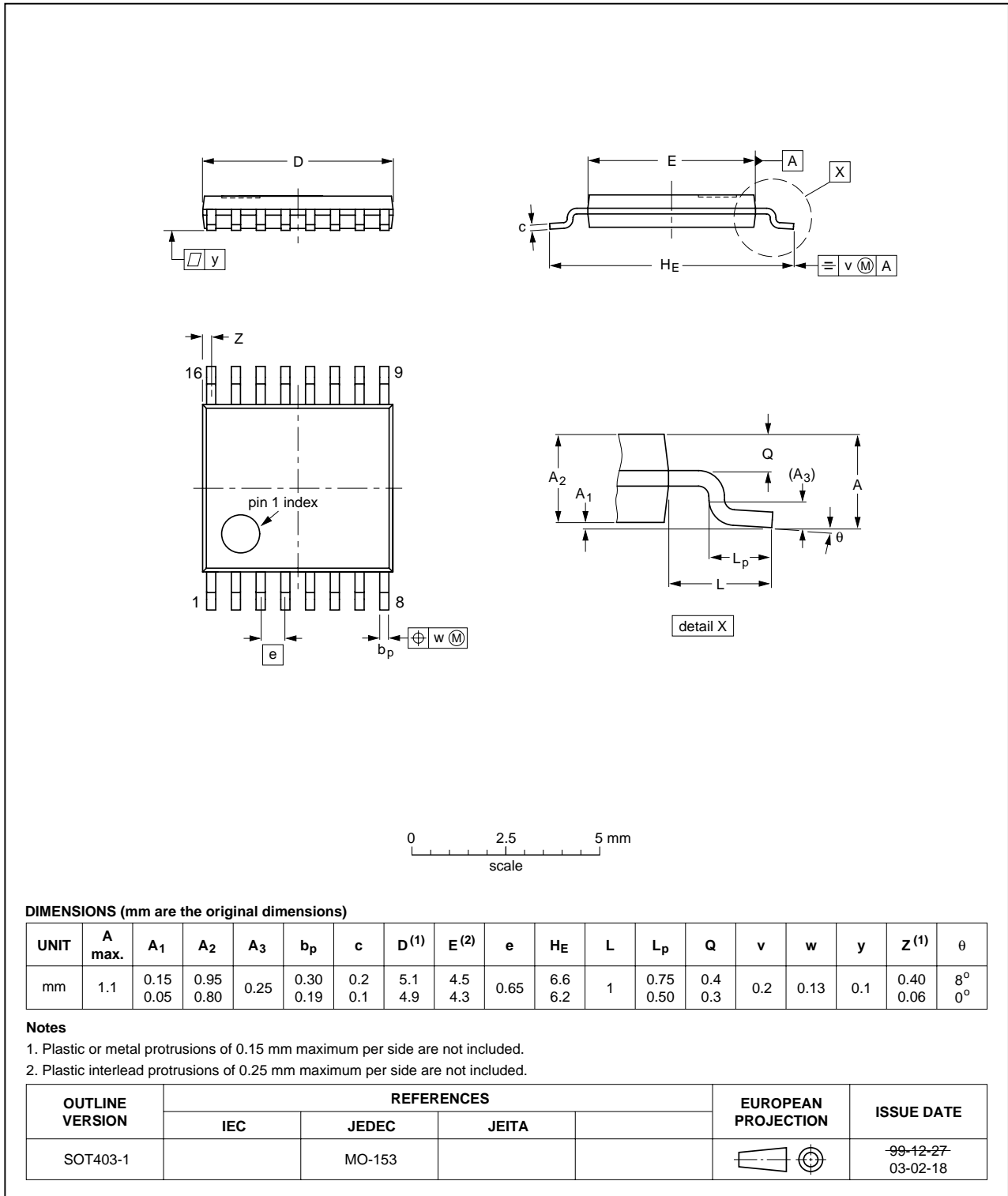


Fig 21. Package outline SOT403-1 (TSSOP16)

14. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--------------|--|---------------|-------------------|
| 74HC_HCT193_3 | 20070523 | Product data sheet | - | 74HC_HCT193_CNV_2 |
| Modifications: | | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Family specification included | | |
| 74HC_HCT193_CNV_2 | 19970828 | Product specification | - | - |

15. Legal information

16. Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 23 May 2007

Document identifier: 74HC_HCT193_3



Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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