

BGA  
Commercial Temp  
Industrial Temp

256K x 18, 128K x 32, 128K x 36  
4Mb Sync Burst SRAMs

250 MHz–150 MHz  
3.3 V  $V_{DD}$   
3.3 V and 2.5 V I/O

## Features

- $\overline{FT}$  pin for user-configurable flow through or pipelined operation
- Single Cycle Deselect (SCD) operation
- 3.3 V  $\pm 10\%$  core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$  pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipelined mode
- Byte Write ( $\overline{BW}$ ) and/or Global Write ( $\overline{GW}$ ) operation
- Common data inputs and data outputs
- Clock control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 119-bump BGA package
- RoHS-compliant 119-bump BGA package

## Functional Description

### Applications

The GS84018/32/36C is a 4,718,592-bit (4,194,304-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications ranging from DSP main store to networking chip set support. The GS84018/32/36A is available in a JEDEC standard 100-lead TQFP or 119-Bump BGA package.

### Controls

Addresses, data I/Os, chip enables ( $\overline{E}_1$ ,  $E_2$ ,  $\overline{E}_3$ ), address burst control inputs ( $\overline{ADSP}$ ,  $\overline{ADSC}$ ,  $\overline{ADV}$ ), and write control inputs ( $\overline{Bx}$ ,  $\overline{BW}$ ,  $\overline{GW}$ ) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ( $\overline{G}$ ) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either  $\overline{ADSP}$  or  $\overline{ADSC}$  inputs. In Burst mode, subsequent burst addresses are generated

internally and are controlled by  $\overline{ADV}$ . The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ( $\overline{LBO}$ ) input. The burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

### Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the  $\overline{FT}$  mode pin/bump (pin 14 in the TQFP and bump 5R in the BGA). Holding the  $\overline{FT}$  mode pin/bump low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding  $\overline{FT}$  high places the RAM in Pipelined mode, activating the rising-edge-triggered Data Output Register.

### SCD Pipelined Reads

The GS84018/32/36C is an SCD (Single Cycle Deselect) pipelined synchronous SRAM. DCD (Dual Cycle Deselect) versions are also available. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers.

### Byte Write and Global Write

Byte write operation is performed by using byte write enable ( $\overline{BW}$ ) input combined with one or more individual byte write signals ( $\overline{Bx}$ ). In addition, Global Write ( $\overline{GW}$ ) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

### Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

### Core and Interface Voltages

The GS84018/32/36C operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power ( $V_{DDQ}$ ) pins are used to de-couple output noise from the internal circuit.

## Parameter Synopsis

		-250	-200	-166	-150	Unit
Pipeline	tCycle	4.0	5.5	6.0	6.7	ns
	tKQ	2.5	3.0	3.5	3.8	ns
	Curr (x18)	195	170	150	140	MHz
	Curr (x32/x36)	225	195	185	160	MHz
Flow Through	tKQ	5.5	6.5	7.0	7.5	ns
	tCycle	5.5	6.5	7.0	7.5	ns
	Curr (x18)	160	140	140	128	MHz
	Curr (x32/x36)	180	160	155	145	MHz

## GS84018C Pad Out—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
B	NC	E <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	$\overline{\text{E}}_3$	NC
C	NC	A	A	V <sub>DD</sub>	A	A	NC
D	DQB	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQPA	NC
E	NC	DQB	V <sub>SS</sub>	$\overline{\text{E}}_1$	V <sub>SS</sub>	NC	DQA
F	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{\text{G}}$	V <sub>SS</sub>	DQA	V <sub>DDQ</sub>
G	NC	DQB	$\overline{\text{B}}_B$	$\overline{\text{ADV}}$	NC	NC	DQA
H	DQB	NC	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQA	NC
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	NC	DQB	V <sub>SS</sub>	CK	V <sub>SS</sub>	NC	DQA
L	DQB	NC	NC	NC	$\overline{\text{B}}_A$	DQA	NC
M	V <sub>DDQ</sub>	DQB	V <sub>SS</sub>	$\overline{\text{BW}}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
N	DQB	NC	V <sub>SS</sub>	A <sub>1</sub>	V <sub>SS</sub>	DQA	NC
P	NC	DQP <sub>B</sub>	V <sub>SS</sub>	A <sub>0</sub>	V <sub>SS</sub>	NC	DQA
R	NC	A	$\overline{\text{LBO}}$	V <sub>DD</sub>	$\overline{\text{FT}}$	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V <sub>DDQ</sub>	NC	NC	NC	NC	NC	V <sub>DDQ</sub>

## GS84032C Pad Out—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
B	NC	E <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	$\overline{\text{E}}_3$	NC
C	NC	A	A	V <sub>DD</sub>	A	A	NC
D	DQc	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	NC	DQB
E	DQc	DQc	V <sub>SS</sub>	$\overline{\text{E}}_1$	V <sub>SS</sub>	DQB	DQB
F	V <sub>DDQ</sub>	DQc	V <sub>SS</sub>	$\overline{\text{G}}$	V <sub>SS</sub>	DQB	V <sub>DDQ</sub>
G	DQc	DQc	$\overline{\text{B}}_c$	$\overline{\text{ADV}}$	$\overline{\text{B}}_b$	DQB	DQB
H	DQc	DQc	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQB	DQB
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQd	DQd	V <sub>SS</sub>	CK	V <sub>SS</sub>	DQA	DQA
L	DQd	DQd	$\overline{\text{B}}_d$	NC	$\overline{\text{B}}_a$	DQA	DQA
M	V <sub>DDQ</sub>	DQd	V <sub>SS</sub>	$\overline{\text{BW}}$	V <sub>SS</sub>	DQA	V <sub>DDQ</sub>
N	DQd	DQd	V <sub>SS</sub>	A <sub>1</sub>	V <sub>SS</sub>	DQA	DQA
P	DQd	NC	V <sub>SS</sub>	A <sub>0</sub>	V <sub>SS</sub>	NC	DQA
R	NC	A	$\overline{\text{LBO}}$	V <sub>DD</sub>	$\overline{\text{FT}}$	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V <sub>DDQ</sub>	NC	NC	NC	NC	NC	V <sub>DDQ</sub>

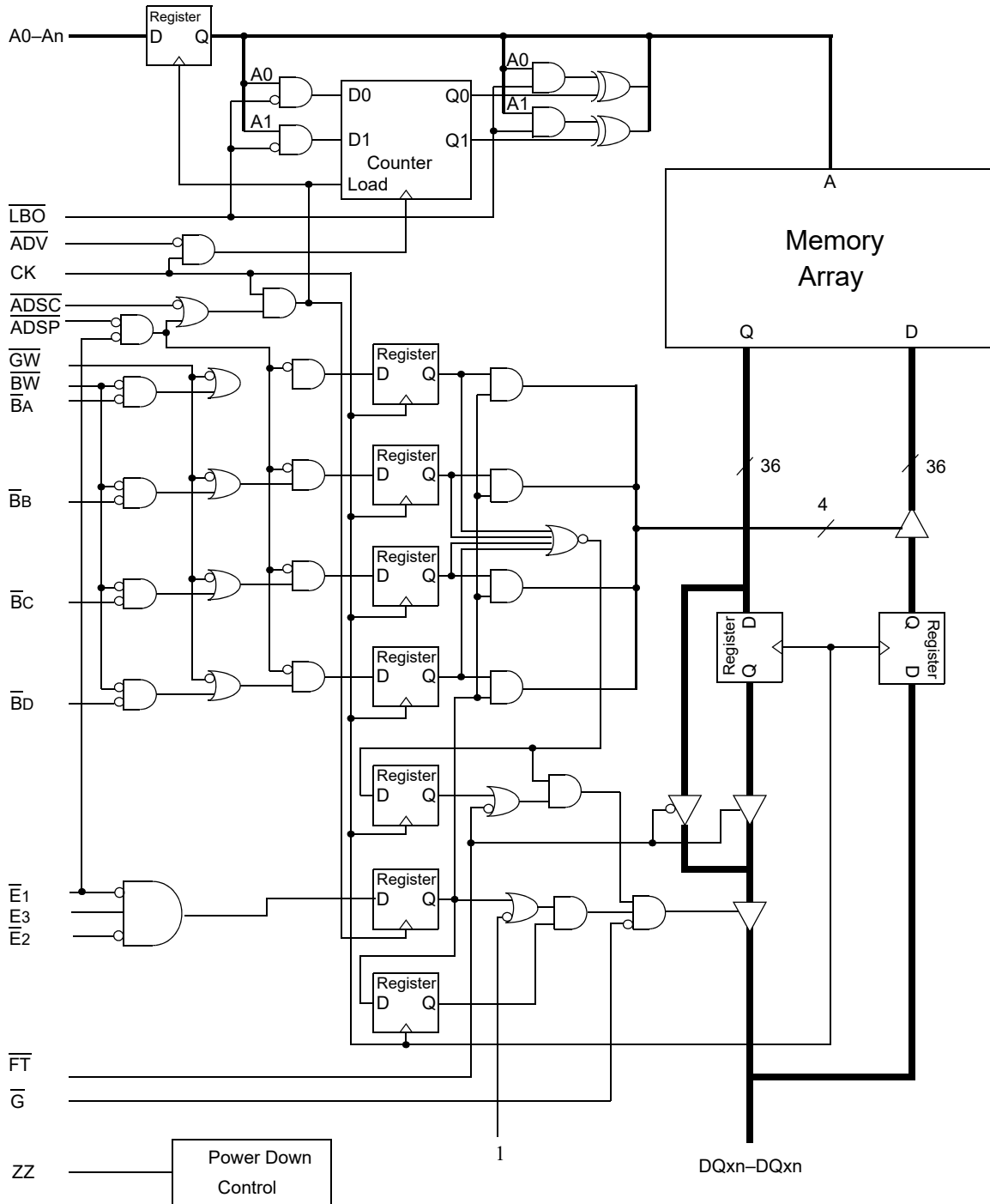
## GS84036C Pad Out—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
B	NC	E <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	$\overline{\text{E}}_3$	NC
C	NC	A	A	V <sub>DD</sub>	A	A	NC
D	DQc	DQPc	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQPb	DQb
E	DQc	DQc	V <sub>SS</sub>	$\overline{\text{E}}_1$	V <sub>SS</sub>	DQb	DQb
F	V <sub>DDQ</sub>	DQc	V <sub>SS</sub>	$\overline{\text{G}}$	V <sub>SS</sub>	DQb	V <sub>DDQ</sub>
G	DQc2	DQc	$\overline{\text{B}}_c$	$\overline{\text{ADV}}$	$\overline{\text{B}}_b$	DQb	DQb2
H	DQc	DQc	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQb	DQb
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQd	DQd	V <sub>SS</sub>	CK	V <sub>SS</sub>	DQA	DQA
L	DQd	DQd	$\overline{\text{B}}_d$	NC	$\overline{\text{B}}_a$	DQA	DQA
M	V <sub>DDQ</sub>	DQd	V <sub>SS</sub>	$\overline{\text{BW}}$	V <sub>SS</sub>	DQA	V <sub>DDQ</sub>
N	DQd	DQd	V <sub>SS</sub>	A <sub>1</sub>	V <sub>SS</sub>	DQA	DQA
P	DQd	DQPd	V <sub>SS</sub>	A <sub>0</sub>	V <sub>SS</sub>	DQPA	DQA
R	NC	A	$\overline{\text{LBO}}$	V <sub>DD</sub>	$\overline{\text{FT}}$	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V <sub>DDQ</sub>	NC	NC	NC	NC	NC	V <sub>DDQ</sub>

## BGA Pin Description

Symbol	Type	Description
A <sub>0</sub> , A <sub>1</sub>	I	Address field LSBs and Address Counter Preset Inputs
A	I	Address Inputs
$\overline{B}_A$	In	Byte Write signal for data inputs DQ <sub>A</sub> ; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ <sub>B</sub> ; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ <sub>C</sub> ; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ <sub>D</sub> ; active low
CK	I	Clock Input Signal; active high
$\overline{B}W$	I	Byte Write—Writes all enabled bytes; active low
$\overline{G}W$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1, \overline{E}_3$	I	Chip Enable; active low
$\overline{E}_2$	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
$\overline{A}DV$	I	Burst address counter advance enable; active low
$\overline{A}DSP, \overline{A}DSC$	I	Address Strobe (Processor, Cache Controller); active low
DQ <sub>A</sub>	I/O	Byte A Data Input and Output pins
DQ <sub>B</sub>	I/O	Byte B Data Input and Output pins
DQ <sub>C</sub>	I/O	Byte C Data Input and Output pins
DQ <sub>D</sub>	I/O	Byte D Data Input and Output pins
DQP <sub>A</sub>	I/O	9th Data I/O Pin; Byte A
DQP <sub>B</sub>	I/O	9th Data I/O Pin; Byte B
DQP <sub>C</sub>	I/O	9th Data I/O Pin; Byte C
DQP <sub>D</sub>	I/O	9th Data I/O Pin; Byte D
ZZ	I	Sleep Mode control; active high
$\overline{F}T$	I	Flow Through or Pipeline mode; active low
$\overline{L}BO$	I	Linear Burst Order mode; active low
V <sub>DD</sub>	I	Core power supply
V <sub>SS</sub>	I	I/O and Core Ground
V <sub>DDO</sub>	I	Output driver power supply
NC	-	No Connect

GS84018/32/36C Block Diagram



Note: Only x36 version shown for simplicity.

## Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

**Note:**

There is a pull-up device on the  $\overline{\text{FT}}$  pin and a pull-down device on the ZZ pin, so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

## Burst Counter Sequences

### Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

**Note:**

The burst counter wraps to initial state on the 5th clock.

### Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

**Note:**

The burst counter wraps to initial state on the 5th clock.

## Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{BA}$	$\overline{BB}$	$\overline{BC}$	$\overline{BD}$	Notes
Read	H	H	X	X	X	X	1
Write No Bytes	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

## Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs,  $\overline{BA}$ ,  $\overline{BB}$ ,  $\overline{BC}$  and/or  $\overline{BD}$ .
2. Byte Write Enable inputs  $\overline{BA}$ ,  $\overline{BB}$ ,  $\overline{BC}$  and/or  $\overline{BD}$  may be used in any combination with  $\overline{BW}$  to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "c" and "d" are only available on the x32 and x36 versions.



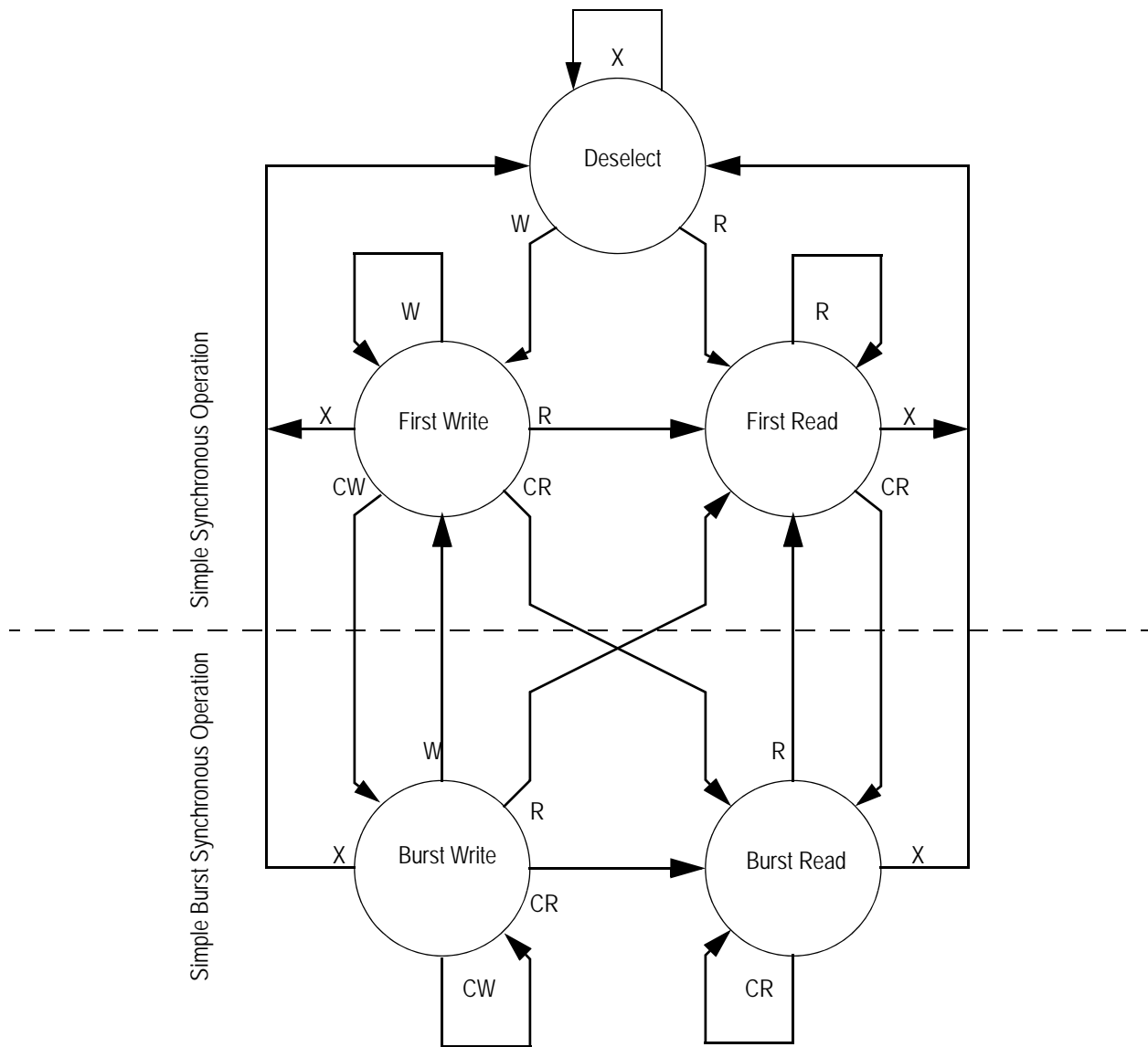
## Synchronous Truth Table

Operation	Address Used	State Diagram Key	$\bar{E}_1$	E2	$\bar{E}_3$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\bar{W}$	DQ <sup>3</sup>
Deselect Cycle, Power Down	None	X	L	X	H	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	L	X	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	X	H	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	L	X	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	H	X	X	X	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	H	L	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	H	L	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	H	L	H	L	X	T	D
<i>Read Cycle, Continue Burst</i>	<i>Next</i>	<i>CR</i>	<i>X</i>	<i>X</i>	<i>X</i>	<i>H</i>	<i>H</i>	<i>L</i>	<i>F</i>	<i>Q</i>
Read Cycle, Continue Burst	Next	CR	H	X	X	X	H	L	F	Q
<i>Write Cycle, Continue Burst</i>	<i>Next</i>	<i>CW</i>	<i>X</i>	<i>X</i>	<i>X</i>	<i>H</i>	<i>H</i>	<i>L</i>	<i>T</i>	<i>D</i>
Write Cycle, Continue Burst	Next	CW	H	X	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	X	H	H	T	D

## Notes:

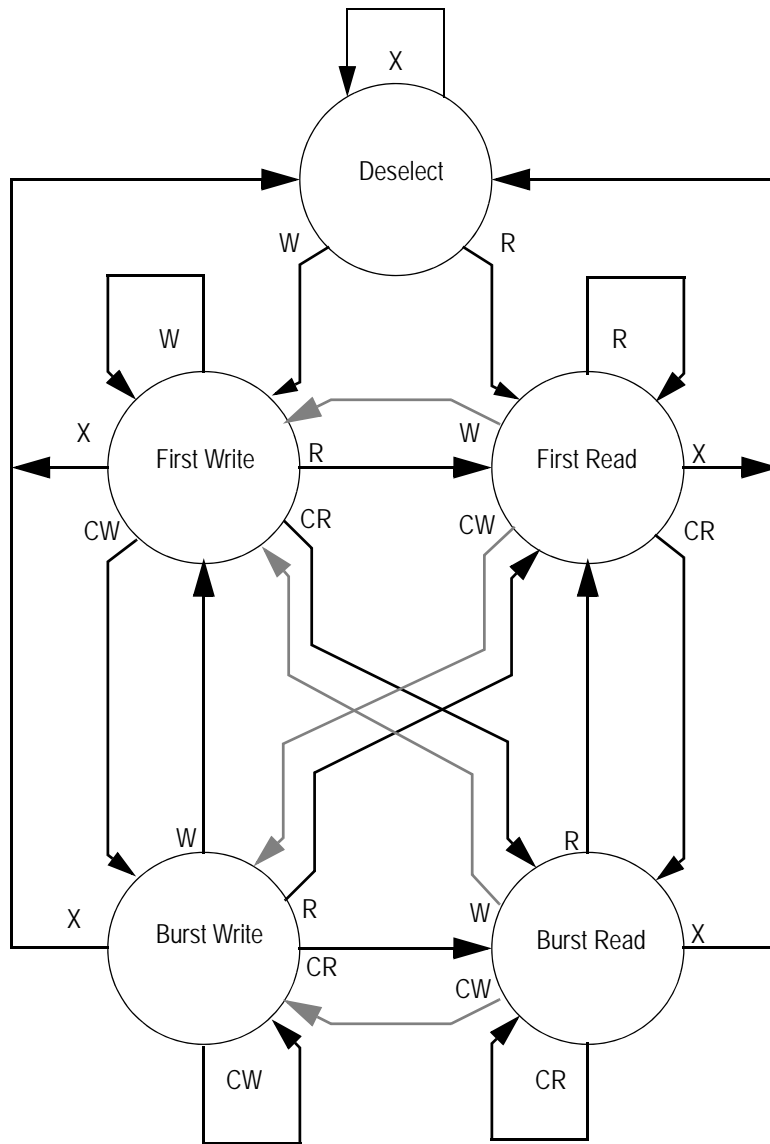
1. X = Don't Care, H = High, L = Low
2. E = T (True) if E<sub>2</sub> = 1 and  $\bar{E}_1 = \bar{E}_3 = 0$ ; E = F (False) if E<sub>2</sub> = 0 or  $\bar{E}_1 = 1$  or  $\bar{E}_3 = 1$
3.  $\bar{W}$  = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4.  $\bar{G}$  is an asynchronous input.  $\bar{G}$  can be driven high at any time to disable active output drivers.  $\bar{G}$  low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying  $\overline{ADSP}$  high and  $\overline{ADSC}$  low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying  $\overline{ADSP}$  high and  $\overline{ADV}$  low while using  $\overline{ADSC}$  to load new addresses allows simple burst operations. See *ITALIC* items above.

## Simplified State Diagram



## Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes  $\overline{G}$  is tied Low.
2. The upper portion of the diagram assumes active use of only the Enable ( $\overline{E}_1, E_2, \overline{E}_3$ ) and Write ( $\overline{B}_A, \overline{B}_B, \overline{B}_C, \overline{B}_D, \overline{B}_W$  and  $\overline{G}_W$ ) control inputs and that  $\overline{ADSP}$  is tied high and  $\overline{ADSC}$  is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write and  $\overline{ADSC}$  control inputs and assumes  $\overline{ADSP}$  is tied high and  $\overline{ADV}$  is tied low.

Simplified State Diagram with  $\overline{G}$ 

**Notes:**

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of  $\overline{G}$ .
2. Use of "Dummy Reads" (Read Cycles with  $\overline{G}$  High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume  $\overline{G}$  has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

## Absolute Maximum Ratings

(All voltages reference to  $V_{SS}$ )

Symbol	Description	Value	Unit
$V_{DD}$	Voltage on $V_{DD}$ Pins	-0.5 to 4.6	V
$V_{DDQ}$	Voltage in $V_{DDQ}$ Pins	-0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 4.6$ V max.)	V
$V_{IN}$	Voltage on Other Input Pins	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
$I_{IN}$	Input Current on Any Pin	+/-20	mA
$I_{OUT}$	Output Current on Any I/O Pin	+/-20	mA
$P_D$	Package Power Dissipation	1.5	W
$T_{STG}$	Storage Temperature	-55 to 125	$^{\circ}C$
$T_{BIAS}$	Temperature Under Bias	-55 to 125	$^{\circ}C$

### Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

## Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3 V Supply Voltage	$V_{DD3}$	3.0	3.3	3.6	V
2.5 V Supply Voltage	$V_{DD2}$	2.3	2.5	2.7	V
3.3 V $V_{DDQ}$ I/O Supply Voltage	$V_{DDQ3}$	3.0	3.3	3.6	V
2.5 V $V_{DDQ}$ I/O Supply Voltage	$V_{DDQ2}$	2.3	2.5	2.7	V

## $V_{DD3}$ Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	$V_{IH}$	2.0	—	$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

### Note:

$V_{IHQ}$  (max) is voltage on  $V_{DDQ}$  pins plus 0.3 V.

## V<sub>DD2</sub> Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V <sub>IH</sub>	0.6*V <sub>DD</sub>	—	V <sub>DD</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.3*V <sub>DD</sub>	V

**Note:**

V<sub>IHQ</sub> (max) is voltage on V<sub>DDQ</sub> pins plus 0.3 V.

## Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Temperature (Commercial Range Versions)	T <sub>A</sub>	0	25	70	°C
Ambient Temperature (Industrial Range Versions)*	T <sub>A</sub>	-40	25	85	°C

**Note:**

\* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

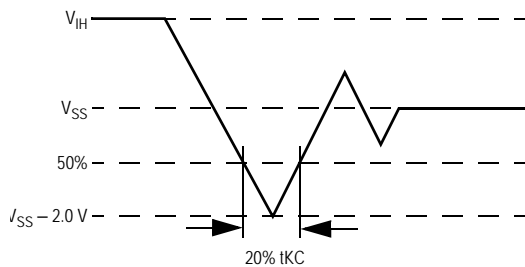
## Thermal Impedance

Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
119 BGA	4-layer	28.0	24.8	23.7	17.4	8.3

**Notes:**

1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

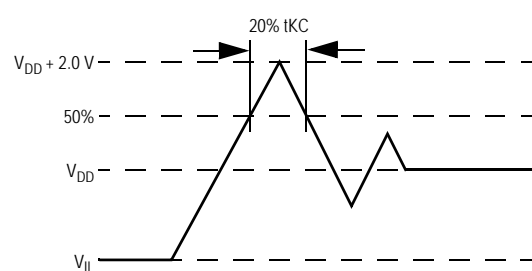
### Undershoot Measurement and Timing



**Note:**

Input Under/overshoot voltage must be -2 V > V<sub>i</sub> < V<sub>DDn</sub>+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t<sub>KC</sub>.

### Overshoot Measurement and Timing



## Capacitance

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{DD} = 2.5\text{ V}$ )

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0\text{ V}$	6	7	pF

### Note:

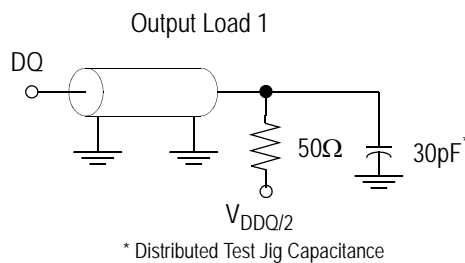
These parameters are sample tested.

## AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	$0.2\text{ V}$
Input slew rate	$1\text{ V/ns}$
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	Fig. 1

### Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Device is deselected as defined by the Truth Table.



## DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	$I_{IL}$	$V_{IN} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
ZZ Input Current	$I_{IN1}$	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0 V \leq V_{IN} \leq V_{IH}$	-1 $\mu$ A -1 $\mu$ A	1 $\mu$ A 100 $\mu$ A
$\overline{FT}$ , SCD, ZQ Input Current	$I_{IN2}$	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0 V \leq V_{IN} \leq V_{IL}$	-100 $\mu$ A -1 $\mu$ A	1 $\mu$ A 1 $\mu$ A
Output Leakage Current	$I_{OL}$	Output Disable, $V_{OUT} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
Output High Voltage	$V_{OH2}$	$I_{OH} = -8$ mA, $V_{DDQ} = 2.375$ V	1.7 V	—
Output High Voltage	$V_{OH3}$	$I_{OH} = -8$ mA, $V_{DDQ} = 3.135$ V	2.4 V	—
Output Low Voltage	$V_{OL}$	$I_{OL} = 8$ mA	—	0.4 V

## Operating Currents

Parameter	Test Conditions	Mode	Symbol	-250		-200		-166		-150		Unit	
				0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C		
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x32/ x36)	Pipeline	$I_{DD}$ $I_{DDQ}$	195 30	215 30	170 25	190 25	160 25	180 25	140 20	160 20	mA
			Flow Through	$I_{DD}$ $I_{DDQ}$	155 25	175 25	140 20	160 20	135 20	155 20	130 15	150 15	mA
		(x18)	Pipeline	$I_{DD}$ $I_{DDQ}$	180 15	200 15	155 15	175 15	140 10	160 10	130 10	150 10	mA
			Flow Through	$I_{DD}$ $I_{DDQ}$	145 15	165 15	130 10	150 10	125 15	145 15	120 8	140 8	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	$I_{SB}$	25	45	25	45	25	45	25	45	mA
			Flow Through	$I_{SB}$	25	45	25	45	25	45	25	45	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	$I_{DD}$	65	85	65	85	65	85	60	80	mA
			Flow Through	$I_{DD}$	65	85	65	85	65	85	60	80	mA

## AC Electrical Characteristics

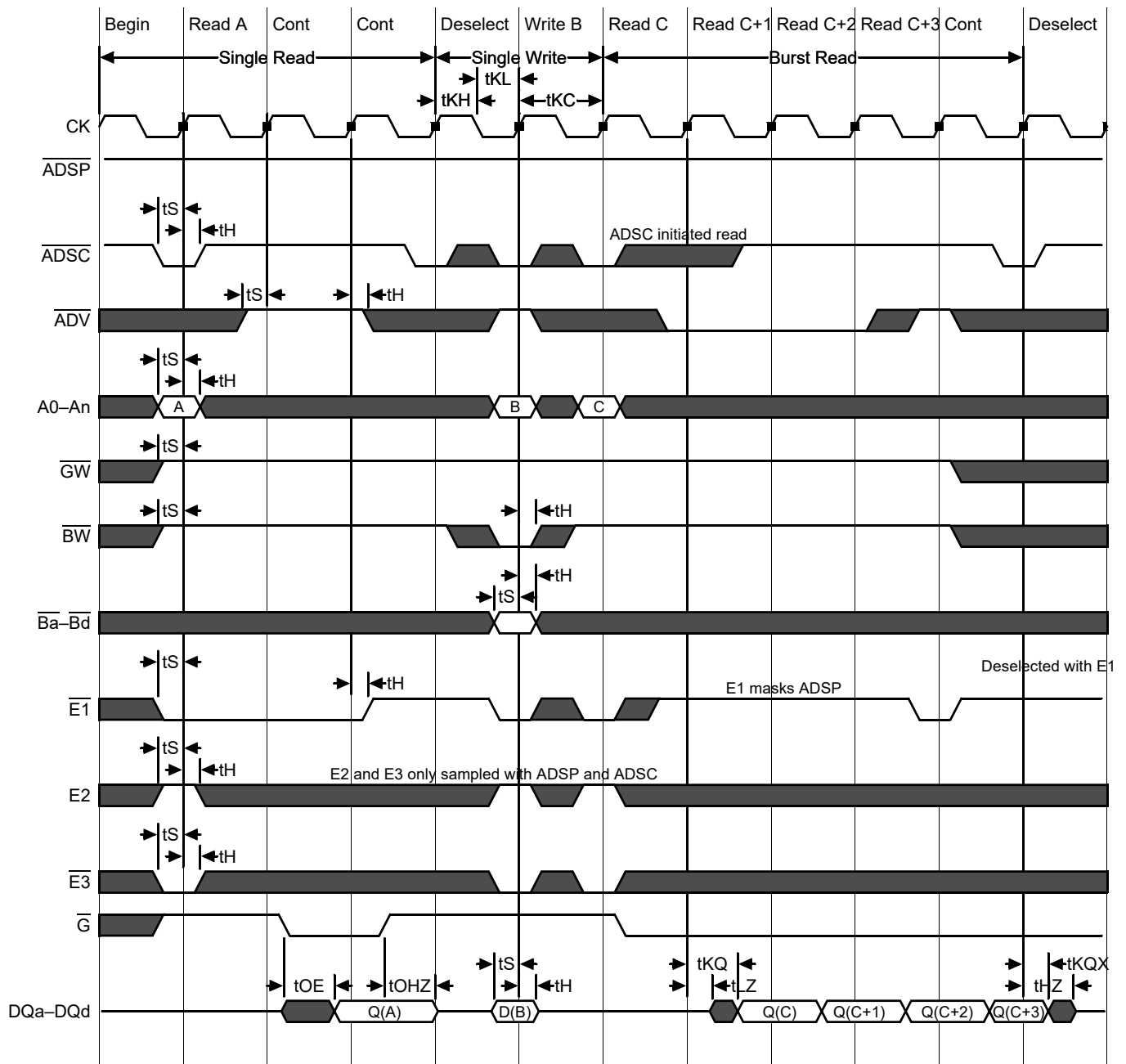
	Parameter	Symbol	-250		-200		-166		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	t <sub>KC</sub>	4.0	—	5.5	—	6.0	—	6.7	—	ns
	Clock to Output Valid	t <sub>KQ</sub>	—	2.5	—	3.0	—	3.5	—	3.8	ns
	Clock to Output Invalid	t <sub>KQX</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	t <sub>lZ</sub> <sup>1</sup>	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	t <sub>S</sub>	1.2	—	1.4	—	1.5	—	1.5	—	ns
	Hold time	t <sub>H</sub>	0.2	—	0.4	—	0.5	—	0.5	—	ns
Flow Through	Clock Cycle Time	t <sub>KC</sub>	5.5	—	6.5	—	7.0	—	7.5	—	ns
	Clock to Output Valid	t <sub>KQ</sub>	—	5.5	—	6.5	—	7.0	—	7.5	ns
	Clock to Output Invalid	t <sub>KQX</sub>	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	t <sub>lZ</sub> <sup>1</sup>	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Setup time	t <sub>S</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t <sub>H</sub>	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	t <sub>KH</sub>	1.3	—	1.3	—	1.3	—	1.3	—	ns
	Clock LOW Time	t <sub>KL</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in High-Z	t <sub>hZ</sub> <sup>1</sup>	1.5	2.5	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\bar{G}$ to Output Valid	t <sub>OE</sub>	—	2.5	—	3.0	—	3.5	—	3.8	ns
	$\bar{G}$ to output in Low-Z	t <sub>OLZ</sub> <sup>1</sup>	0	—	0	—	0	—	0	—	ns
	$\bar{G}$ to output in High-Z	t <sub>OHZ</sub> <sup>1</sup>	—	2.5	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	t <sub>ZZS</sub> <sup>2</sup>	5	—	5	—	5	—	5	—	ns
	ZZ hold time	t <sub>ZZH</sub> <sup>2</sup>	1	—	1	—	1	—	1	—	ns
	ZZ recovery	t <sub>ZZR</sub>	20	—	20	—	20	—	20	—	ns

## Notes:

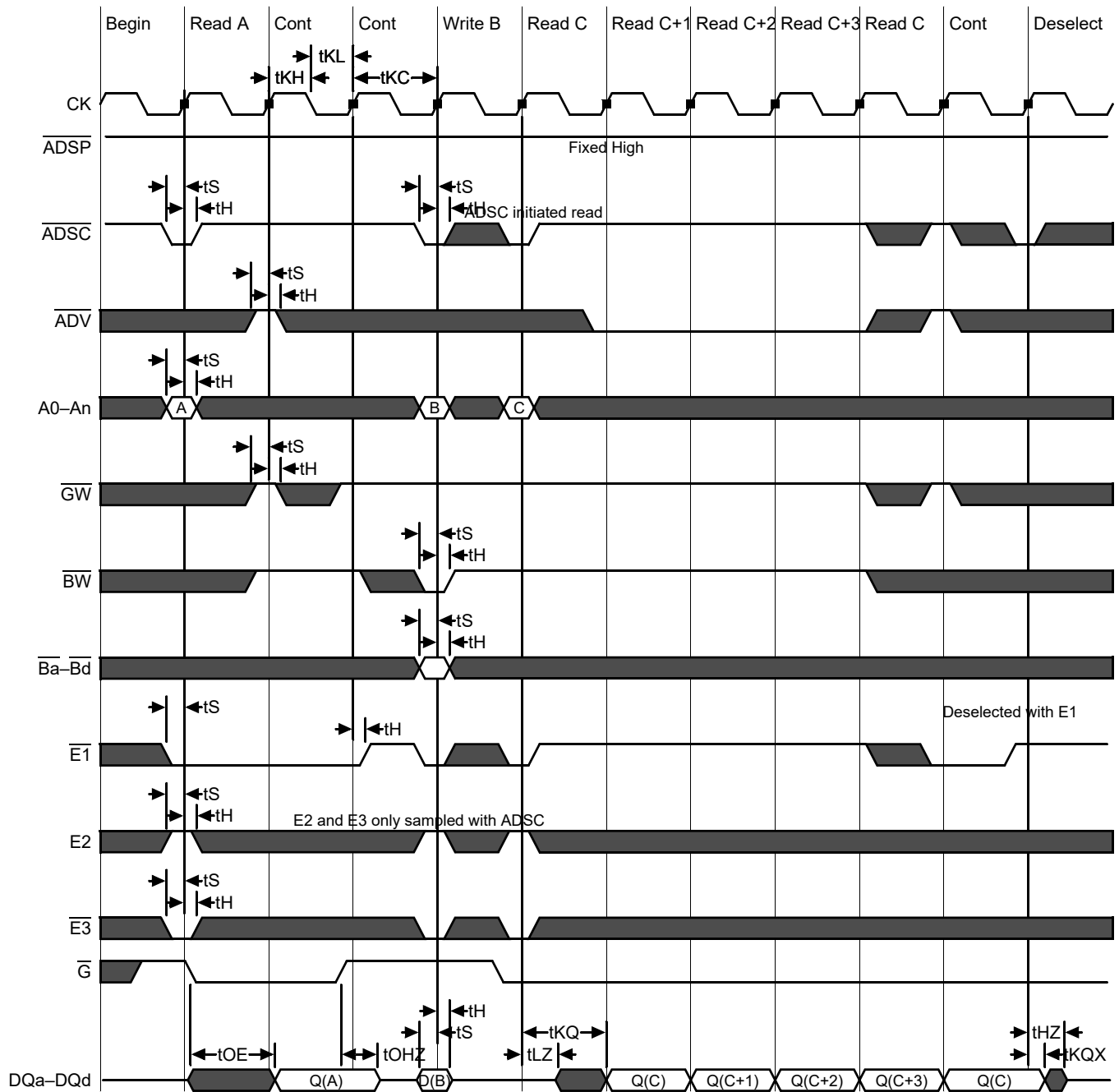
1. These parameters are sampled and are not 100% tested
2. ZZ is an asynchronous signal. However, In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.



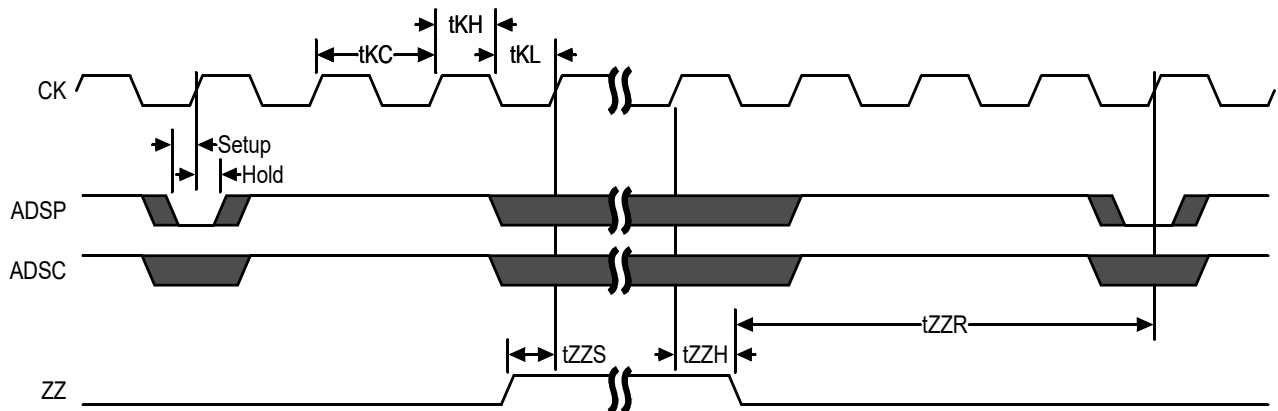
## Pipeline Mode Timing



## Flow Through Mode Timing



## Sleep Mode Timing Diagram

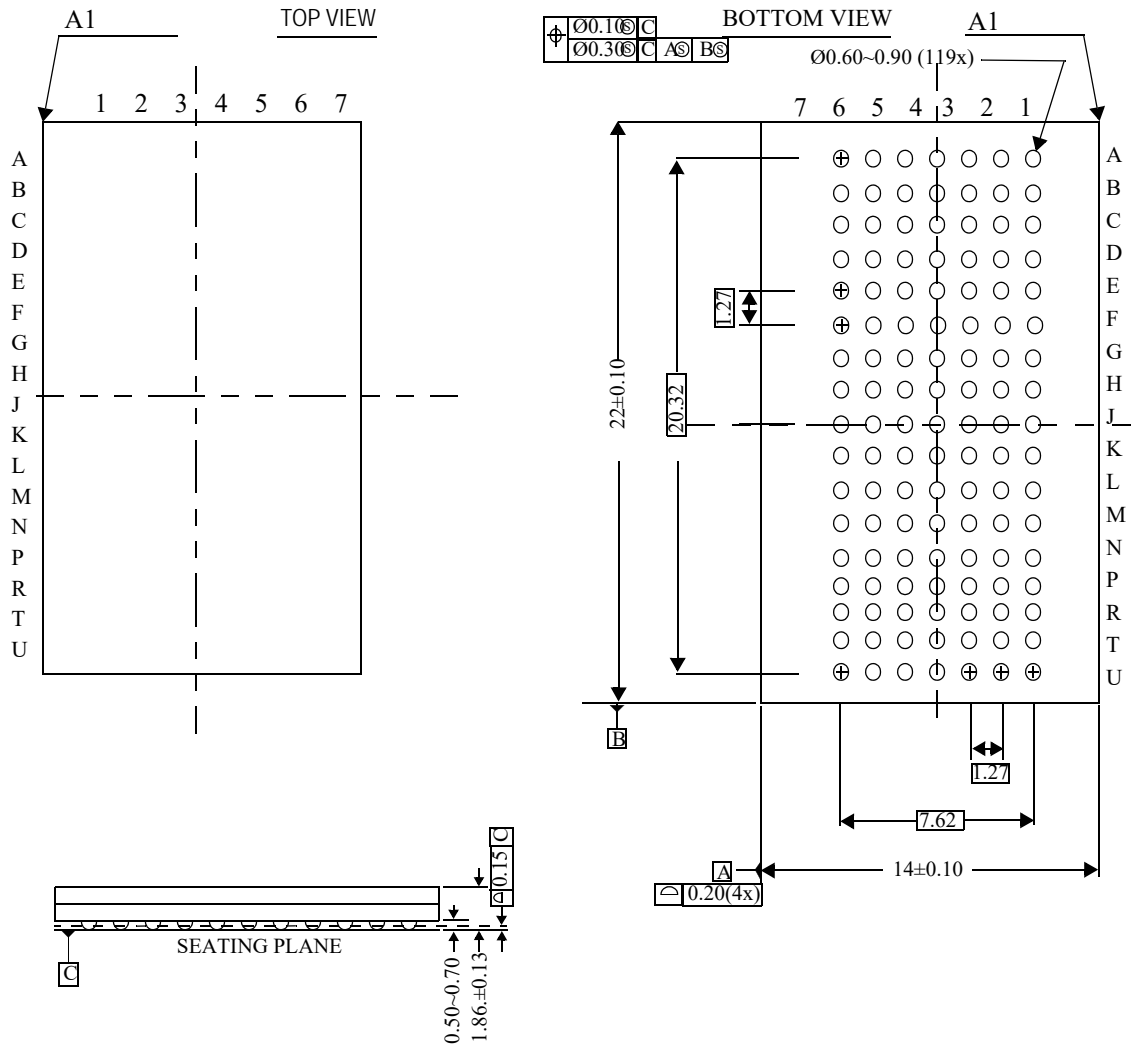


## Application Tips

## Single and Dual Cycle Deselect

SCD devices force the use of “dummy read cycles” (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

Package Dimensions—119-Bump FPBGA (Package B, Variation 2)



## Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number <sup>1</sup>	Type	Package	Speed <sup>2</sup> (MHz/ns)	T <sub>A</sub> <sup>3</sup>
256K x 18	GS84018CB-250	Pipeline/Flow Through	119 BGA (var. 1)	250/6.5	C
256K x 18	GS84018CB-200	Pipeline/Flow Through	119 BGA (var. 1)	200/6.5	C
256K x 18	GS84018CB-166	Pipeline/Flow Through	119 BGA (var. 1)	166/7.0	C
256K x 18	GS84018CB-150	Pipeline/Flow Through	119 BGA (var. 1)	150/7.5	C
128K x 32	GS84032CB-250	Pipeline/Flow Through	119 BGA (var. 1)	250/6.5	C
128K x 32	GS84032CB-200	Pipeline/Flow Through	119 BGA (var. 1)	200/6.5	C
128K x 32	GS84032CB-166	Pipeline/Flow Through	119 BGA (var. 1)	166/7.0	C
128K x 32	GS84032CB-150	Pipeline/Flow Through	119 BGA (var. 1)	150/7.5	C
128K x 36	GS84036CB-250	Pipeline/Flow Through	119 BGA (var. 1)	250/6.5	C
128K x 36	GS84036CB-200	Pipeline/Flow Through	119 BGA (var. 1)	200/6.5	C
128K x 36	GS84036CB-166	Pipeline/Flow Through	119 BGA (var. 1)	166/7.0	C
128K x 36	GS84036CB-150	Pipeline/Flow Through	119 BGA (var. 1)	150/7.5	C
256K x 18	GS84018CB-250I	Pipeline/Flow Through	119 BGA (var. 1)	250/6.5	I
256K x 18	GS84018CB-200I	Pipeline/Flow Through	119 BGA (var. 1)	200/6.5	I
256K x 18	GS84018CB-166I	Pipeline/Flow Through	119 BGA (var. 1)	166/7.0	I
256K x 18	GS84018CB-150I	Pipeline/Flow Through	119 BGA (var. 1)	150/7.5	I
128K x 32	GS84032CB-250I	Pipeline/Flow Through	119 BGA (var. 1)	250/6.5	I
128K x 32	GS84032CB-200I	Pipeline/Flow Through	119 BGA (var. 1)	200/6.5	I
128K x 32	GS84032CB-166I	Pipeline/Flow Through	119 BGA (var. 1)	166/7.0	I
128K x 32	GS84032CB-150I	Pipeline/Flow Through	119 BGA (var. 1)	150/7.5	I
128K x 36	GS84036CB-250I	Pipeline/Flow Through	119 BGA (var. 1)	250/6.5	I
128K x 36	GS84036CB-200I	Pipeline/Flow Through	119 BGA (var. 1)	200/6.5	I
128K x 36	GS84036CB-166I	Pipeline/Flow Through	119 BGA (var. 1)	166/7.0	I
128K x 36	GS84036CB-150I	Pipeline/Flow Through	119 BGA (var. 1)	150/7.5	I
256K x 18	GS84018CGB-250	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	250/6.5	C
256K x 18	GS84018CGB-200	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	200/6.5	C
256K x 18	GS84018CGB-166	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	166/7.0	C
256K x 18	GS84018CGB-150	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	150/7.5	C
128K x 32	GS84032CGB-250	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	250/6.5	C
128K x 32	GS84032CGB-200	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	200/6.5	C

**Notes:**

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS84032CB-250T.
- The speed column indicates the cycle frequency (MHz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
- C = Commercial Temperature Range. I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site ([www.gsistechnology.com](http://www.gsistechnology.com)) for a complete listing of current offerings.

**Ordering Information for GSI Synchronous Burst RAMs (Continued)**

Org	Part Number <sup>1</sup>	Type	Package	Speed <sup>2</sup> (MHz/ns)	T <sub>A</sub> <sup>3</sup>
128K x 32	GS84032CGB-166	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	166/7.0	C
128K x 32	GS84032CGB-150	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	150/7.5	C
128K x 36	GS84036CGB-250	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	250/6.5	C
128K x 36	GS84036CGB-200	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	200/6.5	C
128K x 36	GS84036CGB-166	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	166/7.0	C
128K x 36	GS84036CGB-150	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	150/7.5	C
256K x 18	GS84018CGB-250I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	250/6.5	I
256K x 18	GS84018CGB-200I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	200/6.5	I
256K x 18	GS84018CGB-166I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	166/7.0	I
256K x 18	GS84018CGB-150I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	150/7.5	I
128K x 32	GS84032CGB-250I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	250/6.5	I
128K x 32	GS84032CGB-200I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	200/6.5	I
128K x 32	GS84032CGB-166I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	166/7.0	I
128K x 32	GS84032CGB-150I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	150/7.5	I
128K x 36	GS84036CGB-250I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	250/6.5	I
128K x 36	GS84036CGB-200I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	200/6.5	I
128K x 36	GS84036CGB-166I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	166/7.0	I
128K x 36	GS84036CGB-150I	Pipeline/Flow Through	RoHS-compliant 119 BGA (var. 1)	150/7.5	I

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## 9Mb Sync SRAM Datasheet Revision History

File Name	Types of Changes Format or Content	Revisions
840xxCB_r1		<ul style="list-style-type: none"><li>• Creation of new datasheet</li></ul>
840xxCB_r1_01	Content	<ul style="list-style-type: none"><li>• Updated with new speed bins</li><li>• (Rev1.01a: Updated core power supply in Features on pg 1)</li></ul>



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