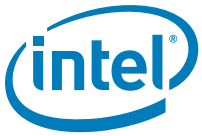
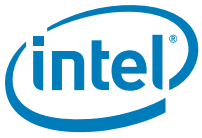


Intel® Ethernet Network Connection I347-AT4 Datasheet

May 2012

Revision 2.2



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Revision History

Rev	Date	Comments
2.2	May 2012	Added Thermal Design Recommendations.
2.1	March 2012	Added power consumption table to section 5.2.
2.0[1]	December 2011	Changed 1.8V power rail to 1.9V. Updated the pin interface section (added RCLK1, RCLK2, and SCLK). Initial public release.
0.75	April 2011	Added clocking source descriptions (Recovered Clock and Reference Clock Select).
0.7	February 2011	Added I347-AT4 SGMII-to-copper dual-port mode details.
0.6	November 2010	Major revision (all sections).
0.5	September 2010	Initial Release (Intel Confidential).

1. No releases between revision 0.75 and 2.0.

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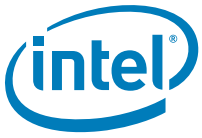
Contents



1.0 Introduction

The Intel® Ethernet Network Connection I347-AT4 (I347-AT4) quad, single-chip device contains four independent Gigabit Ethernet (GbE) transceivers on a single monolithic Integrated Circuit (IC) that supports SGMII on the MAC interface in an SGMII-to-copper application. Each transceiver performs all the Physical Layer (PHY) functions for 100BASE-TX and 1000BASE-T full- or half-duplex Ethernet on a CAT 5 twisted pair cable, and 10BASE-T full- or half-duplex Ethernet on a CAT 3, 4, and 5 cable.

Note: The I347-AT4 can also operate in dual-port mode. When set by the MAC, the I347-AT4 uses two independent GbE transceivers (Port 0 and Port 1) in an SGMII-to-copper application.

The I347-AT4 integrates MDI interface termination resistors and capacitors into the PHY. This resistor integration simplifies board layout and lowers board cost by reducing the number of external components. The new calibrated resistor scheme achieves and exceeds the accuracy requirements of the IEEE 802.3 return loss specifications.

The I347-AT4 consumes less than 500 mW per port; thereby, reducing overall system cost by eliminating heat-sink and reducing air-flow requirements.

The I347-AT4 is fully compliant with the IEEE 802.3 standard. It includes the PMD, PMA, and PCS sublayers and performs:

- PAM5, 8B/10B, 4B/5B, MLT-3, NRZI, and Manchester encoding/decoding
- Digital clock/data recovery
- Stream cipher scrambling/descrambling
- Digital adaptive equalization for the receiver data path as well as digital filtering for pulse-shaping for the line transmitter
- Auto-negotiation and management functions.

The I347-AT4 also supports auto-MDI/MDIX at all three speeds to enable easier installation and reduce installation costs.

The I347-AT4 uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit-per-second data rate. The I347-AT4 dissipates very low power while achieving robust performance in noisy environments.

In addition, the I347-AT4 supports a cable tester feature that enables fault detection and advanced cable performance monitoring.

The I347-AT4 is available in a 15 mm x 15 mm, 196-pin TFBGA package.

1.1 I347-AT4 Features

- Two or four ports SGMII-to-copper (see Figure 1 and Figure 2)
- Integrated MDI interface termination resistors and capacitors
- Low power consumption (< 500 mW per port)
- Integrated cable diagnostic feature
- Downshift mode for two-pair cable installations
- Supports up to four LEDs per port programmable to indicate link, speed, duplex, and activity functions
- Supports Advance Power Management (APM) modes for significant power savings
- Automatic MDI/MDIX crossover for all three speeds of operation (10/100/1000BASE-T)
- Automatic polarity correction
- 25 MHz clock input option
- Loopback mode for diagnostics
- Supports IEEE 1149.1 JTAG and 1149.6 AC JTAG
- Available in RoHS 6 and Halogen Free packages
- Manufactured in a 15 x 15 mm 196-pin TFBGA package

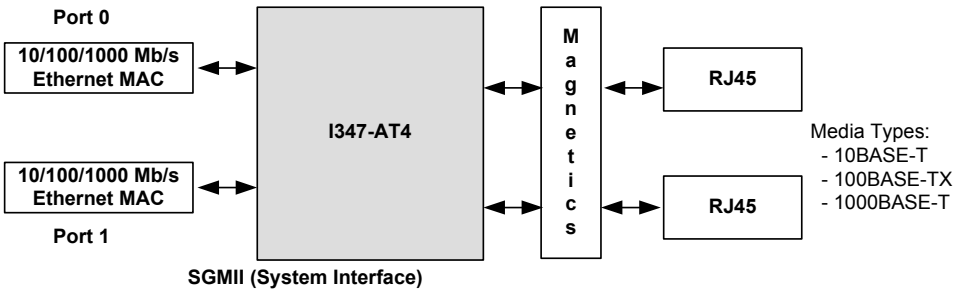


Figure 1. SGMII (System) to Copper — Dual Port Mode

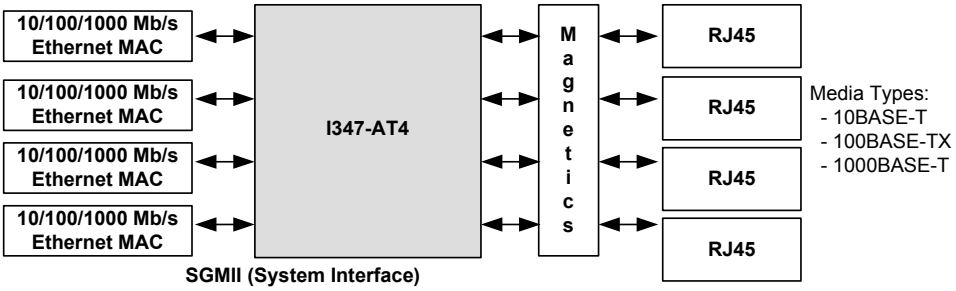


Figure 2. SGMII (System) to Copper — Quad Port Mode

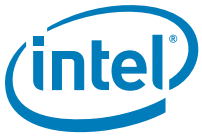
2.0 Pin Interface

2.1 Pin Assignment

The I347-AT4 is manufactured in a 15 x 15 mm 196-pin TFBGA package.

2.1.1 Signal Type Definitions

Signal Type	Definition
H	Input with hysteresis
I/O	Input/output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open-drain output
Z	Tri-state output
mA	DC sink capability



2.1.2 Media Dependent Interface

Table 1. Media Dependent Interface Port 0

Pin #	Pin Name	Pin Type	Description
N3 P3	P0_MDIP[0] P0_MDIN[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. Unused MDI pins must be left floating. The I347-AT4 contains an internal 100 Ω resistor between the MDIP/N[0] pins.
N4 P4	P0_MDIP[1] P0_MDIN[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. Unused MDI pins must be left floating. The I347-AT4 contains an internal 100 Ω resistor between the MDIP/N[1] pins.
P5 N5	P0_MDIP[2] P0_MDIN[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. Unused MDI pins must be left floating. The I347-AT4 contains an internal 100 Ω resistor between the MDIP/N[2] pins.
M5 M6	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. Unused MDI pins must be left floating. The I347-AT4 contains an internal 100 Ω resistor between the MDIP/N[3] pins.

Table 2. Media Dependent Interface Port 1

Pin #	Pin Name	Pin Type	Description
M8 M7	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface[0] for Port 1. Refer to P0_MDI[0]P/N.
N8 P8	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface[1] for Port 1. Refer to P0_MDI[1]P/N.
N7 P7	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface[2] for Port 1. Refer to P0_MDI[2]P/N.
N6 P6	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface[3] for Port 1. Refer to P0_MDI[3]P/N.

Table 3. Media Dependent Interface Port 2

Pin #	Pin Name	Pin Type	Description
P9 N9	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface[0] for Port 2. Refer to P0_MDI[0]P/N.
P10 N10	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface[1] for Port 2. Refer to P0_MDI[1]P/N.
P11 N11	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface[2] for Port 2. Refer to P0_MDI[2]P/N.
M9 M10	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface[3] for Port 2. Refer to P0_MDI[3]P/N.

Table 4. Media Dependent Interface Port 3

Pin #	Pin Name	Pin Type	Description
N14 P14	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface[0] for Port 3. Refer to P0_MDI[0]P/N.
M12 M11	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface[1] for Port 3. Refer to P0_MDI[1]P/N.
N13 P13	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface[2] for Port 3. Refer to P0_MDI[2]P/N.
N12 P12	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface[3] for Port 3. Refer to P0_MDI[3]P/N.

2.1.3 SGMI

Table 5. SGMII Interface Port 0

Pin #	Pin Name	Pin Type	Description
B1 A1	P0_S_INP P0_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
B2 A2	P0_S_OUTP P0_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 6. SGMII Interface Port 1

Pin #	Pin Name	Pin Type	Description
A4 B4	P1_S_INP P1_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
A3 B3	P1_S_OUTP P1_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

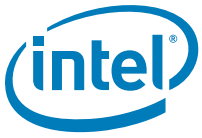


Table 7. SGMII Interface Port 2

Pin #	Pin Name	Pin Type	Description
A11 B11	P2_S_INP P2_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
A12 B12	P2_S_OUTP P2_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 8. SGMII Interface Port 3

Pin #	Pin Name	Pin Type	Description
B14 A14	P3_S_INP P3_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
B13 A13	P3_S_OUTP P3_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

2.1.4 Reserved Pins

Pin #	Pin Name	Pin Type	Description
B9 A9	RSVD_NC RSVD_NC	I	Reserved, do not connect.
A8 B8	RSVD_NC RSVD_NC	O	Reserved, do not connect.

2.1.5 Management/Control

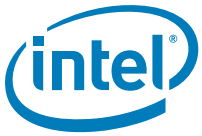
Pin #	Pin Name	Pin Type	Description
B6	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12 MHz.
A6	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 KΩ to 10 KΩ.
D2	INTn	OD	Interrupt pin. The pull-up resistor used for the INTn must be connected to the VDDOL level. The pull-up resistor should not be connected to voltage higher than VDDOL.

2.1.6 LED

Pin #	Pin Name	Pin Type	Description
F2 E1 E2 D1	P0_LED[3] P0_LED[2] P0_LED[1] P0_LED[0]	O	Parallel LED Output port 0.
H1 G1 G2 F1	P1_LED[3] P1_LED[2] P1_LED[1] P1_LED[0]	O	Parallel LED Output port 1.
K2 K1 J1 H2	P2_LED[3] P2_LED[2] P2_LED[1] P2_LED[0]	O	Parallel LED Output port 2.
M2 M1 L2 L1	P3_LED[3] P3_LED[2] P3_LED[1] P3_LED[0]	O	Parallel LED Output port 3.
L3 K3 P1 N1	CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	I	Global hardware configuration. See Section 3.21 for details.
J2	V18_L	I	VDDOL voltage control. Tie to VSS = VDDOL operating at 3.3V Floating = VDDOL operating at 1.9V
E13	V18_R	I	VDDOR voltage control. Tie to VSS = VDDOR operating at 3.3V Floating = VDDOR operating at 1.9V
C7	V12_EN	I	VDDOM voltage control. Tie to VSS = VDDOM operating at 3.3V Floating = VDDOM operating at 1.9V

2.1.7 JTAG

Pin #	Pin Name	Pin Type	Description
G14	TDI	I, PU	Boundary scan test data input. TDI contains an internal 150 KΩ pull-up resistor.
G13	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 KΩ pull-up resistor.
G12	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 KΩ pull-up resistor.
E12	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 KΩ pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 KΩ pull-down resistor.
D12	TDO	O	Boundary scan test data output.



2.1.8 Master Clock/Reset

Pin #	Pin Name	Pin Type	Description
J13	XTAL_IN	I	25 MHz Clock Input 25 MHz ± 50 ppm tolerance crystal reference or oscillator input. XTAL_IN should be left floating when it is not used. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin should be ac-coupled with a 0.1 nF capacitor. No additional AC capacitor is needed if a capacitor divider is already used for level shifting.
J14	XTAL_OUT	O	25 MHz Crystal Output. 25 MHz ± 50 ppm tolerance crystal reference. XTAL_OUT should be left floating when it is not used.
D13 D14	REF_CLKP REF_CLKN	I	125 MHz/156.25 MHz Reference Clock Input Positive and Negative ± 50 ppm tolerance differential clock inputs. REF_CLKP/N are LVDS differential inputs with a 100 Ω differential internal termination resistor. If not used, REF_CLKP must be pulled high with a 1 KΩ resistor to 1.9V. If not used, REF_CLKN must be pulled to GND with a 1 KΩ resistor.
H13 H14	CLK_SEL[1] CLK_SEL[0]	I	Reference Clock Selection 00b = Reserved. 01b = Reserved. 10b = Use 25 MHz XTAL_IN/XTAL_OUT[1]. 11b = Use 25 MHz XTAL_IN/XTAL_OUT. CLK_SEL[1:0] must be connected to VDDOR for configuration high.
E3	RESETn	I	Hardware reset. XTAL_IN must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be in inactive state for normal operation. 1b = Normal operation 0b = Reset

1. See Section 3.21 for details.

2.1.9 Test

Pin #	Pin Name	Pin Type	Description
L14 L13	HSDACP HSDACN	O	AC Test Point. Positive and Negative. These pins are also used to bring out a differential TX_TCLK. Connect these pins with a 50 Ω termination resistor to VSS for IEEE testing and debug purposes. If debug and IEEE testing are not of importance, these pins can be left floating.
K13	TSTPT	O	DC Test Point. The TSTPT pin should be left floating.
C8	TSTPTF	O	DC test point. The TSTPTF pin should be left floating.
A5 B5	TEST[1] TEST[0]	I, PD	Test Control. This pin should be left floating.

2.1.10 References

Pin #	Pin Name	Pin Type	Description
K12	RSET	I	Resistor Reference External 5.0 KΩ 1% resistor connected to ground.

2.1.11 Power and Ground

Pin #	Pin Name	Pin Type	Description
E6, E7, E8, E9, F4, F11, F12, G4, G11, H4, J4	DVDD	Power	1.0V Digital Supply
D4, D5, D8, D9, D10, D11, E4, E5, E10, E11, K11, L4, L5, L6, L7, L8, L9, L10, L11	AVDDH	Power	1.9V Analog Supply.
H12	VDDC	Power	1.9V Supply[1].
D6, D7	VDDOM	Power	1.9V or 3.3V I/O Supply[2].
F13	VDDOR	Power	1.9V or 3.3V I/O Supply[3].
F3, G3, H3, J3	VDDOL	Power	1.9V or 3.3V I/O Supply[4].
A7, A10, B7, B10, C1, C2, C3, C4, C5, C6, C9, C10, C11, C12, C13, C14, D3, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, H11, J5, J6, J7, J8, J9, J10, J11, K4, K5, K6, K7, K8, K9, K10, L12, M3, M4, M13, M14, N2, P2	VSS	Ground	Ground.
J12	VSSC	Ground	Ground.

1. VDDC supplies XTAL_IN/OUT.
2. VDDOM supplies digital I/O pins for MDC, MDIO, and TEST.
3. VDDOR supplies digital I/O pins for TDO, TDI, TMS, TCK, TRSTn, REF_CLKP/N, and CLK_SEL[1:0].
4. VDDOL supplies digital I/O pins for RESETn, LED, CONFIG, and INTn.

2.1.12 Clocking

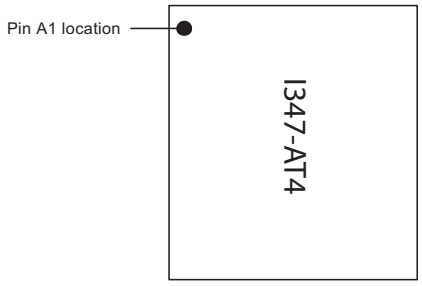
Pin #	Pin Name	Pin Type	Description
E14	RCLK1	O	25/125 MHz Gigabit Recovered Clock1. If not used pins must be left unconnected.
F14	RCLK2	O	25/125 MHz Gigabit Recovered Clock2. If not used pins must be left unconnected.
K14	SCLK	I	25 MHz input reference clock. Do not electrically short the SCLK to XTAL_IN. If not used pins must be left unconnected.

2.1.13 Pins I/O State at Various Test or Reset Modes

Pin(s)	Loopback	Software Reset	Hardware Reset	Power Down
MDI[3:0]P/N	Active	Tri-state	Tri-state	Tri-state
S_OUTP/N	Active	Internally pulled up by terminations of 50 Ω	Internally pulled up by terminations of 50 Ω	Reg. 16.3 state 0b = Internally pulled up by terminations of 50 Ω 1b = Active
MDIO	Active	Active	Tri-state	Active
INTn	Active	Tri-state	Tri-state	Tri-state
LED	Active	See Section 2.27.5	Tri-state	See Section 2.27.5
TDO	Active	Active	Active	Active

2.2 Pinouts (Top View)

2.2.1 Pin A1 Location



2.2.2 Pinouts (A1 Through P7)

	1	2	3	4	5	6	7	
A	P0_S_INN	P0_S_OUTN	P1_S_OUTP	P1_S_INP	TEST[1]	MDIO	VSS	A
B	P0_S_INP	P0_S_OUTP	P1_S_OUTN	P1_S_INN	TEST[0]	MDC	VSS	B
C	VSS	VSS	VSS	VSS	VSS	VSS	V12_EN	C
D	P0_LED[0]	INTn	VSS	AVDDH	AVDDH	VDDOM	VDDOM	D
E	P0_LED[2]	P0_LED[1]	RESETn	AVDDH	AVDDH	DVDD	DVDD	E
F	P1_LED[0]	P0_LED[3]	VDDOL	DVDD	VSS	VSS	VSS	F
G	P1_LED[2]	P1_LED[1]	VDDOL	DVDD	VSS	VSS	VSS	G
H	P1_LED[3]	P2_LED[0]	VDDOL	DVDD	VSS	VSS	VSS	H
J	P2_LED[1]	V18_L	VDDOL	DVDD	VSS	VSS	VSS	J
K	P2_LED[2]	P2_LED[3]	CONFIG[2]	VSS	VSS	VSS	VSS	K
L	P3_LED[0]	P3_LED[1]	CONFIG[3]	AVDDH	AVDDH	AVDDH	AVDDH	L
M	P3_LED[2]	P3_LED[3]	VSS	VSS	P0_MDIP[3]	P0_MDIN[3]	P1_MDIN[0]	M
N	CONFIG[0]	VSS	P0_MDIP[0]	P0_MDIP[1]	P0_MDIN[2]	P1_MDIP[3]	P1_MDIP[2]	N
P	CONFIG[1]	VSS	P0_MDIN[0]	P0_MDIN[1]	P0_MDIP[2]	P1_MDIN[3]	P1_MDIN[2]	P
	1	2	3	4	5	6	7	

2.2.3 Pinouts (A8 Through P14)

	8	9	10	11	12	13	14	
A	RSVD_NC	RSVD_NC	VSS	P2_S_INP	P2_S_OUTP	P3_S_OUTN	P3_S_INN	A
B	RSVD_NC	RSVD_NC	VSS	P2_S_INN	P2_S_OUTN	P3_S_OUTP	P3_S_INP	B
C	TSTPTF	VSS	VSS	VSS	VSS	VSS	VSS	C
D	AVDDH	AVDDH	AVDDH	AVDDH	TDO	RSVD_NC	RSVD_NC	D
E	DVDD	DVDD	AVDDH	AVDDH	TRSTn	V18_R	RCLK1	E
F	VSS	VSS	VSS	DVDD	DVDD	VDDOR	RCLK2	F
G	VSS	VSS	VSS	DVDD	TCK	TMS	TDI	G
H	VSS	VSS	VSS	VSS	VDDC	CLK_SEL[1]	CLK_SEL[0]	H
J	VSS	VSS	VSS	VSS	VSSC	XTAL_IN	XTAL_OUT	J
K	VSS	VSS	VSS	AVDDH	RSET	TSTPT	SCLK	K
L	AVDDH	AVDDH	AVDDH	AVDDH	VSS	HSDACN	HSDACP	L
M	P1_MDIP[0]	P2_MDIP[3]	P2_MDIN[3]	P3_MDIN[1]	P3_MDIP[1]	VSS	VSS	M
N	P1_MDIP[1]	P2_MDIN[0]	P2_MDIN[1]	P2_MDIN[2]	P3_MDIP[3]	P3_MDIP[2]	P3_MDIP[0]	N
P	P1_MDIN[1]	P2_MDIP[0]	P2_MDIP[1]	P2_MDIP[2]	P3_MDIN[3]	P3_MDIN[2]	P3_MDIN[0]	P
	8	9	10	11	12	13	14	

3.0 Device Functionality

The I347-AT4 is a 2- or 4-port 10/100/1000BASE-T Gigabit Ethernet transceiver. Each port of the I347-AT4 can operate completely independent of each other, but they are identical in performance and functionality. The functional description and electrical specifications for the I347-AT4 are applicable to each port. For simplicity, the functional description in this document describes the operation of a single transceiver.

Port numbers have been omitted from many diagrams and descriptive text indicating that the functionality applies to all ports. In this document, the pins for each port are specified by the port number, pin name, and signal number, respectively.

For example, LED 1 pin for Port 0 shown in Figure 3 (P0_LED[1]):

However, the MDIO pin supported by the I347-AT4 are global to the chip and do not have port numbers. Figure 3 and Figure 4 show the functional block diagram of the I347-AT4.

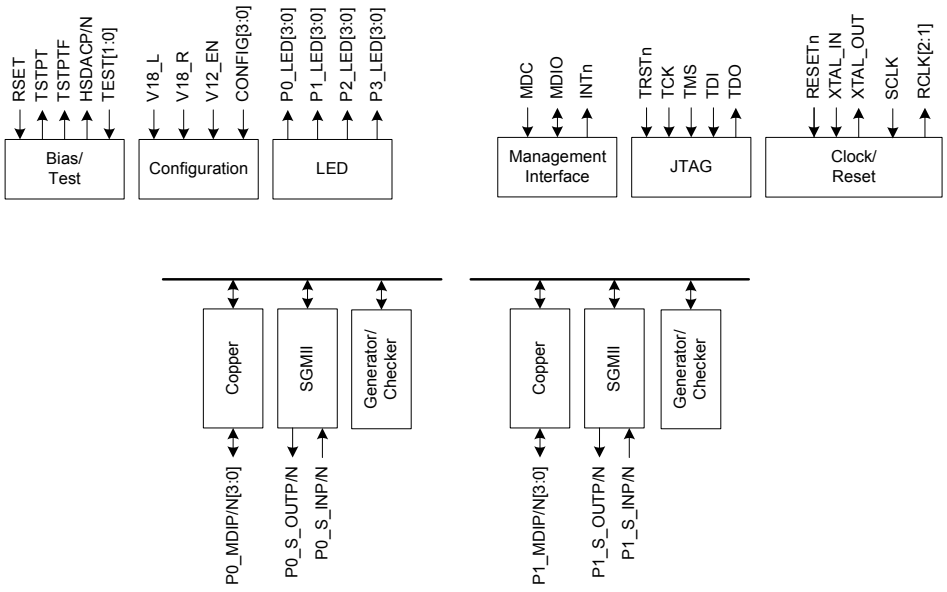


Figure 3. Functional Block Diagram — Dual-Port Mode

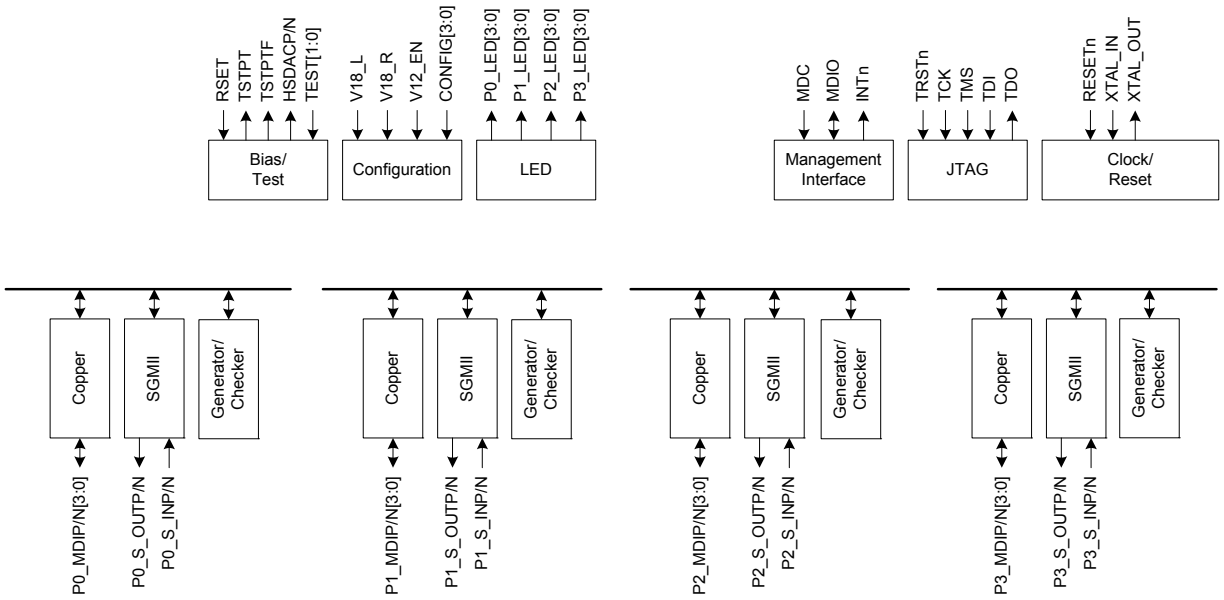


Figure 4. Functional Block Diagram — Quad-Port Mode

3.1 I347-AT4 Operation and Major Interfaces

The I347-AT4 supports an MDI interface-to-copper cable interface.

The MDI Interface is always a media interface. (The system interface is also known as MAC interface. It is typically the connection between the PHY and the MAC or the system ASIC.) For example:

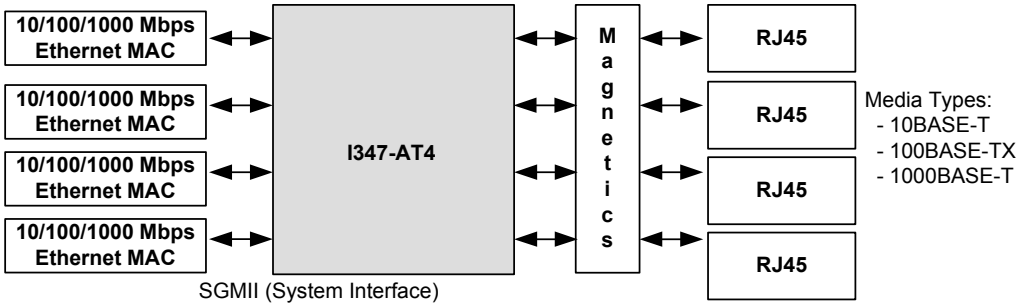


Figure 5. SGMII System Interface Example — Quad-Port Mode

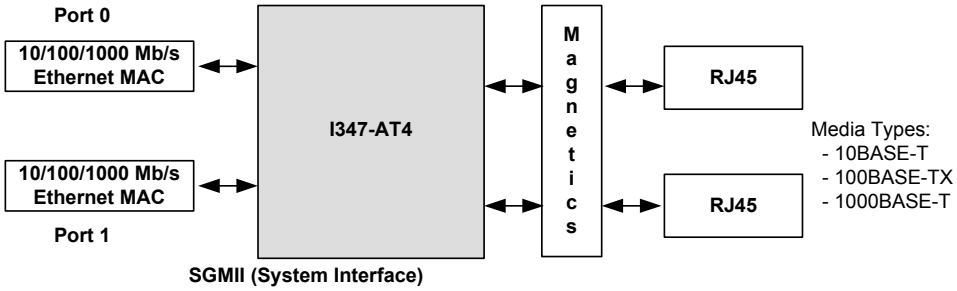


Figure 6. SGMII System Interface Example — Dual-Port Mode

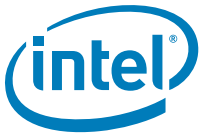
As can be seen from this example, the SGMII interface acts as a system interface.

The I347-AT4 supports one mode of operation: SGMII (system)-to-copper (Register 20_6.2:0 (001b).

3.2 Copper Media Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation.

The I347-AT4 integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the magnetics. The resistors have to be very accurate to meet the strict IEEE return loss requirements. Typically, ± 1% accuracy resistors are used on the board. These additional components between the PHY and the magnetics complicate board layout. Integrating the resistors has many advantages including component cost savings, better ICT yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements.



3.2.1 Transmit Side Network Interface

3.2.1.1 Multi-mode TX Digital-to-Analog Converter

The I347-AT4 incorporates a multi-mode transmit DAC to generate filtered 4D PAM 5, MLT3, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

3.2.1.2 Slew Rate Control and Waveshaping

In 1000BASE-T mode, partial response filtering and slew rate control is used to minimize high frequency EMI. In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

3.2.2 Encoder

3.2.2.1 1000BASE-T

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D PAM 5 symbols. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple the I347-AT4 from outputting the same sequence during idle, which helps to reduce EMI.

3.2.2.2 100BASE-TX

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled.

3.2.2.3 10BASE-T

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

3.2.3 Receive Side Network Interface

3.2.3.1 Analog-to-Digital Converter

The I347-AT4 incorporates an advanced high speed ADC on each receive channel with greater resolution than the ADC used in the reference model of the 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore, lower error rates. Proprietary architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 125 MHz.

3.2.3.2 Active Hybrid

The I347-AT4 employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to use the same transformer for coupling to the twisted pair cable, which reduces the cost of the overall system.

3.2.3.3 Echo Canceller

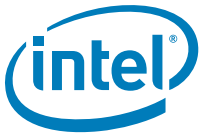
Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The I347-AT4 employs a fully developed digital echo canceller to adjust for echo impairments from more than 100 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

3.2.3.4 NEXT Canceller

The 1000BASE-T physical layer uses all 4 pairs of wires to transmit data to reduce the baud rate requirement to only 125 MHz. This results in significant high frequency crosstalk between adjacent pairs of cable in the same bundle. The I347-AT4 employs 3 parallel NEXT cancellers on each receive channel to cancel any high frequency crosstalk induced by the adjacent 3 transmitters. A fully adaptive digital filter is used to compensate for the time varying nature of channel conditions.

3.2.3.5 Baseline Wander Canceller

Baseline wander is more problematic in the 1000BASE-T environment than in the traditional 100BASE-TX environment due to the DC baseline shift in both the transmit and receive signals. The I347-AT4 employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.



3.2.3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of Feed Forward Equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

3.2.3.7 Digital Phase Lock Loop

In 1000BASE-T mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty canceling the echo and NEXT components. In the I347-AT4, an advanced DPLL is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own, thereby maximizing the achievable SNR.

3.2.3.8 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDIP/N pins.

In 100BASE-TX and 1000BASE-T modes, link is established by scrambled idles.

If Force Link Good register 16_0.10 is set high, the link is forced to be good and the link monitor is bypassed for 100BASE-TX and 10BASE-T modes. In the 1000BASE-T mode, register 16_0.10 has no effect.

3.2.3.9 Signal Detection

In 1000BASE-T mode, signal detection is based on whether the local receiver has acquired lock to the incoming data stream.

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDIP/N pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

3.2.4 Decoder

3.2.4.1 1000BASE-T

In 1000BASE-T mode, the receive idle stream is analyzed so that the scrambler seed, the skew among the 4 pairs, the pair swap order, and the polarity of the pairs can be accounted for. Once calibrated, the 4D PAM 5 symbols are converted to 9-bit symbols that are then descrambled into 8-bit data values. If the descrambler loses lock for any reason, the link is brought down and calibration is restarted after the completion of auto-negotiation.

3.2.4.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is put in parallel and then 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler "locks" to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

3.2.4.3 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

3.2.5 Electrical Interface

The input and output buffers are internally terminated to 50 Ω impedance. The output swing can be adjusted by programming register 26_1.2:0.

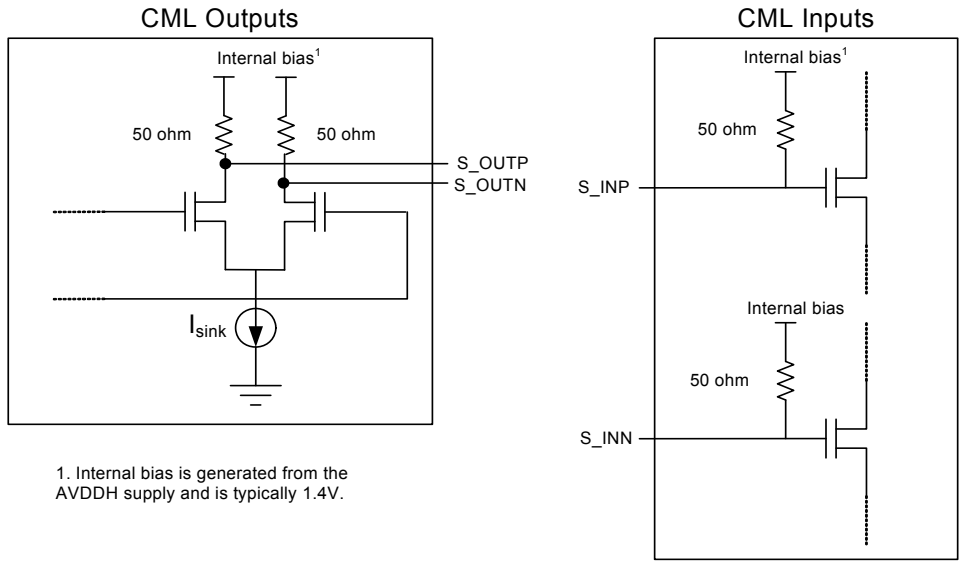


Figure 7. CML I/Os

3.2.6 SGMII Speed and Link

When the SGMII MAC interface is used, the interface is copper . The operational speed of the SGMII MAC interface is determined according to Table 9 media interface status and/or loopback mode.

Table 9. SGMII (MAC Interface) Operational Speed

Link Status or Media Interface Status	SGMII (MAC Interface) Speed
No Link	Determined by speed setting of 21_2.2:0
MAC Loopback	Determined by speed setting of 21_2.2:0

3.2.7 SGMII TRR Blocking

When the SGMII receives a packet with odd number of bytes, a single symbol of carrier extension will be passed on and transmitted onto 1000BASE-T. This carrier extension may cause problems with full-duplex MACs that incorrectly handle the carrier extension symbols. When register 16_1.13 is set to 1, all carrier extend and carrier extend with error symbols received by the SGMII will be converted to idle symbols when operating in full-duplex. Carrier extend and carrier extend with error symbols will not be blocked when operating in half-duplex, or if register 16_1.13 is set to 0b. Note that symbol errors will continue to be propagated regardless of the setting of register 16_1.13.

This function is on by default as the SGMII rev 1.8 standard requires this function to be implemented.

3.3 Loopback

The I347-AT4 implements various different loopback paths.

3.3.1 System Interface Loopback

The functionality, timing, and signal integrity of the system interface can be tested by placing the I347-AT4 in system interface loopback mode. This can be accomplished by setting register 0_0.14 = 1b, 0_1.14 = 1b, or 0_4.14 = 1b. In loopback mode, the data received from the MAC is not transmitted out on the media interface. Instead, the data is looped back and sent to the MAC. During loopback, link will be lost and packets will not be received.

If loopback is enabled while auto-negotiating, FLP auto-negotiation codes will be transmitted. If loopback is enabled in forced 10BASE-T mode, 10BASE-T idle link pulses will be transmitted on the copper side. If loopback is enabled in forced 100BASE-T mode, 100BASE-T idles will be transmitted on the copper side.

The speed of the SGMII interface is determined by register 21_2.2:0 during loopback. 21_2.2:0 is 100b = 10 Mb/s, 101b = 100 Mb/s, 110b = 1000 Mb/s.

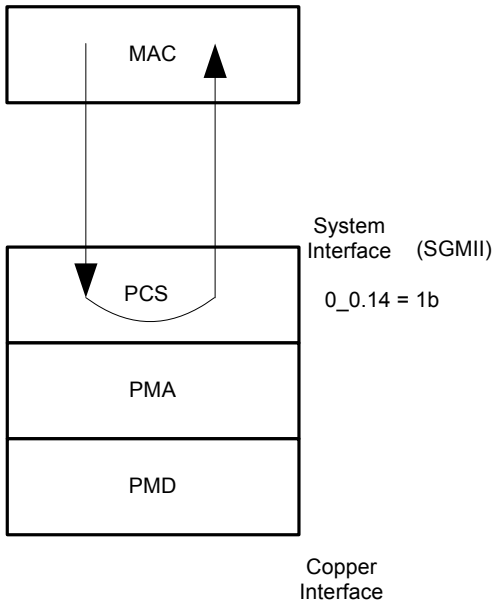


Figure 8. MAC Interface Loopback Diagram - Copper Media Interface

3.3.2 Line Loopback

Line loopback allows a link partner to send frames into the I347-AT4 to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. Refer to Figure 9. This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If auto-negotiation is enabled, both link partners should advertise the same speed and full-duplex. If auto-negotiation is disabled, both link partners need to be forced to the same speed and full-duplex. Once link is established, the line loopback mode can be enabled.

Register 21_2.14 = 1b enables the line loopback on the copper interface.

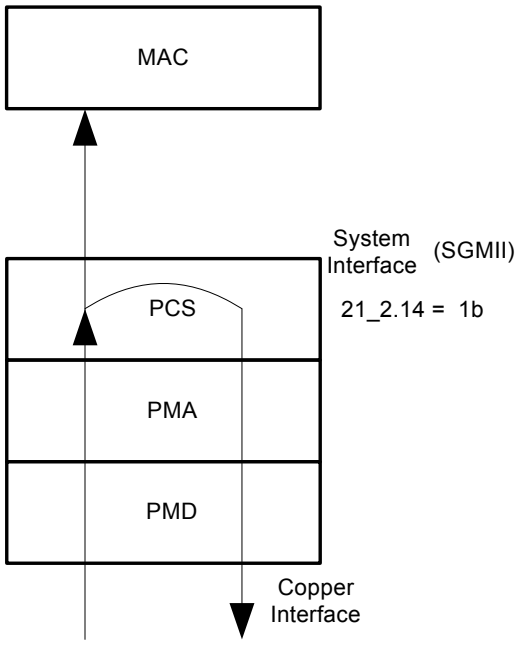


Figure 9. Copper Line Loopback Data Path

3.3.3 External Loopback

For production testing, an external loopback stub allows testing of the complete data path.

For 10BASE-T and 100BASE-TX modes, the loopback test requires no register writes. For 1000BASE-T mode, register 18_6.3 must be set to 1b to enable the external loopback. All copper modes require an external loopback stub.

The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1, 2 to pair 3, 6 and connecting pair 4, 5 to pair 7, 8, as seen in Figure 10.

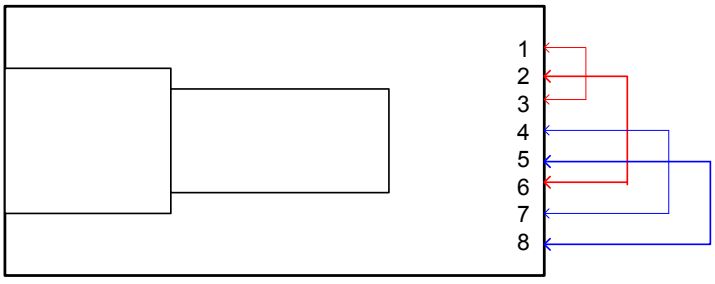


Figure 10. Loopback Stub (Top View With Tab Up)

The external loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link at 1000 Mb/s. It also allows the actual external loopback. See Figure 11. The MAC should see the same packets it sent, looped back to it.

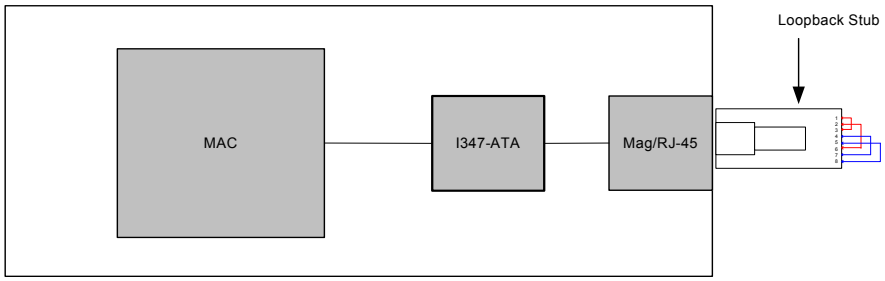
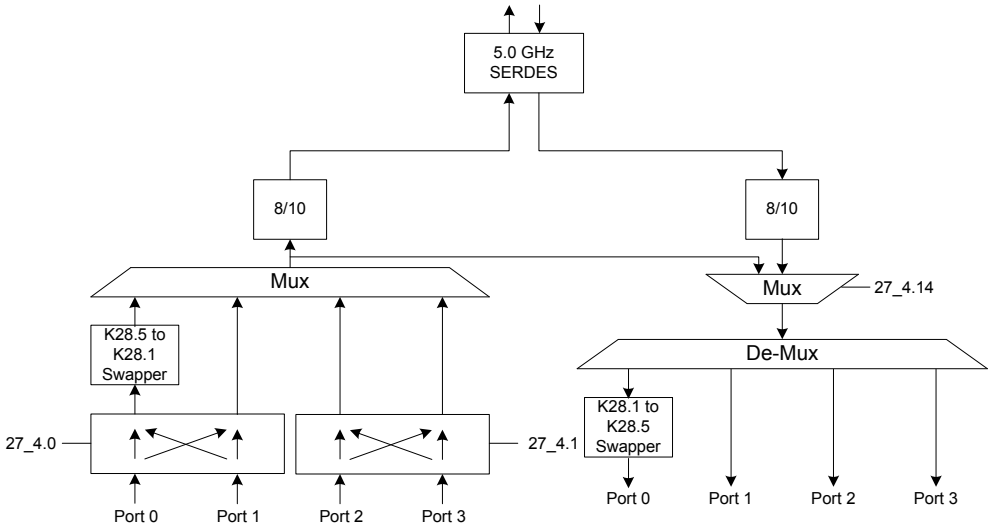


Figure 11. Test Setup for 10/100/1000 Mb/s Modes using an External Loopback Stub

3.4 Synchronizing FIFO



The I347-AT4 has a transmit and receive synchronizing FIFO to reconcile frequency differences between the clocks of the MAC interface and the media side. The FIFO depths can be increased in length to support longer frames. The I347-AT4 can handle jumbo frame sizes up to 16 KB with up to ± 100 PPM clock jitter. The deeper the FIFO depth, the higher the latency is.

For the I347-AT4, the status of the FIFO can be interrogated as in Table 10. Registers 19_2.3:2 are set depending on whether the copper transmit FIFO inserted or deleted idle symbols. Idles inserted or deleted will be flagged only if the inter packet gap is 24 bytes or less at the input of the FIFO. Inserted or deleted idles are ignored if the inter-packet gap is greater than 24 bytes.

The FIFO status bits can generate interrupts by setting the corresponding bits in register 18_1, 18_2, and 18_4.

Table 10. I347-AT4 FIFO Status Bits

Register	Function	Setting
19_2.7	Copper Transmit FIFO Over/Underflow	1b = Over/Underflow error 0b = No FIFO error
19_2.3	Copper Transmit FIFO Idle Inserted	1b = Idle inserted 0b = No idle inserted
19_2.2	Copper Transmit FIFO Idle Deleted	1b = Idle deleted 0b = No idle deleted

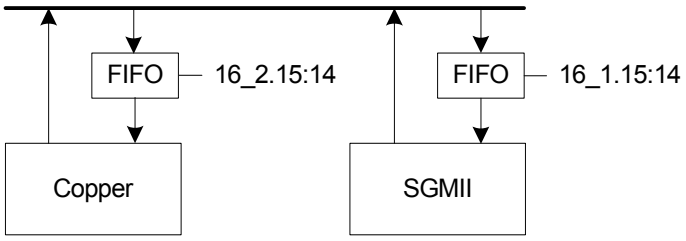


Figure 12. FIFO Locations

3.5 Resets

In addition to the hardware reset pin (RESETn) there are several software reset bits as listed in Table 11.

Register 27_4.15 is a software bit that emulates the hardware reset. The entire chip is reset as if the RESETn pin is asserted. Once triggered, registers are not accessible through the MDIO until the chip reset completes.

The copper circuit is reset per port via register 0_0.15.

Register 20_6.15 resets the mode control, port power management, and generator and checkers.

All the reset registers previously described are self cleared. However, register 20_6.9 is not self clearing. When register 20_6.9 is set to 1b, registers in banks 8, 9, 10 and 11 are not accessible.

Table 11. Reset Control Bits

Reset Register	Register Effect	Block
27_4.15	Chip Hardware Reset.	Entire chip.
0_0.15	Software Reset for Bank 0, 2, 3, 5, 7.	Copper - per port.
0_1.15	Software Reset for Bank 1.	SGMII - per port.
20_6.15	Software Reset for Bank 6.	Generator/Checker/Mode (per port).
20_6.9	Reserved	Reserved

3.6 Power Management

The I347-AT4 supports several advanced power management modes that conserve power.

3.6.1 Manual Power Down

There are multiple power down control bits on chip and they are listed in Table 12. Each power down control independently powers down its respective circuits. In general, it is not necessary to power down an unused interface. The PHY automatically powers down any unused circuit.

The automatic PHY power management can be overridden by setting the power down control bits. These bits have priority over the PHY power management in that the circuit cannot be powered up by power management when it's associated power down bit is set to 1b. When a circuit is powered back up by setting the bit to 0b, a software reset is also automatically sent to the corresponding circuit.

Note that register 0_0.11 and 16_0.2 are logically ORed to form a power down control.

Table 12. Power Down Control Bits

Reset Register	Register Effect
0_0.11	Copper Power Down.
16_0.2	Copper Power Down.

3.6.2 MAC Interface Power Down

In some applications, the MAC interface must run continuously regardless of the state of the network interface. Additional power is required to keep the MAC interface running during low power states.

If absolute minimal power consumption is required during network interface power down mode or in cable detect mode, then register 16_2.3 or 16_1.3 should be set to 0b to enable the MAC interface to power down.

Table 13 lists which bit controls the automatic MAC interface power down, and the MAC interface that is powered down. In general 16_2.3 is used when the network interface is copper.

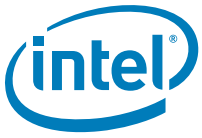


Table 13. Automatic MAC Interface Power Down

Register 20_6.2:0	Mode	MAC Interface Power Down Control Bit	MAC Interface Powered Down
001	SGMII (System) to Copper	16_2.3	SGMII

3.6.3 Copper Detect Mode

The I347-AT4 can be placed in cable detect mode power down modes by selecting either of the two cable detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The status of the cable detect is reported in register 17_0.4 and the cable detect changes are reported in register 19_0.4.

3.6.3.1 Cable Detect (Mode 1)

Cable detect mode (Mode 1) is entered by setting register 16_0.9:8 to 10.

In Mode 1, only the signal detection circuitry and serial management interface are active. If the PHY detects energy on the line, it starts to auto-negotiate sending FLPs for five seconds. If at the end of five seconds the auto-negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If auto-negotiation completes, then the PHY goes into normal 10/100/1000 Mb/s operation. If during normal operation the link is lost, the PHY re-starts auto-negotiation. If no energy is detected after five seconds, the PHY goes back to monitoring receive energy.

3.6.3.2 Cable Detect Mode (Mode 2)

Cable detect mode (Mode 2) is entered by setting register 16_0.9:8 to 11.

In Mode 2, the PHY sends out a single 10 Mb/s Normal Link Pulse (NLP) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the I347-AT4 is in Mode 1, it cannot wake up a connected device; therefore, the connected device must be transmitting NLPs, or either device must be woken up through register access. If the I347-AT4 is in Mode 2, then it can wake a connected device.

3.6.3.3 Normal 10/100/1000 Mb/s Operation

Normal 10/100/1000 Mb/s operation can be entered by turning off cable detect mode by setting register 16_0.9:8 to 0x0.

3.6.3.4 Power State Upon Exiting Power Down

When the PHY exits power down (register 0_0.11 or 16_0.2) the active state depends on whether the cable detect mode function is enabled (register 16_0.9:8 = 1x). If the cable detect mode function is enabled, the PHY transitions to the cable detect mode state first and wakes up only if there is a signal on the wire.

Table 14. Power State after Exiting Power Down

Register 0_0.11	Register 16_0.2	Register 16_0.9:8	Behavior
1b	x	xx	Power down.
x	1b	xx	Power down.
1b to 0b	0b	00b	Transition to power up.
0b	1b to 0b	00b	Transition to power up.
1b to 0b	0b	1x	Transition to cable detect mode state.
0b	1b to 0b	1x	Transition to cable detect mode state.

3.6.4 Low Power Modes

Three low power modes are supported in the I347-AT4.

- IEEE 22.2.4.1.5 compliant power down
- Cable Detect Mode (Mode 1)
- Cable Detect Mode (Mode 2)

IEEE 22.2.4.1.5 power down compliance enables the PHY to be placed in a low-power consumption state by register control.

Cable detect mode (Mode 1) enables the I347-AT4 to wake up when energy is detected on the wire.

Cable detect mode (Mode 2) is identical to Mode 1 with the additional capability to wake up a link partner. In Mode 2, the 10BASE-T link pulses are sent once every second while listening for energy on the line.

Details of each mode follows.

3.6.5 Low Power Operating Modes

3.6.5.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 0_0.11. In this mode, the PHY does not respond to any SGMII signals except the MDC/MDIO. It also does not respond to any activity on the copper media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 0_0.11 and 16_0.2 = 0b.

Upon deassertion of hardware reset, Register 0_0.11 and 16_0.2 are set to 1b to default the I347-AT4 to a power down state.

Register 0_0.11 and 16_0.2 are logically ORed to form a power down control.

3.6.5.2 Cable Detect Power Down Modes

The I347-AT4 can be placed in cable detect power down modes by selecting either of the two cable detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The cable detect modes only apply to the copper media. The cable detect modes do not work while Copper Auto Select (Section 3.4) is enabled. The status of the cable detect is reported in register 17_0.4 and the cable detect changes are reported in register 19_0.4.

3.6.6 SGMII Effect on Low Power Modes

In some applications, SGMII must run continuously regardless of the state of the PHY. Additional power is required to keep this SGMII interface running during low power states.

If absolute minimal power consumption is required during the IEEE power down mode or the cable detect modes, then register 16_2.3 should be set to 0b to enable SGMII to power down. Note that for these settings to take effect a software reset must be issued.

3.7 Auto-Negotiation

The I347-AT4 supports 10/100/1000BASE-T Copper auto-negotiation (IEEE 802.3 Clauses 28 and 40).

Auto-negotiation provides a mechanism for transferring information from the local station to the link partner to establish speed, duplex, and master/slave preference during a link session.

Auto-negotiation is initiated upon any of the following conditions:

- Power-up reset
- Hardware reset
- Software reset (register 0_0.15, 0_1.15, or 0_4.15)
- Restart auto-negotiation (register 0_0.9, 0_1.9, 0_4.9)
- Transition from power down to power up (register 0.0_0.11, 0_1.11, or 0_4.11)
- The link goes down

The following sections describe each of the auto-negotiation modes in detail.

3.7.1 10/100/1000BASE-T Auto-Negotiation

The 10/100/1000BASE-T auto-negotiation is based on Clause 28 and 40 of the IEEE802.3 specification. It is used to negotiate speed, duplex, and flow control over CAT5 UTP cable. Once auto-negotiation is initiated, the I347-AT4 determines whether or not the remote device has auto-negotiation capability. If so, the I347-AT4 and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have auto-negotiation capability, the I347-AT4 uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 clauses 28 and 40 for a full description of auto-negotiation.

After hardware reset, 10/100/1000BASE-T auto-negotiation can be enabled and disabled via Register 0_0.12. Auto MDI/MDIX and auto-negotiation can be disabled and enabled independently. When auto-negotiation is disabled, the speed and duplex can be set via registers 0_0.13, 0_0.6, and 0_0.8, respectively. When auto-negotiation is enabled the abilities that are advertised can be changed via registers 4_0 and 9_0.

Changes to registers 0_0.12, 0_0.13, 0_0.6 and 0_0.8 do not take effect unless one of the following takes place:

- Software reset (registers 0_0.15)
- Restart auto-negotiation (register 0_0.9)
- Transition from power down to power up (register 0_0.11)
- The copper link goes down

To enable or disable auto-negotiation, Register 0_0.12 should be changed simultaneously with either register 0_0.15 or 0_0.9. For example, to disable auto-negotiation and force 10BASE-T half-duplex mode, register 0_0 should be written with 0x8000.

Registers 4_0 and 9_0 are internally latched once every time the auto-negotiation enters the ability detect state in the arbitration state machine. Hence, a write into Register 4_0 or 9_0 has no effect once the I347-AT4 begins to transmit Fast Link Pulses (FLPs).This guarantees that sequences of FLPs transmitted are consistent with one another.

Register 7_0 is treated in a similar way as registers 4_0 and 9_0 during additional next page exchanges.

If 1000BASE-T mode is advertised, then the I347-AT4 automatically sends the appropriate next pages to advertise the capability and negotiate master/slave mode of operation. If the user does not wish to transmit additional next pages, then the next page bit (Register 4_0.15) can be set to zero, and the user needs to take no further action.

If next pages in addition to the ones required for 1000BASE-T are needed, then the user can set register 4_0.15 to one, and send and receive additional next pages via registers 7_0and 8_0, respectively. The I347-AT4 stores the previous results from register 8 in internal registers, so that new next pages can overwrite register 8_0.

Note that 1000BASE-T next page exchanges are automatically handled by the I347-AT4 without user intervention, regardless of whether or not additional next pages are sent.

Once the I347-AT4 completes auto-negotiation, it updates the various status in registers 1_0, 5_0, 6_0, and 10_0. Speed, duplex, page received, and auto-negotiation completed status are also available in registers 17_0 and 19_0.

See Section 3 for more details.

3.8 Downshift Feature

Without the downshift feature enabled, connecting between two Gigabit link partners requires a four-pair RJ-45 cable to establish 10, 100, or 1000 Mb/s link. However, there are existing cables that have only two-pairs, which are used to connect 10 Mb/s and 100 Mb/s Ethernet PHYs. With the availability of only pairs 1, 2 and 3, 6, Gigabit link partners can auto-negotiation to 1000 Mb/s, but fail to link. The Gigabit PHY repeatedly goes through the auto-negotiation but fails 1000 Mb/s link and never tries to link at 10 Mb/s or 100 Mb/s.

With the downshift feature enabled, the I347-AT4 is able to auto-negotiation with another Gigabit link partner using cable pairs 1, 2 and 3, 6 to downshift and link at 10 Mb/s or 100 Mb/s, whichever is the next highest advertised speed common between the two Gigabit PHYs.

In the case of a three pair cable (additional pair 4, 5 or 7, 8 - but not both) the same downshift function for two-pair cables applies.

By default, the downshift feature is turned off. Refer to register 16_0.14:11, which describes how to enable this feature and how to control the downshift algorithm parameters.

To enable the downshift feature, the following registers must be set:

- Register 16_0.11 = 1b — enables downshift
- Register 16_0.14:12 — sets the number of link attempts before downshifting

3.9 Fast 1000BASE-T Link Down Indication

Per the IEEE 802.3 Clause 40 standard, a 1000BASE-T PHY is required to wait 750 ms or more to report that link is down after detecting a problem with the link. For metro Ethernet applications, a fast failover in 50 ms is specified, which cannot be met if the PHY follows the 750 ms wait time. This delay can be reduced by intentionally violating the IEEE standard by setting register 26_0.9 to 1b.

The delay at which link down is reported can be selected by setting register 26_0.11:10 as follows:

- 00b = 0 ms
- 01b = 10 ± 2 ms
- 10b = 20 ± 2ms
- 11b = 40 ± 2ms

3.10 Cable Tester

The I347-AT4 uses Time Domain Reflectometry (TDR) to determine the quality of the cables, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The I347-AT4 transmits a signal of known amplitude (+1V) down each of the four pairs of an attached cable. It conducts the cable diagnostic test on each pair, testing the MDI_0_0P/N, MDI_0_1P/N, MDI_0_2P/N, and MDI_0_3P/N pairs sequentially. The transmitted signal continues down the cable until it reflects off of a cable imperfection.

Cable tester has four modes of operation that is programmable via register 23_5.7:6. The first mode returns the peak with the maximum amplitude that is above a certain threshold. The second mode returns the first peak detected that is above a certain threshold. The third mode measures the systematic offset at the receiver. The fourth mode measures the amplitude seen at a certain specified distance.

The cable tester is initiated by setting register 23_5.15 to 1b. This bit self clears when the test completes. Register 23_5.14 is set to a 1b indicating that the TDR results in the registers are valid.

Each point in the cable testerreflected waveform is sampled multiple times and averaged. The number of samples to take is programmable via register 23_5.10:8.

Each time the cable tester is enable, the results seen on the four receive channels are reported in registers 16_5, 17_5, 18_5, and 19_5. Register 23_5.13:11 selects which channel transmits the test pulse.

When register 23_5.13:11 is set to 000b the same channel reflection is recorded. In other words, channel 0 transmits a pulse and the reflection seen on channel 0 receiver is reported. Channel 1 transmits a pulse and the reflection seen on channel 1 receiver is reported. The same for channel 2 and channel 3.

When register 23_5.13:11 is set to 100b all four receive channels report the reflection seen by a pulse transmitted by channel 0.

When register 23_5.13:11 is set to 101b all four receive channels report the reflection seen by a pulse transmitted by channel 1.

When register 23_5.13:11 is set to 110b all four receive channels report the reflection seen by a pulse transmitted by channel 2.

When register 23_5.13:11 is set to 111b all four receive channels report the reflection seen by a pulse transmitted by channel 3.

As a result, if only the reflection seen on the same channel is desired the cable tester should be run with 23_5.13:11 = 000b. If all same channel and cross channel combinations are desired then the cable tester must be run four times with 23_5.13:11 set to 100b, 101b, 110b, and 111b for the four runs. Registers 16_5, 17_5, 18_5, and 19_5 should be read and stored between each run.

3.10.1 Maximum Peak

When register 23_5.7:6 is set to 00b, the maximum peak above a certain threshold is reported. Pulses are sent out and recorded according to the setting of register 25_5.13:11.

There are 10 threshold settings for same channel reflections and are specified by registers 26_5.6:0, 26_5.14:8, 27_5.6:0, 27_5.14:8, and 28_5.6:0 for positive reflections and 26_7.6:0, 26_7.14:8, 27_7.6:0, 27_7.14:8, and 28_7.6:0 for negative reflections.

These settings correspond to the amplitude threshold the reflected signal has to exceed before it is counted. Any reflected signal below this threshold level is ignored. The threshold settings are based on cable length with the breakpoints at 10 m, 50 m, 110 m, and 140 m.

There are four threshold settings for cross-channel specified by registers 25_5.6:0 and 25_5.14:8 for positive reflections and 25_7.6:0 and 25_7.14:8 for negative reflections. The threshold settings are based on cable length with the breakpoints at 10 m.

The default values are targeted to 85 Ω to 115 Ω. However these threshold settings should be calibrated for the desired impedance setting on the target system.

The results are stored in registers 16_5, 17_5, 18_5, and 19_5. Bits 7:0 report the distance of the peak. The distance can be converted to using the trend line in Figure 13. Bits 14:8 report the reflected amplitude. Bit 15 reports whether the reflected amplitude was positive or negative. When bits 15:8 return a value of 0x80, it means there was no peak detected above the threshold. If bits 15:8 return a value of 0x00 then the test failed.

Register 28_5.7 controls the exact distance that is reported. When set to 0b the distance where the amplitude falls to 50% of the peak amplitude is reported. When set to 1b the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude is reported in bits 14:8.

In the maximum peak mode, register 24_5.7:0 is used to set the starting distance of the sweep. Normally this value should be set to 0b. If this value is set to a non-zero value, any reflection below the starting distance is ignored. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

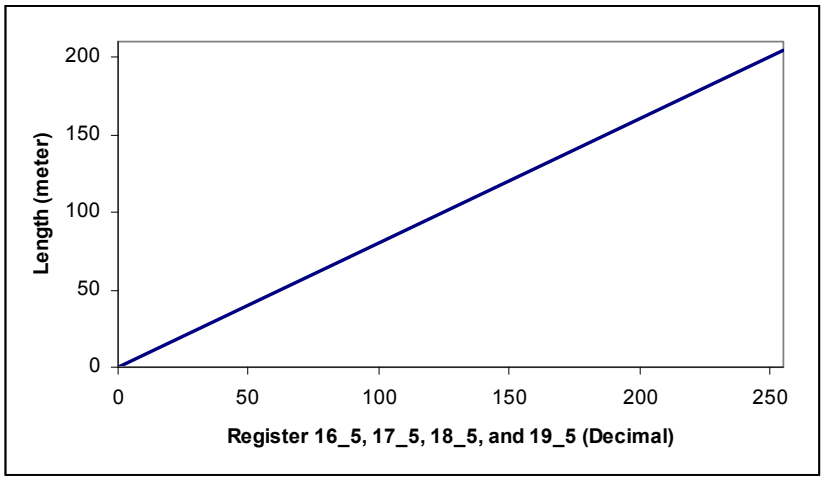


Figure 13. Cable Fault Distance Trend Line

3.10.2 First Peak

When register 23_5.7:6 is set to 01b, the first peak above a certain threshold is reported. The first peak operates in exactly the same way as the maximum peak except that there has to be some qualification as to what constitutes a peak since the first peak is not necessarily the maximum peak. The first peak is defined as the maximum amplitude seen before the reflected amplitude drops by some value below this peak. This hysteresis value is defined by register 23_5.5:0.

For example, in Figure 14, if Pa is greater than the hysteresis value in 23_5.5:0 and Va is above the threshold value, then Va and Da are reported since it is the first peak that is above the threshold.

If Pa is less than the hysteresis value in 23_5.5:0, then Va and Da are not reported as the first peak. Vb and Db will be reported as the first peak if Pb is greater than the hysteresis value in 23_5.5:0 and Vb is above the threshold value.

If Pa is greater than the hysteresis value in 23_5.5:0 but Va is below the threshold value then Va and Da are not reported as the first peak. Vb and Db will be reported as the first peak if Pb is greater than the hysteresis value in 23_5.5:0 and Vb is above the threshold value.

Register 28_5.7 controls the exact distance that is reported. When set to 0b the distance where the amplitude falls below the peak amplitude minus the hysteresis level as defined in register 23_5.5:0 is reported. When set to 1b the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude of the first peak is reported in bits 14:8.

In the first peak mode register 24_5.7:0 is used to set the starting distance of the sweep. Normally, this value should be set to 0b. If this value is set to a non-zero value, any reflection below the starting distance is ignored. This may be useful to ignore reflections at the transformer that are reported as the first peak. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

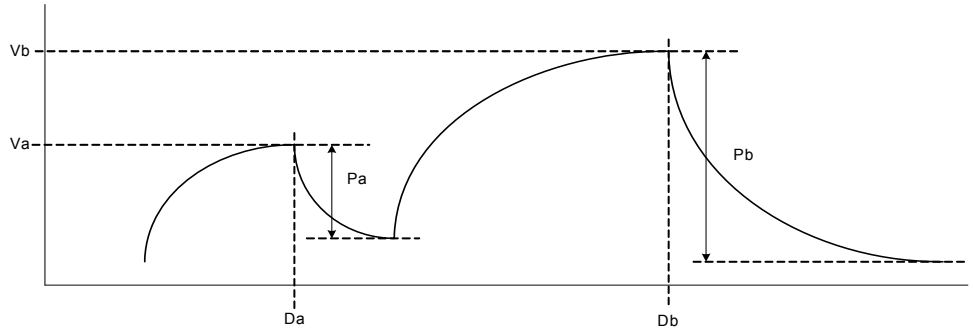


Figure 14. First Peak Example

3.10.3 Offset

The offset reports the offset seen at the receiver. This is a debug mode. Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 have no meaning. When bits 15:8 return a value of 0x80 it means there is zero offset. If bit 15:8 returns a value of 0x00 then the test failed.

Note that in the maximum peak, first peak, and sample point modes, the systematic offset is automatically subtracted from the results.

3.10.4 Sample Point

When register 20_8.7:6 is set to 11b, the amplitude of the reflected pulse at a particular distance on the cable is reported. Unlike the maximum peak and first peak modes which only measures up to about 200 meters of cable, the sample point mode can measure up to 400 meters of cable.

The sample point returns the amplitude of the reflected pulse at a particular distance on the cable. The distance is set by register 24_5.8:0. The threshold registers 25_5, 26_5, 27_5, 28_5.6:0, 25_7, 26_7, 27_7, and 28_7.6:0 are ignored.

Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 return the same value as 24_5.7:0. Note that register 24_5.8 is not returned. Bits 14:8 return the amplitude, and bit 15 the sign of the amplitude. If the test failed bits 15:8 returns 0x00000000 (zero amplitude will always return as 0x10000000).

By programming register 24_5.8:0 from 0x000 to 0x1FF and running the sample point test at each distance it is possible to reconstruct the reflected amplitude. Note that since the threshold is ignored, it is possible that some small reflections in the same channel measurements will be reported at short cable lengths when there are none. This is because the analog hybrid does not 100% cancel out the transmitted signal.

3.10.5 Pulse Amplitude and Pulse Width

The transmitted pulse amplitude and pulse width can be adjusted via registers 28_5.9:8 and 28_5.11:10, respectively. They should normally be set to full amplitude and full pulse width.

3.10.6 Drop Link

When register 28_5.12 is set to 0b the circuit waits 1.5 seconds to break the link before starting cable tester. When set to 1b this delay is bypassed.

3.10.7 Cable Test with Link Up

The following status requires the PHY to link up with a link partner.

- Register 20_5 reports the pair skew of each pair of wires relative to each other.
- Register 21_5.3:0 reports the polarity of each pair of wires.
- Register 21_5.6:5 reports the crossover status.
- Register 20_5 and 21_5 are not valid unless register 21_5.6 is set to 1b.

3.11 Data Terminal Equipment (DTE) Detect

The I347-AT4 supports the DTE power function. The DTE power function is used to detect if a link partner requires power supplied by the I347-AT4.

The DTE power function is enabled by writing to register 26_0.8. When DTE is enabled, the I347-AT4 first monitors for any activity transmitted by the link partner. If the link partner is active, then the link partner has power and power from the POE PSE device is not required. If there is no activity coming from the link partner, DTE power engages, and special pulses are sent to detect if the link partner requires DTE power. If the link partner has a low pass filter (or similar fixture) installed, the link partner is detected as requiring DTE power.

The DTE power status register (Register 17_0.2) immediately comes up as soon as the link partner is detected as a device requiring DTE power. Register 19_0.2 is a stray bit that reports the DTE power status has changed states.

If a link partner that requires DTE power is unplugged, the DTE power status (register 17_0.2) drops after a user-controlled delay (default is 20 seconds - Register 26_0.7:4) to avoid DTE power status register drop during the link partner powering up (for most applications), since the low pass filter (or similar fixture) is removed during power up. If DTE power status drop is desired to be reported immediately, write register 26_0.7:4 to 0x0000.

A detailed description of the register bits used for DTE power detection for the I347-AT4 are listed in Table 15.

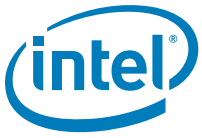


Table 15. Registers for DTE Power

Register	Description
26_0.8 - Enable power over Ethernet detection	1b = Enable DTE detect. 0b = Disable DTE detect. A soft reset is required to enable this feature. Hardware reset: 0b. Software reset: Update.
17_0.2 - Power over Ethernet detection status	1b = Need power. 0b = Do not need power. Hardware reset: 0b. Software reset: 0b.
19_0.2 - Power over Ethernet detection state changed	1b = Changed. 0b = No change. Hardware reset: 0b. Software reset: 0b.
26_0.7:4 - DTE detect status drop	Once the PHY no longer detects that the link partner filter, the PHY waits a period of time before clearing the power over Ethernet detection status bit (17_0.2). The wait time is 5 seconds multiplied by the value of these bits. Example: (5 * 0x4 = 20 seconds). Default at hardware reset: 0x4. At software reset: retain.

3.12 CRC Error Counter and Frame Counter

The CRC counter and frame counters, normally found in MACs, are available in the I347-AT4. The error counter and frame counter features are enabled through register writes and each counter is stored in eight register bits.

Register 18_6.2:0 controls which path the CRC checker and packet counter is counting.

If register 18_6.2:0 is set to 010b then the copper receive path is checked.

3.12.1 Enabling The CRC Error Counter and Frame Counter

To enable both counters to count, set 18_6.2:0 to a non-zero value.

To disable and clear both counters, set 18_6.2:0 to 000b.

To read the CRC counter and frame counter, read register 17_6.

17_6.15:8 (Frame count is stored in these bits).

17_6.7:0 (CRC error count is stored in these bits).

The CRC counter and frame counter do not clear on a read command. To clear the counters, disable/reset the CRC checker by writing Reg 18_6.2:0 = 000b.

3.13 Packet Generator

The I347-AT4 contains a very simple packet generator. Section 4.1.50 lists the I347-AT4 Packet Generator register details.

The packet generator is enabled when:

Register 16_6.7:6 controls which path the packet generator is connected to.

If register 16_6.7:6 is set to 01b then the input into the SGMII is ignored and the packet is generated onto the copper transmit path.

If register 16_6.7:6 is set to 10b then the copper receiver is ignored and the packet is generated onto the SGMII output path.

If register 16_6.7:6 is set to 11b then the copper receiver or the SGMII is ignored.

Once enabled, a fixed length packet of 64- or 1518- byte frame (including CRC) is transmitted separated by 12 bytes of IPG. The preamble length is 8 bytes. The payload of the frame is either a fixed 5A, A5, 5A, A5 pattern or a pseudo random pattern. A correct IEEE CRC is appended to the end of the frame. An error packet can also be generated.

The registers are as follows:

- 16_6.7:6 — Packet generation enable. 00b = Normal operation, Else = Enable internal packet generator
- 16_6.2 — Payload type. — 0b = Pseudo random, 1b = Fixed 5A, A5, 5A, A5,...
- 16_6.1 — Packet length. — 0b = 64 bytes, 1b = 1518 bytes.
- 16_6.0 — Error packet — 0b = Good CRC, 1b = Symbol error and corrupt CRC.
- 16_6.15:8 — Packet Burst Size. — 0x00 = Continuous, 0x01 to 0xFF = Burst 1 to 255 packets.

If register 16_6.15:8 is set to a non-zero value, then register 16_6.7:6 self clears once the required number of packets are generated. Note that if register 16_6.7:6 is manually set to 0b while packets are still bursting, the bursting ceases immediately once the current active packet finishes transmitting. The value in register 16_6.15:8 should not be changed while 16_6.7:6 is set to a non-zero value.

3.14 RX_ER Byte Capture

Each time there is an RX_ER in the internal GMII interface the PHY captures four bytes before RX_ER is asserted. Once the bytes preceding the RX_ER assertion are captured into the registers, they are not over written by new errors and they are only cleared after the registers are read.

There is one set of RX_ER capture registers. It captures the receive path of the copper path. These capture registers are always running.

The copper path is accessed via register 20_2. The following description applies to the copper path.

Once an error event is captured, register 20_2.15 is set to 1b indicating that the capture data is valid. No further errors are captured until all captured registers are read. Register 20_2.13:12 is set to 00b. Register 20_2.9:0 outputs the byte that is the earliest received. Once register 20_2 is read register 20_2.13:12 increments and register 20_2.9.0 is updated with the next earliest byte. The register is incremented and byte updated until the fourth read occurs. After the fourth read to register 20_2 completes, register 20_2.15 is set to 0b and the error capturing resumes four RX_CLK cycles after the final read completes. The 4 RX_CLK cycle delay is required to insure that the register has four valid bytes loaded prior to being frozen. Note that a side effect of doing this is the RX_ER might be high in the captured bytes.

Table 16. Error Byte Capture

Register	Function	Setting
20_2.15	Capture Data Valid	1b = Bits 14:0 valid. 0b = Bits 14:0 invalid.
20_2.13:12	Byte Number	00b = 4 bytes before RX_ER asserted. 01b = 3 bytes before RX_ER asserted. 10b = 2 bytes before RX_ER asserted. 11b = 1 byte before RX_ER asserted. The byte number increments after every read when register 20_2.15 is set to 1b.
20_2.9	RX_ER	RX Error. Normally this bit is low since the capture is triggered by RX_ER being high. However, it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
20_2.8	RX_DV	RX Data Valid.
20_2.7:0	RXD[7:0]	RX Data.

3.15 MDI/MDIX Crossover

The I347-AT4 automatically determines whether or not it needs to cross over between pairs as listed in Table 17 so that an external crossover cable is not required. If the I347-AT4 interoperates with a device that cannot automatically correct for crossover, the I347-AT4 makes the necessary adjustment prior to commencing auto-negotiation. If the I347-AT4 interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 clause 40.4.4 determines which device performs the crossover.

When the I347-AT4 interoperates with legacy 10BASE-T devices that do not implement auto-negotiation, the I347-AT4 follows the same algorithm as previously described since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement auto-negotiation (such as, link pulses are not present), the I347-AT4 uses signal detect to determine whether or not to crossover.

The auto MDI/MDIX crossover function can be disabled via register 16_0.6:5.

The pin mapping in MDI and MDIX modes is listed in Table 17.

Table 17. Media Dependent Interface Pin Mapping

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	unused	unused	BI_DD±	unused	unused
MDIP/N[3]	BI_DD±	unused	unused	BI_DC±	unused	unused

Note: Table 17 assumes no crossover on PCB.

The MDI/MDIX status is indicated by Register 17_0.6. This bit indicates whether the receive pairs (3, 6) and (1, 2) are crossed over. In 1000BASE-T operation, the I347-AT4 can correct for crossover between pairs (4, 5) and (7, 8) as listed in Table 17. However, this is not indicated by Register 17_0.6.

If 1000BASE-T link is established, pairs (1, 2) and (3, 6) crossover is reported in register 21_5.4, and pairs (4, 5) and (7, 8) crossover is reported in register 21_5.5.

3.16 Unidirectional Transmit

IEEE 802.3ah requires OAM support with unidirectional transmit capability. Unidirectional transmit enables a PHY to transmit data when the PHY does not have link due to potential issues on the receive path. 802.3ah formally requires two bits for this capability. Register 0.5 enables this capability, and 1.7 advertises this ability. This ability only applies to 100BASE-TX or 1000BASE-X. It doesn't apply to 1000BASE-T since 1000BASE-T requires Master/Slave relationship and training with both link partners participating, which requires that link exists for any data transmit.

The I347-AT4 supports transmits of packets when there is no link by using register bit 16_0.10 = 1b (*Force Copper Link Good*). This is not the official bit specified by the 802.3ah but serves the same function.

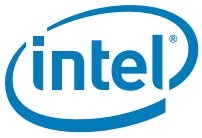
3.17 Polarity Correction

The I347-AT4 automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The polarity correction status is indicated by Register 17_0.1. This bit indicates whether the receive pair (3, 6) is polarity reversed in MDI mode of operation. In MDIX mode of operation, the receive pair is (1, 2) and Register 17_0.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, Register 17_0.1 only indicates polarity reversal on the pairs described above.



If 1000BASE-T link is established register 21_5.3:0 reports the polarity on all four pairs.

Polarity correction can be disabled by register write 16_0.1 = 1b. Polarity is then forced to normal 10BASE-T mode.

3.18 FLP Exchange Complete with No Link

Sometimes when link does not come up, it is difficult to determine whether the failure is due to the auto-negotiation Fast Link Pulse (FLP) not completing or from the 10/100/1000BASE-T link not being able to come up.

Register 19_0.3 is a sticky bit that gets set to 1b each time the FLP exchange completes but the link cannot be established for some reason. Once the bit is set, it is cleared only by reading the register.

This bit is not set if the FLP exchange does not complete, or if link is established.

3.18.0.1 Compound LED Modes

Compound LED modes are defined in Table 18.

Table 18. Compound LED Status

Compound Mode	Description
Activity	Transmit activity or receive activity.
Copper Link	10BASE-T link OR 100BASE-TX link or 1000BASE-T link.
Link	Copper link.

3.18.0.2 Speed Blink

When 16_3.3:0 is set to 0010b the LED[0] pin takes on the following behavior.

LED[0] outputs the sequence listed in Table 19 depending on the status of the link. The sequence consists of eight segments. If a 1000 Mb/s link is established the LED[0] outputs 3 pulses, 100 Mb/s 2 pulses, 10 Mb/s 1 pulse, and no link 0 pulses. The sequence repeats over and over again indefinitely.

The odd numbered segment pulse duration is specified in 18_3.1:0. The even numbered pulse duration is specified in 18_3.3:2 (Table 20).

Table 19. Speed Blinking Sequence

Segment	10 Mb/s	100 Mb/s	1000 Mb/s	No Link	Duration
1	On	On	On	Off	18_3.1:0
2	Off	Off	Off	Off	18_3.3:2
3	Off	On	On	Off	18_3.1:0
4	Off	Off	Off	Off	18_3.3:2
5	Off	Off	On	Off	18_3.1:0
6	Off	Off	Off	Off	18_3.3:2
7	Off	Off	Off	Off	18_3.1:0
8	Off	Off	Off	Off	18_3.3:2

Table 20. Speed Blink

Register	Pin	Definition
18_3.3:2	Pulse Period for even segments	00b = 84 ms. 01b = 170 ms. 10b = 340 ms. 11b = 670 ms.
18_3.1:0	Pulse Period for odd segments	00b = 84 ms. 01b = 170 ms. 10b = 340 ms. 11b = 670 ms.

3.18.0.3 Manual Override

When 19_3.7:6, 19_3.3:2,16_3.15:14, 16_3.11:10, 16_3.7:6, and 16_3.3:2 are set to 10b the LED[5:0] are manually forced. Registers 19_3.5:4, 19_3.1:0,16_3.13:12, 16_3.9:8, 16_3.5:4, and 16_3.1:0 then select whether the LEDs are to be on, off, Hi-Z, or blink.

If bi-color LEDs are used, the manual override selects only one of the two colors. In order to get the third color by mixing, MODE 1 and MODE 2 should be used (Section 3.18.0.4).

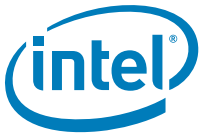
3.18.0.4 MODE 1, MODE 2, MODE 3, MODE 4

MODE 1 to 4 are dual LED modes. These are used to mix a third color using bi-color LEDs.

When 19_3.3:0,16_3.11:8 or 16_3.3:0 is set to 11xxb then one of the 4 modes are enabled.

MODE 1 – Solid mixed color.

MODE 2 – Blinking mixed color.



MODE 3 – Behavior according to Table 21.

MODE 4 – Behavior according to Table 22.

Note: MODE 4 is the same as MODE 3 except the 10 Mb/s and 100 Mb/s are reversed.

Table 21. MODE 3 Behavior

Status	LED[5] LED[3] LED[1]	LED[4] LED[2] LED[0]
1000 Mb/s Link - No Activity	Off	Solid On
1000 Mb/s Link - Activity	Off	Blink
100 Mb/s Link - No Activity	Solid Mix	Solid Mix
100 Mb/s Link - Activity	Blink Mix	Blink Mix
10 Mb/s Link - No Activity	Solid On	Off
10 Mb/s Link - Activity	Blink	Off
No link	Off	Off

Table 22. MODE 4 Behavior

Status	LED[5] LED[3] LED[1]	LED[4] LED[2] LED[0]
1000 Mb/s Link - No Activity	Off	Solid On
1000 Mb/s Link - Activity	Off	Blink
100 Mb/s Link - No Activity	Solid On	Off
100 Mb/s Link - Activity	Blink	Off
10 Mb/s Link - No Activity	Solid Mix	Solid Mix
10 Mb/s Link - Activity	Blink Mix	Blink Mix
No link	Off	Off

3.18.1 Behavior in Various Low Power States

When the PHY is in software reset, powered down, or the cable detect state, the LEDs are set to the inactive state in order to save power unless overridden by the designer.

If the LED[x] control (Registers 16_3.11:8, 16_3.7:4, and 16_3.3:0 is set to 10xxb (forced mode) then the LEDs are forced regardless of the power state. This enables designers to have direct control over the LEDs. Note that the LED does not BLINK when the PHY is in low power state.

If the LED[x] control is not set to 10xxb, then the LEDs are forced off when the PHY is in the software reset, power down state or in the cable detect state. The off value for LED[x] is defined by the setting in registers 17_3.7:6, 17_3.5:4, 17_3.3:2, 17_3.1:0, 19_3.11:10, and 19_3.9:8.

When the PHY is in the powered up state and not in the cable detect state, the LED[x] operates normally.

3.18.2 Serial LED

When the CLK_SEL[1:0] is set to 10b at the de-assertion of hardware reset and the PTP_EN configuration bit is set to 1b, the serial LED mode is enabled. All regular LED functions are disabled and registers 16_3, 17_3, 18_3, and 19_3 are ignored.

In the serial LED mode the data is clocked through a shift register and the shifted values are output on the 16 LED pins when strobed.

CONFIG[1] is used as the data input.

CONFIG[2] is used as the clock.

CLK_SEL[0] is used as the strobe. Note that this pin must be set to 0b at the de-assertion of hardware reset to enable the serial LED mode.

In addition to the above four pins register 27_4.9 is used to control whether all 16 LEDs are tri-stated or not.

0b = Tristate

1b = Output (hardware default)

Register 27_4.11:10 determines how many LEDs per port are in the shift chain. In all cases, P0_LED[0] is the last bit to be shifted in. (P3_LED[3] is the first bit to be shifted in if 27_4.11:10 = 11).

00b = Shift through P0_LED[0], P1_LED[0], P2_LED[0], P3_LED[0].

01b = Shift through P0_LED[0], P0_LED[1], P1_LED[0], P1_LED[1], P2_LED[0], P2_LED[1], P3_LED[0], P3_LED[1].

10b = Shift through P0_LED[0], P0_LED[1], P0_LED[2], P1_LED[0], P1_LED[1], P1_LED[2], P2_LED[0], P2_LED[1], P2_LED[2], P3_LED[0], P3_LED[1], P3_LED[2].

11b = Shift through P0_LED[0], P0_LED[1], P0_LED[2], P0_LED[3], P1_LED[0], P1_LED[1], P1_LED[2], P1_LED[3], P2_LED[0], P2_LED[1], P2_LED[2], P2_LED[3], P3_LED[0], P3_LED[1], P3_LED[2], P3_LED[3]. (hardware default).

Register 27_4.13:12 determines at what point in the shift register chain should be output to RCLK.

00b = Output after port 0.

01b = Output after port 1.

10b = Output after port 2.

1b1 = Output after port 3. (hardware default)

The initial value of the shift registers and the LED outputs are that LED[1] and LED[3] output 0 and LED[0] and LED[2] output 1 for all ports.

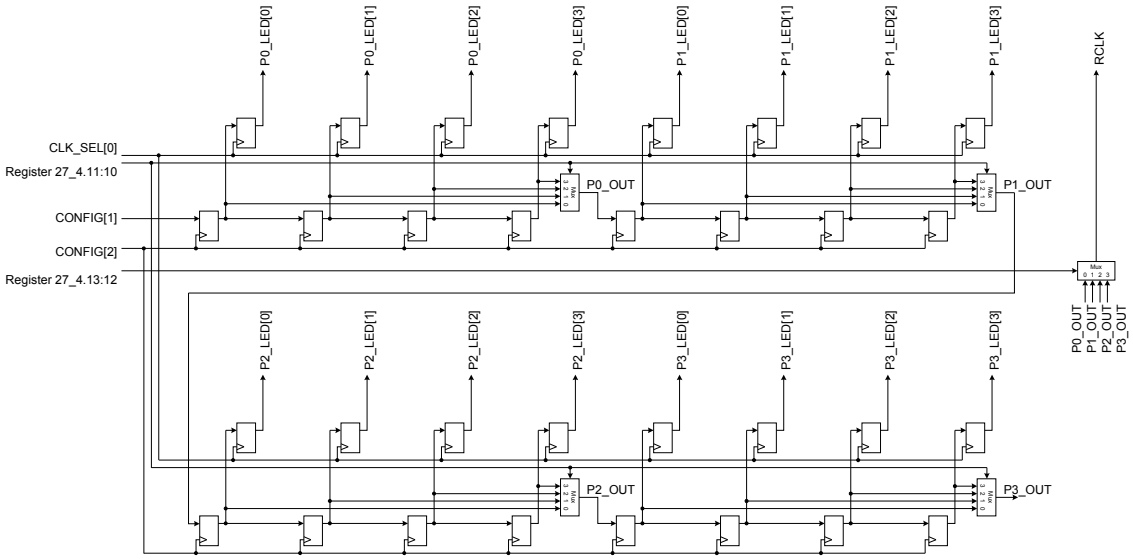


Figure 15. Serial LED

3.19 IEEE 1149.1 and 1149.6 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The IEEE 1149.6 standard defines a test access port and boundary-scan architecture for AC coupled signals.

This standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The I347-AT4 implements the instructions listed in Table 23. Upon reset, ID_CODE instruction is selected. The PROG_HYST is a proprietary command used to adjust the test receiver hysteresis threshold. The instruction opcodes are shown in Table 23.

Table 23. TAP Controller OPCodes

Instruction	OpCode
EXTEST	0x00000000
SAMPLE/PRELOAD	0x00000001
CLAMP	0x00000010
HIGH-Z	0x00000011
ID_CODE	0x00000100
EXTEST_PULSE	0x00000101
EXTEST_TRAIN	0x00000110
PROG_HYST	0x00001000
BYPASS	0x11111111

The I347-AT4 reserves five pins called the Test Access Port (TAP) to provide test access: Test Mode Select Input (TMS), Test Clock Input (TCK), Test Data Input (TDI), and Test Data Output (TDO), and Test Reset Input (TRSTn). To ensure race-free operation all input and output data is synchronous with the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details refer to the IEEE 1149.1 Boundary Scan Architecture document.

3.19.1 BYPASS Instruction

The BYPASS instruction uses the bypass register. This register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the I347-AT4 when test operation is not required. This arrangement allows rapid movement of test data to and from other testable devices in the system.

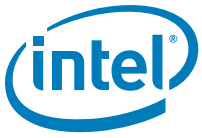
3.19.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction enables scanning of the boundary-scan register without causing interference to the normal operation of the I347-AT4. Two functions are performed when this instruction is selected: sample and preload.

Sample enables a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload enables an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This step ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

Table 24. Boundary Scan Chain Order

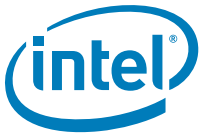


Pin	I/O
P3_LED[3]	Output
P3_LED[2]	Output
P3_LED[1]	Output
P3_LED[0]	Output
P3_LED[3]	Output Enable
P3_LED[2]	Output Enable
P3_LED[1]	Output Enable
P3_LED[0]	Output Enable
P2_LED[3]	Output
P2_LED[2]	Output
P2_LED[1]	Output
P2_LED[0]	Output
P2_LED[3]	Output Enable
P2_LED[2]	Output Enable
P2_LED[1]	Output Enable
P2_LED[0]	Output Enable
P1_LED[3]	Output
P1_LED[2]	Output
P1_LED[1]	Output
P1_LED[0]	Output
P1_LED[3]	Output Enable
P1_LED[2]	Output Enable
P1_LED[1]	Output Enable
P1_LED[0]	Output Enable
P0_LED[3]	Output
P0_LED[2]	Output
P0_LED[1]	Output
P0_LED[0]	Output
P0_LED[3]	Output Enable
P0_LED[2]	Output Enable
P0_LED[1]	Output Enable
P0_LED[0]	Output Enable
CONFIG[3]	Input
CONFIG[2]	Input
CONFIG[1]	Input
CONFIG[0]	Input
MDC	Input
MDIO	Input
MDIO	Output
MDIO	Output Enable
RESET	Input

Pin	I/O
CLK_SEL[1]	Input
CLK_SEL[0]	Input
RCLK1	Output
RCLK1	Output Enable
RCLK2	Output
RCLK2	Output Enable
INTn	Output
INTn	Output Enable
P3_S_OUTP/P3_S_OUTN	Output Enable
P3_S_OUTP/P3_S_OUTN	Output
Port 3 AC/DC Select	AC/DC Select
P3_S_INN	Input
P3_S_INP	Input
P2_S_OUTP/P2_S_OUTN	Output Enable
P2_S_OUTP/P2_S_OUTN	Output
Port 2 AC/DC Select	AC/DC Select
P2_S_INN	Input
P2_S_INP	Input
Q_OUTN/Q_OUTP	Output Enable
Q_OUTN/Q_OUTP	Output
Q_INP	Input
Q_INN	Input
P1_S_OUTP/P1_S_OUTN	Output Enable
P1_S_OUTP/P1_S_OUTN	Output
Port 1 AC/DC Select	AC/DC Select
P1_S_INN	Input
P1_S_INP	Input
P0_S_OUTP/P0_S_OUTN	Output Enable
P0_S_OUTP/P0_S_OUTN	Output
Port 0 AC/DC Select	AC/DC Select
P0_S_INN	Input
P0_S_INP	Input

Table 25. Boundary Scan Exclusion List

Pin	I/O
P0_MDIP[0]	Analog
P0_MDIN[0]	Analog
P0_MDIP[1]	Analog
P0_MDIN[1]	Analog
P0_MDIP[2]	Analog
P0_MDIN[2]	Analog



Pin	I/O
P0_MDIP[3]	Analog
P0_MDIN[3]	Analog
P1_MDIP[0]	Analog
P1_MDIN[0]	Analog
P1_MDIP[1]	Analog
P1_MDIN[1]	Analog
P1_MDIP[2]	Analog
P1_MDIN[2]	Analog
P1_MDIP[3]	Analog
P1_MDIN[3]	Analog
P2_MDIP[0]	Analog
P2_MDIN[0]	Analog
P2_MDIP[1]	Analog
P2_MDIN[1]	Analog
P2_MDIP[2]	Analog
P2_MDIN[2]	Analog
P2_MDIP[3]	Analog
P2_MDIN[3]	Analog
P3_MDIP[0]	Analog
P3_MDIN[0]	Analog
P3_MDIP[1]	Analog
P3_MDIN[1]	Analog
P3_MDIP[2]	Analog
P3_MDIN[2]	Analog
P3_MDIP[3]	Analog
P3_MDIN[3]	Analog
XTAL_IN	Analog
XTAL_OUT	Analog
SCLK	Analog
RSET	Analog
TSTPT	Analog
TSTPTF	Analog
HSDACP	Analog
HSDACN	Analog
TEST[1:0]	Analog
V18_L	Analog
V18_R	Analog
V12_EN	Analog
VDDOL	Power
VDDOR	Power
VDDOM	Power

Pin	I/O
VDDC	Power
AVDDH	Power
DVDD	Power
VSS	Power

3.19.3 EXTEST Instruction

The EXTEST instruction enables circuitry external to the I347-AT4 (typically the board interconnections) to be tested. Prior to executing the EXTEST instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/ preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the I347-AT4 to its external connections. Note that the S_OUTP/N and Q_OUTP/N pins are driven to static levels. The positive and negative legs of the S_OUTP/N and Q_OUTP/N pins are controlled via a single boundary scan cell.The positive leg outputs the level specified by the boundary scan cell while the negative leg outputs the opposite level.

3.19.4 The CLAMP Instruction

The CLAMP instruction enables the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins do not change while the clamp instruction is selected.

3.19.5 The HIGH-Z Instruction

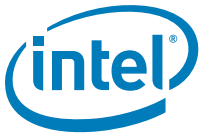
The HIGH-Z instruction places all of the digital component system logic outputs in an inactive high-impedance drive state. In this state, an in-circuit test system might drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

3.19.6 ID CODE Instruction

The ID CODE contains the manufacturer identity, part and version.

Table 26. ID CODE Instruction

Version	Part Number	Manufacturer Identity	
Bit 31 to 28	Bit 27 to 12	Bit 11 to 1	0
0000	0000000000001110	00111101110	1



3.19.7 EXTEST_PULSE Instruction

The AC or DC JTAG test modes can be selected for each port individually by scanning in the desired bit value into AC/DC select scan registers shown in the scan chain (Table 24). When the AC/DC select is set to DC the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction except for the behavior of the S_OUTP/N and Q_OUTP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the S_OUTP and Q_OUTP pins output the level specified by the test stimulus and S_OUTN and S_CLKN pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the S_OUTN and Q_OUTN pins output the level specified by the test stimulus and S_OUTP and Q_OUTP pins output the opposite level.

When the TAP controller exits the Run-Test/Idle state, the S_OUTP and Q_OUTP pins again output the level specified by the test stimulus and S_OUTN and Q_OUTN pins output the opposite level.

3.19.8 EXTEST_TRAIN Instruction

When the AC/DC select is set to DC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction except for the behavior of the S_OUTP/N and Q_OUTP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the S_OUTP and Q_OUTP pins output the level specified by the test stimulus and S_OUTN and Q_OUTN pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the S_OUTP/N and Q_OUTP/N will toggle between inverted and non-inverted levels on the falling edge of TCK. This toggling will continue for as long as the TAP controller remains in the Run-Test/Idle state.

When the TAP controller exits the Run-Test/Idle state, the S_OUTP and Q_OUTP pins again output the level specified by the test stimulus and S_OUTN and Q_OUTN pins output the opposite level.

3.19.9 AC-JTAG Fault Detection

The fault detection across AC coupled connections can be detected with a combination of (DC) EXTEST and any one of the AC JTAG commands. The AC coupled connection is shown in Figure 16. The fault signature is listed in Table 27. Column 1 lists the fault type.

Columns 2 to 5 lists the behavior when both the transmitter and receiver are running the EXTEST_TRAIN and EXTEST_PULSE commands. Column 2 shows the expected value captured by the boundary scan cell that is connected to the test receiver, which is connected to the positive input when a negative differential pulse is transmitted. Column 3 is the same as column 2 except for the negative input. Columns 4 and 5 are similar to columns 2 and 3 except a positive differential pulse is transmitted.

Columns 6 to 9 is similar to columns 2 to 5 except both the transmitter and receiver are running the (DC) EXTEST command.

While it is not possible to identify precisely which fault is occurring based on the fault signature, the signature to the no fault condition is unique when the (DC) EXTEST command is run with at least one of the EXTEST_TRAIN, or EXTEST_PULSE commands. Note that running only AC JTAG commands is not sufficient since the no fault condition signature is not distinguishable from the TX to RX short (see shaded cells in Table 27).

Table 27. AC Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
TX+ Open	0b	X	0b	X	1b	X	1b	X
TX- Open	X	0b	X	0b	X	1b	X	1b
RX+ Open	0b	X	0b	X	1b	X	1b	X
RX- Open	X	0b	X	0b	X	1b	X	1b
TX+ short to power	0b[1]	X	0b[1]	X	1b	X	1b	X
TX- short to power	X	0b[1]	X	0b[1]	X	1b	X	1b
RX+ short to power	0b[1]	X	0b[1]	X	1b	X	1b	X
RX- short to power	X	0b[1]	X	0b[1]	X	1b	X	1b
TX+ short to ground	0b	X	0b	X	1b	X	1b	X
TX- short to ground	X	0b	X	0b	X	1b	X	1b
RX+ short to ground	0b	X	0b	X	0b	X	0b	X
RX- short to ground	X	0b	X	0b	X	0b	X	0b
TX+ short to TX-	2	2	2	2	1b	1b	1b	1b
RX+ short to RX-	2	2	2	2	1b	1b	1b	1b
TX+ short to RX-	X	0b	X	1b	X	0b	X	1b

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
TX- short to RX+	1b	X	0b	X	1b	X	0b	X
TX+ short to RX+	0b	X	1b	X	0b	X	1b	X
TX- short to RX-	X	1b	X	0b	X	1b	X	0b
No Fault	0b	1b	1b	0b	1b	1b	1b	1b

1. A solid short to power is assumed. If the short has high inductance then a pulse can still be sent at the receiver and is mistaken as a good connection.
2. A short on a positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out then the output on both legs is zero. If one driver dominates the other, then both legs are either both one or both zero. In any case, the result is that both legs have same value.

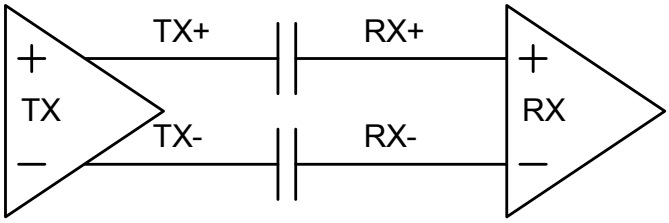


Figure 16. AC Coupled Connection

The fault detection across DC coupled connections can be detected with any one of the AC JTAG or (DC) EXTEST commands. The DC coupled connection is shown in Figure 17. The fault signature is listed in Table 28.

Table 28. DC Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
RX+ Open	0b	X	0b	X	1b	X	1b	X
RX- Open	X	0b	X	0b	X	1b	X	1b
RX+ short to power	0b[1]	X	0b[1]	X	1b	X	1b	X
RX- short to power	X	0b[1]	X	0b[1]	X	1b	X	1b
RX+ short to ground	0b	X	0b	X	0b	X	0b	X
RX- short to ground	X	0b	X	0b	X	0b	X	0b
RX+ short to RX-	2	2	2	2	2	2	2	2

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
No Fault	0b	1b	1b	0b	0b	1b	1b	0b

1. A solid short to power is assumed. If the short has high inductance then a pulse can still be sent at the receiver and is mistaken as a good connection.
2. A short on the positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out then output on both legs is zero. If one driver dominates the other then both legs are either both one or both zero. In any case, the result is that both legs has the same value.

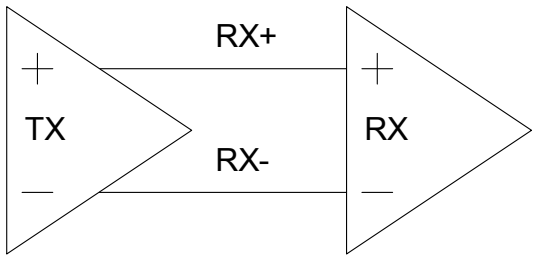


Figure 17. DC Coupled Connection

3.20 Interrupt

The INTn pin supports the interrupt function. INTn is active low.

Registers 18_0, 18_1, 18_2, 18_4, and 26_6.7 are the Interrupt Enable registers.

Registers 19_0, 19_1, 19_2, 19_4, and 26_6.6 are the Interrupt Status registers.

Registers 23_0 is the Interrupt Status summary registers. Register 23_0 lists the ports that have active interrupts. Register 23_0 provides a quick way to isolate the interrupt so that the MAC or switch does not have to poll register 19 for all ports. Reading register 23_0 does not de-assert the INTn pin. Note that register 23_0 can be accessed by reading register 23_0 using the PHY address of any of the four ports.

The various pages of register 18 and 26_6.7 are used to select the interrupt events that can activate the interrupt pin. The interrupt pin will be activated if any of the selected events on any page of register 18 or 26_67 occurs.

If a certain interrupt event is not enabled for the INTn pin, it will still be indicated by the corresponding interrupt status bits if the interrupt event occurs. The unselected events do not cause the INTn pin to be activated.

3.21 Configuring The I347-AT4

The I347-AT4 can be configured two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

All hardware configuration options can be overwritten by software except PHYADR[4:2] and PHY_ORDER.

3.21.1 Hardware Configuration

After the deassertion of RESETn, the I347-AT4 is hardware configured.

The I347-AT4 is configured through the CONFIG[3:0] pins and CLK_SEL[1:0].

CLK_SEL[1:0] are used to select the reference clock input option as well as the serial LED feature:

Table 29. CLK_SEL[1:0] Configuration Settings

CLK_SEL[1:0]	Clock Input	SER_LED	SER_LED Feature
10b	25 MHz XTAL_IN/XTAL_OUT	0b	Not supported
		1b	Not supported
11b	25 MHz XTAL_IN/XTAL_OUT	0b	Not supported
		1b	

Each CONFIG[3:0] pin is used to configure four bits. The 4-bit value is set depending on what is connected to the CONFIG pins soon after the deassertion of hardware reset. The 4-bit mapping is shown in Table 30.

Table 30. Four Bit Mapping

Pin	Bit 3, 2,1,0
VSS	0000
P0_LED[1]	0001
P0_LED[2]	0010
P0_LED[3]	0011
P1_LED[0]	0100
P1_LED[1]	0101
P1_LED[2]	0110
P1_LED[3]	0111
P2_LED[0]	1000
P2_LED[1]	1001
P2_LED[2]	1010
P2_LED[3]	1011
P3_LED[0]	1100
P3_LED[1]	1101
P3_LED[2]	1110
VDDO	1111
P0_LED[0]	Reserved
P3_LED[3]	Reserved

The four bits for each CONFIG pin is mapped as listed in Table 30. CONFIG[2:1] are reserved and should not be used as configuration pins.

3.21.2 Configuration Mapping

Table 31. Configuration Mapping

Pin	SER_LED	Bit3	Bit 2	Bit1	Bit 0
CONFIG[0]	X	PHY_ORDER	PHYAD[4]	PHYAD[3]	PHYAD[2]
CONFIG[1]	0b	SEL_MS	ENA_PAUSE	C_ANEG[1]	C_ANEG[0]
	1b	Reserved			
CONFIG[2]	0b	S_ANEG	ENA_XC	DIS_SLEEP	PDOWN
	1b	Reserved			
CONFIG[3]	X	Reserved, set to 0b	MODE[2]	MODE[1]	MODE[0]

Table 32. I347-AT4 PDOWN Register Setting as a Function of MODE[2:0]

MODE[2:0]	PDOWN	0_0.11	0_1.11	0_4.11
xxx	0b	0b	0b	0b
000b	1b	1b	0b	0b
001b	1b	1b	0b	0b
010b	1b	0b	1b	0b
011b	1b	0b	1b	0b
100b	1b	0b	1b	0b
101b	1b	0b	0b	1b
110b	1b	1b	1b	0b
111b	1b	1b	1b	0b

3.21.3 Software Configuration - Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u clause 22. MDC is the management data clock input and, it can run from DC to a maximum rate of 12 MHz. At high MDIO fanouts the maximum rate can be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 KΩ to 10 KΩ that pulls the MDIO high during the idle and turnaround.

PHY address is configured during the hardware reset sequence. Refer to Section 3.21.1 for more information on how to configure PHY addresses.

Typical read and write operations on the management interface are shown in Figure 18 and Figure 19. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in Section 4.0.

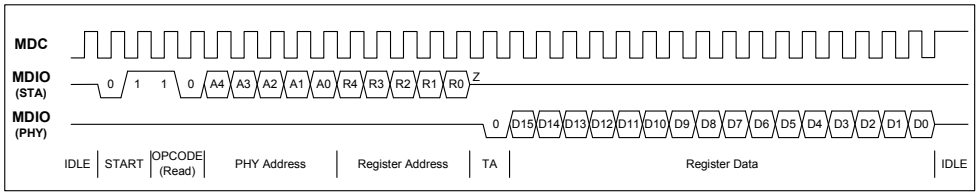


Figure 18. Typical MDC/MDIO Read Operation

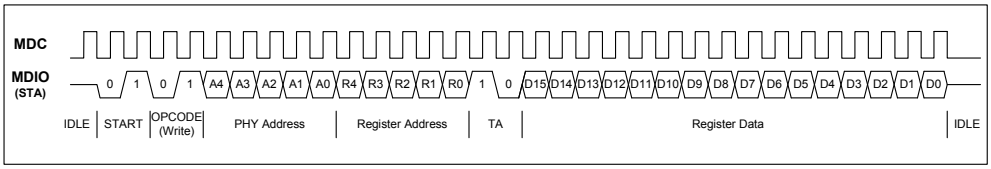


Figure 19. Typical MDC/MDIO Write Operation

Table 33 is an example of a read operation.

Table 33. Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	OpCode Read = 10b Write = 01b	5-Bit PHY Device Address	5-Bit PHY Register Address (MSB)	2-Bit Turn around Read = z0b Write = 10b	16-Bit Data Field	Idle
11111111b	01b	10b	01100b	00000b	z0b	0001001100000000b	11111111b

3.21.3.1 Extended Register Access

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. For register address 0 to 21, and 23 to 28 register 22 bits 7 to 0 are used to specify the page. For registers 30 and 31 register 29 bits 5:0 are used to specify the page. There is no paging for registers 22 and 29.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 16 page 2 bits 5 to 2 is specified as 16_2.5:2.

Register 16 page 2 bits 5 is specified as 16_2.5.

Currently there it takes four MDIO write commands to write the same register to the same value on all four ports. Register 22.15:14 can be used to selectively ignore PHYAD[4:2] and PHYAD[1:0] as listed in Table 34 so that the same register address can be written to all four ports in one MDIO write command. PHYAD[4:0] is still decoded for read commands.

Care must be taken to setup multiple port write. To enable the concurrent write access write register 22 four times in a row with bit 14 set to 1b – once to each PHYAD[4:0]. The values written on all 16 bits must be the same otherwise unpredictable behavior can occur.

Once the four write commands to register 22 are issued, all subsequent writes are concurrent to all ports including writes to register 22.

Concurrent write access continues as long as every write to register 22 sets 22.14 to a 1b.

To disable concurrent write access, write register 22:14 to 0b.

Table 34. Page Address

Register	Function	Setting	Mode	HW Rst	SW Rst
22.15	Ignore PHYAD[4:2]	0b = Use PHYAD[4:2] to decode write commands 1b = Ignore PHYAD[4:2] to decode write commands	R/W	0b	Retain
22.14	Ignore PHYAD[1:0]	0b = Use PHYAD[1:0] to decode write commands 1b = Ignore PHYAD[1:0] to decode write commands	R/W	0b	Retain
22.13:8	Reserved	00000000b	RO	0b	0b
22.7:0	Page select for registers 0 to 28	Page Number	R/W	00b	Retain

3.21.3.2 Preamble Suppression

The I347-AT4 is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

3.22 Reference Clock

The I347-AT4 can use a 25 MHz crystal or 25 MHz oscillator as the reference clock.. The connection to the reference clock pins are shown in Section 35. The reference frequency used must be indicated by the CLK_SEL[1:0] pins.

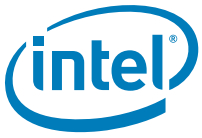
Table 35. Reference Clock Pin Connections

Reference Source	CLK_SEL[1:0]	XTAL_IN	XTAL_OUT	REF_CLKP	REF_CLKN
25 MHz Crystal	1xb	Connect to Crystal	Connect to Crystal	Pull-up to 1.9V with 1 KΩ resistor	Pull-down to GND with 1 KΩ resistor
25 MHz Oscillator	1xb	Connect to Driver	Leave Floating	Pull-up to 1.9V with 1 KΩ resistor	Pull-down to GND with 1 KΩ resistor

3.23 Temperature Sensor

The I347-AT4 contains an internal temperature sensor. Register 26_6.4:0 reports the die temperature and is updated approximately once per second. The result can be read back on any port as long as the port is not disabled (such as register 0.11 = 1b).

An interrupt can be generated when the temperature exceeds a certain threshold.



Register 26_6.6 is set high each time the temperature is greater than or equal to the value programmed in register 26_6.12:8. Register 26_6.6 remains high until read.

Register 26_6.7 controls whether the interrupt pin is asserted when register 26_6.6 is high.

The interrupt should be enabled on only one port since there is only one temperature sensor for the entire chip.

Table 36. Temperature Sensor

Register	Function	Setting	Mode	HW Rst	SW Rst
26_6.12:8	Temperature Threshold	Temperature in °C = 5 x 26_6.4:0 - 25. For example, for 100 °C the value is 11001b.	R/W	11001b	Retain
26_6.7	Temperature Sensor Interrupt Enable	1b = Interrupt Enable. 0b = Interrupt Enable.	R/W	0b	Retain
26_6.6	Temperature Sensor Interrupt	1b = Temperature Reached Threshold. 0b = Temperature Below Threshold.	RO, LH	0b	0b
26_6.4:0	Temperature Sensor	Temperature in °C = 5 x 26_6.4:0 - 25. For example, for 100 °C the value is 11001b.	RO	xxxxx	xxxxx

3.24 Power Supplies

The I347-AT4 requires two power supplies: 1.9V and 1.0V. If a 3.3V I/O is required (such as, for JTAG or MDC/MDIO pins), then a third supply of 3.3V is required.

For I/Os to be 3.3V tolerant, VDDO must be 3.3V.

3.24.1 AVDDH

AVDDH is used as the 1.9V analog supply.

3.24.2 VDDC

VDDC is used as the 1.9V XTAL_IN/OUT supply. These inputs are not 3.3V tolerant.

3.24.3 DVDD

DVDD is used for the digital logic. DVDD is the 1.0V digital supply.

3.24.4 VDDOL

VDDOL supplies the digital I/O pins for RESETn, LED, CONFIG, and INTn.

V18_L should be tied to VSS if the VDDOL voltage is set to 3.3V.

V18_L should be floating if the VDDOL voltage is set to 1.9V.

3.24.5 VDDOR

VDDOR supplies the digital I/O pins for TDO, TDI, TMS, TCK, TRSTn, REF_CLKP/N, or CLK_SEL[1:0].

V18_R should be tied to VSS if the VDDOR voltage is set to 3.3V.

V18_R should be floating if the VDDOR voltage is set to 1.9V.

3.24.6 VDDOM

VDDOM supplies the digital I/O pins for MDC, MDIO, and TEST.

V12_EN should be tied to VSS if the VDDOM voltage is set to 3.3V.

V12_EN should be floating if the VDDOM voltage is set to 1.9V.

3.24.7 Power Supply Sequencing

On power-up, no special power supply sequencing is required.

3.25 Clocking Support

There two components to clocking support: Recovered Clock and Reference Clock Select. The first is to output a recovered clock. The second is to select between the local reference clock and a cleaned-up recovered clock.

3.25.1 Recovered Clock

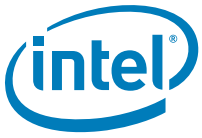
The RCLK1 and RCLK2 pins of the chip outputs either a 125 MHz or 25 MHz clock that is based on the 125 MHz recovered clock on the copper receive path when linked to 1000BASE-T or 100BASE-TX. If a 25 MHz clock is selected, the 125 MHz recovered clock is internally divided by 5 with 60% low and 40% high.

Register 16_2.11 selects whether RCLK outputs 25 MHz XTAL clock or drives LOW when the link is down or when the copper receiver is linked to 10BASE-T.

- 0b = RCLK outputs 25 MHz XTAL clock during link down or 10BASE-T
- 1b = RCLK drives LOW during link down or 10BASE-T

RCLK1 pin is enabled when register 16_2.8 is set to 1b, and RCLK2 pin is enabled when register 16_2.9 is set to 1b. Each of these bits should be set to 1b for only one port (16_2.8 set to 1b in port 0 and 16_2.9 set to 1b for port 1). If the bit is set high for multiple ports then the highest numbered physical port that is enabled is selected. The highest numbered physical port is defined to be the port connected to MDIP/N3 and not necessarily the port with the highest PHYAD[4:0] value. (the PHY_ORDER setting affects the PHYAD[1:0] setting.)

Register 16_2.12 selects whether RCLK 25 MHz outputs 25 MHz or 125 MHz. 0b = 25 MHz, 1 = 125 MHz.



3.25.2 Reference Clock Select

The 25 MHz reference clock source to the copper unit is independently selectable per port. On hardware reset XTAL_IN or REF_CLKP/N is selected as the reference clock source for all ports. SCLK can be selected as the reference clock source on a per port basis.

Register 16_2.7 selects whether the reference clock for the copper interface is based on XTAL_IN/REF_CLKP/N or SCLK. 0b = XTAL_IN or REF_CLKP/N, 1b = SCLK.

Register 16_2.6 selects whether the reference clock for the 1.25 GHz SERDES interface is based on XTAL_IN/REF_CLKP/N or SCLK. 0 = XTAL_IN or REF_CLKP/N, 1 = SCLK.

The CLK_SEL[1:0] must be set to 11b in order to do the reference clock selection.

Since changing the reference clocks disturbs the PHY, a software reset must be issued before any change to the clock select takes place.

4.0 Programmer's Visible State

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. For register address 0 to 21, and 23 to 28 register 22 bits 7 to 0 are used to specify the page. For registers 30 and 31 register 29 bits 5:0 are used to specify the page. There is no paging for registers 22 and 29.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 16 page 2 bits 5 to 2 is specified as 16_2.5:2.

Register 16 page 2 bits 5 is specified as 16_2.5.

Register 2 bit 3 to 0 is specified as 2.3:0.

Note that in this context the setting of the page register (register 22) has no effect.

Register 2 bit 3 is specified as 2.3.

Table 37 lists the register types used in the register map.

Table 37. Register Types

Type	Description
C	Clear after read.
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
Retain	The register value is retained after software reset is executed.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROS	Read only, Set high after read.
ROC	Read only clear. After read, register field is cleared.
RW	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All field bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
RWR	Read/Write clear on read. All field bits are readable and writable. After reset, register field is cleared to 0.

Type	Description
RWS	Read/Write set. All field bits are readable and writable. After reset, register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field doesn't take effect until soft reset is executed.
WO	Write only. Reads to this type of register field return undefined data.

For all binary equations appearing in the register map, the symbol | is equal to a binary OR operation.

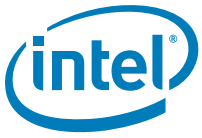
4.1 Register Map

Table 38 lists the registers used in the I347-AT4.

Table 38. I347-AT4 Register Names and Addresses

Register Name	Register Address	Page
Copper Control Register	Page 0, Register 0	65
Copper Status Register	Page 0, Register 1	66
PHY Identifier 1	Page 0, Register 2	67
PHY Identifier 2	Page 0, Register 3	68
Copper Auto-Negotiation Advertisement Register	Page 0, Register 4	68
Copper Link Partner Ability Register - Base Page	Page 0, Register 5	70
Copper Auto-Negotiation Expansion Register	Page 0, Register 6	71
Copper Next Page Transmit Register	Page 0, Register 7	72
Copper Link Partner Next Page Register	Page 0, Register 8	72
1000BASE-T Control Register	Page 0, Register 9	73
1000BASE-T Status Register	Page 0, Register 10	74
Extended Status Register	Page 0, Register 15	74
Copper Specific Control Register 1	Page 0, Register 16	75
Copper Specific Status Register 1	Page 0, Register 17	76
Copper Specific Interrupt Enable Register	Page 0, Register 18	77
Copper Interrupt Status Register	Page 0, Register 19	78
Copper Specific Control Register 2	Page 0, Register 20	79
Copper Specific Receive Error Counter Register	Page 0, Register 21	80
Page Address	Page Any, Register 22	80
Global Interrupt Status	Page 0, Register 23	80
Copper Specific Control Register 3	Page 0, Register 26	80

Register Name	Register Address	Page
PHY Identifier	Page 1, Register 2	81
PHY Identifier	Page 1, Register 3	81
Extended Status Register	Page 1, Register 15	81
PRBS Control	Page 1, Register 23	82
PRBS Error Counter LSB	Page 1, Register 24	82
PRBS Error Counter MSB	Page 1, Register 25	82
MAC Specific Control Register 1	Page 2, Register 16	83
MAC Specific Interrupt Enable Register	Page 2, Register 18	83
MAC Specific Status Register	Page 2, Register 19	84
Copper RX_ER Byte Capture	Page 2, Register 20	84
MAC Specific Control Register 2	Page 2, Register 21	85
LED[3:0] Function Control Register	Page 3, Register 16	85
LED[3:0] Polarity Control Register	Page 3, Register 17	87
LED Timer Control Register	Page 3, Register 18	87
LED[5:4] Function Control and Polarity Register	Page 3, Register 19	88
Cable Tester TX to MDI[0] Rx Coupling	Page 5, Register 16	90
Cable Tester TX to MDI[1] Rx Coupling	Page 5, Register 17	91
Cable Tester TX to MDI[2] Rx Coupling	Page 5, Register 18	92
Cable Tester TX to MDI[3] Rx Coupling	Page 5, Register 19	92
1000BASE-T Pair Skew Register	Page 5, Register 20	93
1000BASE-T Pair Swap and Polarity	Page 5, Register 21	93
Cable Tester Control	Page 5, Register 23	94
Cable Tester Sample Point Distance	Page 5, Register 24	95
Cable Tester Cross Pair Positive Threshold	Page 5, Register 25	95
Cable Tester Same Pair Impedance Positive Threshold 0 and 1	Page 5, Register 26	95
Cable Tester Same Pair Impedance Positive Threshold 2 and 3	Page 5, Register 27	96
Cable Tester Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control	Page 5, Register 28	96
Packet Generation	Page 6, Register 16	97
CRC Counters	Page 6, Register 17	97



Register Name	Register Address	Page
Checker Control	Page 6, Register 18	97
General Control Register	Page 6, Register 20	98
Late Collision Counters 1 & 2	Page 6, Register 23	98
Late Collision Counters 3 & 4	Page 6, Register 24	99
Late Collision Window Adjust/Link Disconnect	Page 6, Register 25	99
Misc Test	Page 6, Register 26	99

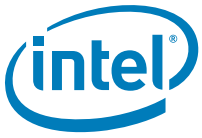
4.1.1 Copper Control Register - Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Reset	R/W, SC	0x0	SC	Copper Software Reset. Affects pages 0, 2, 3, 5, and 7. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. Loopback speed is determined by Registers 21_2.2:0. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
12	Auto-Negotiation Enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 is set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Power Down	R/W	See Descr	Retain	Power down is controlled via register 0_0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. Upon hardware reset this bit takes on the value of PDOWN and (MODE[2:0] = 00x or 11x) 1 = Power down 0 = Normal operation
10	Isolate	RO	0x0	0x0	This bit has no effect.
9	Restart Copper Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Copper Duplex Mode	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation 1 = Full-duplex 0 = Half-duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved	RO	0x00	0x00	Will always be 0.

4.1.2 Copper Status Register - Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	0x0	0x0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	Reserved	RO	0x1	0x1	Reserved



Bits	Field	Mode	HW Rst	SW Rst	Description
13	Reserved	RO	0x1	0x1	Reserved
12	10 Mbps Full-Duplex	RO	0x1	0x1	1 = PHY able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	0x1	0x1	1 = PHY able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	0x0	0x0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	0x0	0x0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	0x1	0x1	1 = Extended status information in Register 15
7	Reserved	RO	0x0	0x0	Must always be 0.
6	MF Preamble Suppression	RO	0x1	0x1	1 = PHY accepts management frames with preamble suppressed
5	Copper Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Copper Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	0x1	0x1	1 = PHY able to perform Auto-Negotiation
2	Copper Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Jabber Detect	RO,LH	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
0	Extended Capability	RO	0x1	0x1	1 = Extended register capabilities

4.1.3 PHY Identifier 1 - Page 0, Register 2

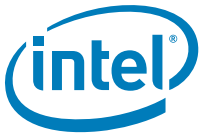
Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

4.1.4 PHY Identifier 2 - Page 0, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	0x03	0x03	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit24
9:4	Model Number	RO	0x1C	0x1C	Model Number 011100
3:0	Revision Number	RO	See Descr	See Descr	Rev Number Contact FAEs for information on the device revision number.

4.1.5 Copper Auto-Negotiation Advertisement Register - Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	0x0	0x0	Must be 0.
13	Remote Fault	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Reserved	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down Reserved bit is R/W to allow for forward compatibility with future IEEE standards.

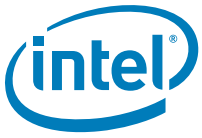


Bits	Field	Mode	HW Rst	SW Rst	Description
11	Asymmetric Pause	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of ENA_PAUSE. 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of ENA_PAUSE. 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	R/W	0x0	Retain	0 = Not capable of 100BASE-T4
8	100BASE-TX Full-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit takes on the value of C_ANEG[1]. 1 = Advertise 0 = Not advertised
7	100BASE-TX Half-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit takes on the value of C_ANEG[1]. 1 = Advertise 0 = Not advertised

Bits	Field	Mode	HW Rst	SW Rst	Description
6	10BASE-TX Full-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit takes on the value of C_ANEG[1]. 1 = Advertise 0 = Not advertised
5	10BASE-TX Half-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit takes on the value of C_ANEG[1]. 1 = Advertise 0 = Not advertised
4:0	Selector Field	R/W	0x01	Retain	Selector Field mode 00001 = 802.3

4.1.6 Copper Link Partner Ability Register - Base Page - Page 0, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
13	Remote Fault	RO	0x0	0x0	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Technology Ability Field	RO	0x0	0x0	Received Code Word Bit 12



Bits	Field	Mode	HW Rst	SW Rst	Description
11	Asymmetric Pause	RO	0x0	0x0	Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	Pause Capable	RO	0x0	0x0	Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
9	100BASE-T4 Capability	RO	0x0	0x0	Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
8	100BASE-TX Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
7	100BASE-TX Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
6	10BASE-T Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
5	10BASE-T Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
4:0	Selector Field	RO	0x00	0x00	Selector Field Received Code Word Bit 4:0

4.1.7 Copper Auto-Negotiation Expansion Register - Page 0, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.
4	Parallel Detection Fault	RO,LH	0x0	0x0	Register 6_0.4 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	Link Partner Next page Able	RO	0x0	0x0	Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	0x1	0x1	Register 6_0.2 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Local Device is Next Page able 0 = Local Device is not Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_0.1 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A New Page has been received 0 = A New Page has not been received

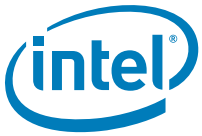
Bits	Field	Mode	HW Rst	SW Rst	Description
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	Register 6_0.0 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

4.1.8 Copper Next Page Transmit Register - Page 0, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_0 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Link fail will clear Reg 7_0. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

4.1.9 Copper Link Partner Next Page Register - Page 0, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0



4.1.10 1000BASE-T Control Register - Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	R/W	0x0	Retain	TX_CLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (Register 0_0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
12	MASTER/SLAVE Manual Configuration Enable	R/W	0x0	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/SLAVE Configuration Value	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of SEL_MS. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
10	Port Type	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. Upon hardware reset this bit takes on the value of SEL_MS. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of C_ANEG[0]. 1 = Advertise 0 = Not advertised

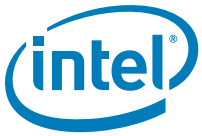
Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Reserved	R/W	0x00	Retain	0

4.1.11 1000BASE-T Status Register - Page 0, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER/SLAVE Configuration Fault	RO,LH	0x0	0x0	This register bit will clear on read. 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected
14	MASTER/SLAVE Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE
13	Local Receiver Status	RO	0x0	0x0	1 = Local Receiver OK 0 = Local Receiver is Not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote Receiver OK 0 = Remote Receiver Not OK
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T full-duplex 0 = Link Partner is not capable of 1000BASE-T full-duplex
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T half-duplex 0 = Link Partner is not capable of 1000BASE-T half-duplex
9:8	Reserved	RO	0x0	0x0	Reserved
7:0	Idle Error Count	RO, SC	0x00	0x00	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

4.1.12 Extended Status Register - Page 0, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Reserved
14	Reserved	RO	Always 0	Always 0	Reserved
13	1000BASE-T Full-Duplex	RO	Always 1	Always 1	1 =1000BASE-T full-duplex capable
12	1000BASE-T Half-Duplex	RO	Always 1	Always 1	1 =1000BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000



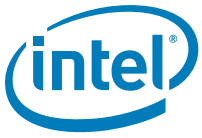
4.1.13 Copper Specific Control Register 1 - Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable Link Pulses	R/W	0x0	0x0	1 = Disable Link Pulse 0 = Enable Link Pulse
14:12	Downshift counter	R/W	0x3	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1x, 2x, ...8x is the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed. 000 = 1x 100 = 5x 001 = 2x 101 = 6x 010 = 3x 110 = 7x 011 = 4x 111 = 8x
11	Downshift Enable	R/W	0x0	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Enable downshift. 0 = Disable downshift.
10	Force Copper Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. In 1000BASE-T mode this has no effect. 1 = Force link good 0 = Normal operation
9:8	Cable Detect	R/W	See Descr.	Update	Upon hardware reset both bits takes on the inverted value of DIS_SLEEP. 0x = Off 10 = Sense only on Receive (Cable Detect) 11 = Sense and periodically transmit NLP (Cable Detect)
7	Enable Extended Distance	R/W	0x0	Retain	When using cable exceeding 100m, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 1 = Lower 10BASE-T receive threshold 0 = Normal 10BASE-T receive threshold
6:5	MDI Crossover Mode	R/W	See Descr.	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. Upon hardware reset bits defaults as follows: ENA_XC Bits 6:5 0 01 1 11 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Reserved	R/W	0x0	Retain	Set to 0
3	Copper Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable
2	Power Down	R/W	0x0	Retain	Power down is controlled via register 0_0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. 1 = Power down 0 = Normal operation

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Polarity Reversal Disable	R/W	0x0	Retain	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled The detected polarity status is shown in Register 17_0.1, or in 1000BASE-T mode, 21_5.3:0.
0	Disable Jabber	R/W	0x0	Retain	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

4.1.14 Copper Specific Status Register 1 - Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x2	Retain	These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled 17_0.11 = 1. 1 = Resolved 0 = Not resolved
10	Copper Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
8	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
7	Reserved	RO	0x0	0x0	0
6	MDI Crossover Status	RO	0x1	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI



Bits	Field	Mode	HW Rst	SW Rst	Description
5	Downshift Status	RO	0x0	0x0	1 = Downshift 0 = No Downshift
4	Copper Cable Detect Status	RO	0x0	0x0	1 = Sleep 0 = Active
3	Global Link Status	RO	0x0	0x0	1 = Copper link is up 0 = Copper link is down
2	DTE power status	RO	0x0	0x0	1 = Link partner needs DTE power 0 = Link partner does not need DTE power
1	Polarity (real time)	RO	0x0	0x0	1 = Reversed 0 = Normal Polarity reversal can be disabled by writing to Register 16_0.1. In 1000BASE-T mode, polarity of all pairs are shown in Register 21_5.3:0.
0	Jabber (real time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

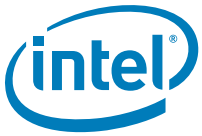
4.1.15 Copper Specific Interrupt Enable Register - Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Auto-Negotiation Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	Reserved	R/W	0x0	Retain	0
6	MDI Crossover Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5	Downshift Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Copper Cable Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3	FLP Exchange Complete but no Link Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	DTE power detection status changed interrupt enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

4.1.16 Copper Interrupt Status Register - Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Auto-Negotiation Error	RO,LH	0x0	0x0	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
14	Copper Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Copper Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Copper Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Copper Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Copper Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Copper Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	Copper False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	Reserved	RO	Always 0	Always 0	0
6	MDI Crossover Changed	RO,LH	0x0	0x0	1 = Crossover changed 0 = Crossover not changed
5	Downshift Interrupt	RO,LH	0x0	0x0	1 = Downshift detected 0 = No down shift



Bits	Field	Mode	HW Rst	SW Rst	Description
4	Copper Cable Detect Changed	RO,LH	0x0	0x0	1 = Cable Detect state changed 0 = No Cable Detect state change detected
3	FLP Exchange Complete but no Link	RO,LH	0x0	0x0	1 = FLP Exchange Completed but Link Not Established 0 = No Event Detected
2	DTE power detection status changed interrupt	RO,LH	0x0	0x0	1 = DTE power detection status changed 0 = No DTE power detection status change detected
1	Polarity Changed	RO,LH	0x0	0x0	1 = Polarity Changed 0 = Polarity not changed
0	Jabber	RO,LH	0x0	0x0	1 = Jabber 0 = No jabber

4.1.17 Copper Specific Control Register 2 - Page 0, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	R/W	0x000	Retain	Write all 0s
6	Break Link On Insufficient IPG	R/W	0x0	Retain	0 = Break link on insufficient IPGs in 10BASE-T and 100BASE-TX. 1 = Do not break link on insufficient IPGs in 10BASE-T and 100BASE-TX.
5	100 BASE-T Transmitter Clock Source	R/W	0x1	Update	1 = Local Clock 0 = Recovered Clock
4	Accelerate 100BASE-T Link Up	R/W	0x0	Retain	0 = No Acceleration 1 = Accelerate
3	Reverse MDIP/N[3] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity
2	Reverse MDIP/N[2] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity
1	Reverse MDIP/N[1] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity
0	Reverse MDIP/N[0] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity

4.1.18 Copper Specific Receive Error Counter Register - Page 0, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

4.1.19 Page Address Register - Any Page, Register 22

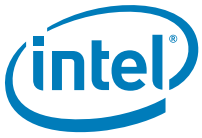
Bits	Field	Mode	HW Rst	SW Rst	Description
15	Ignore PHYAD[4:2]	R/W	0x0	Retain	0 = Use PHYAD[4:2] to decode write commands 1 = Ignore PHYAD[4:2] to decode write commands
14	Ignore PHYAD[1:0]	R/W	0x0	Retain	0 = Use PHYAD[1:0] to decode write commands 1 = Ignore PHYAD[1:0] to decode write commands
13:8	Reserved	RO	0x00	0x00	00000000
7:0	Page select for registers 0 to 28	R/W	0x00	Retain	Page Number

4.1.20 Global Interrupt Status - Page 0, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	0
3:0	Port X Interrupt	RO	0x0	0x0	1 = Interrupt active on port X 0 = No interrupt active on port X

4.1.21 Copper Specific Control Register 3 - Page 0, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000 BASE-T Transmitter type	R/W	0x0	Retain	0 = Class B 1 = Class A
14	Reserved	R/W	0x0	Retain	Write 0
13	Reserved	R/W	0x0	Retain	Write 0
12	100 BASE-T Transmitter type	R/W	0x0	Retain	0 = Class B 1 = Class A
11:10	Gigabit Link Down Delay	R/W	0x0	Retain	This register only have effect if register 26_0.9 is set to 1. 00 = 0ms 01 = 10 ± 2ms 10 = 20 ± 2ms 11 = 40 ± 2ms
9	Speed Up Gigabit Link Down Time	R/W	0x0	Retain	1 = Enable faster gigabit link down 0 = Use IEEE gigabit link down



Bits	Field	Mode	HW Rst	SW Rst	Description
8	DTE detect enable	R/W	0x0	Update	1 = Enable DTE detection 0 = Disable DTE detection
7:4	DTE detect status drop hysteresis	R/W	0x4	Retain	0000: report immediately 0001: report 5s after DTE power status drop ... 1111: report 75s after DTE power status drop
3:2	100 MB test select	R/W	0x0	Retain	0x = Normal Operation 10 = Select 112 ns sequence 11 = Select 16 ns sequence
1	10 BT polarity force	R/W	0x0	Retain	1 = Force negative polarity for Receive only 0 = Normal Operation
0	Reserved	R/W	0x0	Retain	Set to 0

4.1.22 PHY Identifier Register - Page 1, Register

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

4.1.23 PHY Identifier Register - Page 1, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	0x00	Organizationally Unique Identifier bits 19:24 000011 ^.....^ bit 19...bit24
9:4	Model Number	RO	Always 011100	0x00	Model Number 011100
3:0	Revision Number	RO	Always 0000	0x0	Rev Number = 0000

4.1.24 Extended Status Register - Page 1, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X full-duplex capable 0 = Not 1000BASE-X full-duplex capable

Bits	Field	Mode	HW Rst	SW Rst	Description
14	1000BASE-X Half-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X half-duplex capable 0 = Not 1000BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	0x0	0x0	0 = Not 1000BASE-T full-duplex capable
12	1000BASE-T Half-Duplex	RO	0x0	0x0	0 = Not 1000BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

4.1.25 PRBS Control - Page 1, Register 23

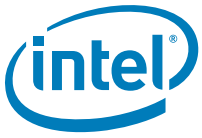
Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Set to 0s
7	Invert Checker Polarity	R/W	0x0	Retain	0 = Invert 1 = Normal
6	Invert Generator Polarity	R/W	0x0	Retain	0 = Invert 1 = Normal
5	PRBS Lock	R/W	0x0	Retain	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first
4	Clear Counter	R/W, SC	0x0	0x0	0 = Normal 1 = Clear Counter
3:2	Reserved	R/W	0x0	Retain	Set to 0s
1	PRBS Checker Enable	R/W	0x0	0x0	0 = Disable 1 = Enable
0	PRBS Generator Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

4.1.26 PRBS Error Counter LSB - Page 1, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count LSB	RO	0x0000	Retain	A read to this register freezes register 25_1. Cleared only when register 23_1.4 is set to 1.

4.1.27 PRBS Error Counter MSB - Page 1, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count MSB	RO	0x0000	Retain	This register does not update unless register 24_1 is read first. Cleared only when register 23_1.4 is set to 1.



4.1.28 MAC Specific Control Register 1 - Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Copper Transmit FIFO Depth	R/W	0x1	Retain	00 = ± 16 Bits 01 = ± 24 Bits 10 = ± 32 Bits 11 = ± 40 Bits
13	Reserved	R/W	0x0	Update	Set to 0
12	RCLK Frequency Select	R/W	0x0	Retain	0 = 25 MHz 1 = 125 MHz
11	RCLK Link Down Disable	R/W	0x0	Retain	0 = RCLK outputs 25 MHz clock during link down and 10BASE-T. 1 = RCLK low during link down and 10BASE-T.
10	Reserved	R/W	0x0	Retain	Set to 0
9	RCLK2 Select	R/W	0x0	Retain	The highest numbered port with this bit set will output the clock. The 125 MHz recovered clock is output as is or divided by 5 and output on RCLK2 depending on the setting of 16_2.12. 1 = Output recovered clock on RCLK2 0 = Do not output recovered clock on RCLK2
8	RCLK1 Select	R/W	0x0	Retain	The highest numbered port with this bit set will output the clock. The 125 MHz recovered clock is output as is or divided by 5 and output on RCLK1 depending on the setting of 16_2.12. 1 = Output recovered clock on RCLK1 0 = Do not output recovered clock on RCLK1
7	Copper Reference Clock Source Select	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 1 = Use SCLK as 25MHz source 0 = Use XTAL_IN/REF_CLKP/N as source
6	Reserved	R/W	0x0	Update	Reserved
5:4	Reserved	R/W	0x0	Retain	Set to 0s
3	MAC Interface Power Down	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether the MAC Interface powers down when Register 0_0.11, 16_0.2 are used to power down the device or when the PHY enters the cable detect state. 1 = Always power up 0 = Can power down
2:0	Reserved	R/W	0x0	Retain	Set to 0s

4.1.29 MAC Specific Interrupt Enable Register - Page 2, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	000000000
7	FIFO Over/ Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

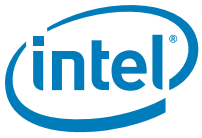
Bits	Field	Mode	HW Rst	SW Rst	Description
6:4	Reserved	R/W	0x0	Retain	000
3	FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1:0	Reserved	R/W	0x0	Retain	00

4.1.30 MAC Specific Status Register - Page 2, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	00000000
7	Copper FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:4	Reserved	RO	Always 0	Always 0	000
3	Copper FIFO Idle Inserted	RO,LH	0x0	0x0	1 = Idle Inserted 0 = No Idle Inserted
2	Copper FIFO Idle Deleted	RO,LH	0x0	0x0	1 = Idle Deleted 0 = Idle not Deleted
1:0	Reserved	RO	Always 0	Always 0	00

4.1.31 Copper RX_ER Byte Capture - Page 2, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Capture Data Valid	RO	0x0	0x0	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
14	Reserved	RO	0x0	0x0	0
13:12	Byte Number	RO	0x0	0x0	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 20_2.15 is set to 1.
11:10	Reserved	RO	0x0	0x0	000
9	RX_ER	RO	0x0	0x0	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
8	RX_DV	RO	0x0	0x0	RX Data Valid



Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	RXD[7:0]	RO	0x00	0x00	RX Data

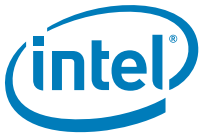
4.1.32 MAC Specific Control Register 2 - Page 2, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	0
14	Copper Line Loopback	R/W	0x0	0x0	1 = Enable Loopback of MDI to MDI 0 = Normal Operation
13:12	Reserved	R/W	0x1	Update	1
11:7	Reserved	R/W	0x00	0x00	00000
6	Reserved	R/W	0x1	Update	1
5:4	Reserved	R/W	0x0	Retain	0
3	Block Carrier Extension Bit	R/W	0x0	Retain	1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
2:0	Default MAC interface speed	R/W	0x6	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. MAC Interface Speed during Link down while Auto-Negotiation is enabled. Bit Speed 0XX = Reserved 100 = 10 Mbps 101 = 100 Mbps 110 = 1000 Mbps 111 = Reserved

4.1.33 LED[3:0] Function Control Register - Page 3, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LED[3] Control	R/W	0x1	Retain	If 16_3.11:10 is set to 11 then 16_3.15:12 has no effect 0000 = On - Reserved, Off - Else 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = Reserved 0110 = On - 10 Mb/s or 1000 Mb/s Master, Off - Else 0111 = On - Full-Duplex, Off - Half-Duplex 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved

Bits	Field	Mode	HW Rst	SW Rst	Description
11:8	LED[2] Control	R/W	0x7	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = PTP Output 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000 Mbps Link, Off - Else 0111 = On - 10 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)
7:4	LED[1] Control	R/W	0x7	Retain	If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On - Copper Link, Off - Else 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - 100 Mb/s Link, Off - Else 0110 = On - 100/1000 Mb/s Link, Off - Else 0111 = On - 100 Mb/s Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
3:0	LED[0] Control	R/W	0x7	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mb/s 2 blinks - 100 Mb/s 1 blink - 10 Mb/s 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mb/s Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)



4.1.34 LED[3:0] Polarity Control Register - Page 3, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LED[5], LED[3], LED[1] mix percentage	R/W	0x8	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
11:8	LED[4], LED[2], LED[0] mix percentage	R/W	0x8	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
7:6	LED[3] Polarity	R/W	0x0	Retain	00 = On - drive LED[3] low, Off - drive LED[3] high 01 = On - drive LED[3] high, Off - drive LED[3] low 10 = On - drive LED[3] low, Off - tristate LED[3] 11 = On - drive LED[3] high, Off - tristate LED[3]
5:4	LED[2] Polarity	R/W	0x0	Retain	00 = On - drive LED[2] low, Off - drive LED[2] high 01 = On - drive LED[2] high, Off - drive LED[2] low 10 = On - drive LED[2] low, Off - tristate LED[2] 11 = On - drive LED[2] high, Off - tristate LED[2]
3:2	LED[1] Polarity	R/W	0x0	Retain	00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1]
1:0	LED[0] Polarity	R/W	0x0	Retain	00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0]

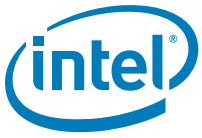
4.1.35 LED Timer Control Register - Page 3, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INTn	R/W	0x0	Retain	1 = Interrupt pin forced to be asserted 0 = Normal Operation
14:12	Pulse Stretch Duration	R/W	0x4	Retain	000 = no pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3 s 111 = 1.3 s to 2.7 s
11	Reserved	R/W	0x1	Retain	Must be set to 1.

Bits	Field	Mode	HW Rst	SW Rst	Description
10:8	Blank Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:4	Reserved	R/W	0x0	Retain	0000
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

4.1.36 LED[5:4] Function Control and Polarity - Page 3, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LED[3] function pin mapping	R/W	0x0	Retain	0 = Map LED[3] function to LED[3] pin 1 = Map LED[5] function to LED[3] pin
14	LED[2] function pin mapping	R/W	0x0	Retain	0 = Map LED[2] function to LED[2] pin 1 = Map LED[4] function to LED[2] pin
13	Filter PTP Activity	R/W	0x0	Retain	1 = Filter PTP packets from LED activity 0 = Do not filter PTP packets from LED activity
12	Reserved	R/W	0x0	Retain	0
11:10	LED[5] Polarity	R/W	0x0	Retain	00 = On - drive LED[5] low, Off - drive LED[5] high 01 = On - drive LED[5] high, Off - drive LED[5] low 10 = On - drive LED[5] low, Off - tristate LED[5] 11 = On - drive LED[5] high, Off - tristate LED[5]
9:8	LED[4] Polarity	R/W	0x0	Retain	00 = On - drive LED[4] low, Off - drive LED[4] high 01 = On - drive LED[4] high, Off - drive LED[4] low 10 = On - drive LED[4] low, Off - tristate LED[4] 11 = On - drive LED[4] high, Off - tristate LED[4]



Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	LED[5] Control	R/W	0x7	Retain	If 19_3.3:2 is set to 11 then 19_3.7:4 has no effect 0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Full-Duplex, Off - Half-Duplex 0111 = On - Full-Duplex, Blink - Collision Off - Half-Duplex 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
3:0	LED[4] Control	R/W	0x3	Retain	0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Full-Duplex, Off - Half-Duplex 0111 = On - Full-Duplex, Blink - Collision Off - Half-Duplex 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

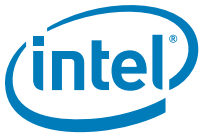
4.1.37 SGMII Link Partner Ability Register - SGMII (Media mode) Mode (Register 16_4.0 = 1b) - Page 4, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13 Must be 0

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Duplex Status	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the link Partner is capable of Full-Duplex 0 = Copper Interface on the link partner is capable of Half-Duplex
11:10	Speed Status	RO	0x0	0x0	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
9	Transmit Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 9 1 = Enabled 0 = Disabled
8	Receive Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 8 1 = Enabled 0 = Disabled
7	Copper Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 7 1 = Reserved 0 = Copper media
6:0	Reserved	RO	0x00	0x00	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bits 6:0 Must be 0000001

4.1.38 Cable Tester TX to MDI[0] Rx Coupling - Page 5, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection



Bits	Field	Mode	HW Rst	SW Rst	Description
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 100 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 100 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note: This register reports the reflection seen based on the setting of register 23_5.13:11

000 = MDI[0] Tx to MDI[0] Rx
100 = MDI[0] Tx to MDI[0] Rx
101 = MDI[1] Tx to MDI[0] Rx
110 = MDI[2] Tx to MDI[0] Rx
111 = MDI[3] Tx to MDI[0] Rx

4.1.39 Cable Tester TX to MDI[1] Rx Coupling - Page 5, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 101 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 101 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note: This register reports the reflection seen based on the setting of register 23_5.13:11

000 = MDI[1] Tx to MDI[1] Rx
100 = MDI[0] Tx to MDI[1] Rx
101 = MDI[1] Tx to MDI[1] Rx
110 = MDI[2] Tx to MDI[1] Rx
111 = MDI[3] Tx to MDI[1] Rx

4.1.40 Cable Tester TX to MDI[2] Rx Coupling - Page 5, Register 18

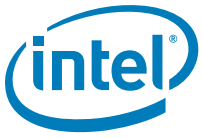
Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 110 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 110 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note: This register reports the reflection seen based on the setting of register 23_5.13:11

000 = MDI[2] Tx to MDI[2] Rx
100 = MDI[0] Tx to MDI[2] Rx
101 = MDI[1] Tx to MDI[2] Rx
110 = MDI[2] Tx to MDI[2] Rx
111 = MDI[3] Tx to MDI[2] Rx

4.1.41 Cable Tester TX to MDI[3] Rx Coupling - Page 5, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection 0 = Negative reflection



Bits	Field	Mode	HW Rst	SW Rst	Description
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 111 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 111 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

Note: This register reports the reflection seen based on the setting of register 23_5.13:11

000 = MDI[3] Tx to MDI[3] Rx
100 = MDI[0] Tx to MDI[3] Rx
101 = MDI[1] Tx to MDI[3] Rx
110 = MDI[2] Tx to MDI[3] Rx
111 = MDI[3] Tx to MDI[3] Rx

4.1.42 1000BASE-T Pair Skew Register - Page 5, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 7,8 (MDI[3]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns. The contents of 20_5.15:0 are valid only if Register 21_5.6 = 1
11:8	Pair 4,5 (MDI[2]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns.
7:4	Pair 3,6 (MDI[1]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns.
3:0	Pair 1,2 (MDI[0]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns.

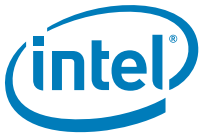
4.1.43 1000BASE-T Pair Swap and Polarity - Page 5, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Reserved for future use.
6	Register 20_5 and 21_5 valid	RO	0x0	0x0	The contents of 21_5.5:0 and 20_5.15:0 are valid only if Register 21_5.6 = 1 1= Valid . 0 = Invalid

Bits	Field	Mode	HW Rst	SW Rst	Description
5	C, D Crossover	RO	0x0	0x0	1 = Channel C received on MDI[2]± Channel D received on MDI[3]± 0 = Channel D received on MDI[2]± Channel C received on MDI[3]±
4	A, B Crossover	RO	0x0	0x0	1 = Channel A received on MDI[0]± Channel B received on MDI[1]± 0 = Channel B received on MDI[0]± Channel A received on MDI[1]±
3	Pair 7,8 (MDI[3]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
2	Pair 4,5 (MDI[2]±) Polarity		0x0	0x0	1 = Negative 0 = Positive
1	Pair 3,6 (MDI[1]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
0	Pair 1,2 (MDI[0]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive

4.1.44 Cable Tester Control - Page 5, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable Test	R/W, SC	0x0	0x0	0 = Disable test 1 = Enable test This bit will self clear when the test is completed
14	Test status	RO	0x0	0x0	0 = Test not started/in progress 1 = Test completed
13:11	Transmitter Channel Select	R/W	0x0	0x0	000 - Tx 0 => Rx 0, Tx 1 => Rx 1, Tx 2 => Rx 2, Tx 3 => Rx 3. 100 - Tx 0 => Rx 0, Tx 0 => Rx 1, Tx 0 => Rx 2, Tx 0 => Rx 3. 101 - Tx 1 => Rx 0, Tx 1 => Rx 1, Tx 1 => Rx 2, Tx 1 => Rx 3. 110 - Tx 2 => Rx 0, Tx 2 => Rx 1, Tx 2 => Rx 2, Tx 2 => Rx 3. 111 - Tx 3 => Rx 0, Tx 3 => Rx 1, Tx 3 => Rx 2, Tx 3 => Rx 3. 01x - reserved 0x1 - reserved
10:8	Number of Sample Averaged	R/W	6	Retain	0 = 2 samples 1 = 4 samples 2 = 8 samples 3 = 16 samples 4 = 32 samples 5 = 64 samples 6 = 128 samples 7 = 256 samples



Bits	Field	Mode	HW Rst	SW Rst	Description
7:6	Mode	R/W	0x0	Retain	00 = Maximum peak above threshold 01 = First or last peak above threshold. See register 28_5.13. 10 = Offset 11 = Sample point at distance set by 24_5.7:0
5:0	Peak Detection Hysteresis	R/W	0x03	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x3F = ± 492 mv

4.1.45 Cable Tester Sample Point Distance - Page 5, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	0x00	0
9:0	Distance to measure/ Distance to start	R/W	0x000	Retain	When 23_5.7:6 = 11 the measurement is taken at this distance. (00 to 3FF) When 23_5.7:6 = 0x any distance below this distance is not considered (00 to FF). Bit 9:8 is ignored.

4.1.46 Cable Tester Cross Pair Positive Threshold - Page 5, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14:8	Cross Pair Positive Threshold > 30m	R/W	0x01	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv
7	Reserved	RO	0x0	0x0	0
6:0	Cross Pair Positive Threshold < 30m	R/W	0x04	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv

4.1.47 Cable Tester Same Pair Impedance Positive Threshold 0 and 1 - Page 5, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14:8	Same-Pair Positive Threshold 10m - 50m	R/W	0x0F	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv
7	Reserved	RO	0x0	0x0	0
6:0	Same-Pair Positive Threshold < 10m	R/W	0x12	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv

4.1.48 Cable Tester Same Pair Impedance Positive Threshold 2 and 3 - Page 5, Register 27

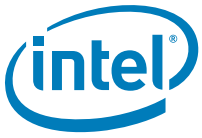
Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14:8	Same-Pair Positive Threshold 110m - 140m	R/W	0x0A	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv
7	Reserved	RO	0x0	0x0	0
6:0	Same-Pair Positive Threshold 50m - 110m	R/W	0x0C	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv

4.1.49 Cable Tester Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control - Page 5, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	0x0	0
13	First Peak/Last Peak Select	R/W	0x0	Retain	This register takes effect only if register 23_5.7:6 = 01. 0 = First Peak 1 = Last Peak
12	Break Link Prior to Measurement	R/W	0x0	Retain	1 = Do not wait 1.5s to break link before starting cable tester 0 = Wait 1.5s to break link before starting cable tester
11:10	Transmit Pulse Width	R/W	0x0	Retain	00 = Full pulse (128ns) 01 = 3/4 pulse 10 = 1/2 pulse 11 = 1/4 pulse
9:8	Transmit Amplitude	R/W	0x0	Retain	00 = Full amplitude 01 = 3/4 amplitude 10 = 1/2 amplitude 11 = 1/4 amplitude

7	Distance Measurement Point	R/W	0x0	Retain	If 23_5.7:6 = 00 then
					0 = Measure distance when amplitude drops to 50% of peak amplitude
					1 = Measure distance at actual maximum amplitude
					If 23_5.7:6 = 01 then
					0 = Measure distance when amplitude drops below hysteresis
					1 = Measure distance at actual maximum amplitude
					If 23_5.7:6 = 1X then this bit is ignored.

6:0	Same-Pair Positive Threshold > 140m	R/W	0x06	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mv



4.1.50 Packet Generation - Page 6, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7:5	Enable Packet Generator	R/W, SC	0x0	Retain	000 = Normal Operation 010 = Generate Packets on Copper Interface 100 = Generate Packets on SGMII Interface 110 = Reserved else = Reserved
4:3	Reserved	R/W	0x0	Retain	Set to 0
2	Payload of packet to transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of packet to transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

4.1.51 CRC Counters - Page 6, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Count	RO	0x00	Retain	0x00 = No packets received 0xFF = 256 packets received (max count). The CRC error counter and Frame counter must be enabled (Reg 18_6.2:0) in order for this register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00 = No CRC errors detected in the packets received. 0xFF = 256 CRC errors detected in the packets received (max count). The CRC error counter and Frame counter must be enabled (Reg 18_6.2:0) in order for this register to be valid.

4.1.52 Checker Control - Page 6, Register 18

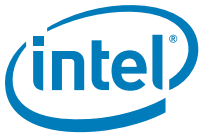
Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	R/W	0x000	Retain	Set to 0s
3	Enable Stub Test	R/W	0x0	Retain	1 = Enable stub test 0 = Normal Operation
2:0	Enable CRC checker	R/W	0x0	Retain	000 = Disable/reset CRC checker 010 = Check data from Copper Interface 100 = Check data from SGMII Interface 110 = Reserved else = Reserved

4.1.53 General Control Register - Page 6, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	SC	Mode Software Reset. Affects page 6. Writing a 1 to this bit causes the main PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14:12	Reserved	R/W	0x0	Retain	Set to 0s
11:10	Snooping	R/W	0x0	Retain	00 = Turn off Snooping 01 = Reserved 10 = Snoop data from network 11 = Snoop data from MAC
9	Reserved	R/W	0x1	Retain	Reservedp
8	Reserved	R/W	See Descr.	Retain	Reserved
7	Reserved	R/W	See Descr.	Retain	Reserved
6	Reserved	R/W	0x0	Retain	Set to 0
5:4	Preferred Media	R/W	0x0	Retain	00 = Link on first media 01 = Copper Preferred 10 = Reserved 11 = Reserved
3	Reserved	R/W	0x0	Update	0 = Normal operation 1 = Reserved.
2:0	MODE[2:0]	R/W	See Descr.	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. On hardware reset these bits take on the value of MODE[2:0].
			0x0	0x0	000 = Reserved 001 = SGMII (System mode) to Copper 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

4.1.54 Late Collision Counters 1 & 2 - Page 6, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Late Collision 97-128 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 97th to 128th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.



Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Late Collision 65-96 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 65th to 96th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.

4.1.55 Late Collision Counters 3 & 4 - Page 6, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Late Collision >192 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received after 192 bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.
7:0	Late Collision 129-192 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 129th to 192nd bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.

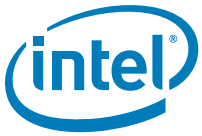
4.1.56 Late Collision Window Adjust/Link Disconnect - Page 6, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	R/W	0x0	Retain	Set to 0s
12:8	Late Collision Window Adjust	R/W	0x00	Retain	Number of bytes to advance in late collision window. 0 = start at 64th byte, 1 = start at 63rd byte, etc.
7:0	Link Disconnect	RO, SC	0x00	Retain	This counter counts the number of times link status changed from up to down. The counter will not roll over and will clear on read.

4.1.57 Misc Test - Page 6, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TX_TCLK Enable	R/W	0x0	0x0	The highest numbered enabled port will drive the transmit clock to the HSDACP/N pin. 1 = Enable 0 = Disable
14:13	Reserved	R/W	0x0	Retain	Set to 0
12:8	Temperature Threshold	R/W	0x19	Retain	Temperature in C = 5 x 26_6.4:0 - 25 i.e. for 100C the value is 11001
7	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = Interrupt Enable 0 = Interrupt Disable
6	Temperature Sensor Interrupt	RO, LH	0x0	0x0	1 = Temperature Reached Threshold 0 = Temperature Below Threshold

Bits	Field	Mode	HW Rst	SW Rst	Description
5	Reserved	R/W	0x0	Retain	Set to 0
4:0	Temperature Sensor	RO	xxxxx	xxxxx	Temperature in C = 5 x 26_6.4:0 - 25 i.e. for 100C the value is 11001



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5.0 Electrical and Timing Specifications

This section describes the electrical and timing specifications for the I347-AT4.

Table 39. Absolute Maximum Ratings[1]

Stresses above those listed in Table 39 might cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods might affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDAH}	Power Supply Voltage on AVDDH with respect to VSS	-0.5		2.5	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.5		1.5	V
V_{DDOL}	Power Supply Voltage on VDDOL with respect to VSS	-0.5		3.6	V
V_{DDOR}	Power Supply Voltage on VDDOR with respect to VSS	-0.5		3.6	V
V_{DDOM}	Power Supply Voltage on VDDOM with respect to VSS	-0.5		3.6	V
V_{DDC}	Power Supply Voltage on VDDC with respect to VSS	-0.5		2.5	V
V_{PIN}	Voltage applied to any digital input pin	-0.5		5.0 or VDDO + 0.7, whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[1]	°C

1. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (such as weeks or longer) should be kept at 85 °C or lower.

5.1 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDAH}[1]	AVDDH supply	For AVDDH	1.8	1.9	2.0	V
V_{DDC}[1]	VDDC supply	For VDDC	1.8	1.9	2.0	V
V_{DD}[1]	DVDD supply	For DVDD at 1.0V	0.95	1.0	1.05	V
V_{DDOL}[1]	VDDOL supply	For VDDOL at 1.9V	1.8	1.9	2.0	V
V_{DDOL}[1]	VDDOL supply	For VDDOL at 3.3V	3.13	3.3	3.47	V

1. On power-up, no special power supply sequencing is required.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDOR}[1]	VDDOR supply	For VDDOR at 1.9V	1.8	1.9	2.0	V
V_{DDOR}[1]	VDDOR supply	For VDDOR at 3.3V	3.13	3.3	3.47	V
V_{DDOM}[1]	VDDOM supply	For VDDOM at 1.9V	1.8	1.9	2.0	V
V_{DDOM}[1]	VDDOM supply	For VDDOM at 3.3V	3.13	3.3	3.47	V
RSET	Internal bias reference	Resistor connected to V_{SS}		5000 ± 1% Tolerance		W
T_A	Ambient operating temperature	Commercial parts	0		70	°C
T_J	Maximum junction temperature				125	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.

5.2 Current Consumption

# Of Ports	Conditions	Link State		3.3V Current Rail (mA)	1.9V Current Rail (mA)	1.0V Current Rail (mA)	External Power (mW)
		Mode	Speed				
4	Max	Active	1000 Mb/s	5.2	1051	876	3034
	Typ	Active	1000 Mb/s	4.5	946	366	2179
			100 Mb/s	4.5	376	67	797
			10 Mb/s	4.5	571	42	1142
		Idle	1000 Mb/s	4.5	948	334	2151
			100 Mb/s	4.5	377	69	800
			10 Mb/s	4.5	380	41	777
			Cable Disconnect	4.5	126	37	292
2	Max	Active	1000 Mb/s	5.2	605	935	2195
	Typ	Active	1000 Mb/s	4.5	539	200	1239
			100 Mb/s	4.5	245	50	530
			10 Mb/s	4.5	336	37	690
		Idle	1000 Mb/s	4.5	533	186	1214
			100 Mb/s	4.5	250	51	541
			10 Mb/s	4.5	250	37	527
			Cable Disconnect	4.5	134	36	305

# Of Ports	Conditions	Link State		3.3V Current Rail (mA)	1.9V Current Rail (mA)	1.0V Current Rail (mA)	External Power (mW)
		Mode	Speed				
1	Typ	Active	1000 Mb/s	4.5	327	117	754
			100 Mb/s	4.5	187	42	412
			10 Mb/s	4.5	235	35	496
		Idle	1000 Mb/s	4.5	328	113	752
			100 Mb/s	4.5	187	42	412
			10 Mb/s	4.5	187	36	406
			Cable Disconnect	4.5	129	35	295

Note: Typical conditions: room temperature (TA) = 25 °C, nominal voltages and continuous network traffic at full duplex.

Maximum conditions: maximum operating temperature values, nominal voltage values and continuous network traffic at full duplex.

5.3 DC Operating Conditions

5.3.1 Digital Pins

Note: Over full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	2.0		VDDO + 0.6V	V
VIH	Input high voltage	All digital inputs	VDDO = 1.9V	1.26		VDDO + 0.6V	V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V	-0.3		0.8	V
VIL	Input low voltage	All digital inputs	VDDO = 1.9V	-0.3		0.54	V
VOH	High level output voltage	All digital outputs	IOH = -4 mA	VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs	IOL = 4 mA			0.4	V
IILK	Input leakage current	With internal pull-up resistor				10 -50	uA
		All others without resistor				10	uA

CIN	Input capacitance	All pins				5	pF

5.3.2 IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

- 10BASE-T IEEE 802.3 Clause 14
- 100BASE-TX ANSI X3.263-1995

Note: Over full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	MDIP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[1:0]	10BASE-T cable model	585[1]			mV
		MDIP/N[1:0	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T[2]	0.67	0.75	0.82	V
	Overshoot[2]	MDIP/N[1:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/ negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-T mode	585[3]			mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the "far end" wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test ; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The I347-AT4 accepts signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The I347-AT4 rejects signals typically with peak-to-peak differential amplitude less than 360 mV.

5.3.3 SGMII Interface

The I347-AT4 adds flexibility by enabling the programmable output voltage swing and supply voltage option as described in Section 2.3.

5.3.3.1 Transmitter DC Characteristics

Symbol	Parameter[1]	Min	Typ	Max	Units
V_{OH}	Output Voltage High			1600	mV
V_{OL}	Output Voltage Low	700			mV
V_{RING}	Output Ringing			10	mV
$\|V_{OD}\|^2$	Output Voltage Swing (differential, peak)	Programmable - see Section 4.1.			mV peak
V_{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see Section 5.3.3.3 for details.			mV
R_O	Output Impedance (single-ended) (50 Ω termination)	40		60	Ωs
Delta R_O	Mismatch in a pair			10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1			25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1			25	mV
I_{S+}, I_{S-}	Output current on short to VSS			40	mA
I_{S+-}	Output current when S_OUT+ and S_OUT- are shorted			12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

1. Parameters are measured with outputs AC connected with 100 Ω differential load.
2. Output amplitude is programmable by writing to Register 26.2:0.

5.3.3.2 Transmitter DC Characteristics

Table 40. Programming SGMII Output Amplitude

Register 26_2 Bits	Field	Description
2:0	SGMII Output Amplitude	Differential voltage peak measured. Note that internal bias minus the differential peak voltage must be greater than 700 mV. 000b = 14 mV 001b = 112 mV 010b = 210 mV 011b = 308 mV 100b = 406 mV 101b = 504 mV 110b = 602 mV 111b = 700 mV

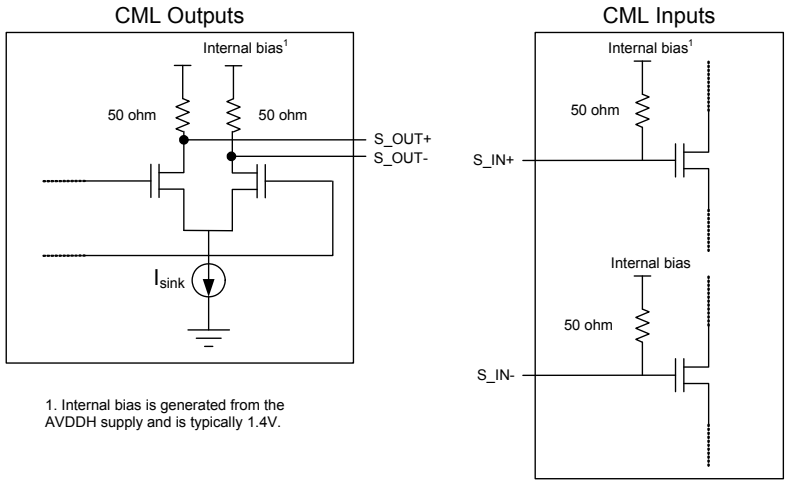

Figure 20. CML I/Os

5.3.3.3 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See Section 3.2.5 and Figure 20 for details. (If AVDDH is used to generate the internal bias, the internal bias value is typically 1.4V.)
- The output voltage swing is programmed by Register 26_2.2:0 (see Section 4.1).

Voffset (such as, common mode voltage) = internal bias - single-ended peak-peak voltage swing. See Figure 21 for details.

If DC coupling is used with a CML receiver, then the DC levels are determined by a combination of the MACs output structure and the device input structure shown in the CML Inputs diagram in Figure 22. Assuming the same MAC CML voltage levels and structure, the common mode output levels are determined by:

- Voffset (such as, common mode voltage) = internal bias - single-ended peak-peak voltage swing/2. See Figure 22 for details.
- If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations previously described, plus the I/O buffer structure of the MAC.

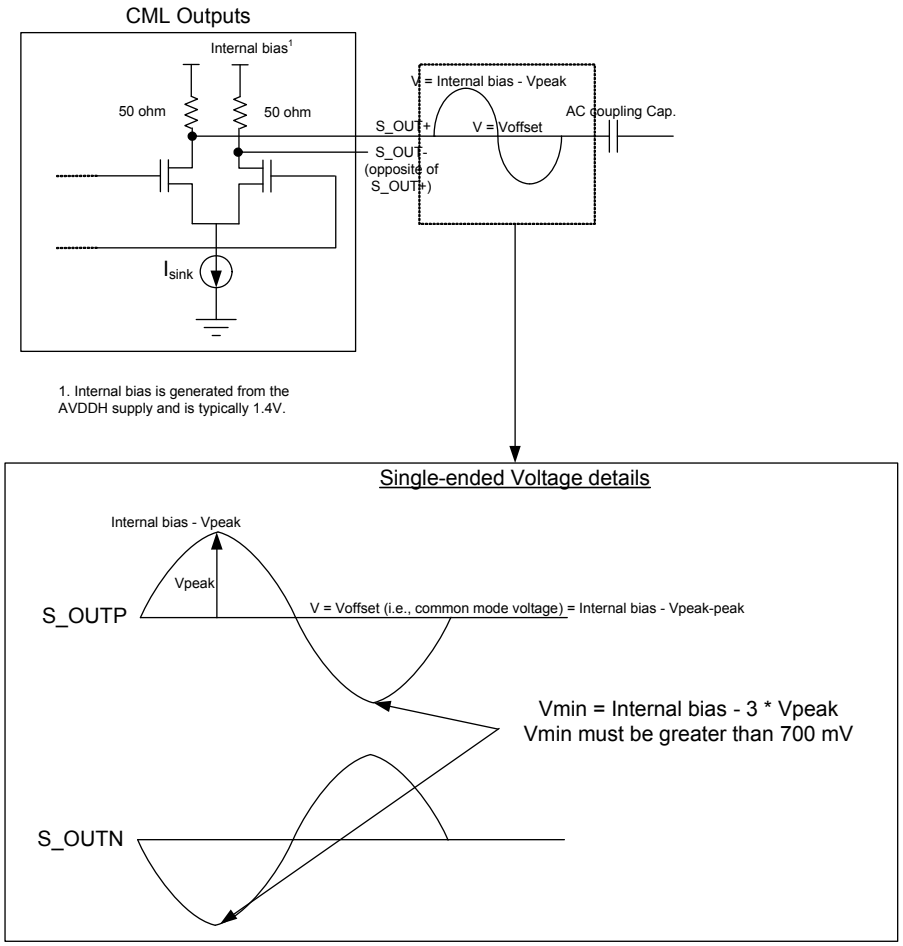

Figure 21. AC Connections (CML or LVDS Receiver) or DC Connection LVDS Receiver

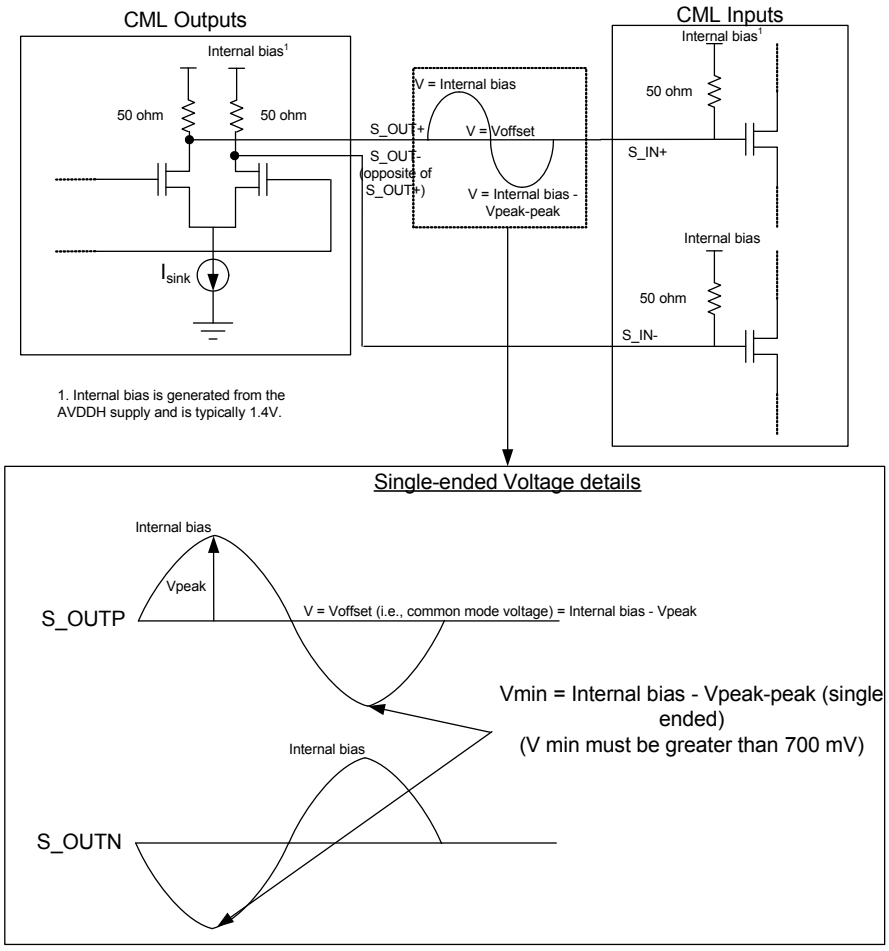

Figure 22. DC Connection to a CML Receiver

5.3.3.4 Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input Voltage Range a or b	675		1725	mV
V_{IDTH}[1]	Input Differential Threshold	200		2100	mV (peak-peak differential)
V_{HYST}[1]	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 Ω Differential Input Impedance	80		120	Ω

1. Receiver is at high level when V_{S_INP} - V_{S_INN} is greater than V_{IDTH}(min) and is at low level when V_{S_INP} - V_{S_INN} is less than -V_{IDTH}(min) . A minimum hysterisis of V_{HYST} is present between -V_{IDTH} and +V_{IDTH} as shown in Figure 23.

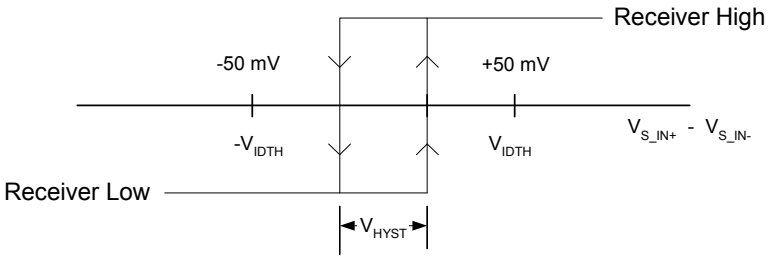

Figure 23. Input Differential Hysteresis

5.4 AC Electrical Specifications

5.4.1 Reset Timing

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESET de-asserted		10			ms
$T_{SU\_XTAL\_IN}$	Number of valid XTAL_IN cycles prior to RESET de-asserted		10			clks
T_{RESET}	Minimum reset pulse width during normal operation		10			ms

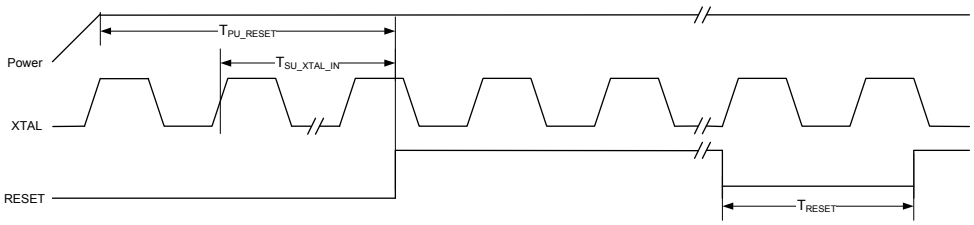

Figure 24. Reset Timing

5.4.2 XTAL_IN/XTAL_OUT (CLK_SEL[1:0] = 10b or 11b[1]) Timing[2]

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_XTAL\_IN}$	XTAL_IN Period		40 -50 ppm	40	40 +50 ppm	ns
$T_{H\_XTAL\_IN}$	XTAL_IN High time		13	20	27	ns
$T_{L\_XTAL\_IN}$	XTAL_IN Low time		13	20	27	ns
$T_{R\_XTAL\_IN}$	XTAL_IN Rise	10% to 90%	-	3.0	-	ns
$T_{F\_XTAL\_IN}$	XTAL_IN Fall	90% to 10%	-	3.0	-	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[1]		-	-	200	ps[2]

1. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
2. In SGMII to Copper mode, Broadband peak-peak = 200 ps, 12 kHz to 20 MHz rms = 3 ps.

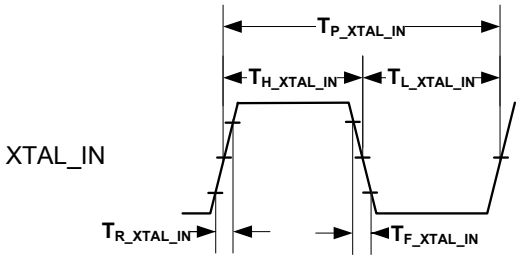

Figure 25. XTAL_IN/XTAL_OUT Timing

5.4.3 LED to CONFIG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_CONFIG}	LED to CONFIG Delay		0		25	ns

1. See Section 3.21 for details.
2. If the crystal option is used, ensure that the frequency is 25 MHz ± 50 ppm. Capacitors must be chosen carefully. Refer to the application note supplied by crystal vendor.

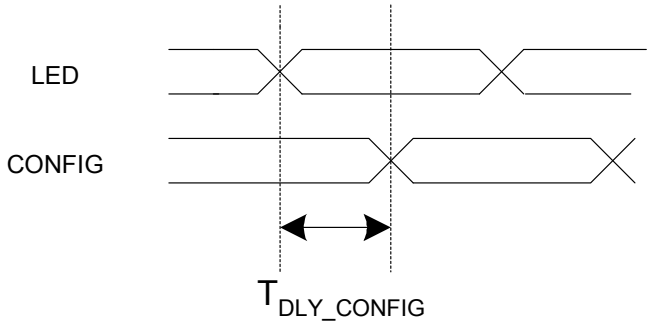

Figure 26. LED-to-CONFIG Timing

5.4.4 Serial LED Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{per}	Clock, Strobe Period	20			ns
T_{pw}	Clock, Strobe High/Low time	5.0			ns
T_{su}	Shift in to Clock Setup	4.0			ns
T_{hd}	Shift in Clock Hold	1.5			ns
T_{cs}	Clock rising edge to Strobe rising edge	4.0			ns
T_{dly}	Clock to shift out delay, Strobe to LED out delay	2.0		12	ns

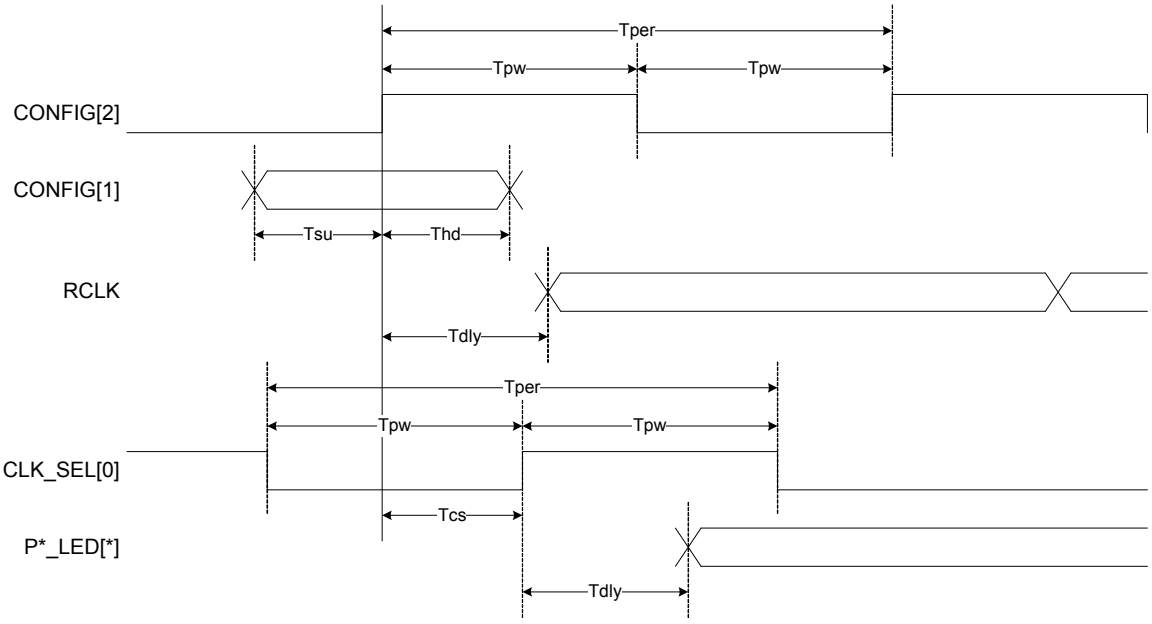

Figure 27. Serial LED TIming Diagram

5.5 SGMII Interface Timing

5.5.1 SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{SKEW1}[1]	Skew between two members of a differential pair			20	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.

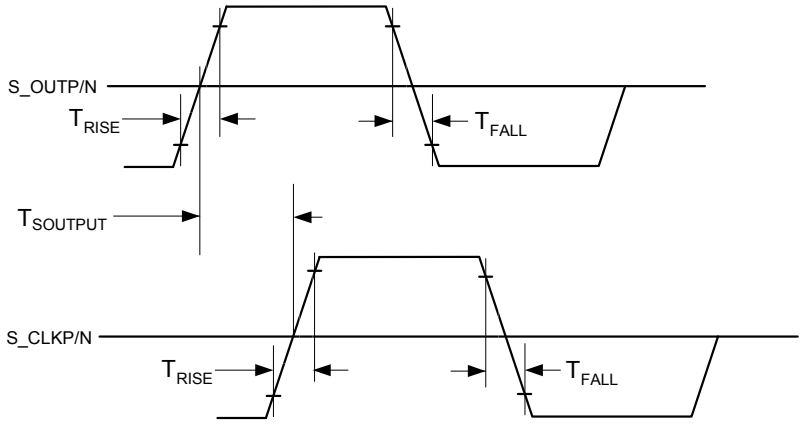

Figure 28. Serial Interface Rise and Fall Times

5.5.2 SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

5.6 MDC/MDIO Timing

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		83.333			ns[1]
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns
V_{HYST}	VDDO Input Hysteresis			360		mV

1. Maximum frequency = 12 MHz.

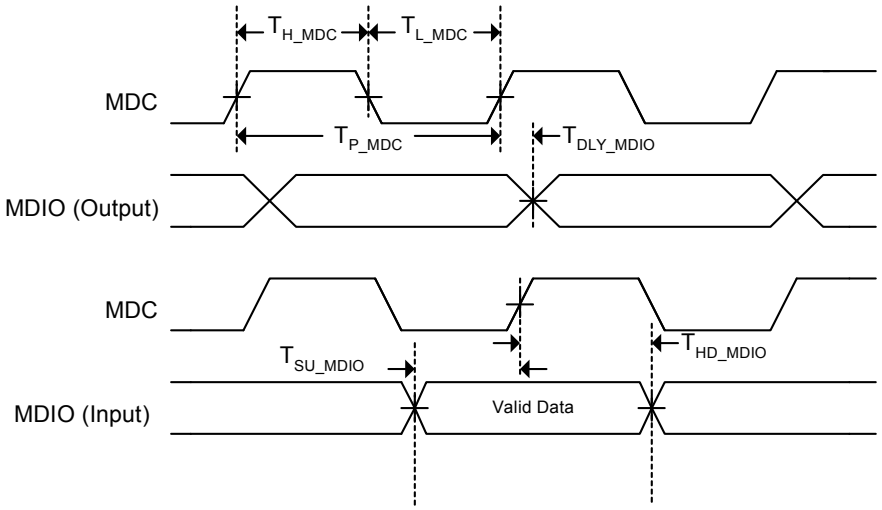

Figure 29. MDC/MDIO Timing

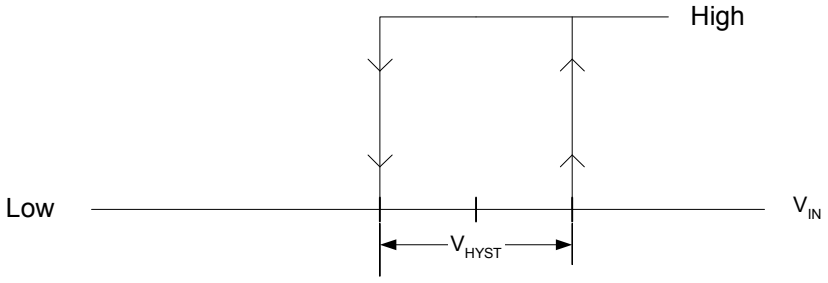

Figure 30. MDC/MDIO Input Hysteresis

5.7 JTAG Timing

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period		60			ns
T_{H_TCK}	TCK High		12			ns
T_{L_TCK}	TCK Low		12			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time		10			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time		10			ns
T_{DLY_TDO}	TCK to TDO Delay		0		15	ns

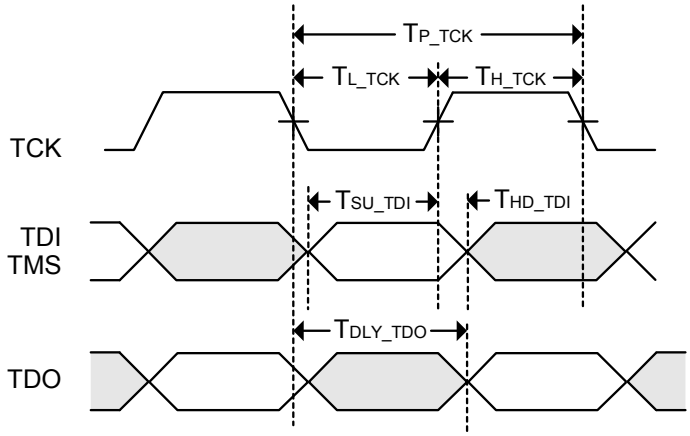

Figure 31. JTAG Timing

5.8 IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:

- 10BASE-T IEEE 802.3 Clause 14-2000
- 100BASE-TX ANSI X3.263-1995
- 1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2. Figure 40-26 shows the template waveforms for transmitter electrical specifications.

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/ TFALL Symmetry		MDIP/N[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3.

5.9 Latency Timing

5.9.1 10/100/1000BASE-T to SGMII Latency Timing

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_SERTX\_1000}$	MDI SSD1 to S_OUTP/N Start of Packet		292[1,2]		336	ns
$T_{DA\_MDI\_SERTX\_1000}$	MDI CSReset, CSExtend, CSExtend_Err to S_OUTP/ N/T/		292[1,2,3]		336	ns
$T_{AS\_MDI\_SERTX\_100}$	MDI /J/ to S_OUTP/N Start of Packet		620[2]		732	ns
$T_{DA\_MDI\_SERTX\_100}$	MDI /T/ to S_OUTP/N/T/		620[2,3]		732	ns
$T_{AS\_MDI\_SERTX\_10}$	MDI Preamble to S_OUTP/ N Start of Packet		4817[2,4]		5603	ns
$T_{DA\_MDI\_SERTX\_10}$	MDI ETD to S_OUTP/N/T/		4817[2,3,4]		5603	ns

1. In 1000BASE-T, the signals on the four MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00b, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mb/s, 40 ns in 100 Mb/s, and 400 ns in 10 Mb/s.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUTP/ N. The worst case variation is outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

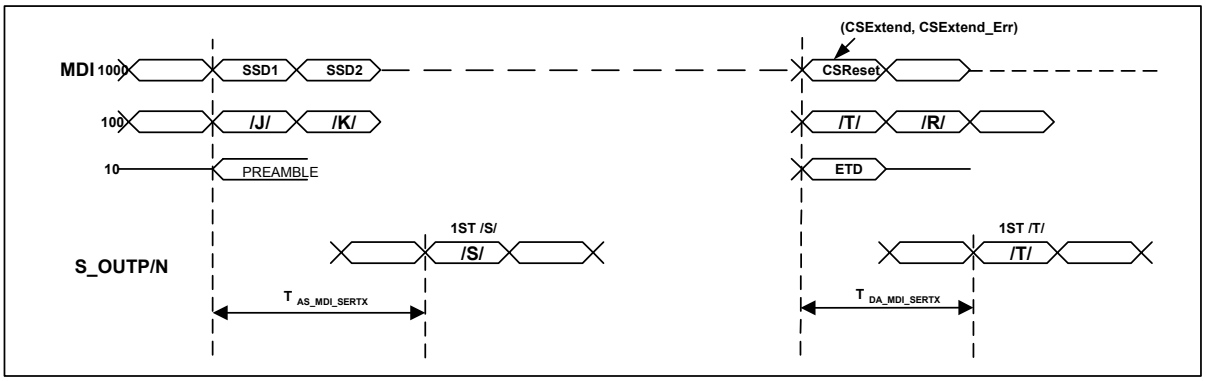

Figure 32. 10/100/1000BASE-T-to-SGMII Latency Timing

5.9.2 SGMII to 10/100/1000BASE-T Latency Timing

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERRX\_MDI\_1000}$	S_INP/N Start of Packet /S/ to MDI SSD1		192[1]		216	ns
$T_{DA\_SERRX\_MDI\_1000}$	S_INP/N /T/ to MDI CSReset, CSExtend, CSExtend_Err		192[1,2]		216	ns
$T_{AS\_SERRX\_MDI\_100}$	S_INP/N Start of Packet /S/ to MDI /J/		528[1]		612	ns
$T_{DA\_SERRX\_MDI\_100}$	S_INP/N /T/ to MDI /T/		528[1,2]		612	ns
$T_{AS\_SERRX\_MDI\_10}$	S_INP/N Start of Packet /S/ to MDI Preamble		3822[1]		4634	ns
$T_{DA\_SERRX\_MDI\_10}$	S_INP/N /T/ to MDI ETD		3822[1,2]		4634	ns

1. Assumes register 16.15:14 is set to 00b, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mb/s, 40 ns in 100 Mb/s, and 400 ns in 10 Mb/s.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_INP/N. The worst case variation is outside these limits, if there is a frequency difference.

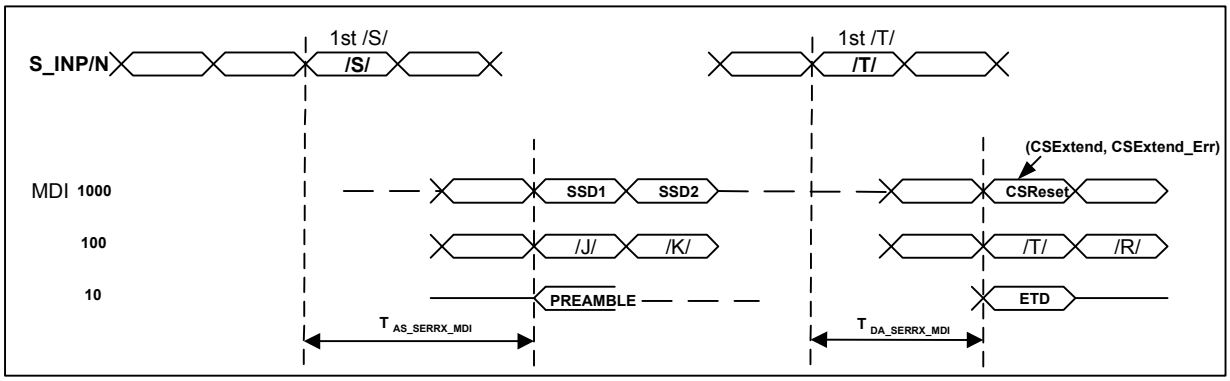

Figure 33. SGMII-to-10/100/1000BASE-T Latency Timing

5.9.2.1 10/100/1000BASE-T to SGMII Latency Timing (Register 27_4.14 = 1b)

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_SERTX\_1000}$	MDI SSD1 to S_OUTP/N Start of Packet		404[1,2]		484	ns
$T_{DA\_MDI\_SERTX\_1000}$	MDI CSReset, CSExtend, CSExtend_Err to S_OUTP/N /T/		404[1,2,3]		484	ns
$T_{AS\_MDI\_SERTX\_100}$	MDI /J/ to S_OUTP/N Start of Packet		1048[2]		1300	ns
$T_{DA\_MDI\_SERTX\_100}$	MDI /T/ to S_OUTP/N /T/		1048[2,3]		1300	ns
$T_{AS\_MDI\_SERTX\_10}$	MDI Preamble to S_OUTP/N Start of Packet		8577[2,4]		10583	ns
$T_{DA\_MDI\_SERTX\_10}$	MDI ETD to S_OUTP/N /T/		8577[2,3,4]		10583	ns

1. In 1000BASE-T the signals on the four MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00b, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mb/s, 40 ns in 100 Mb/s, and 400 ns in 10 Mb/s.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUTP/N. The worst case variation is outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

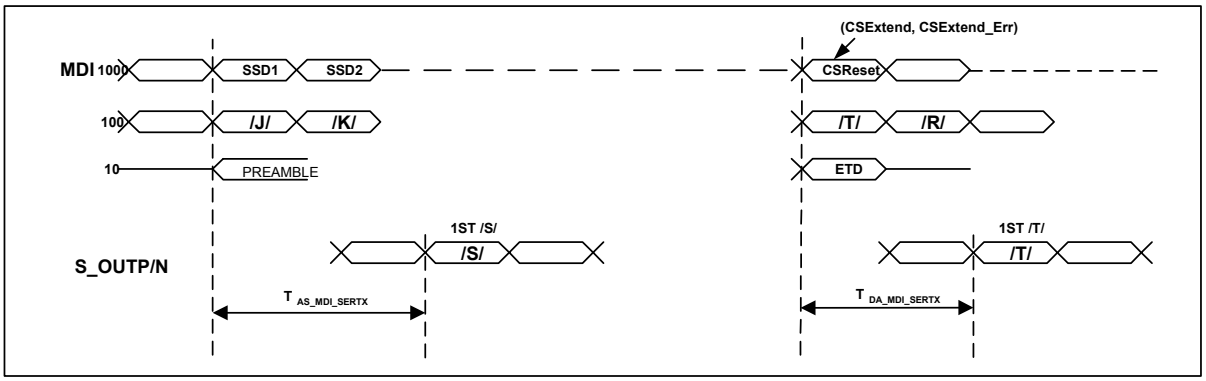

Figure 34. 10/100/1000BASE-T to SGMII Latency Timing (Register 27_4.14 = 1b)

5.9.2.2 SGMII to 10/100/1000BASE-T Latency Timing (Register 27_4.14 = 1b)

Over a full range of values listed in Section 5.1 unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERRX\_MDI\_1000}$	S_INP/N Start of Packet /S/ to MDI SSD1		304[1]		364	ns
$T_{DA\_SERRX\_MDI\_1000}$	S_INP/N/T/ to MDI CSReset, CSExtend, CSExtend_Err		304[1,2]		364	ns
$T_{AS\_SERRX\_MDI\_100}$	S_INP/N Start of Packet /S/ to MDI /J/		952[1]		1180	ns
$T_{DA\_SERRX\_MDI\_100}$	S_INP/N /T/ to MDI /T/		952[1,2]		1180	ns
$T_{AS\_SERRX\_MDI\_10}$	S_INP/N Start of Packet /S/ to MDI Preamble		7582[1]		9615	ns
$T_{DA\_SERRX\_MDI\_10}$	S_INP/N/T/ to MDI ETD		7582[1,2]		9615	ns

1. Assumes register 16.15:14 is set to 00b, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mb/s, 40 ns in 100 Mb/s, and 400 ns in 10 Mb/s.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_INP/N. The worst case variation is outside these limits, if there is a frequency difference.

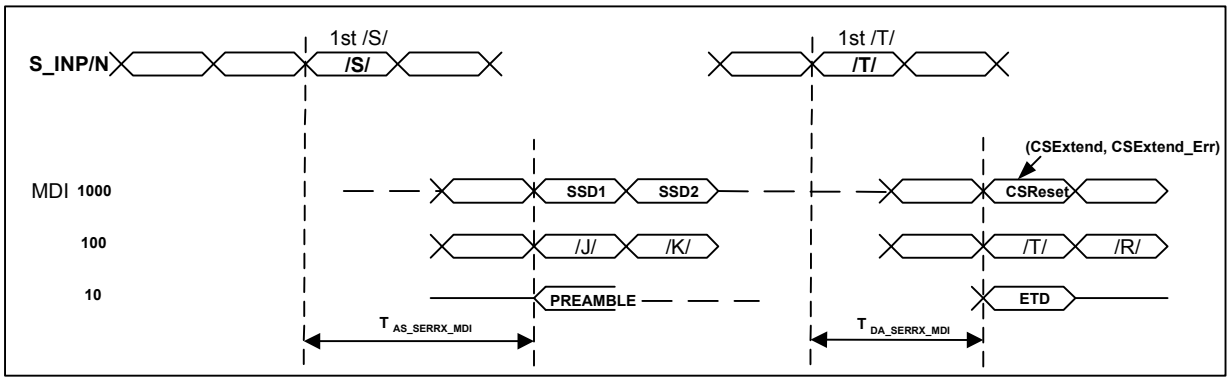

Figure 35. SGMII to 10/100/1000BASE-T Latency Timing (Register 27_4.14 = 1b)

5.10 Crystal Specifications

Parameter	Name Symbol	Recommended Value	Max/Min Range	Conditions
Frequency	fo	25.000 [MHz]		@25 [°C]
Vibration Mode		Fundamental		
Frequency Tolerance	Δf/fo @25°C	±30 [ppm]		@25 [°C]
Temperature Tolerance	Δf/fo	±30 [ppm]		0 to +70 [°C]
Series Resistance	Rs		50 [Ω] max	@25 [MHz]
Crystal Load Capacitance	Cload	18 [pF]		
Shunt Capacitance	Co		6 [pF] max	
Drive Level	D_L		500 [µW] max	
Aging	Δf/fo		±5 ppm per year max	
Calibration Mode		Parallel		
Insulation Resistance	IR		500 [MΩ] min	@ 100 V dc
External Capacitors	C1, C2	27 [pF]		

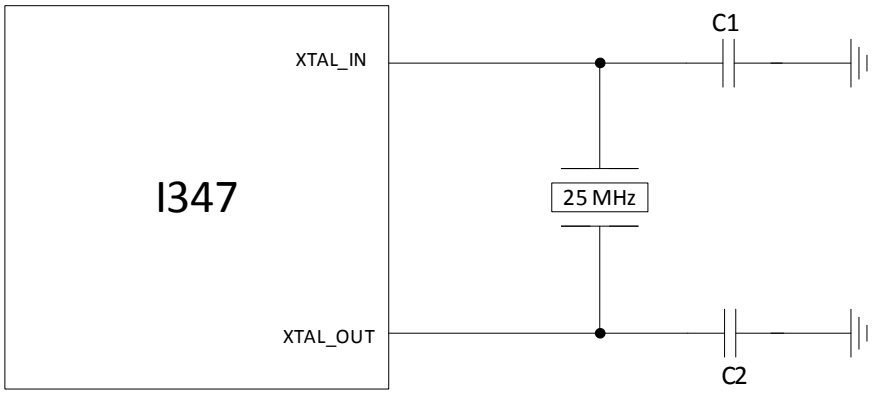

Figure 36. Crystal Layout

6.0 Package

The I347-AT4 is a 15 x 15 mm 196-pin TFBGA Halogen free package.

Table 41. 196-Pin TFBGA Package Dimensions (mm)

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.50
A1	0.30	0.40	0.50
A2	---	0.89	---
c	---	0.36	---
D	14.90	15.00	15.10
E	14.90	15.00	15.10
D1	---	13.00	---
E1	---	13.00	---
e	---	1.00	---
b	0.40	0.50	0.60
aaa	0.20		
bbb	0.25		
ccc	0.35		
ddd	0.12		
eee	0.25		
fff	0.10		
MD/ME	14/14		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

6.1 196-Pin TFBGA Package

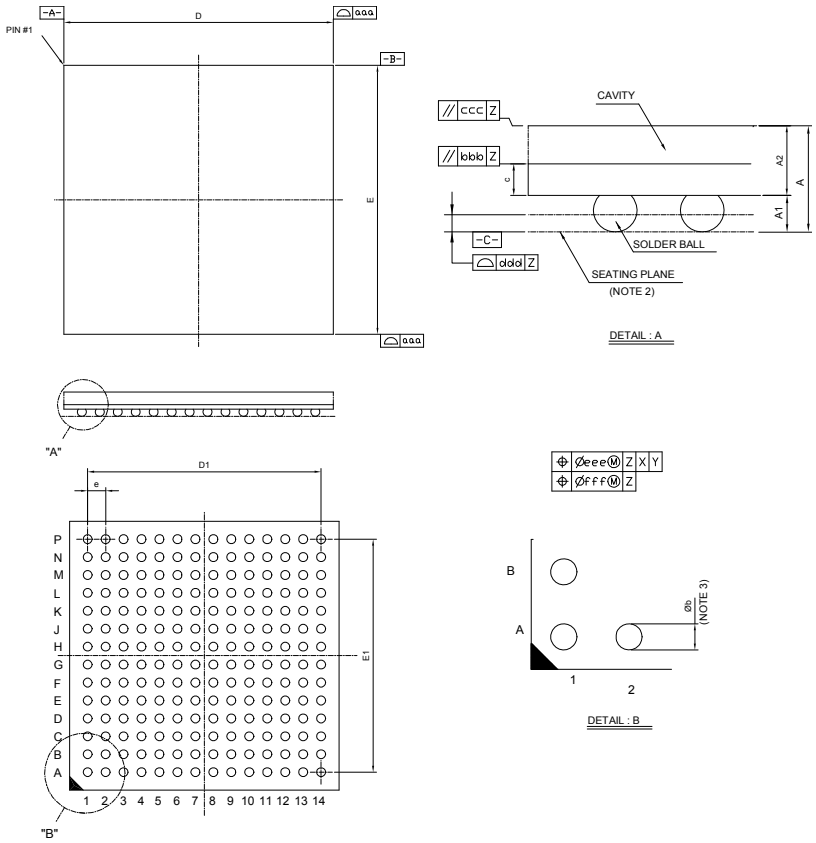

Figure 37. 196-Pin TFBGA Package Mechanical Drawing

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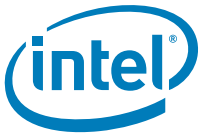


7.0 Thermal Design Recommendations

7.1 Introduction

This section can be used as an aid to designing a thermal solution for systems implementing the I347-AT4 product line. It details the maximum allowable operating junction and case temperatures and provides the methodology necessary to measure these values. It also outlines the results of thermal simulations of the I347-AT4 in a standard JEDEC test environment with a 2s2p board using various thermal solutions.

7.2 Intended Audience

The intended audience for this section is system design engineers using the I347-AT4. System designers are required to address component and system-level thermal challenges as the market continues to adopt products with higher speeds and port densities. New designs might be required to provide more effective cooling solutions for silicon devices depending on the type of system and target operating environment.

7.3 Thermal Considerations

In a system environment, the temperature of a component is a function of both the system and component thermal characteristics. System-level thermal constraints consist of the local ambient temperature at the component, the airflow over the component and surrounding board, and the physical constraints at, above, and surrounding the component that might limit the size of a thermal solution.

The component's case and die temperature are the result of:

- Component power dissipation
- Component size
- Component packaging materials
- Type of interconnection to the substrate and motherboard
- Presence of a thermal cooling solution
- Power density of the substrate, nearby components, and motherboard

All of these parameters are pushed by the continued trend of technology to increase performance levels (higher operating speeds, MHz) and power density (more transistors). As operating frequencies increase and package size decreases, the power density increases and the thermal cooling solution space and airflow become more constrained. The result is an increased emphasis on optimizing system design to ensure that thermal design requirements are met for each component in the system.

7.4 Thermal Management Importance

The objective of thermal management is to ensure that all system component temperatures are maintained within their functional limits. The functional temperature limit is the range in which the electrical circuits are expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors, or cause device and/or system damage. Temperatures exceeding the maximum operating limits can result in irreversible changes in the device operating characteristics. Also note that sustained operation at a component maximum temperature limit might affect long-term device reliability. See Section 7.6.2 for more details.

7.5 Terminology and Definitions

The following is a list of the terminology that is used in this section and their definitions:

TFBGA — Thin Profile Fine Pitch Ball Grid Array: A surface-mount package using a BGA structure whose PCB-interconnect method consists of a Pb-free solder ball array on the interconnect side of the package and is attached to a near chip-scale size substrate.

2s2p — A 4-layer board with two signal layers on the outside and two internal plane layers.

Thermal Resistance — The resulting change in temperature per watt of heat that passes from one reference point to another.

Junction — Refers to a P-N (diode) junction on the silicon. In this section, it is used as a temperature reference point (for example, Θ_{JA} refers to the junction-to-ambient thermal resistance).

Ambient — Refers to the local ambient temperature of the bulk air approaching the component. It can be measured by placing a thermocouple approximately 1 inch upstream from the component edge.

Lands — The pads on the PCB to which BGA balls are soldered.

PCB — Printed Circuit Board.

Printed Circuit Assembly (PCA) — A PCB that has components assembled on it.

Thermal Design Power (TDP) — The estimated maximum possible/expected power generated in a component by a realistic application. TDP is a system design target associated with the maximum component operating temperature specifications. Maximum power values are determined based on typical DC electrical specification and maximum ambient temperature for a worst-case realistic application running at maximum use.

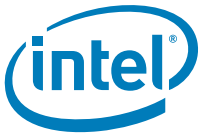
LFM — A measure of airflow velocity in Linear Feet per Minute.

Θ_{JA} (Theta JA) — Thermal resistance from component junction to ambient, °C/W.

Ψ_{JT} (Psi JT) — Junction-to-top (of package) thermal characterization parameter, °C/W. Ψ_{JT} does not represent thermal resistance, but instead is a characteristic parameter that can be used to convert between T_j and T_{case} when knowing the total TDP. Ψ_{JT} is easy to characterize in simulations or measurements and is defined as follows:

$$\Psi_{JT} = \frac{T_J - T_{Case}}{TDP}$$

This parameter can vary with environmental conditions, such as airflow, thermal solution presence, and design.



7.6 Package Thermal/Mechanical Specifications and Limits

7.6.1 Thermal Limits - Max Junction/Case

To ensure proper operation of the I347-AT4, the thermal solution must dissipate the heat generated by the component and maintain a case temperature at or below the values listed in Table 7.1. Table 7.2 lists the thermal performance parameters per JEDEC JESD51-2 standard.

The I347-AT4 is designed to operate properly as long as the T_{case} rating is not exceeded. Section 7.10.1 describes the proper guidelines for measuring the case temperature.

Table 7.1. Absolute Maximum Junction/Case Temperature

Application	Measured TDP (W)	$T_{case-max}$ (°C)[1]
I347-AT4	3.0 W @ 125 °C T_{j-max}	108.11

1. Max T_{case} is based on 27 x 27 x 10 mm Thermalloy heat sink as shown in Figure 7.3.

The thermal limits previously defined are based on simulated results of the package assembled on a standard multi-layer, 2s2p board with 1 oz internal planes and 2 oz external trace layers in a forced convection environment. The maximum case temperature is based on the maximum junction temperature and defined by the relationship, $T_{case-max} = T_{j-max} – (\Psi_{JT} * P_{TDP})$ where Ψ_{JT} is the junction-to-top (of package) thermal characterization parameter. If the case temperature exceeds the specified $T_{case-max}$, thermal enhancements such as heat sinks or forced air are required.

Analysis indicates that real applications are unlikely to cause the I347-AT4 to be at $T_{case-max}$ for sustained periods of time, given a properly designed thermal solution. Sustained operation at $T_{case-max}$ might affect long-term reliability of the I347-AT4 and the system and thus should be avoided.

7.6.2 Thermal Specifications

Table 7.2 lists the package-specific parameters under different conditions and environments. The values Θ_{JA} and Ψ_{JT} should be used as references only as they can vary by system environments and thermal solutions. Unless otherwise noted, the simulations were run in a JEDEC environment with a four layer (2s2p), 76.2 mm x 114.3 mm board with no heat sink.

Table 7.2. Package Thermal Characteristics in Standard JEDEC Environment for Reference

Parameter	Equation	Conditions	No Heat Sink (°C/W)	Heat Sink 1 (°C/W)[1]	Heat Sink 2 (°C/W)[2]
Θ_{JA}	$\frac{T_J - T_A}{P}$ P = TDP	No Airflow	31	22	19.2
		1 m/s	28.3	16.4	14
		2 m/s	27	14	12.1
		3 m/s	25.9	-	-
Ψ_{JT}	$\frac{T_J - T_{top}}{P}$ P = TDP	No Airflow	0.75	5.3	5.4
		1 m/s	0.87	5.4	5.6
		2 m/s	0.96	5.5	5.63
		3 m/s	1.03	-	-
Θ_{JC}	$\frac{T_J - T_C}{P_{top}}$ P_{top} = Power through top of package	No Airflow	7.9	-	-
Θ_{JB}	$\frac{T_J - T_B}{P_{bot}}$ P_{bot} = Power through bottom of package	No Airflow	23.5	-	-

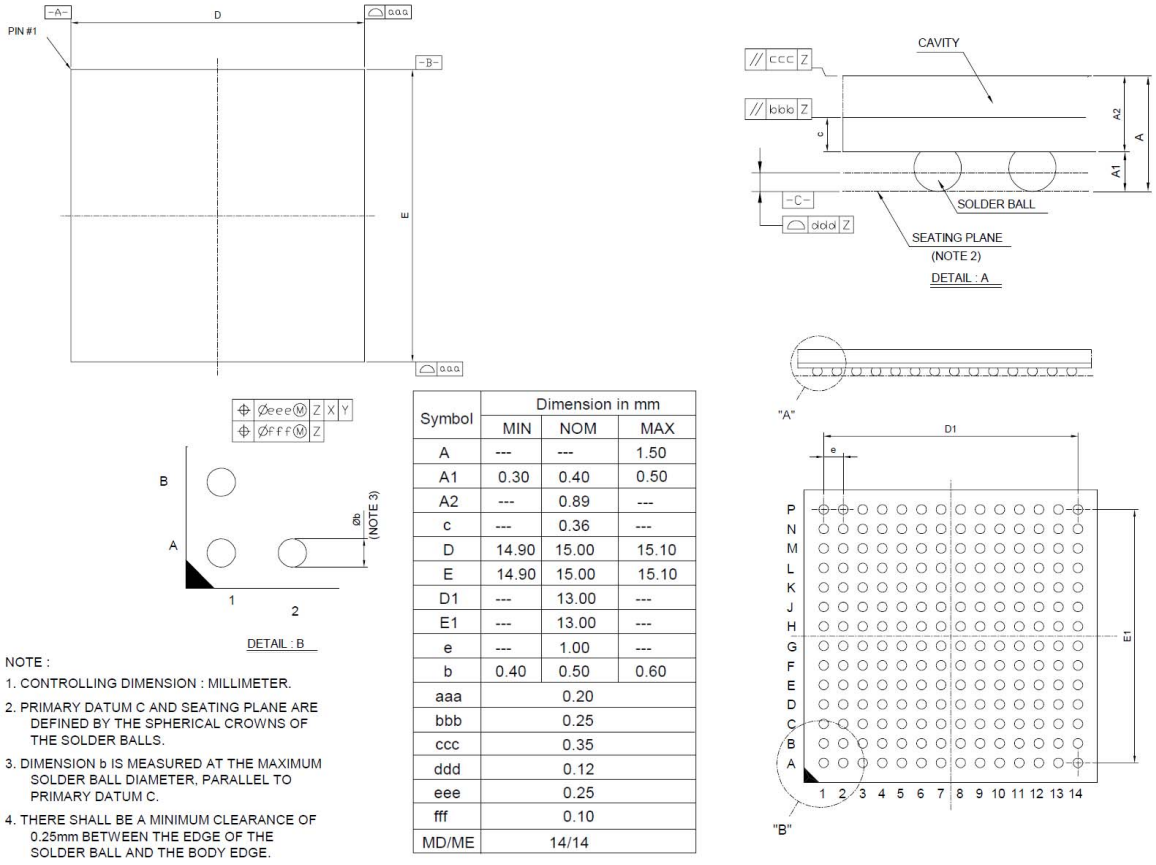
1. 101.5 mm x 114.5 mm, 2s2p JEDEC board using 19 x 19 x 6.3 mm Alpha Novatech* heat sink as shown in Figure 7.2.
2. 101.5 mm x 114. 5mm, 2s2p JEDEC board using 27 x 27 x 10 mm Thermalloy* heat sink as shown in Figure 7.3.

7.6.3 Mechanical Limits - Maximum Static Normal Load

The I347-AT4 package is capable of sustaining a maximum static normal load of 8 lbf (35.6 N). This load is an evenly distributed, uniform, compressive load in a direction perpendicular to the top surface of the package. This limit must not be exceeded during heat sink installation, mechanical stress testing, standard shipping conditions, and/or any other use condition. The load put on the package by the heat sink attachment method should also not exceed this value. The PCB under the package must be fully supported during heat sink installation to prevent any deformation of the PCB. This load specification is based on limited testing for design characterization, and is for the package only.

7.6.4 Mechanical Specifications

The I347-AT4 is packaged in a 15 x 15 mm TFBGA as shown in Figure 7.1.



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.50
A1	0.30	0.40	0.50
A2	---	0.89	---
c	---	0.36	---
D	14.90	15.00	15.10
E	14.90	15.00	15.10
D1	---	13.00	---
E1	---	13.00	---
e	---	1.00	---
b	0.40	0.50	0.60
aaa	0.20		
bbb	0.25		
ccc	0.35		
ddd	0.12		
eee	0.25		
fff	0.10		
MD/ME	14/14		

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

Figure 7.1. I347-AT4 TFBGA Mechanical Drawing

7.7 Thermal Solutions

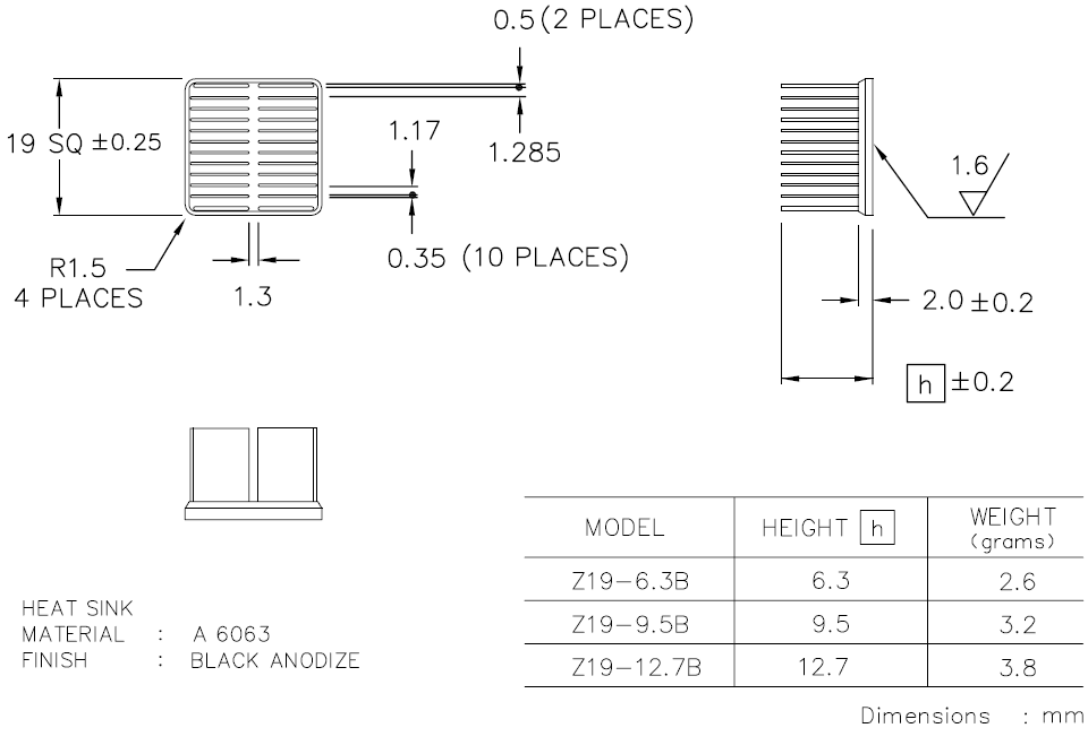
One method frequently used to improve thermal performance is to attach a metallic heat sink to the top of the device. The heat sink increases the surface area exposed to the ambient air promoting higher rates of heat transfer. This in turn reduces the thermal resistance from the device junction to the air (Θ_{JA}). In order to be effective, heat sinks should have a pocket of air around them that is free of obstructions. This enables air to more easily flow through the fins of the heat sink, further increasing its effectiveness.

Good system airflow is critical to dissipate the highest possible thermal power. The size and number of fans, vents, and ducts, as well as their placement in relation to components and airflow channels within the system determine the airflow path and volumetric flow rates throughout the system. Note that acoustic noise constraints might limit the size and types of fans, vents, and ducts that can be used in a particular design.

To develop a robust, reliable, cost-effective thermal solution, all system variables must be considered. Use system-level thermal characteristics and simulations to account for individual component thermal requirements.

7.7.1 Extruded Heat Sinks

If required, the following extruded heat sinks are suggested for I347-AT4 thermal solutions. They can be seen as shown in Figure 7.2 and Figure 7.3 with their respective mechanical drawings.



MODEL	HEIGHT [h]	WEIGHT (grams)
Z19−6.3B	6.3	2.6
Z19−9.5B	9.5	3.2
Z19−12.7B	12.7	3.8

Dimensions : mm

Figure 7.2. 6.3 mm Tall Passive Heat Sink (Alpha Novatech, Inc. PN: Z19-6.3B)

Width	Length	Height	Fin Thickness Across Width	Fin Thickness Across Length	Base Thickness	# of fins across width	# of fins across length
27mm	27mm	10mm	0.90mm	0.93mm	1.50mm	12	13

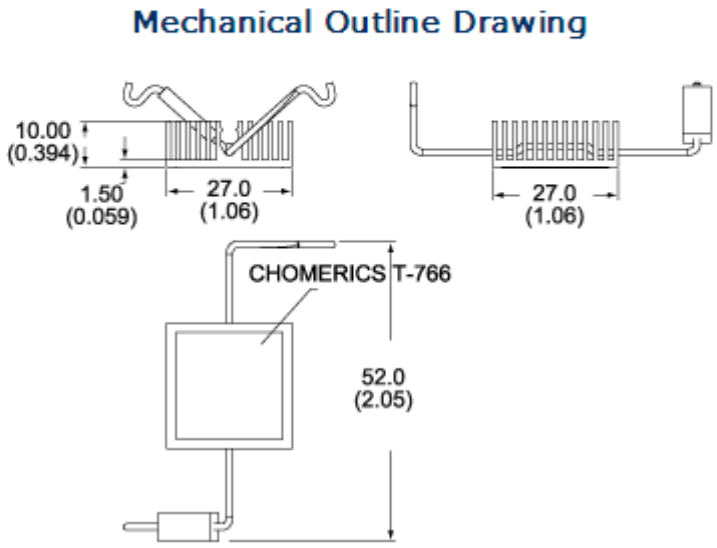


Figure 7.3. 10 mm Tall Passive Heat Sink (AAVID Thermalloy PN: 374324B60023G)

7.7.2 Thermal Interface Materials for Heat Sink Solutions

To maximize the effectiveness of any thermal solution, it is important to understand the interface between the package surface and the heat sink base. The purpose of the Thermal Interface Material (TIM) is to enhance the heat transfer between two objects in contact (see Figure 7.4). At a microscopic level, surfaces are often rough and contain many peaks and valleys. They only contact each other at random points across the interfacing surfaces, thus heat only conducts effectively through those small points of contact. Heat also conducts through the air in the areas that are not touching; however, air is a very poor thermal conductor. This results in a high thermal resistance between the two objects.

When a thermal interface material is applied, it fills the remaining gaps between the two surfaces and provides a much more effective heat path. This enables more heat to conduct through to the heat sink, reducing the temperature drop across the interface.

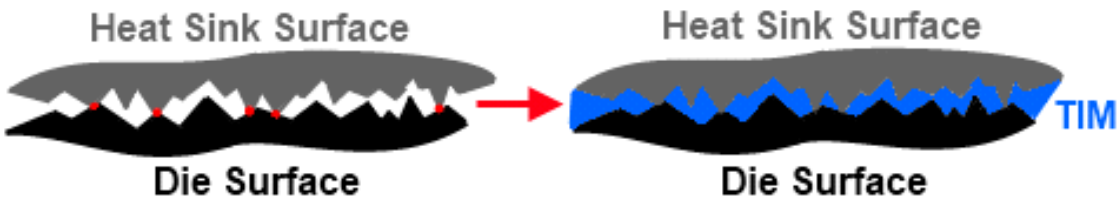


Figure 7.4. TIM Function

7.7.2.1 TIM Types and Performance

There are several different types of TIMs, such as:

- Greases — A tacky, liquid like substance.
- Phase Change Materials (PCM) — A material that starts out as a dry film and changes to a liquid above a specific temperature.
- Gap Pads — Compressible (typically) non-liquid material designed to fill a large gap between the heat sink and package.
- Pressure Sensitive Adhesives (PSA's) — A permanent adhesive applied to the bottom of a heat sink.

PCMs and greases tend to be the most effective as they offer the thinnest bond lines with great wetting/spreading characteristics. The effectiveness of each of these different material types is governed primarily by the following:

- Material Wetting/Filling Characteristics — determines how well the material flows to fill in the small gaps between interfacing surfaces. The more completely the material fills the voids at the interface, the lower the resulting thermal resistance.
- Bond Line Thickness — the resulting thickness of material between the heat sink and package surface once the heat sink has been installed and the material has heated to its equilibrium temperature. Greases and phase change materials tend to flow after they have been heated above a temperature specific to that TIM.
- Material Thermal Conductivity — The thermal conductivity of the interface material.

While the wetting and thermal conductivity are material dependent characteristics, the bond line thickness is primarily controlled by the interfacial pressure between the heat sink and package (as well as the TIM malleability). Typically, higher interfacial pressure leads to lower thermal conductivity as demonstrated (for example only) in the plot the follows.

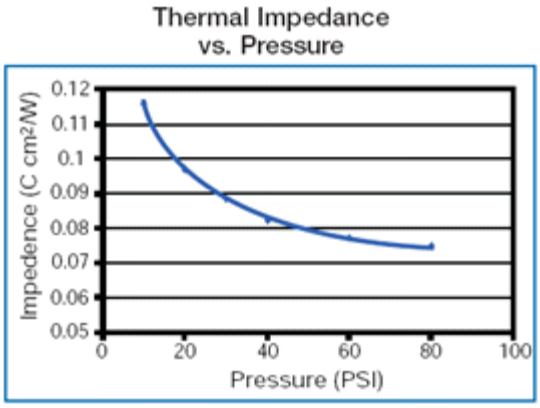


Figure 7.5. Thermal Impedance vs. Interfacial Pressure

Note: Caution should be taken so that the maximum normal force as explained in Section 7.6.3 is never exceeded.

7.7.2.2 PCM45 Series TIM

The recommended thermal interface material is the PCM45 Series from Honeywell*. The PCM45 Series thermal interface pads are phase change materials formulated for use in high performance devices requiring minimum thermal resistance for maximum heat sink performance and component reliability. These pads consist of an electrically non-conductive, dry film that softens at device operating temperatures resulting in a greasy-like performance. However, Intel has not fully validated the PCM45 Series TIM.

If adequate thermal margin exists, cheaper TIM with less performance can be used, especially for low power applications. The selected material should be fully evaluated for long term reliability issues such as dry-out and pump-out (if applicable). Double-sided PSAs should also be carefully evaluated to ensure they provide robust, long term reliability and will not lose their adhesion.

Other TIM vendors to consider are Laird*, Chromerics*, and 3M*.

7.7.3 Attaching the Extruded Heat Sink

There are several different ways of attaching the heat sink to the component such as sheet metal clips, wire gates, PSAs, or spring loaded push pins. Each of these solutions has their own pros and cons. For detailed attaching methods, please contact the heat sink manufacturer. A well designed clip, wire gate, or spring loaded push pin can offer a high level of reliability and rework-ability.

7.8 Reliability

Each PCA, system, heat sink, and TIM combination varies in attach strength, long-term adhesive performance, and TIM reliability. Carefully evaluate the reliability of the completed assembly prior to high-volume use. Some reliability recommendations are listed in Table 7.3.

Table 7.3. Reliability Validation

Test	Requirement	Pass/Fail Criteria
Mechanical Shock	50 G trapezoidal, board level 11 ms, 3 shocks/axis	Visual and electrical check.
Random Vibration	7.3 G, board level 45 minutes/axis, 50 to 2000 Hz	Visual and electrical check.
High Temperature Life	85 °C 2000 hours total Checkpoints occur at 168, 500, 1000, and 2000 hours	Visual and mechanical/electrical check.
Thermal Cycling	Per-Target Environment (for example: -40 °C to +85 °C) 500 cycles	Visual and mechanical/electrical check.
Humidity	85% relative humidity 85 °C, 1000 hours	Visual and mechanical/electrical check.

7.9 JEDEC Simulation Results

7.9.1 Designing for Thermal Performance

Section 7.12 and Section 7.13 describe the PCB and system design recommendations that can aid in achieving the I347-AT4 thermal performance documented in this section.

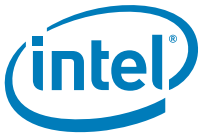
7.9.2 Simulation Setup

A simulation environment conforming to the JEDEC JESD51-2 standard was developed using a 101.5 mm x 114.5 mm, 2s2p board according to JEDEC JESD 51-9. Simulations were run with different combinations of ambient temperature and airflow speed for three different thermal solution scenarios as follows:

- No heat sink
- 19 mm x 19mm x 6.3 mm heat sink (Figure 7.2)
- 27 mm x 27 mm x 10 m heat sink (Figure 7.3)

Note: Keep the following in mind when reviewing the data that is included in this section:

- All data is preliminary and is not validated against physical samples.
- Your system design might be significantly different.
- A larger board with more than four copper layers might improve I347-AT4 thermal performance.



7.9.3 Simulation Results

Table 4 shows the T_{case} as a function of airflow and ambient temperature with the component operating at the TDP in the environment previously listed. This table can be used as an aid in determining a starting point for the optimum airflow and heat sink combination for the I347-AT4.

Again, your system design might vary considerably from the environment used to generate these values.

Note: Thermal models are available upon request (Flotherm*: Detailed Model). Contact your local Intel sales representative for I347-AT4 thermal models.

Table 7.4. Thermal Simulation Results for Various Environmental Conditions @ 3 W TDP

Airflow (LFM)

	T_C	0	50	100	150	200	250	300	350	400
Temperature (°C)	45	143.9	139.1	136.4	134.8	133.5	132.4	131.7	130.9	130.1
	50	148.6	143.9	141.3	139.6	138.3	137.3	136.6	135.8	135.1
	55	153.1	148.6	146.1	144.5	143.2	142.3	141.5	140.7	140
	60	157.7	153.4	150.9	149.4	148.1	147.2	146.4	145.6	145
	65	162.3	158.3	155.8	154.2	153	152.1	151.3	150.5	149.9
	70	166.9	163.1	160.6	159.1	157.9	157	156.3	155.5	154.8
	75	171.5	167.9	165.5	164	162.8	161.9	161.2	160.4	159.8
	80	176.1	172.7	170.3	168.8	167.7	166.8	166.1	165.4	164.7
	85	180.7	177.5	175.2	173.7	172.6	171.7	171.1	170.3	169.6

Note: No heat sink.

Airflow (LFM)

	T_C	0	50	100	150	200	250	300	350	400
Temperature (°C)	45	94.96	88.46	84.77	81.01	78.06	75.55	73.62	72.06	70.88
	50	99.25	93.19	88.63	85.23	82.54	80.47	78.57	77.01	75.83
	55	103.8	97.95	92.96	89.82	87.41	85.4	83.51	81.96	80.54
	60	108.4	102.7	97.76	94.54	92.23	90.32	88.45	86.91	85.67
	65	112.9	107.5	102.6	99.33	97.16	95.24	93.39	91.86	90.62
	70	117.5	112.3	107.4	104.1	102	100.2	98.32	96.81	95.58
	75	122.1	117.1	112.3	108.9	106.8	105.1	103.3	101.8	100.5
	80	126.7	122.1	117.1	113.8	111.8	110	108.2	106.7	105.5
	85	131.3	126.7	122	118.6	116.7	114.9	113.1	111.7	110.4

Note: 19 x 19 x 6.3 mm Alpha Novatech HS in Figure 7.2.

Airflow (LFM)

	T_C	0	50	100	150	200	250	300	350	400
Temperature (°C)	45	86.5	79.8	76.45	73.18	70.55	68.5	67.08	65.77	64.68
	50	91.09	84.52	79.94	77.02	74.95	73.24	71.75	70.44	69.44
	55	95.71	89.26	84.65	81.44	79.22	77.56	76.16	75.01	74.1
	60	100.3	94.01	89.45	86.29	84.03	82.39	80.94	79.84	78.97
	65	104.9	98.78	94.28	91.16	88.88	87.18	85.79	84.76	83.93
	70	109.5	103.6	99.1	96.04	93.77	92.07	90.74	89.7	88.86
	75	114.1	108.4	103.9	100.9	98.68	97.06	95.7	94.66	93.8
	80	118.7	113.1	108.7	105.8	103.6	101.9	100.7	99.62	98.75
	85	123.3	117.9	113.6	110.7	108.5	106.9	105.7	104.6	103.7

Note: 27 x 27 10 mmmm Thermalloy HS in Figure 7.3.

The red value(s) indicate airflow/ambient combinations that exceed the allowable case temperature for the I347-AT4 at 3.0 W.

7.10 Component Measurement Methodology

Measurement methodologies for determining the case and junction temperature are outlined in the sections that follow.

7.10.1 Case Temperature Measurements

Special care is required when measuring the T_{case} temperature to ensure an accurate temperature measurement is produced. Use the following guidelines when measuring T_{case}:

- Use 36-gauge (maximum) K-type thermocouples.
- Calibrate the thermocouple before making temperature measurements.
- Measure the surface temperature of the case in the geometric center of the case top.

Note: It is critical that the thermocouple bead be completely in contact with the package surface.

- Use thermally conductive epoxies, as necessary (again, ensuring the thermocouple bead is in contact with the package surface).
- Care must be taken in order to avoid introducing error into the measurements when measuring a surface temperature. Measurement error may be induced by:
  - — Poor thermal contact between the thermocouple junction and the surface of the package.
  - — Contact between the thermocouple cement and the heat-sink base (if used).
  - — Heat loss through thermocouple leads.

7.10.1.1 Attaching the Thermocouple (No Heat Sink)

Following the guidelines listed in Section 7.10.1, attach the thermocouple at a 0° angle if there is no interference with the thermocouple attach location or leads (see Figure 7.6).

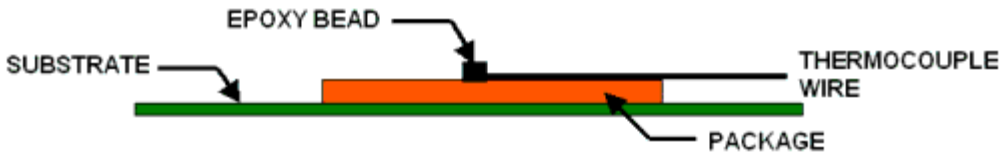


Figure 7.6. Technique for Measuring T_{case} with 0° Angle Attachment, No Heat Sink

7.10.1.2 Attaching the Thermocouple (With a Heat Sink)

In addition to the guidelines listed in Section 7.10.1, the following is also recommended when measuring the T_{case} with a heat sink.

- For testing purposes, a hole (no larger than 0.150 inches in diameter) must be drilled vertically through the center of the heat sink to route the thermocouple wires out.
- Attach the thermocouple at a 90° angle if there is no interference with the thermocouple attach location or leads (see Figure 7.7).
- Ensure there is no contact between the thermocouple cement and heat sink base as that provides a heat transfer path from the thermocouple to the heat sink that can affect the thermocouple reading.

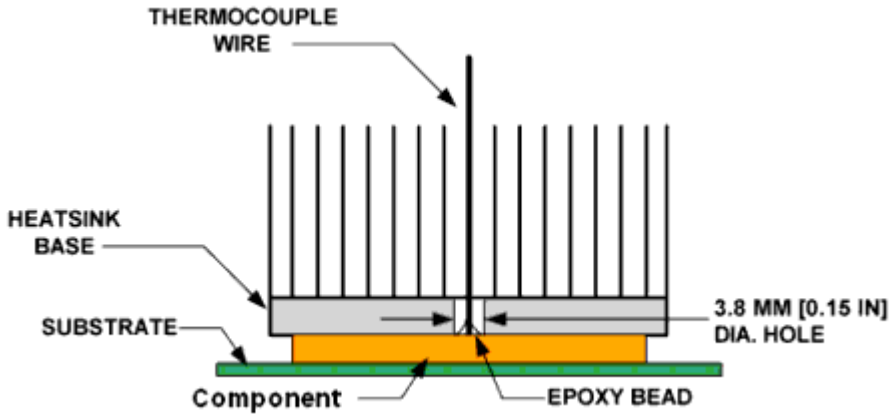


Figure 7.7. Technique for Measuring T_{case} with 90° Angle Attachment

7.11 Conclusion

Increasingly complex systems require more robust and well thought out thermal solutions. The use of system air, ducting, passive or active heat sinks, or any combination thereof can help lead to a low cost solution that meets your environmental constraints.

The simplest and most cost-effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents, and ducts. When additional cooling is required, thermal enhancements can be implemented in conjunction with enhanced system cooling. The size of the fan or heat sink can be varied to balance size and space constraints with acoustic noise.

Use the data and methodologies in this section as a starting point to designing and validating a thermal solution for the I347-AT4. By maintaining the I347-AT4 case temperature below those recommended in this section, the I347-AT4 functions properly and reliably.

7.12 Heat Sink and Attach Suppliers

Table 7.5. Heat Sink and Attach Suppliers

Part	Part Number	Supplier	Contact
Alpha Heat Sinks	LPD40-10B LPD25-7B Z19-6.3B	Alpha Novatech, Inc	Sales Aplha Novatech, Inc. 408-567-8082 sales@alphanovtech.com
Aavid-Thermalloy Heat Sink	374324B60023G	Aavid Thermalloy	Harish Rutti 67 Primrose Dr. Suite 200 Laconia, NH 03246 Business: 972-633-9371 x27
PCM45 Series	PCM45F	Honeywell	North America Technical Contact: Paula Knoll 1349 Moffett Park Dr. Sunnyvale, CA 94089 Cell: 1-858-705-1274 Business: 858-279-2956 paula.knoll@honeywell.com

7.13 PCB Layout Guidelines

The following general PCB design guidelines are recommended to maximize the thermal performance of TFBGA packages:

- When connecting ground (thermal) vias to the ground planes, do not use thermal-relief patterns.
- Thermal-relief patterns are designed to limit heat transfer between the vias and the copper planes, thus constricting the heat flow path from the component to the ground planes in the PCB.
- As board temperature also has an effect on the thermal performance of the package, avoid placing the I347-AT4 adjacent to high-power dissipation devices.
- If airflow exists, locate the components in the mainstream of the airflow path for maximum thermal performance. Avoid placing the components downstream, behind larger devices or devices with heat sinks that obstruct or significantly preheat the air flow.

Note: This information is provided as a general guideline to help maximize the thermal performance of the components.

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