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November 2013

# FQP11N40C / FQPF11N40C

# N-Channel QFET<sup>®</sup> MOSFET 400 V, 10.5 A, 530 m $\Omega$

### **Features**

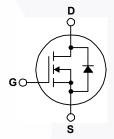
- 10.5 A, 400 V,  $R_{DS(on)}$  = 530 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 5.25 A
- · Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 85 pF)
- · 100% Avalanche Tested

# Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.







# MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQP11N40C	FQPF11N40C	Unit	
V <sub>DSS</sub>	Drain to Source Voltage		400		V	
I <sub>D</sub>	Danim Cumant	-Continuous (T <sub>C</sub> = 25°C)	-Continuous (T <sub>C</sub> = 25°C)		10.5 *	Α
	Drain Current	-Continuous (T <sub>C</sub> = 100°C)	-Continuous (T <sub>C</sub> = 100°C)		6.6 *	Α
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	42	42 *	Α
V <sub>GSS</sub>	Gate to Source Voltage		± 30		V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Not		(Note 2)	360		mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	11		Α
E <sub>AR</sub>	Repetitive Avalanche Energy		(Note 1)	13.5		mJ
dv/dt	Peak Diode Recovery dv/dt (No		(Note 3)	4.5		V/ns
P <sub>D</sub>	Dower Dissination	(T <sub>C</sub> = 25°C)		135	44	W
	Power Dissipation - Derate above 25°C		-	1.07	0.35	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150		°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300		°C	

<sup>\*</sup>Drain current limited by maximum junction temperature

### **Thermal Characteristics**

Symbol	Parameter	FQP11N40C	FQPF11N40C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.93	2.86	°C/W
$R_{\theta JA}$	A Thermal Resistance, Junction to Ambient, Max		62.5	°C/W

# **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQP11N40C	FQP11N40C	TO-220	Tube	N/A	50 units
FQPF11N40C	FQPF11N40C	TO-220F	Tube	N/A	50 units

# **Electrical Characteristics** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	400			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.54		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V			1	μА
		V <sub>DS</sub> = 320 V, T <sub>C</sub> = 125°C			10	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.25 A		0.43	0.53	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 5.25 A	\	7.1		S
	ic Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		840	1090	pF
Coss	Output Capacitance	f = 1.0 MHz		250	325	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			85	110	pF
Switchi	ng Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 200 V, I <sub>D</sub> = 10.5 A,		14	40	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		89	190	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			81	170	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		81	170	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 320 V, I <sub>D</sub> = 10.5 A,	/	28	35	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		4		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)	-	15		nC
Drain-S	ource Diode Characteristics and	d Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode			10.5	Α	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				42	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10.5 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10.5 A,		290		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		2.4		μС

#### Notes

<sup>1.</sup> Repetitive Rating : Pulse width limited by maximum junction temperature.

<sup>2.</sup> L = 5.7 mH, I  $_{AS}$  = 10.5 A, V  $_{DD}$  = 50 V, R  $_{G}$  = 25  $\Omega,$  starting  $\,$  T  $_{J}$  = 25  $^{\circ}C.$ 

<sup>3.</sup>  $I_{SD} \le 10.5$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J$  = 25°C.

<sup>4.</sup> Essentially independent of operating temperature.

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

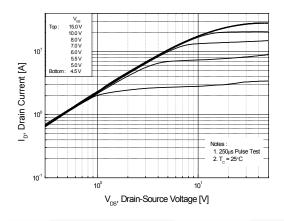


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

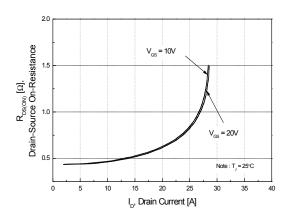


Figure 5. Capacitance Characteristics

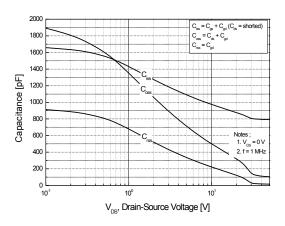


Figure 2. Transfer Characteristics

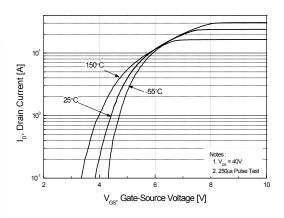


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

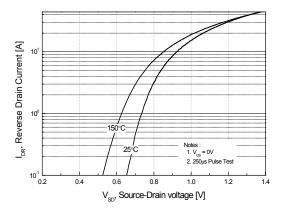
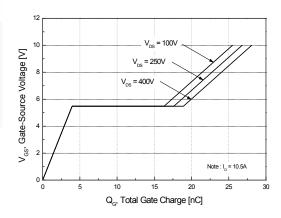


Figure 6. Gate Charge Characteristics



# **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

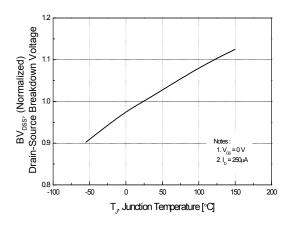


Figure 9-1. Maximum Safe Operating Area of FQP11N40C

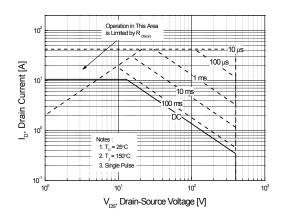


Figure 10. Maximum Drain Current

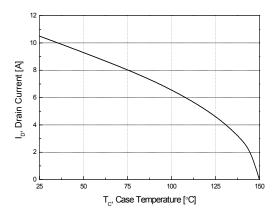


Figure 8. On-Resistance Variation vs. Temperature

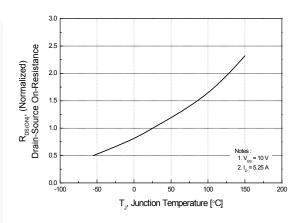
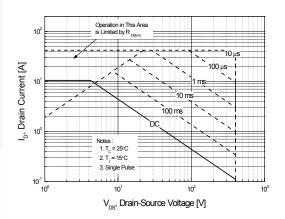


Figure 9-2. Maximum Safe Operating Area of FQPF11N40C



# Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve of FQP11N40C

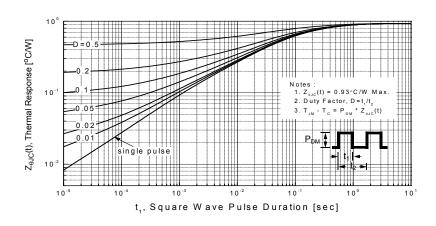


Figure 11-2. Transient Thermal Response Curve of FQPF11N40C

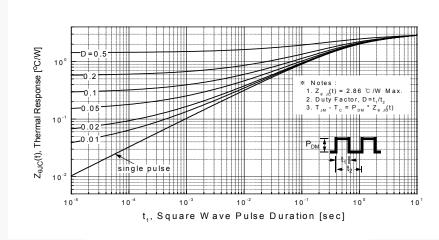


Figure 12. Gate Charge Test Circuit & Waveform

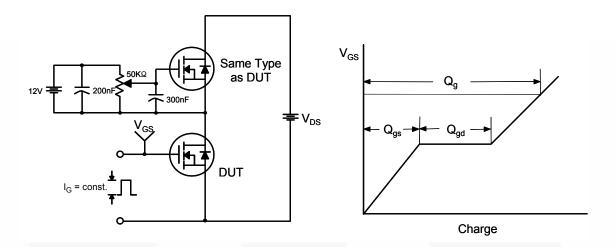


Figure 13. Resistive Switching Test Circuit & Waveforms

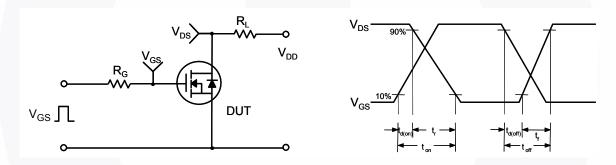
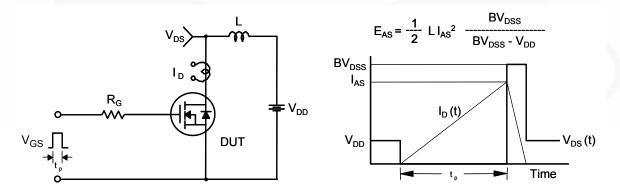


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



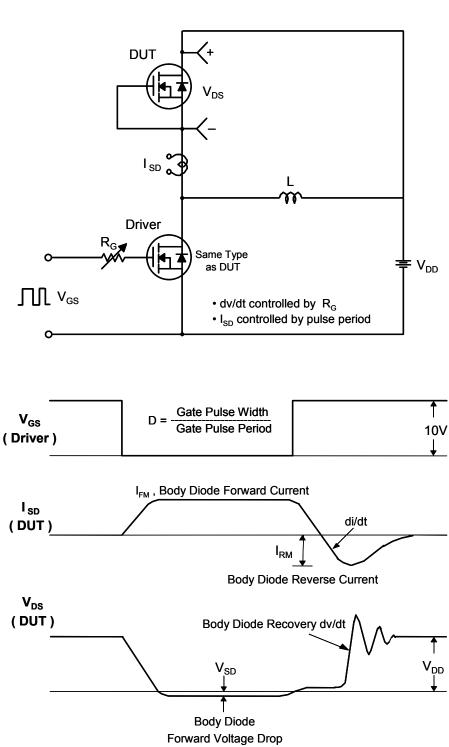


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

# **Mechanical Dimensions**

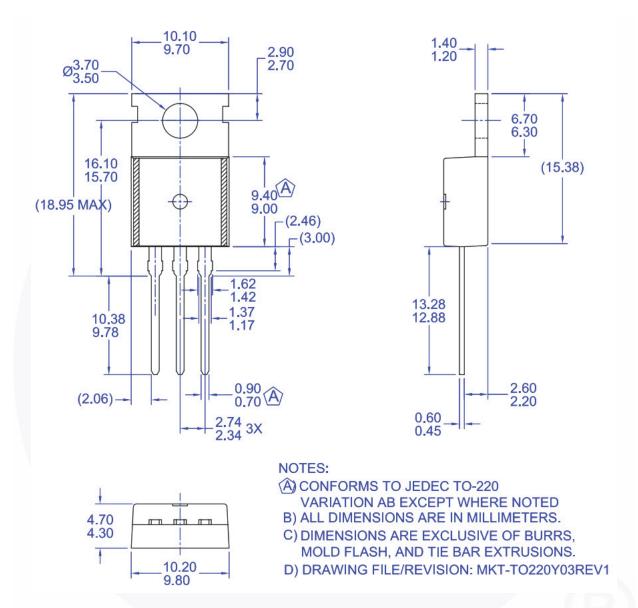


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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# **Mechanical Dimensions**

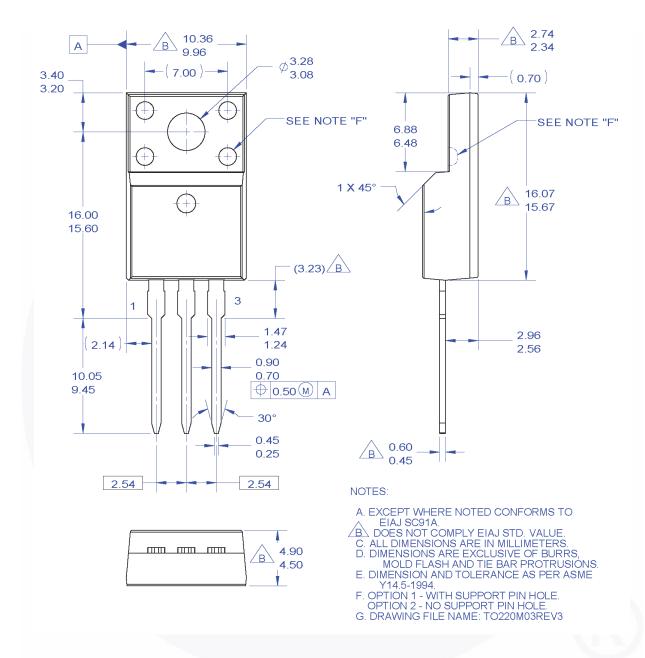


Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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