

BD555BKFV AC/DC Controller IC for mains dimmable LED lighting



BD555BKFV

General Description

The BD555BKFV controller AC/DC controller IC can be used in a wide range of dimmable LED lighting driver applications. The main target application is dimmable retro-fit LED lighting, replacing existing incandescent light bulbs, halogen spot lights, CFL tubes etc.

Features

- Fixed frequency DC/DC controller (selectable)
- Peak current or average current control (PCC/ACC)
- Dynamic Load Current Controller (DLCC)
- Logarithmic compensation of detected dimming level
- Dimmer detector function
- Anti-flash function when dimmer is OFF
- PWM and analog dimming control supported
- Over Current Protection (OCP)
- Thermal Shutdown protection (TSD)
- Under Voltage Lock Out (UVLO)

Applications

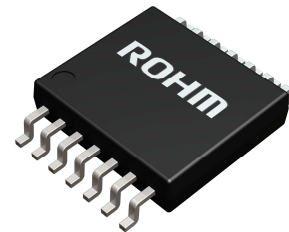
- Retro-fit dimmable LED lighting (E27, E14, GU10, T8 etc.). Wide range of TRIAC and transistor dimmers supported by DLCC function.
- Custom LED lighting with PWM or voltage controlled dimming.

Key Specifications

- Input voltage range.....16~39V
- Regulated supply voltage.....11.5V
- Fixed DC/DC operating frequency.....40~400kHz
- Detectable phase-cut range.....45°~135°
- Typical current consumption.....1mA
- Under Voltage Lock Out detection.....9.0V
- Operating temperature range.....-40~+110°C

Package SSOP-B14

W(Typ.) x D(Typ.) x H(Max.)
5.00mm x 6.40mm x 1.15mm



Typical Application Circuits

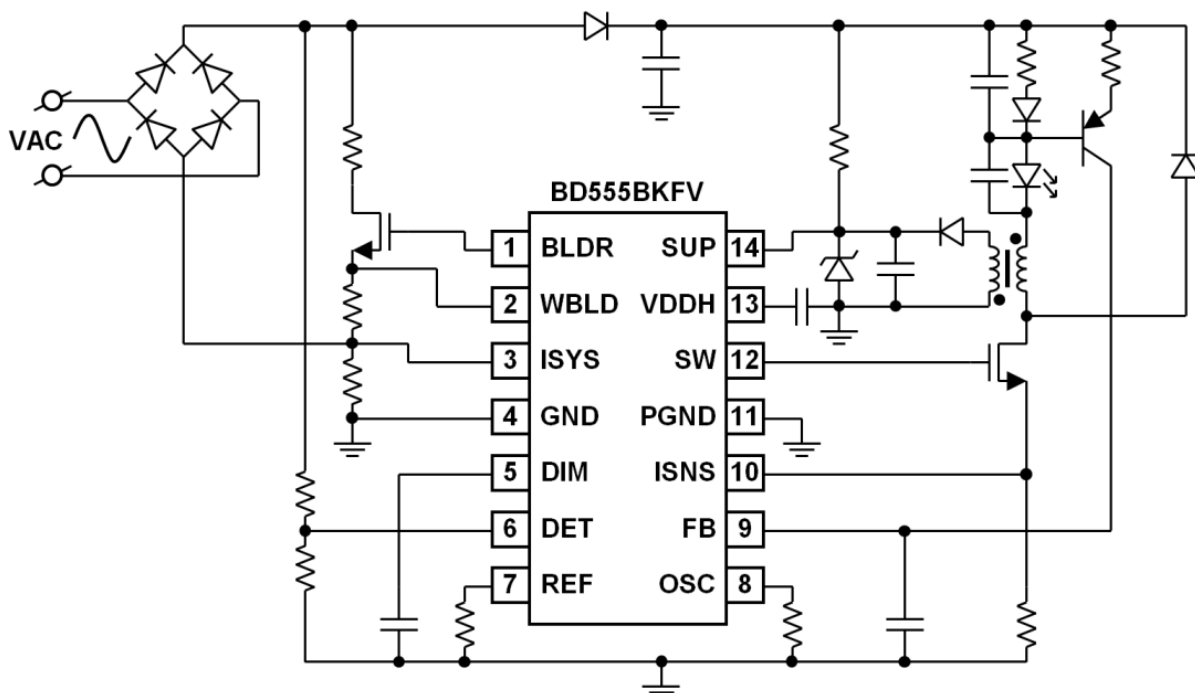


Figure 1. Typical application circuit for non-isolated dimmable buck topology

● Pin Configuration

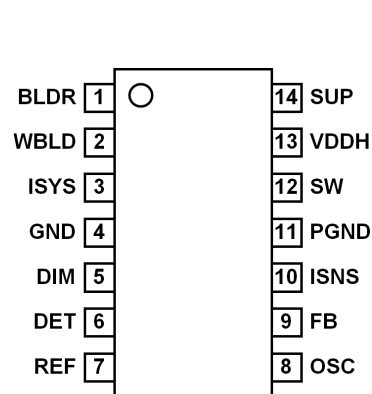


Figure 2. Pin configuration

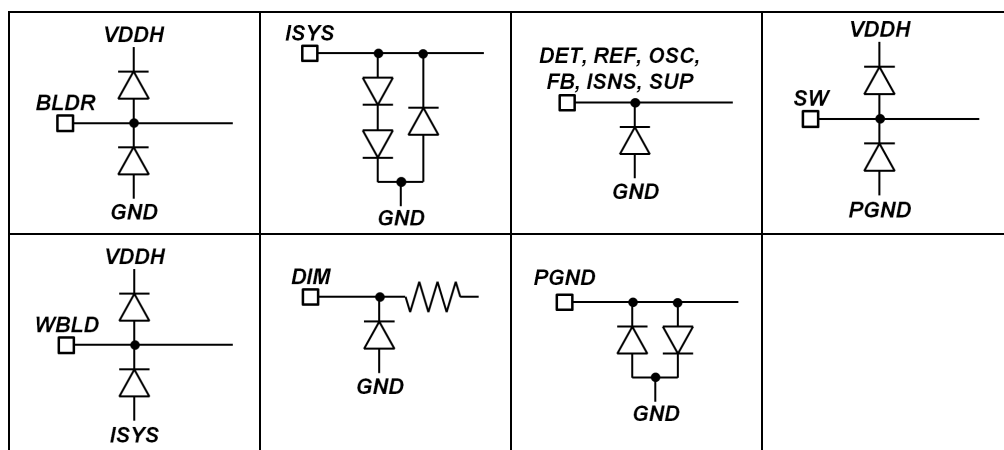


Figure 3. Equivalent circuit

● Pin Description

Pin	Pin name	Function
1	BLDR	Driver for dynamic load current controller (DLCC) transistor
2	WBLD	Internal strong load current input (connected to internal 'open drain' NMOS)
3	ISYS ^{*1}	Sense voltage input for DLCC ON/OFF function
4	GND	Ground terminal
5	DIM	Detected dimming level reference voltage
6	DET	Input for detecting phase-cut angle
7	REF ^{*2}	Pin for external resistor to set LED current (average current control mode)
8	OSC ^{*2}	Pin for external resistor to set DC/DC operating frequency
9	FB ^{*3}	Average current feedback input or PCC mode selection ($V_{FB} < 1.5V$)
10	ISNS	Sense voltage for peak current regulation & over current protection (OCP)
11	PGND ^{*4}	Ground terminal for internal BLDR and SW driver stages
12	SW	Driver output for gate of external DC/DC switching MOSFET
13	VDDH	Regulated supply voltage
14	SUP	Input supply voltage

^{*1} Between ISYS and GND are internal anti-parallel surge diodes

^{*2} Connect only resistive load according to application instructions

^{*3} FB terminal is 'pre-charged' to 4V during start-up in order to have smooth start of the LED current regulation. Never connect this pin directly to GND.

^{*4} Between GND and PGND are internal anti-parallel diodes

●Block Diagram

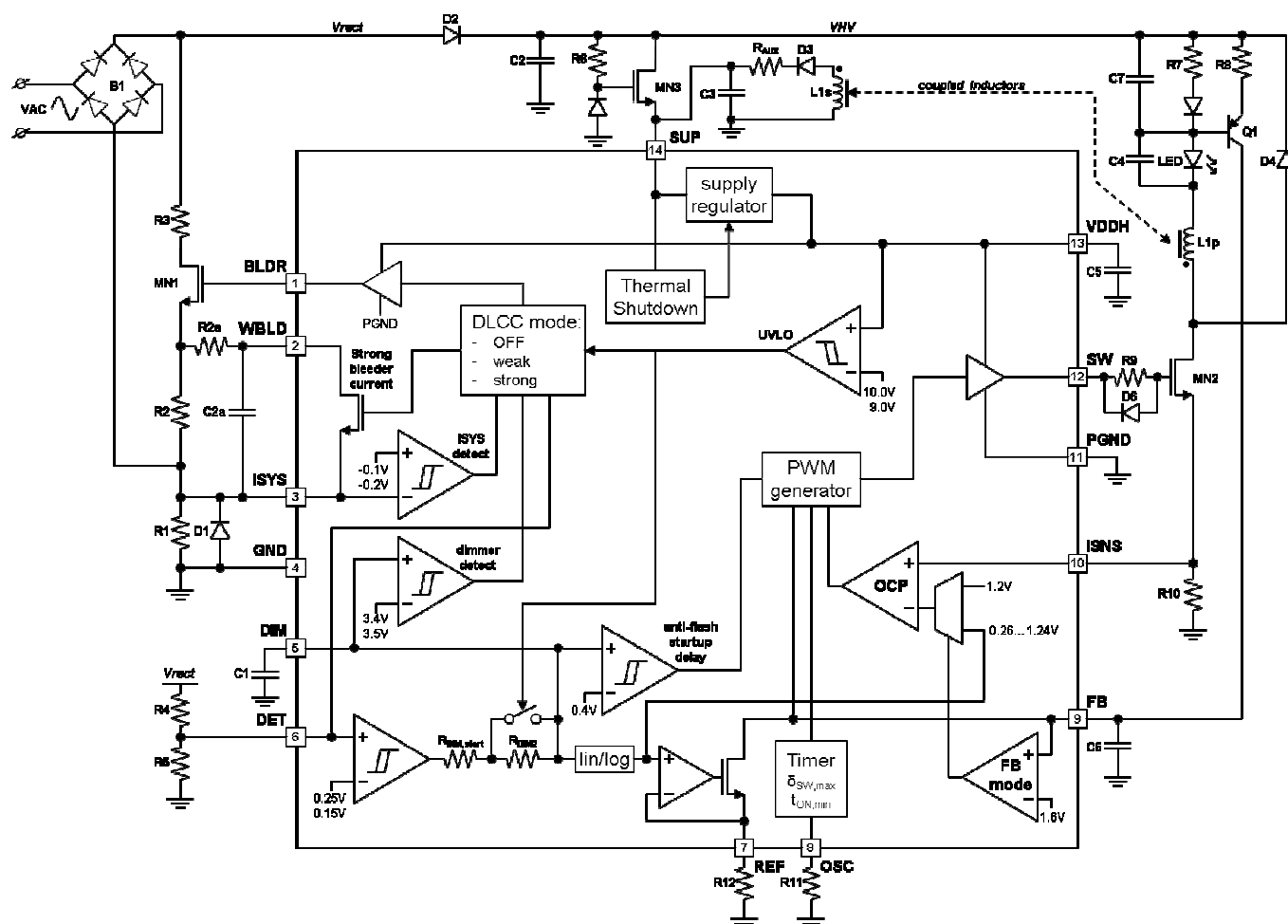


Figure 4. Block diagram of BD555BK FV functions

●Description of Blocks

Startup sequence: when an AC input voltage is applied, the rectified mains voltage (VHV) is buffered by capacitor C2 and starts supplying the BD555BK FV via start-up resistor R6. The VDDH capacitor C5 will be charged by the internal regulator until the system UVLO condition is released, after which a PWM signal from terminal SW can start driving the external NMOS when the anti-flash detector is released.

Anti-flash detector: Some dimmers require a small leakage current to power an internal electronic control circuit or an indicator LED. In order to prevent a 'false start' when the VHV buffer cap was accidentally charged by this leakage current, the detection level voltage on the DIM terminal needs to rise above 400mV, before the SW terminal starts switching, lighting up the LEDs.

DC/DC buck converter: when the SW signal is high, it turns ON the MN2 MOSFET, building up a current in coil L1 via the LED string. During the OFF period of MN2, the current flows via fly-back diode D4. Capacitor C4 stabilizes the LED voltage to reduce the LED current ripple. The LED current is regulated by controlling the LED forward voltage.

Auxiliary supply voltage: The alternating current in the primary side of inductor L1 is coupled $n_p:n_s$ to the secondary side, creating a voltage alternating between V_{VHV} (MN2=ON) and $(V_{LED} + V_{th,D4}) * n_s/n_p$ (MN2=OFF). This last voltage is passed on to capacitor C3 via diode D5. This creates an auxiliary supply which improves efficiency by reducing the resistive power loss in the start-up resistor R6.

LED average current control (ACC) mode: The BD555BK FV features two feedback mechanisms by average current control (ACC) or peak current control (PCC). In ACC mode, the high-side sensing resistor R7 is used in the LED current mirror (typically 1:500), creating an LED feedback current in transistor Q1. This current flows to the FB terminal and creating a reference voltage (for LED current regulation) across resistor R12 at the REF terminal.

LED peak current control (PCC) mode: Alternatively, in PCC mode ($V_{FB} < 1.5V$), the duty-cycle of the SW signal is determined by the 'peak current' through resistor R10. The ISNS terminal senses the voltage across resistor R10. When this voltage reaches the reference voltage, the SW signal will be pulled low. During startup and in ACC mode, this function is used as 'Over Current Protection' to limit the current through inductor L1. In both ACC and PCC mode, the REF voltage will be adjusted to the detected phase-cut in case a dimmer is connected.

Phase-cut detection: via resistive divider R4/R5 at the DET terminal, the rising and falling edge of the phase-cut are detected, generating an internal PWM signal. Via an internal resistor and external capacitor C1, this PWM signal is averaged into a dimming reference voltage at the DIM terminal. An internal conversion function creates a logarithmically corrected voltage at the REF terminal. This allows achieving a 'natural' LED light intensity curve as perceived by the human eye, when turning the dimmer knob.

Dimmer stability: based on the phase-cut detection at the DET terminal, the DLCC dynamically adjusts the total load current for stable operation of 'leading edge' TRIAC dimmers. For 'trailing edge' dimmers, the DLCC load current pulls down the dimmer output voltage, in order to detect the falling edge. In case the VHV current exceeds the minimum load current requirement, the DLCC load current can be disabled completely. This allows to achieve high efficiency without dimmers.

Dimmer detector: when a dimmer is not present, the DLCC will be switched OFF.

●Absolute Maximum Ratings

Parameter	Symbol	Maximum rating	Unit
Supply voltage (SUP terminal)	V_{SUP}	40	V
Internal supply regulator voltage (VDDH terminal)	V_{VDDH}	15.5	V
SW output current	I_{SW}	600 ^{*1}	mA
BLDR output current	I_{BLDR}	60 ^{*1}	mA
WLBD, ISNS terminal voltage	V_{WLBD}, V_{ISNS}	15.5	V
WBLD input current (strong load current)	I_{SBLD}	300 ^{*2}	mA
DIM, DET, OSC, REF, FB terminal voltage	$V_{DIM}, V_{DET}, V_{OSC}, V_{REF}, V_{FB}$	4.5	V
FB input current ($V_{FB}=4.5V$)	I_{FB}	4.0	mA
ISYS, PGND terminal voltage	V_{ISYS}, V_{PGND}	+/- 0.5	V
Operating frequency	$f_{operating}$	400	kHz
Maximum power dissipation	P_d	0.87 ^{*4}	W
Operating ambient temperature range	T_a	-40 ~ +110	℃
Storage temperature range	$T_{storage}$	-55 ~ +150	℃
Maximum junction temperature	$T_{junction,max}$	+150	℃

*1 I_{SW} pulse current duration <100ns@ $f_{operating}$

*2 I_{BLDR} pulse current duration <1us@ f_{mains}

*3 I_{WLBD} pulse current duration <300us@ f_{mains}

*4 SSOP-B14 package thermal resistance $R_{\theta JA}=143^{\circ}C/W$, mounted on a two-layer PCB of 70x70x1.6mm³

●Recommended Operating Range ($T_a = -40 \sim +110^{\circ}C$)

Parameter	Symbol	Range	Unit
Supply voltage	V_{SUP}	16 ~ 39	V

●Electrical Characteristics

Parameter	Symbol	Limits			Unit	Comments
		Min.	Typ.	Max.		
Internal Supply Regulator*1						
Startup current	I _{SUP,start}	-	0.4	0.8	mA	In UVLO condition
Supply current ON	I _{SUP,NS}	-	0.8	1.0	mA	No switching.
Supply current ON 1	I _{SUP,ON1}	-	1.0	1.3	mA	No load on SW/BLDR, f _{SW} =40KHz.
Supply current ON 2	I _{SUP,ON2}	-	2	2.4	mA	No load on SW/BLDR, f _{SW} =400KHz.
VDDH internal regulator voltage	V _{VDDH}	10.0	11.5	15.0	V	VDDH load current I _{VDDH} < 10mA
UVLO release voltage	V _{UVLO,rl}	9.20	10.0	10.8	V	VDDH rising
UVLO trigger voltage	V _{UVLO,tr}	V _{UVLO,tr} - V _{UVLO,hys}			V	VDDH falling
UVLO hysteresis	V _{UVLO,hys}	0.75	1.00	1.25	V	
Switching regulator						
Minimum frequency	f _{SW_min}	32	40	48	kHz	f _{SW} = 9.0×10 ⁶ /R11 (kHz) ^{±20%} , for frequency range 40KHz to 400KHz.
Maximum frequency	f _{SW_max}	320	400	480	kHz	
SW maximum duty cycle	δ _{max}	70	75	80	%	
SW minimum ON-time	t _{ON,min}	-	80	140	ns	Determines minimum duty-cycle

Parameter	Symbol	Limits			Unit	Comments
		Min.	Typ.	Max.		
SW slew rate	t _{SW,slew}	-	50	100	ns	V _{SW} = 1...11V at 1nF load (rising/falling)
SW driver ON resistance (PMOS)	R _{SW,P}	-	15	40	Ω	V _{SW} =0V, I _{SW} =-10mA
SW driver OFF resistance (NMOS)	R _{SW,N}	-	15	40	Ω	V _{SW} = V _{DDH} , I _{SW} =10mA
Duty cycle, FB=3.5V	δ ₂₀	2	20	38	%	ACC mode
Duty cycle, FB=2.9V	δ ₆₀	36	60	80	%	
FB mode selection threshold	V _{FB,mode}	1.4	1.6	1.9	V	PCC (V _{FB} <1.4V), ACC (V _{FB} >1.9V)
ISNS trigger voltage (OCP)	V _{OCP}	1.08	1.20	1.36	V	Inductor current limiter in ACC mode
ISNS blanking time (OCP)	t _{OCP,blank}	90	140	180	ns	Used in PCC & ACC mode
Dimmer phase-cut detector						
DET phase cut voltage (rising)	V _{DET,r}	215	260	300	mV	Monitored at output bridge rectifier
DET phase cut voltage (falling)	V _{DET,f}	75	110	190	mV	
DET phase cut hysteresis	V _{DET,hys}	75	130	180	mV	
DIM voltage (no dimming)	V _{DIM1}	2.85	3.0	3.15	V	Phase-cut = 135°
DIM voltage (max dimming)	V _{DIM2}	0.95	1.0	1.05	V	Phase-cut = 45°
REF voltage (no dimming) ACC	V _{REF,A1}	1.85	2.0	2.15	V	ACC mode (V _{FB} >1.9), 2kΩ < R _{REF} < 10kΩ
REF voltage (max dimming) ACC	V _{REF,A2}	75	100	135	mV	
ISNS voltage (no dimming) PCC	V _{ISNS,P1}	1.12	1.24	1.36	V	PCC mode (V _{FB} < 1.5V). V _{ISNS} peak current threshold, R _{REF} =2kΩ
ISNS voltage (max dimming) PCC	V _{ISNS,P2}	200	260	316	mV	
Dynamic Load Current Controller						
BLDR driver slew rate	t _{BLDR,slew}	-	1	5	μs	V _{SW} = 1...11V at 1nF load (rising/falling)
BLDR driver ON resistance	R _{BLDR,P}	-	100	300	Ω	V _{BLDR} =0V, I _{BLDR} =-10mA
BLDR driver OFF resistance	R _{BLDR,N}	-	100	300	Ω	V _{BLDR} = V _{DDH} , I _{BLDR} =10mA
Strong load current	I _{SBLD,sat}	200	250	-	mA	Strong load current ON (V _{ISYS} <100mV, V _{DIM} <3.4V, V _{VDDH} =11.5V, V _{WBLD} -V _{ISYS} =8V)
Strong load internal NMOS R _{ON}	R _{ON,SBLD}	-	10	300	Ω	Strong load current ON (V _{ISYS} <100mV, V _{DIM} <3.4V, V _{VDDH} =11.5V, V _{WBLD} -V _{ISYS} =8V)
Strong load current OFF delay	t _{SB,OFF}	180	250	320	μs	After phase-cut rising edge
Dimmer detector trigger voltage	V _{DIM,tr}	3.3	3.5	3.7	V	DLCC load current OFF
Dimmer detector release voltage	V _{DIM,rl}	V _{DIM,tr} -V _{DIM,hys}			V	DLCC load current ON
Dimmer detector hysteresis	V _{DIM,hys}	50	100	170	mV	
ISYS load current OFF voltage	V _{ISYS,OFF}	-260	-200	-160	mV	DLCC load current OFF
ISYS load current ON voltage	V _{ISYS,ON}	V _{ISYS,OFF} +V _{ISYS,hys}			mV	DLCC load current ON
ISYS current sense hysteresis	V _{ISYS,hys}	75	100	140	mV	
Anti-flash detector threshold	V _{DIM,start}	360	400	440	mV	DC/DC starts switching (V _{DIM} >400mV)

*1 The supply regulator has a thermal shutdown function that triggers at about 175°C, having a hysteresis of about 20°C. This protects against a too high junction-temperature (e.g. due to 'short' currents of VDDH, SW or BLDR to (P)GND on the PCB or excessive ambient temperatures).

●Application Examples

The BD555BKFV is typically used as a controller IC in retro-fit dimmable LED lighting systems. The external component selection is fully dependent on the type of LED driver. For more information about this, please refer to the BD555BKFV application note. The example circuit below shows a dimmable non-isolated buck converter. A non-isolated topology is suitable for relatively low LED power (e.g. $V_{LED}=100V$ and $I_{LED}=40mA$) applications in which the LED heatsink is electrically isolated by a non-conductive LED lamp casing.

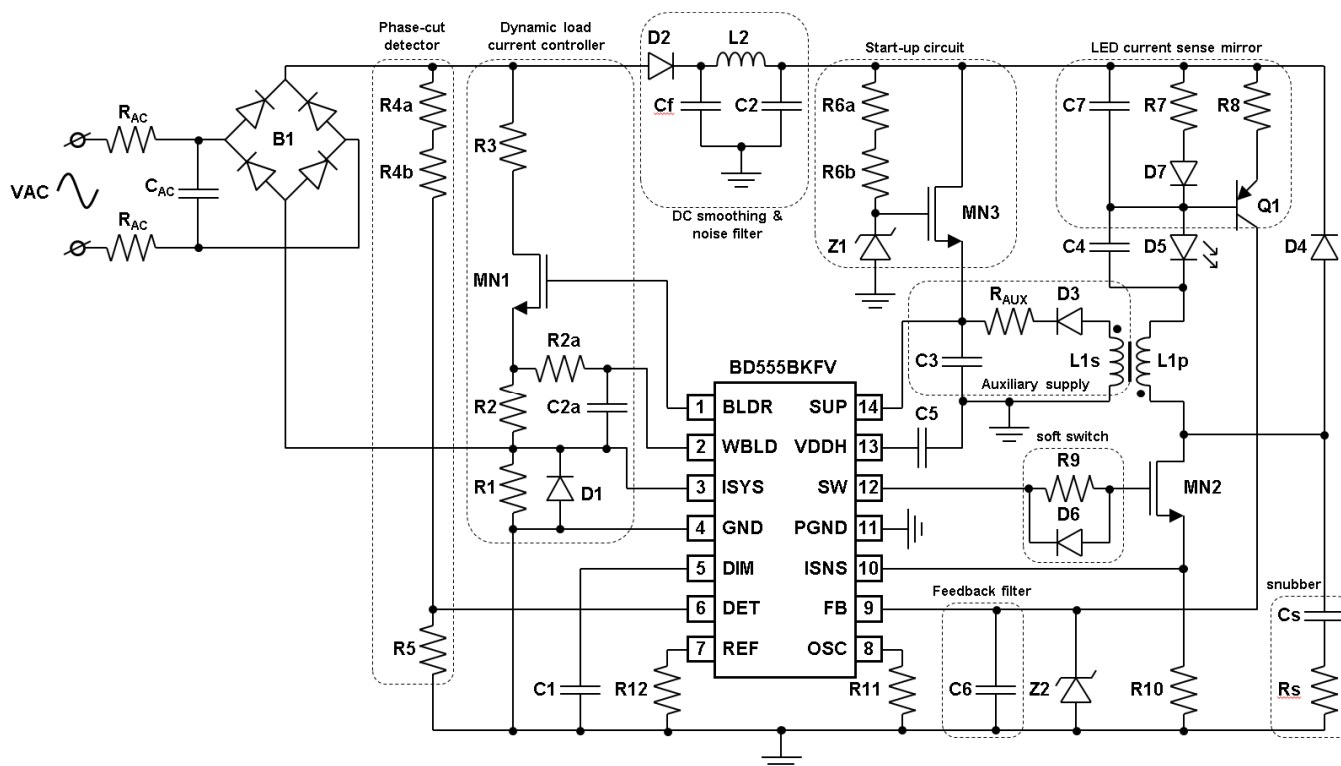


Figure 5. Final application circuit for non-isolated dimmable ACC LED driver

●Notes of board layout

There are a few considerations for designing a small-sized PCB that fits inside a LED lamp casing. Special attention needs to be given to component placement for optimal grounding and minimum distances of high-voltage wiring.

- 1) OCP sense resistor R_{OCP} and snubber resistor R_s need to be connected as close as possible to the minus terminal of the VHV buffer capacitor.
- 2) The drain terminal of switching NMOS MN2 should be close to the inductor $L1p$ and fly-back diode $D4$.
- 3) The GND and PGND terminals need to be connected directly on the PCB.
- 4) For mains-isolated designs (not described in this document), the isolated PCB terminals need to be separated from the 'hot' side electronics.

●Selection of Components Externally Connected

Please refer to the BD555BKFV application note for more information about selecting the external components.

●Power Dissipation

The power dissipation of the BD555BKFV is mainly dependent on the fixed DC/DC operating frequency and the applied load at the SW and BLDR terminals. This power consumption should be less than 80% of the allowable package power dissipation.

●Operational Notes**1) Absolute Maximum Ratings**

When the IC is operated outside of the given absolute maximum ratings, internal devices of the IC can break down and resulting failure modes may be impossible to identify. In case any special operating mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses or overvoltage clamping devices, etc.

2) Special Caution on Terminal Connections

- a. Never connect the FB terminal directly to GND. To enable PCC mode, the FB terminal is best pulled down by a resistor (>10k) to GND.
- b. Always protect the ISYS terminal with a reverse diode to GND in case of using ground current sensing in a dimmable LED driver application. For additional operation stability, a capacitor >1uF is added between GND and ISYS terminals.
- c. Never connect a capacitive load to the REF and OSC terminals. Only resistive loads can be connected to these terminals.
- d. Always short GND and PGND terminals on the application PCB. Special care needs to be taken to keep the GND terminal free from noise. None of the IC terminals except ISYS should have a negative potential.
- e. No external voltage should be applied to the IC terminals when the supply voltage on the SUP terminal is absent.

3) Erroneous Mounting and Terminal Short Circuit

If the IC is mounted incorrectly or in case of a short circuit between supply line, ground and other terminals, the IC may malfunction or break down.

4) Thermal Shut Down

When the IC junction temperature exceeds about 175°C, the TSD function disables internal circuits of the IC and pulls down the internal supply voltage VDDH. The SW terminal will cease switching which stops the DC/DC operation of the application. This safety measure also reduces potential physical damage as a result of overheating in case of a short circuit between VDDH, SW, BLDR and GND terminals. In the thermal design of the application (PCB), the maximum ambient operating temperature and SSOP-B14 maximum power dissipation (Pd) need to be considered to avoid unwanted triggering of the TSD function.

5) Operation in Electromagnetic Fields

The functionality of this IC is not guaranteed in the presence of (strong) electromagnetic fields.

6) External Buffer Capacitors

The capacitor value derating of vs. voltage and temperature and lifetime degradation need to be taken into account in order to ensure proper operation of the IC.

●Status of this document

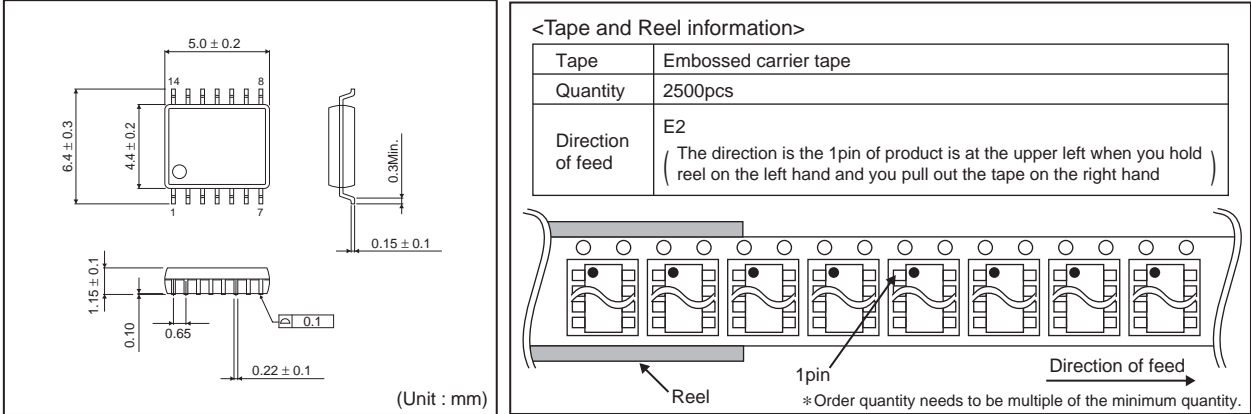
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●Ordering Information

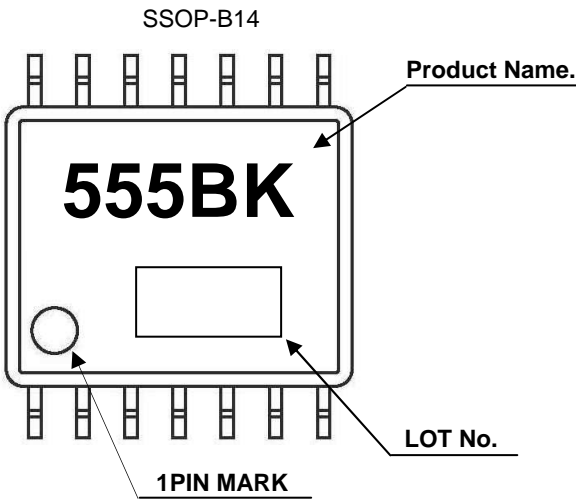
B	D	5	5	5	B	K	F	V	-	E	2
Part No.					Package FV: SSOP14				Packaging and forming specification E2: Embossed tape and reel None: Tray, Tube		

●Physical Dimension Tape and Reel Information

SSOP-B14



●Marking Diagram (TOP VIEW)



●Revision History

Date	Revision	Changes
03.Aug.2012	001	New Release

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