LVDS Interface ICs

27bit LVDS Transmitter

BU90T81

●General Description

The BU90T81 transmitter operates from 20MHz to 112MHz wide clock range, and 27bits data of parallel LVCMOS level inputs(R/G/B24bits and VSYNC,HSYNC,DE) are converted to four channels of LVDS data stream. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less.

The BU90T81 operates from a single 1.8V supply for low power. And the BU90T81 has low swing mode to be able to expect further low power and low EMI .

●Features

- ■24bits data of parallel LVCMOS level inputs are converted to four channels of LVDS data stream.
- ■Support clock frequency from 20MHz up to 112MHz.
- ■Low power 1.8V CMOS design
- ■Power down mode
- ■Clock edge selectable
- ■Support 6bit/8bit mode selectable
- ■Support reduced swing LVDS for low EMI.
- ■Support LVDS Outputs pin reverse function
- ■Support spread spectrum clock generator input

●Key Specifications

■Supply Voltage range	1.65 to 1.95 V
■Operating frequency	20 to 112MHz
■Operating Temperature Range	–20 to 85℃
■Power Consumption	50mW(Typ)

●Packages

VBGA048W040 4.00 ㎜×4.00 ㎜×0.90 ㎜

●Applications

- ■Tablet
- ■Netbook PC
- ■Digital Picture Frame

●Block Diagram

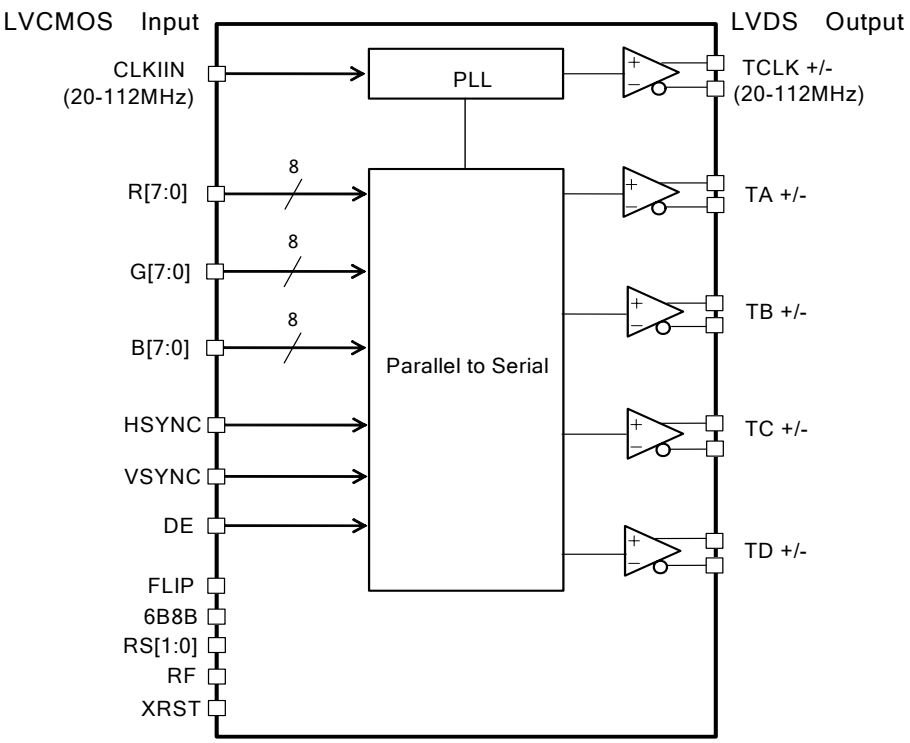


Figure-1 Block Diagram

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●Pin Configuration

Top view

	1	2	3	4	5	6	7
A	G[5]	G[7]	R[1]	R[3]	R[5]	R[6]	R[7]
B	−	G[6]	R[0]	R[2]	R[4]	TA−	TA+
C	G[3]	G[4]	GND	RS[1]	RS[0]	TB−	TB+
D	G[1]	G[2]	RF	VDD	VDD	TC−	TC+
E	G[0]	B[7]	FLIP	6B8B	GND	TCLK−	TCLK+
F	B[6]	B[5]	B[2]	B[0]	DE	TD−	TD+
G	B[4]	B[3]	B[1]	HSYNC	VSYNC	CLKIN	XRST

48pin VBGA

Figure−2 Pin Diagram (Top View)

●Pin Description

Pin Name	Pin No.	Type	Descriptions
TA+/-, TB+/-, TC+/-,TD+/-	B7,B6,C7,C6,D7,D6,F7,F6	LVDS OUT	LVDS Data out
TCLK+/-	E7,6		LVDS Clock out
R[7:0]	A7,A6,A5,B5,A4,B4,A3,B3	CMOS IN	Pixel and control data inputs
G[7:0]	A2,B2,A1,C2,C1,D2,D1,E1		
B[7:0]	E2,F1,F2,G1,G2,F3,G3,F4		
HSYNC,VSYNC, DE	G4,G5,F5		
CLKIN	G6		Clock input
XRST	G7	CMOS IN	Power Down H : Normal operation L : Power down (all LVDS output signal are Hi-z)
RF	D3		Input CLK Triggering Edge Select. H : Rising edge L : Falling edge
RS[1:0]	C3,C5		LVDS swing mode select RS1 / RS0 / LVDS swing L / L / TYP=160mV L / H / TYP=200mV H / L / TYP=350mV H / H / Reserved
6B8B	E4		6bit/8bit mode select H : 6bit mode(FLIP=L TD+/- is Hiz) (FLIP=H TA+/- is Hiz) L : 8bit mode
FLIP	E3		LVDS output pin reverse select. H : Reverse L : Normal
VDD	D4,D5	POWER	1.8V Power supply
GND	C3,E5	GND	Ground Pins

●Absolute Maximum Ratings

Parameter	Symbol	Rating		Units
		Min	Max	
Supply Voltage	V_{DD}	-0.3	2.5	V
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3	V_{DD}+0.3	V
Storage Temperature Range	Tstg	-55	125	℃

●Operating Ratings

Parameter	Symbol	Rating			Units	Conditions
		Min	Typ	Max		
Supply Voltage	V_{DD}	1.65	1.8	1.95	V	
Operating Temperature Range	Topr	-20	-	85	℃	
Operating frequency	Fmax	20	-	112	MHz	

●Package Power

Package	Power Dissipation (mW)	De-rating (mW/℃)*1
VBGA048W040	800*1	8.0*1

*1:Package power when mounting on the PCB board.

The size of PCB board : 114.3×76.2×1.6(mm^3)
The material of PCB board : The FR4 glass epoxy board.

●DC characteristics

Table 1 : LVCMOS DC Specifications(V_{DD}=1.65V～1.95V, Ta=-20℃～+85℃)

Symbol	Parameter	Rating			Units	Conditions
		Min	Typ	Max		
V_{IH}	High Level Input Voltage	V_{DD}×0.7	-	V_{DD}	V	
V_{IL}	Low Level Input Voltage	GND	-	V_{DD}×0.3	V	
I_{INC}	Input Current	-10	-	+10	μA	0V≦V_{IN}≦V_{DD}

Table2: LVDS Transmitter DC Specifications(V_{DD}=1.65V～1.95V, Ta=-20℃～+85℃)

Symbol	Parameter	Rating			Units	Conditions	
		Min	Typ	Max			
V_{OD}	Differential Output Voltage	250	350	450	mV	RL=100Ω	RS[1:0]= HL
		130	200	270	mV		RS[1:0]= LH
		110	160	210	mV		RS[1:0]= LL
ΔV_{OD}	Change in VOD between complementary output states	-	-	35	mV	RL=100Ω	
V_{OC}	Common Mode Voltage	1.125	1.25	1.375	V		
ΔV_{OC}	Change in VOC between complementary output states	-	-	35	mV		
I_{OS}	Output Short Circuit Current	-90	-	-	mA	V_{OUT}=0V	
I_{OZ}	Output TRI-STATE Current	-10	-	+10	μA	XRST=0V, V_{OUT}=0V to V_{DD}	

●AC characteristics

Table 3 : Switching Characteristics（VDD=1.8V, Ta=25℃ RL=100Ω CL=5pF RS[1:0]=HL）

Symbol	Parameter		Min	Typ	Max	Units
t_{TCP}	CLK OUT Period		8.93	-	50	ns
t_{TCIT}	CLK IN Transition time		-	-	5.0	ns
t_{TCH}	CLK IN High Time		$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCL}	CLK IN Low Time		$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TS}	LVSMOS Data Set up to CLK IN		2.5	-	-	ns
t_{TH}	LVCMOS Data Hold from CLK IN		0	-	-	ns
t_{LVT}	LVDS Transition Time		-	0.6	1.5	ns
T_{TSUP}	Differential Output Set up Time	CLKOUT=112MHz	-	-	200	ps
T_{THLD}	Differential Output Hold time	CLKOUT=112MHz	-	-	200	ps
t_{TOP6}	Output Data Position 6		$2\frac{t_{TCP}}{7} - T_{THLD}$	$2\frac{t_{TCP}}{7}$	$2\frac{t_{TCP}}{7} + T_{TSUP}$	ns
t_{TOP5}	Output Data Position 5		$3\frac{t_{TCP}}{7} - T_{THLD}$	$3\frac{t_{TCP}}{7}$	$3\frac{t_{TCP}}{7} + T_{TSUP}$	ns
t_{TOP4}	Output Data Position 4		$4\frac{t_{TCP}}{7} - T_{THLD}$	$4\frac{t_{TCP}}{7}$	$4\frac{t_{TCP}}{7} + T_{TSUP}$	ns
t_{TOP3}	Output Data Position 3		$5\frac{t_{TCP}}{7} - T_{THLD}$	$5\frac{t_{TCP}}{7}$	$5\frac{t_{TCP}}{7} + T_{TSUP}$	ns
t_{TOP2}	Output Data Position 2		$6\frac{t_{TCP}}{7} - T_{THLD}$	$6\frac{t_{TCP}}{7}$	$6\frac{t_{TCP}}{7} + T_{TSUP}$	ns
t_{TOP1}	Output Data Position 1		$7\frac{t_{TCP}}{7} - T_{THLD}$	$7\frac{t_{TCP}}{7}$	$7\frac{t_{TCP}}{7} + T_{TSUP}$	ns
t_{TOP0}	Output Data Position 0		$8\frac{t_{TCP}}{7} - T_{THLD}$	$8\frac{t_{TCP}}{7}$	$8\frac{t_{TCP}}{7} + T_{TSUP}$	ns
t_{TPLL}	Phase Locked Loop Set Time		-	-	10	ms

●AC Timing Diagrams

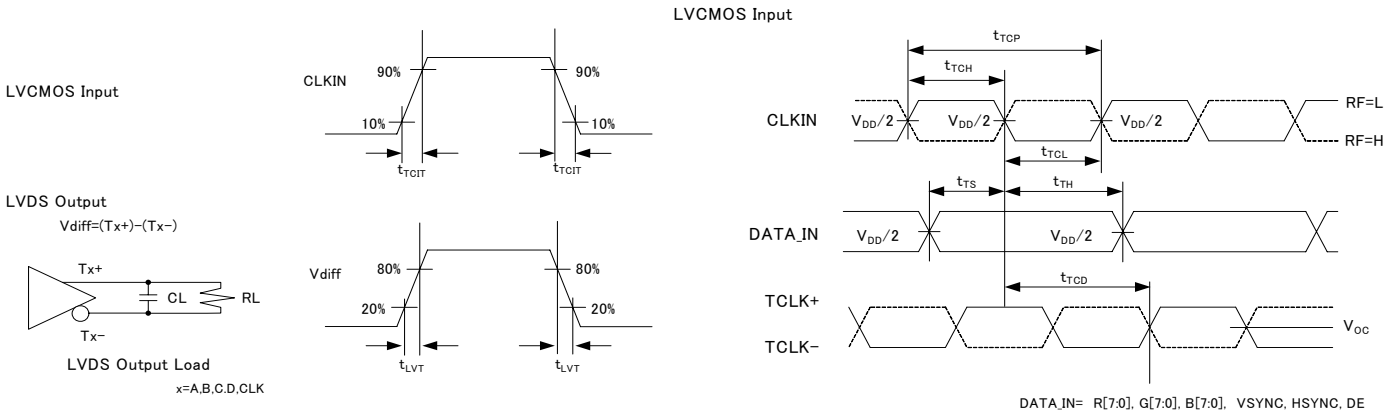


Figure-3 LVCMOS Input AC Timing Diagrams

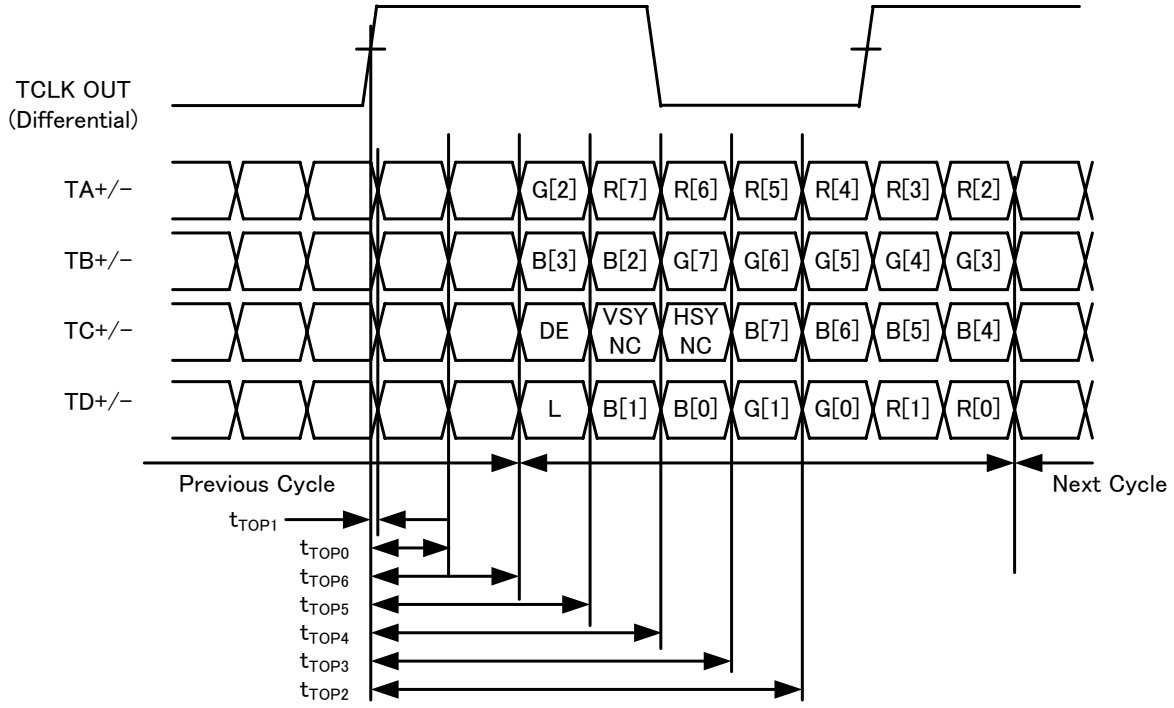


Figure-4 LVDS Output AC Timing Diagrams

●Phase Locked Loop Set Time

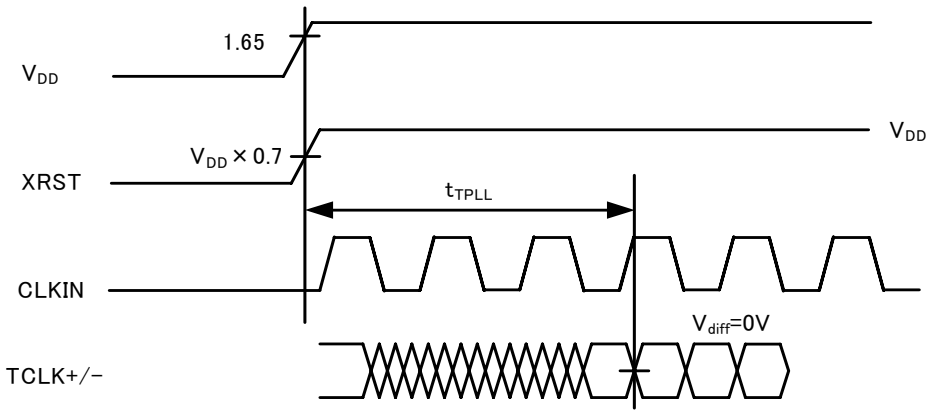


Figure-5 Phase Locked Loop Set Time

●Supply Current

Table 4: Supply Current (6B8B = L)

Symbol	Parameter	Rating			Units	Conditions	
		Min	Typ	Max			
I_{TCCG}	Transmitter Supply Current	-	30.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V,RS[1:0]=HL Gray Scale Pattern	f=85MHz
		-	22.5	-	mA	RL=100Ω,CL=5pF VDD=1.8V,RS[1:0]=LH Gray Scale Pattern	f=85MHz
		-	20.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=LL Gray Scale Pattern	f=85MHz
I_{TCCW}	Transmitter Supply Current	-	32.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=HL Worst case Pattern	f=85MHz
		-	24.5	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=LH Worst case Pattern	f=85MHz
		-	22.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=LL Worst case Pattern	f=85MHz
I_{TCCS}	Transmitter Power Down Supply Current	-	-	10	μA	XRST=L	

Gray Scale Pattern

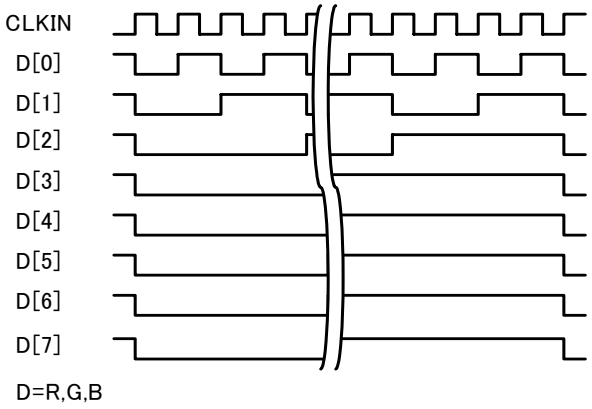


Figure -6 Gray Scale Pattern

Worst Case Pattern (Maximum Power condition)

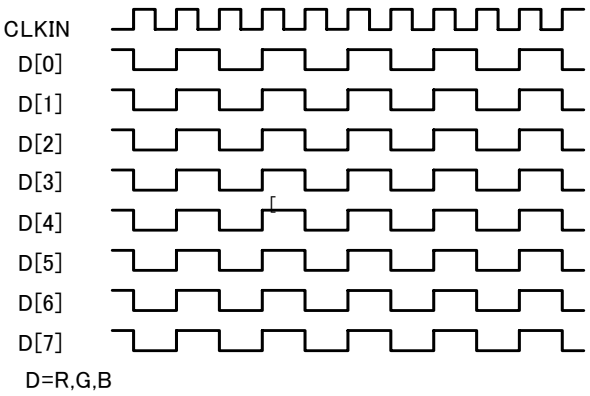
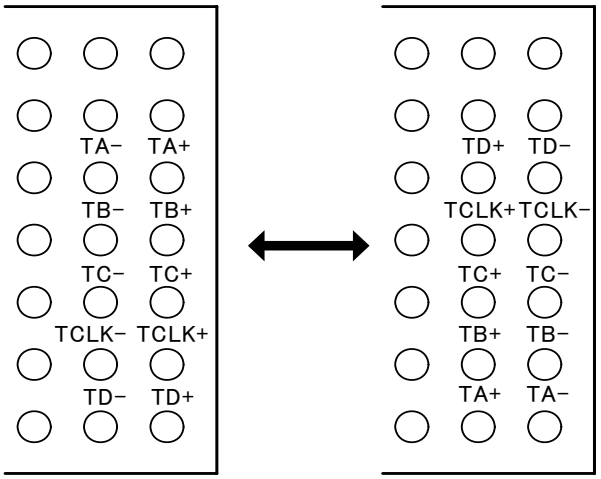


Figure -7 Worst Case Pattern

●LVDS Data Output Table for Function of FLIP pin

Table 5: LVDS Data Output Pin Name

Pin No	Output Pin Names	
	FLIP=L	FLIP=H
B7	TA+	TD-
B6	TA-	TD+
C7	TB+	TCLK-
C6	TB-	TCLK+
D7	TC+	TC-
D6	TC-	TC+
E7	TCLK+	TB-
E6	TCLK-	TB+
F7	TD+	TA-
F6	TD-	TA+



FLIP=L FLIP=H

●LVCMOS Data Inputs Pixel Map Table

Table 6: LVCMOS Data Inputs Pixel Map Table

TFT Panel Data			BU90T81 Input
	24Bit	18Bit	
LSB	R0	-	R0
	R1	-	R0
	R2	R0	R1
	R3	R1	R2
	R4	R2	R3
	R5	R3	R4
	R6	R4	R5
MSB	R7	R5	R6
LSB	G0	-	R7
	G1	-	G0
	G2	G0	G1
	G3	G1	G2
	G4	G2	G3
	G5	G3	G4
	G6	G4	G5
MSB	G7	G5	G6
LSB	B0	-	G7
	B1	-	B0
	B2	B0	B1
	B3	B1	B2
	B4	B2	B3
	B5	B3	B4
	B6	B4	B5
MSB	B7	B5	B6
	VSYNC	VSYNC	B7
	HSYNC	HSYNC	HSYNC
	DE	DE	DE

●LVDS Output Data Mapping

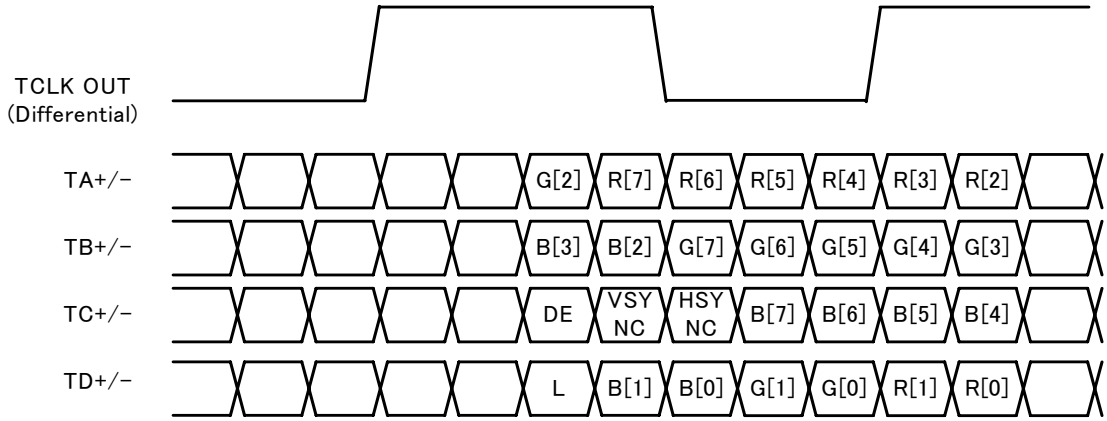


Figure-8 LVDS output mapping (6B8B=L, FLIP=L)

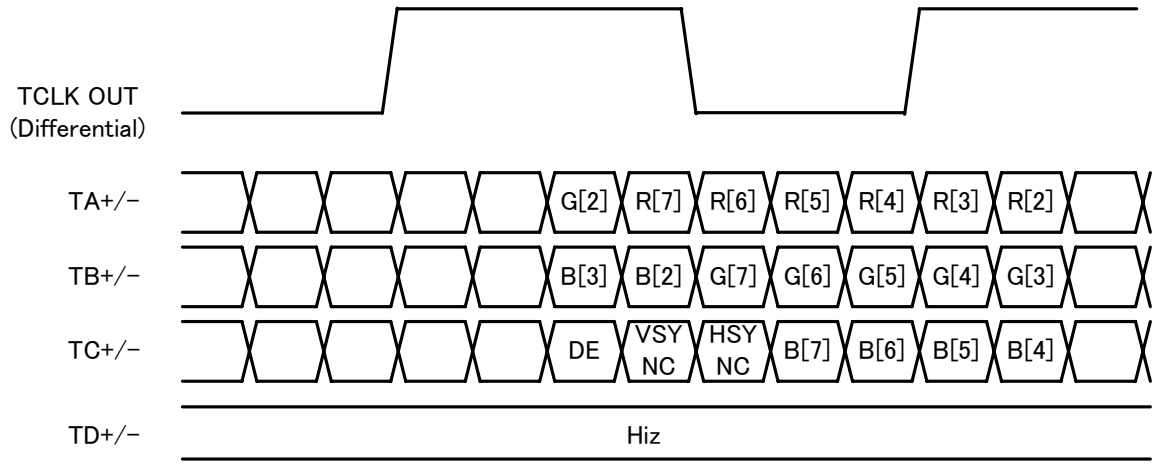


Figure-9 LVDS output mapping (6B8B=H, FLIP=L)

●Typical Application Circuit (24bit mode)

Example
BU90T81: LVCMOS Data Input /rising edge/200mV swing output/normal output mapping

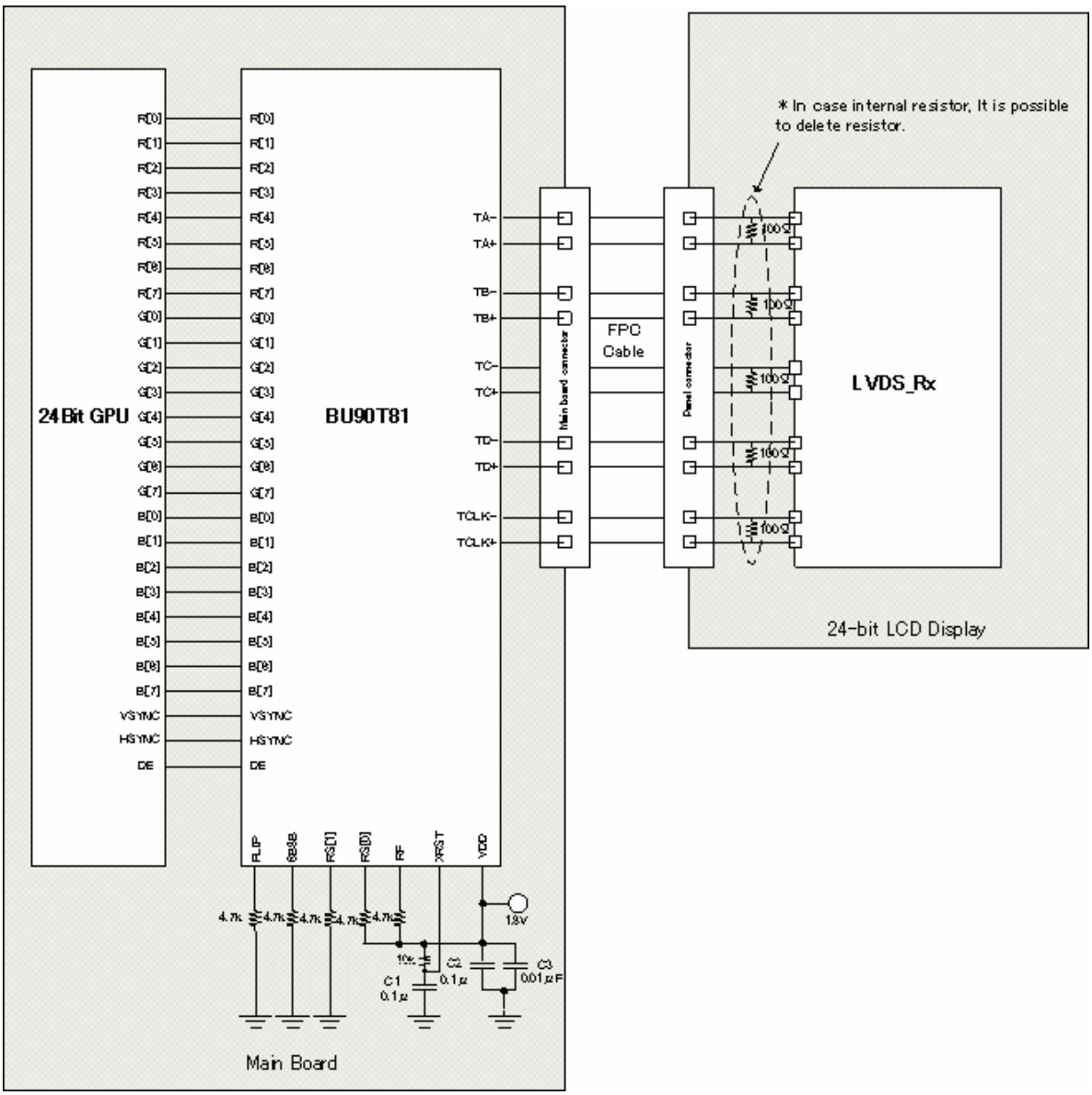


Figure-10 Application Circuit (24bit mode)

●Typical Application Circuit (18bit mode)

Example
BU90T81: LVCMOS Data Input /rising edge/200mV swing output/normal output mapping

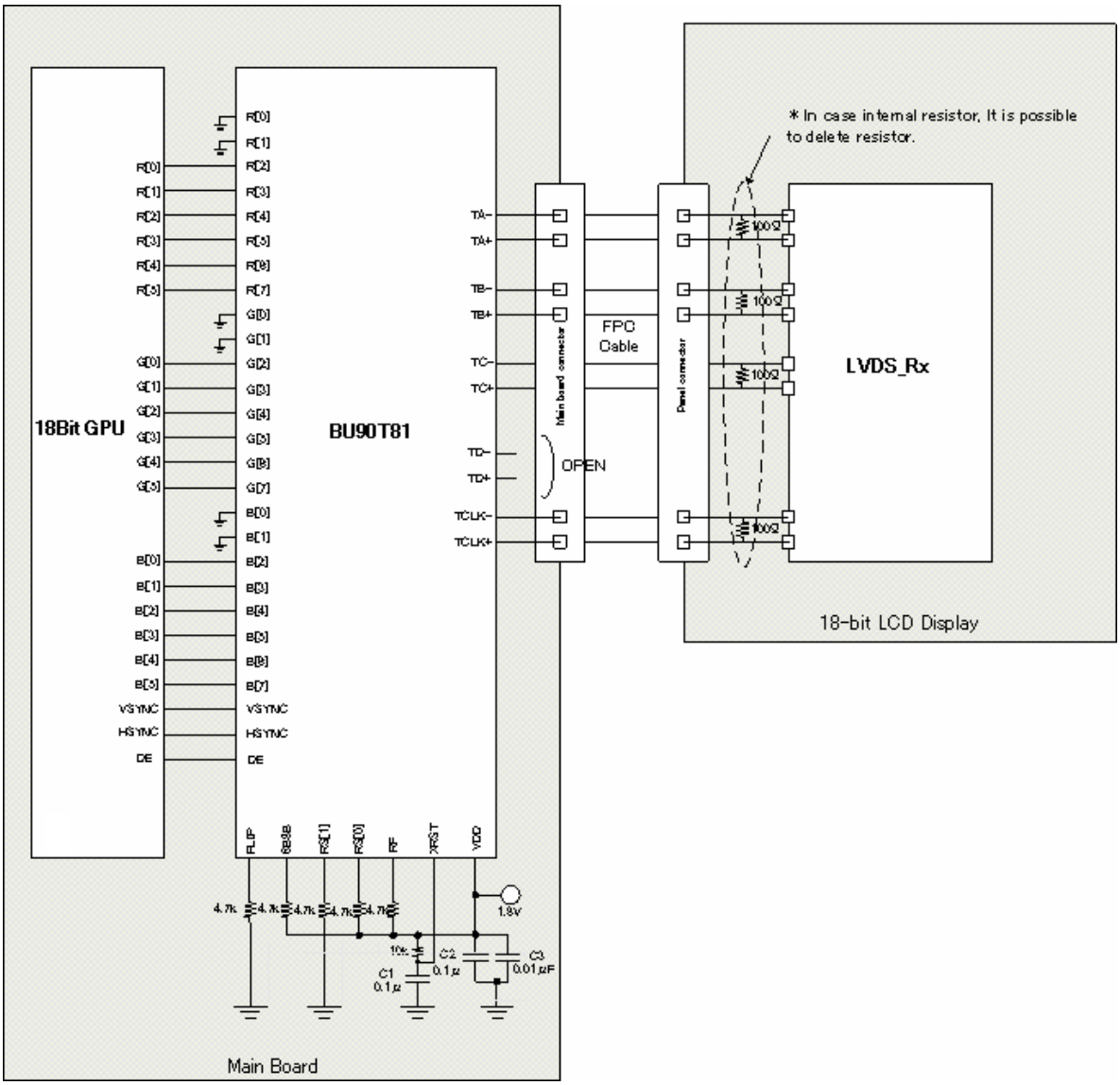


Figure-11 Application Circuit (18bit mode)

●Status of this document

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If there are any differences in translation version of this document formal version takes priority

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