Low Power Stereo ADC for Wireless Handsets and Portable Audio

FEATURES

- **Stereo Audio ADC**
  - **92-dBA Signal-to-Noise Ratio**
  - **Supports ADC Sample Rates From 8 kHz to 96 kHz**
- **Flexible Digital Filtering with RAM Programmable Coefficient, Instructions, and Built-In Standard Modes**
  - **Low Latency IIR Filters for Voice**
  - **Linear Phase FIR Filters for Audio**
  - **Additional Programmable IIR Filters for EQ, Noise Cancellation or Reduction**
  - **Up to 128 Programmable ADC Digital Filter Coefficients**
- **Six Audio Inputs With Configurable Automatic Gain Control (AGC)**
  - **Programmable in Single-Ended or Fully Differential Configurations**
  - **Can be 3-Stated for Easy Interoperability With Other Audio ICs**
- **Low Power Consumption and Extensive Modular Power Control:**
  - **6-mW Mono Record 8-kHz**
  - **11-mW Stereo Record, 8-kHz**
  - **10-mW Mono Record, 48-kHz**
  - **17-mW Stereo Record, 48-kHz**
- **Dual Programmable Microphone Bias**
- **Programmable PLL for Clock Generation**
- **I^2C™ Control Bus**
- **Audio Serial Data Bus Supports I^2S, Left/Right-Justified, DSP, PCM, and TDM Modes**
- **Digital Microphone Input Support**
- **Two GPIOs**
- **Power Supplies:**
  - **Analog: 2.6 V–3.6 V.**
  - **Digital: Core: 1.65 V–1.95 V, I/O: 1.1 V–3.6 V**
- **4mm × 4mm 24-Pin RGE (QFN)**

APPLICATIONS

- **Wireless Handsets**
- **Portable Low Power Audio Systems**
- **Noise Cancellation Systems**
- **Front-End Voice or Audio Processor for Digital Audio**

DESCRIPTION

The TLV320ADC3101 is a low power, stereo audio Analog to Digital Converter (ADC) supporting sampling rates from 8 kHz to 96 kHz with an integrated programmable gain amplifier providing up to 40dB analog gain or AGC. Front-end input coarse attenuation of 0dB, –6dB, or off, is also provided. The inputs are programmable in a combination of single-ended or fully differential configurations. Extensive register-based power control is available via I^2C, enabling mono or stereo recording. Low power consumption makes the TLV320ADC3101 ideal for battery-powered portable equipment.

The AGC programs to a wide range of attack (7ms – 1.4s) and decay (50ms – 22.4s) times. A programmable noise gate function is included to avoid noise pumping. Low-latency IIR filters optimized for voice and telephony are available, as well as linear-phase FIR filters optimized for audio. Programmable IIR filters are also available and may be used for sound equalization, or to remove noise components. The audio serial bus can be programmed to support I^2S, Left-justified, Right-justified, DSP, PCM, and TDM modes. The audio bus may be operated in either master or slave mode.

A programmable integrated PLL is included for flexible clock generation and support for all standard audio rates from a wide range of available MCLKs, varying from 512 kHz to 50 MHz, including the most popular cases of 12-MHz, 13-MHz, 16-MHz, 19.2-MHz, and 19.68-MHz system clocks.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED BLOCK DIAGRAMS

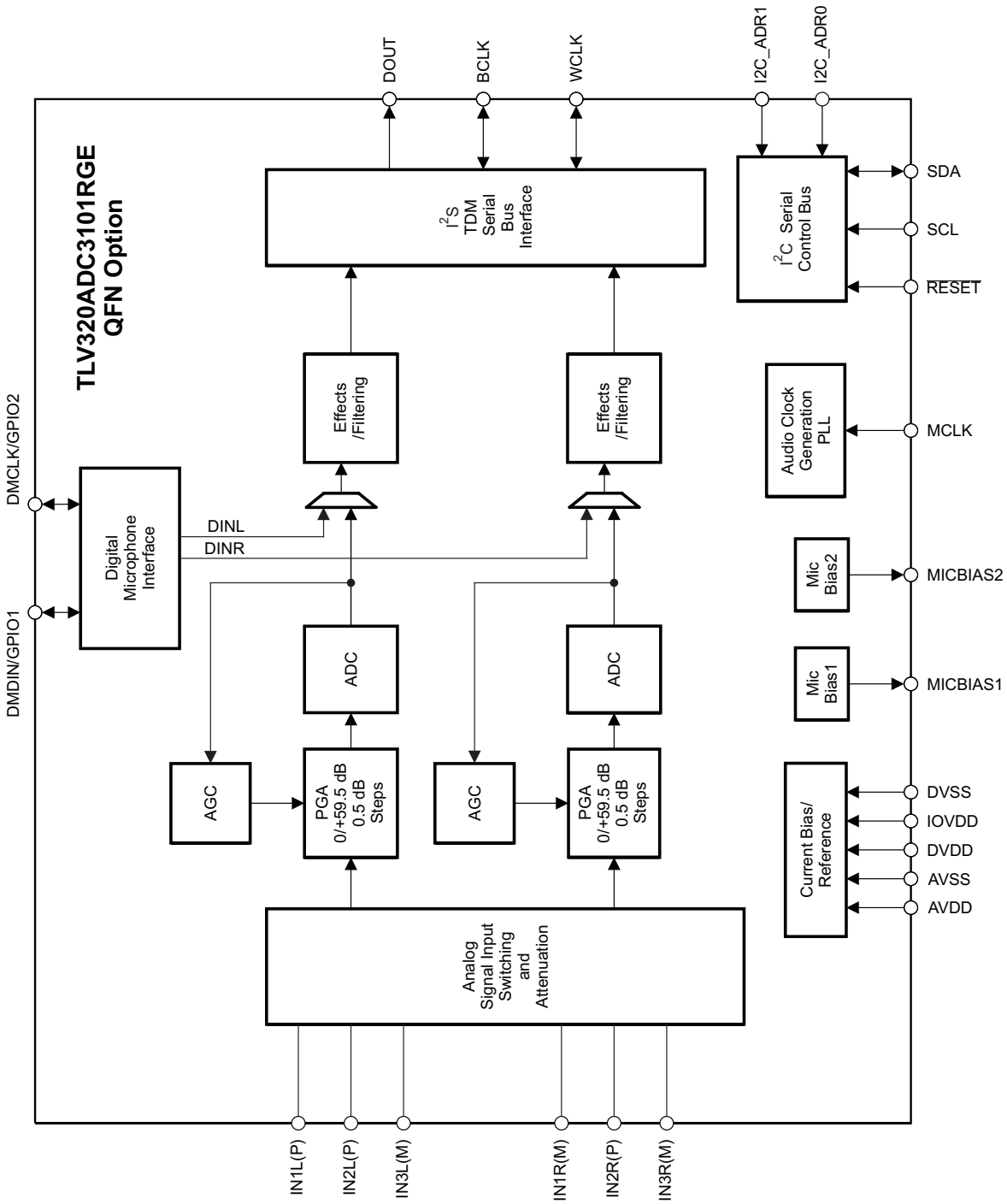


Figure 1. TLV320ADC3101RGE Block Diagram

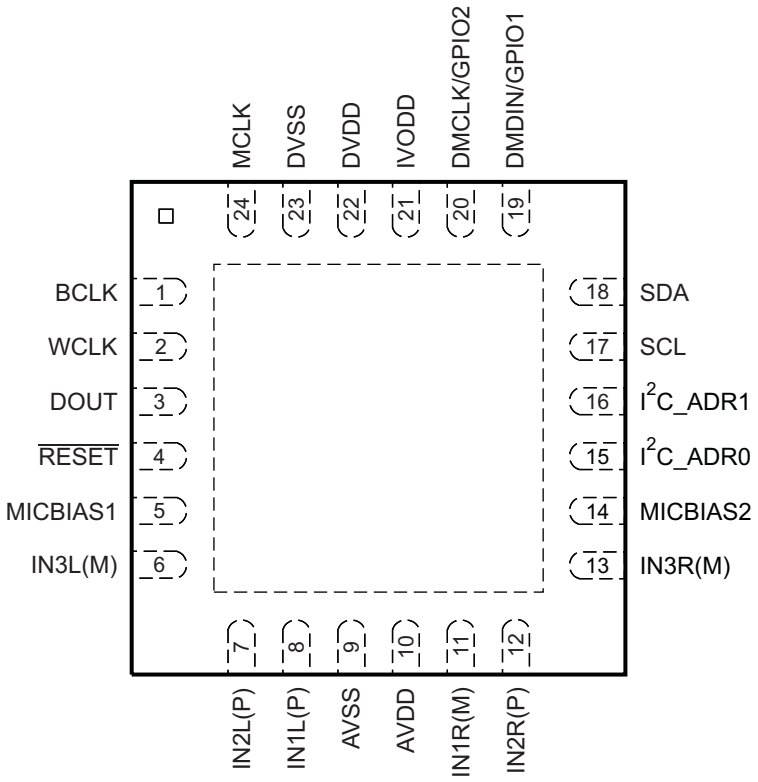
PACKAGING/ORDERING INFORMATION

PRODUCT	PACKAGE(1)	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320ADC3101	QFN-24	RGE	–40°C to 85°C	TLV320ADC3101IRGET	Tape and Reel 250
				TLV320ADC3101IRGER	Tape and Reel 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN ASSIGNMENTS

TLV320ADC3101
RGE PACKAGE
(TOP VIEW)



Connect the QFN thermal pad to AVSS.

PIN FUNCTIONS

TLV320ADC3101RGE QFN	PIN NAME	DESCRIPTION
1	BCLK	Audio Serial Data Bus Bit Clock (Input/Output)
2	WCLK	Audio Serial Data Bus Word Clock (Input/Output)
3	DOUT	Audio Serial Data Bus Data Output (Output)
4	$\overline{\text{RESET}}$	Reset
5	MICBIAS1	Microphone bias voltage output
6	IN3L(M)	Mic or Line Analog Input (Left channel S.E. or D.E Minus)
7	IN2L(P)	Mic or Line Analog Input (Left channel S.E. or D.E Plus)
8	IN1L(P)	Mic or Line Analog Input (Left channel S.E. or D.E Plus, or Right channel)
9	AVSS	Analog Ground Supply, 0 V
10	AVDD	Analog Voltage Supply, 2.6 V - 3.6 V
11	IN1R(M)	Mic or Line Analog Input (Left channel S.E. or D.E Minus, or Left channel)

PIN FUNCTIONS (continued)

TLV320ADC3101RGE QFN	PIN NAME	DESCRIPTION
12	IN2R(P)	Mic or Line Analog Input (Right channel S.E. or D.E Plus)
13	IN3R(M)	Mic or Line Analog Input (Right channel S.E. or D.E Minus)
14	MICBIAS2	Microphone bias voltage output
15	I^2C_ADR0	LSB of I^2C Bus address
16	I^2C_ADR1	LSB+1 of I^2C Bus address
17	SCL	I^2C Serial Clock
18	SDA	I^2C Serial Data Input/Output
19	DMDIN / GPIO1	Digital Microphone Data Input / General-Purpose Input/Output #1 (Input/Output) / PLL Clock Mux Output/ AGC Noise Flag / Multi-function pin based on register programming
20	DMCLK / GPIO2	Digital Microphone Clock / General-Purpose Input/Output #2 (Input/Output) / PLL Clock Input / Audio Serial Data Bus Bit Clock Input/Output / Multi-function pin based on register programming
21	IOVDD	I/O Voltage Supply, 1.1V – 3.6V
22	DVDD	Digital Core Voltage Supply, 1.65 V – 1.95 V
23	DVSS	Digital Ground Supply, 0 V
24	MCLK	Master Clock Input

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
	AVDD to AVSS	–0.3 to 3.9	V
	IOVDD to DVSS	–0.3 to 3.9	V
	DVDD to DVSS	–0.3 to 2.5	V
	Digital input voltage to DVSS	–0.3 V to IOVDD+0.3	V
	Analog input voltage to AVSS	–0.3 V to AVDD+0.3	V
	Operating temperature range	-40 to 85	°C
	Storage temperature range	–65 to 125	°C
T_J Max	Junction temperature	105	°C
	Power dissipation	$(T_J \text{ Max} – T_A) / \theta_{JA}$	
θ_{JA}	Thermal impedance , QFN package	45	°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ESD complacence tested to EIA / JESD22-A114-B and passed.

DISSIPATION RATINGS(1)

PACKAGE TYPE	T_A = 25°C POWER RATING	DERATING FACTOR	T_A = 75°C POWER RATING	T_A = 85°C POWER RATING
QFN	1.7 W	22 mW/°C	665 mW	444 mW

(1) This data was taken using 2 oz. trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in × 3 in PCB.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD(1)	Analog supply voltage	2.6	3.3	3.6	V
DVDD(1)	Digital core supply voltage	1.65	1.8	1.95	V
IOVDD(1)	Digital I/O supply voltage	1.1	1.8	3.6	V
V_I	Analog full-scale 0 dB input voltage (AVDD = 3.3 V)		0.707		Vrms
	Digital output load capacitance		10		pF
T_A	Operating free-air temperature	–40		85	°C

(1) Analog voltage values are with respect to AVSS; digital voltage values are with respect to DVSS.

ELECTRICAL CHARACTERISTICS

At 25°C, AVDD, IOVDD = 1.8 V, DVDD = 1.8 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC						
	Input signal level (0-dB)	Single-ended input		0.707		Vrms
	Signal-to-noise ratio, A-weighted(1) (2)	Fs = 48 kHz, 0 dB PGA gain, IN1 inputs selected and AC-shorted to ground	80	92		dB
	Dynamic range, A-weighted(1) (2)	Fs = 48 kHz, 1-kHz –60 dB full-scale input applied at IN1 inputs, 0-dB PGA gain		92		dB
THD	Total harmonic distortion	Fs = 48 kHz, 1-kHz –2dB full-scale input applied at IN1 inputs, 0-dB PGA gain		–90	–75	dB
				0.003%	0.017%	
	Power supply rejection ratio	234 Hz, 100 mV_{PP} on AVDD, single-ended input		46		dB
		234 Hz, 100 mV_{PP} on AVDD, differential input		68		
	ADC channel separation	1 kHz, –2 dB IN1L to IN1R		–73		dB
	ADC gain error	1 kHz input, 0 dB PGA gain		0.7		dB
	ADC programmable gain amplifier maximum gain	1-kHz input tone, R_{SOURCE} < 50 Ω		40		dB
	ADC programmable gain amplifier step size			0.502		dB
	Input resistance	IN1 inputs, routed to single ADC Input mix attenuation = 0 dB		35		kΩ
		IN2 inputs, input mix attenuation = 0 dB		35		
		IN1 inputs, input mix attenuation = –6 dB		62.5		
		IN2 inputs, input mix attenuation = –6 dB		62.5		
	Input capacitance			10		pF
	Input level control minimum attenuation setting			0		dB
	Input level control maximum attenuation setting			6		dB
	Input level control attenuation step size			6		dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

ELECTRICAL CHARACTERISTICS (continued)

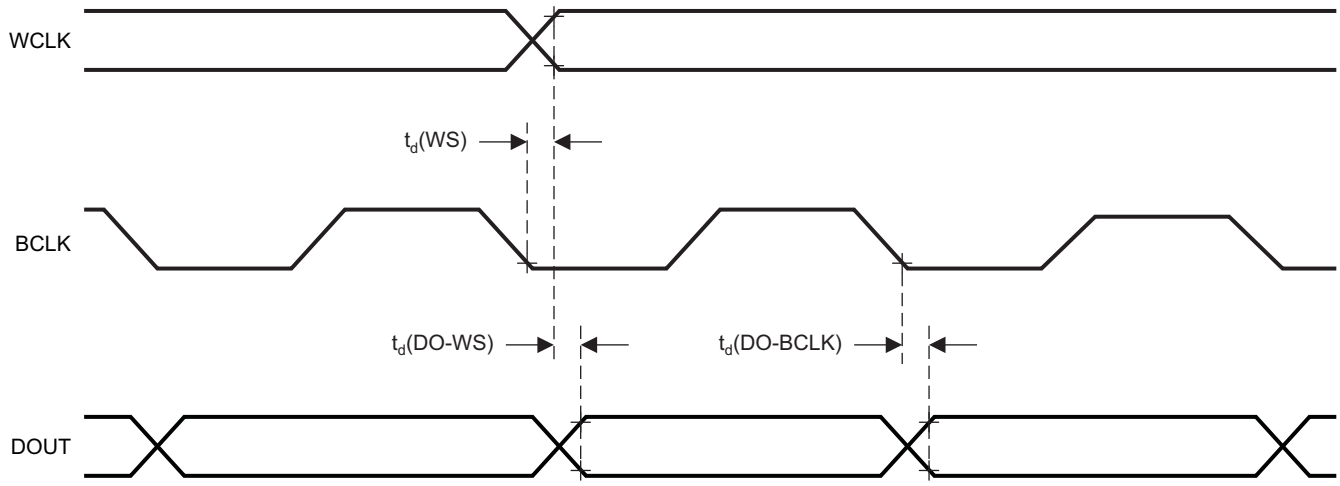
At 25°C, AVDD, IOVDD = 1.8 V, DVDD = 1.8 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC DIGITAL DECIMATION FILTER		**Fs = 48 kHz**					
Filter gain from 0 to 0.39 Fs		Filter A, AOSR = 128 or 64			±0.1		dB
Filter gain from 0.55 Fs to 64 Fs		Filter A, AOSR = 128 or 64			-73		dB
Filter group delay		Filter A, AOSR = 128 or 64			17/Fs		Sec
Filter gain from 0 to 0.39 Fs		Filter B, AOSR = 64			±0.1		dB
Filter gain from 0.60 Fs to 32 Fs		Filter B, AOSR = 64			-46		dB
Filter group delay		Filter B, AOSR = 64			11/fs		Sec
Filter gain from 0 to 0.39 Fs		Filter C, AOSR = 32			±0.033		dB
Filter gain from 0.28 Fs to 16 Fs		Filter C, AOSR = 32			-60		dB
Filter group delay		Filter C, AOSR = 32			11/fs		Sec
MICROPHONE BIAS							
Bias voltage		Programmable settings, load = 750 Ω			2		V
				2.25	2.5	2.75	
					AVDD-0.2		
Current sourcing		2.5 V setting				4	mA
DIGITAL I/O							
V_{IL}	Input low level	I_{IL} = 5µA		–0.3		0.3 × IOVDD	V
V_{IH}	Input high level(3)	I_{IH} = 5µA		0.7 × IOVDD			V
V_{OL}	Output low level	I_{IH} = 2 TTL loads				0.1 × IOVDD	V
V_{OH}	Output high level	I_{OH} = 2 TTL loads		0.8 × IOVDD			V
SUPPLY CURRENT		**Fs = 48-kHz, AVDD=3.3V, DVDD=IOVDD=1.8V**					
Mono record		AVDD	PLL and AGC off		2		mA
		DVDD			1.9		
Stereo record		AVDD	PLL and AGC off		4		mA
		DVDD			2.1		
PLL		AVDD	Additional power consumed when PLL is powered		1.1		mA
		DVDD			0.8		
Power down		AVDD	All supply voltages applied, all blocks programmed in lowest power state		0.04		µA
		DVDD			0.7		

(3) When IOVDD < 1.6V, minimum V_{IH} is 1.1 V.

AUDIO DATA SERIAL INTERFACE TIMING DIAGRAMS

All specifications at 25°C, DVDD = 1.8 V

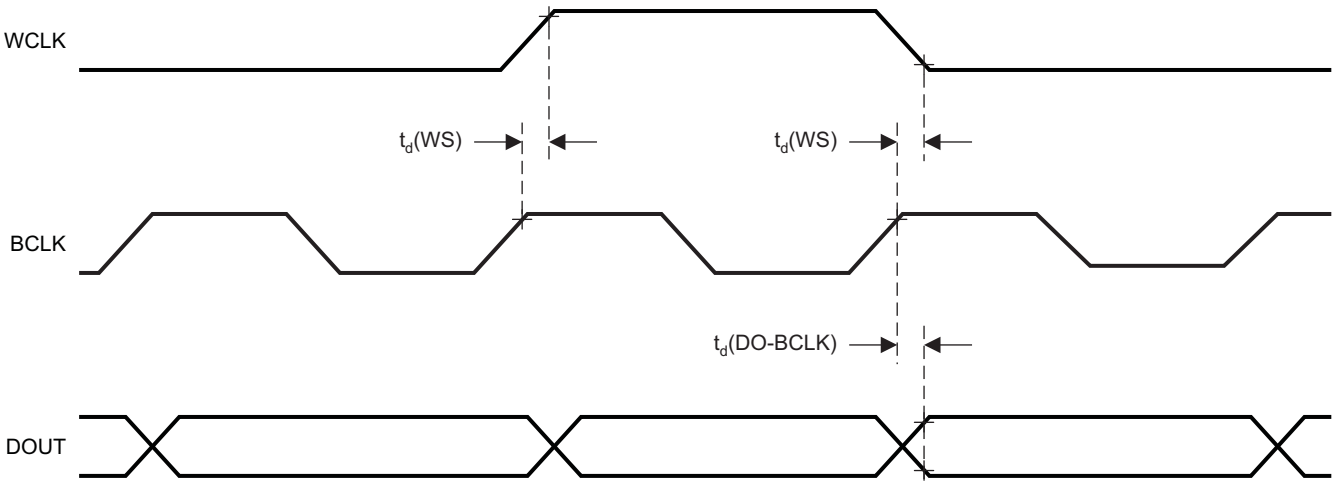


PARAMETER		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	BCLK/WCLK delay time		20		15	ns
t_d(DO-WS)	BCLK/WCLK to DOUT delay time		25		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		20		15	ns
t_r	Rise time		20		15	ns
t_f	Fall time		20		15	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 2. I^2S/LJF/RJF Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V

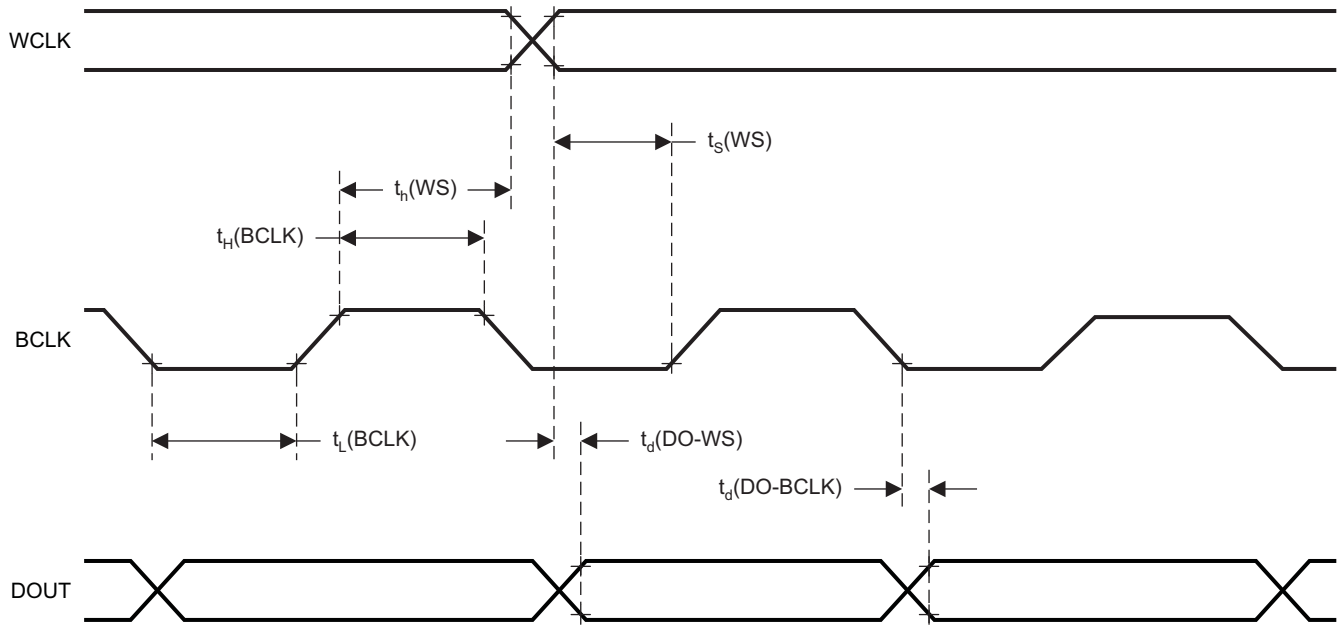


PARAMETER		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	BCLK/WCLK delay time		25		15	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		25		15	ns
t_r	Rise time		20		15	ns
t_f	Fall time		20		15	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 3. DSP Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V

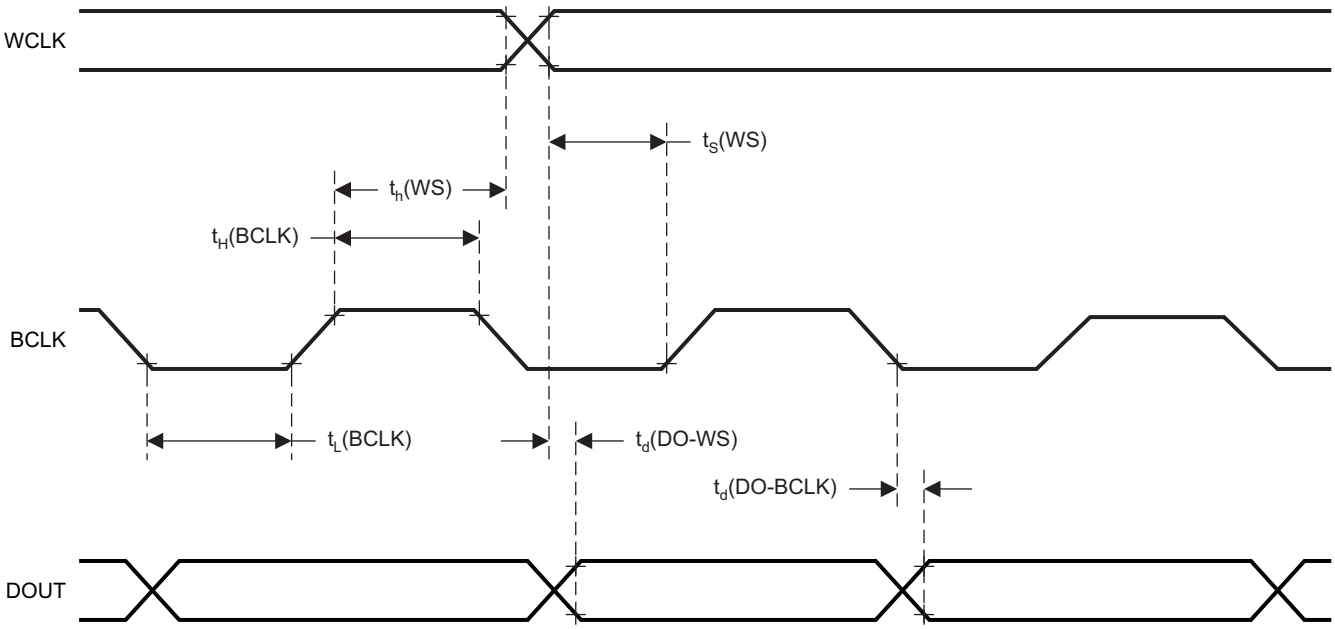


PARAMETER		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	BCLK/WCLK setup time	10		6		ns
t_h(WS)	BCLK/WCLK hold time	10		6		ns
t_d(DO-WS)	BCLK/WCLK to DOUT delay time (for LJF Mode only)		30		30	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		25		20	ns
t_r	Rise time		16		8	ns
t_f	Fall time		16		8	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 4. I²S/LJF/RJF Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V



PARAMETER		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	BCLK/WCLK setup time	10		8		ns
t_h(WS)	BCLK/WCLK hold time	10		8		ns
t_d(DO-BCLK)	BCLK to DOUT delay time		25		20	ns
t_r	Rise time		15		8	ns
t_f	Fall time		15		8	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 5. DSP Timing in Slave Mode

TYPICAL CHARACTERISTICS

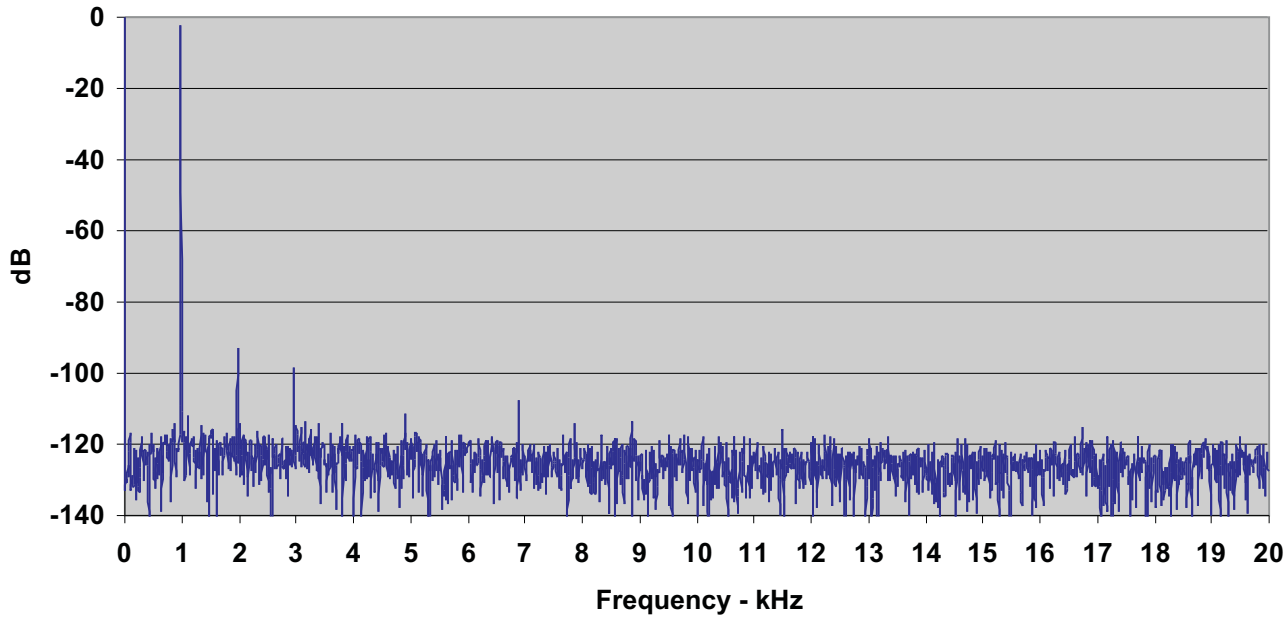


Figure 6. Line Input to ADC FFT Plot

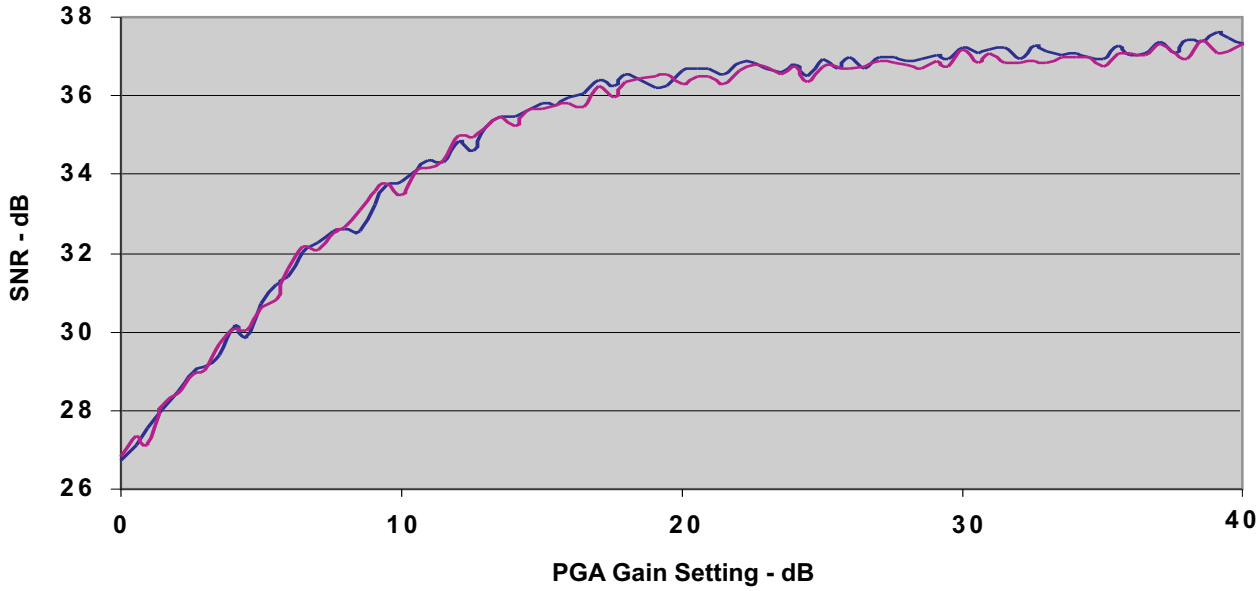


Figure 7. Single-Ended Dynamic Range

TYPICAL CHARACTERISTICS (continued)

Figure 8. Single-Ended Gain Error

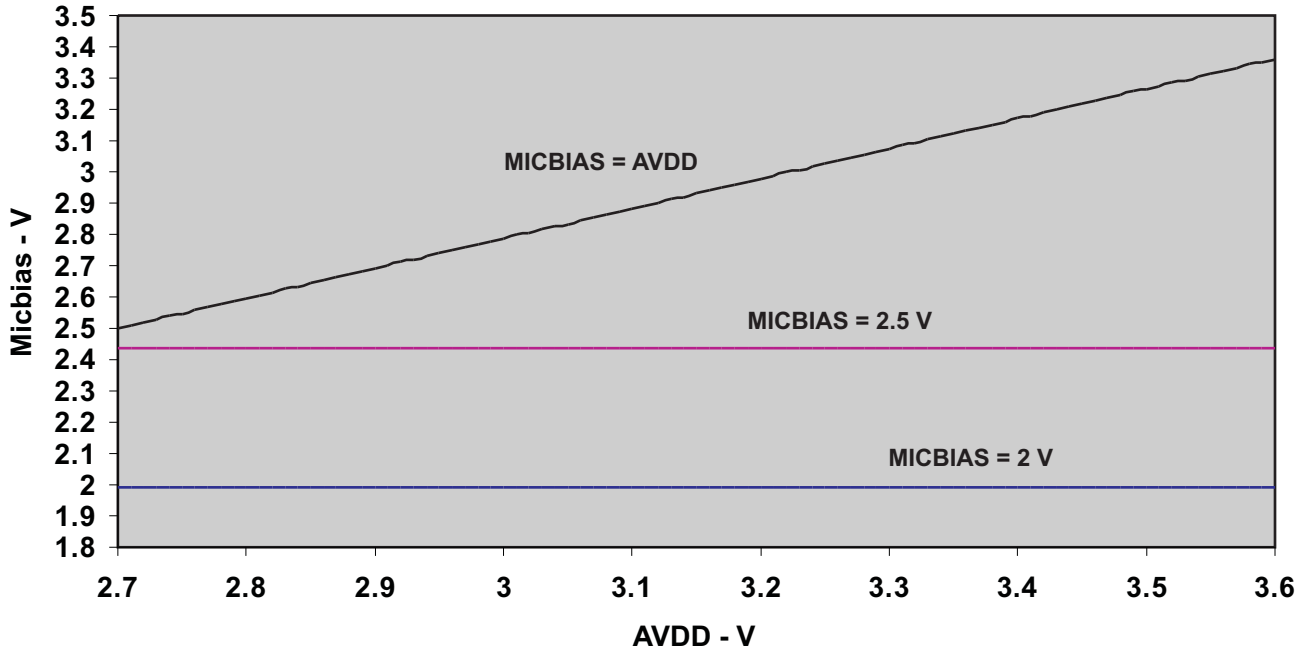


Figure 9. MICBIAS Output Voltage vs AVDD

TYPICAL CHARACTERISTICS (continued)

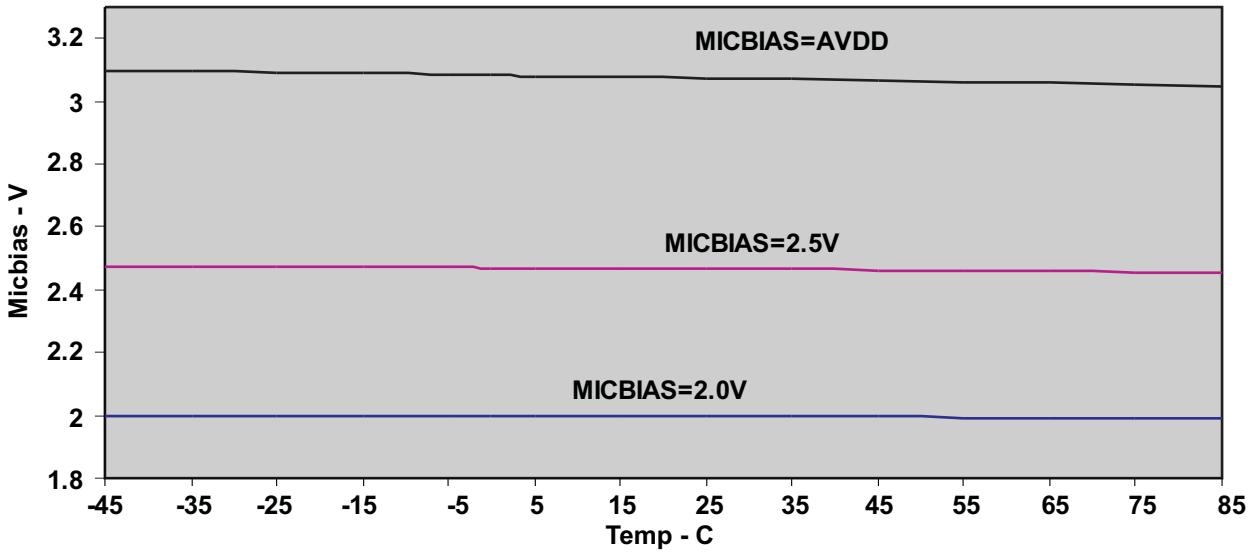


Figure 10. MICBIAS Output Voltage vs Ambient Temperature

TYPICAL CIRCUIT CONFIGURATION

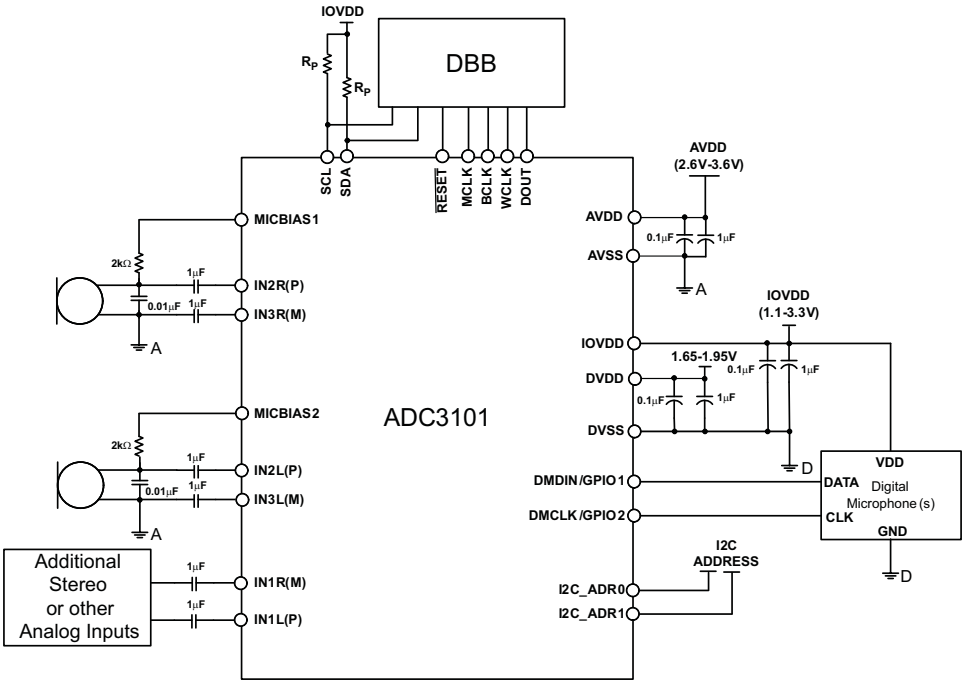


Figure 11. Typical Connections

OVERVIEW

The TLV320ADC3101 is a flexible, low power, stereo audio ADC product with extensive feature integration, intended for applications in smartphones, PDAs, and portable computing, communication, and entertainment applications. The product integrates a host of features to reduce cost, board space, and power consumption in space-constrained, battery-powered, portable applications.

The TLV320ADC310RGE consists of the following blocks:

- Stereo audio multi-bit delta-sigma ADC (8 kHz–96 kHz)
- Programmable digital audio effects processing (3-D, bass, treble, mid-range, EQ, de-emphasis)
- Register configurable combinations of up to six single-ended or three differential audio inputs
- Fully programmable PLL with extensive ADC clock source and divider options for maximum end-system design flexibility

Communication to the TLV320ADC3101 for control is via a two-wire I^2C interface. The I^2C interface supports both standard and fast communication modes.

HARDWARE RESET

The TLV320ADC3101 requires a hardware reset after power-up for proper operation. After all power supplies are at their specified values, the $\overline{\text{RESET}}$ pin must be driven low for at least 10 ns. If this reset sequence is not performed, the 'ADC3101 may not respond properly to register reads/writes.

DIGITAL CONTROL SERIAL INTERFACE

I^2C CONTROL MODE

The TLV320ADC3101 supports the I^2C control protocol and is capable of both standard and fast modes. When in I^2C control mode, the TLV320ADC3101RGE can be configured for one of four different addresses, using the pins I2C_ADR1 and I2C_ADR0, which control the two LSBs of the device address. The 5 MSBs of the device address are fixed as 00110 and cannot be changed, while the two LSBs are given by I2C_ADR1:I2C_ADR0. This results in four possible device addresses:

I^2C slave device addresses for I2C_ADR1, I2C_ADR0 settings.

I2C_ADR1	I2C_ADR0	Device Address
0	0	0011000
0	1	0011001
1	0	0011010
1	1	0011011

I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the TLV320ADC3101 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero; a HIGH indicates the bit is one). Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receivers shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. Under normal circumstances the master drives the clock line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication. They do this by causing a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit.

A not-acknowledge is performed by leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320ADC3101 also responds to and acknowledges a General Call, which consists of the master issuing a command with a slave address byte of 00H.

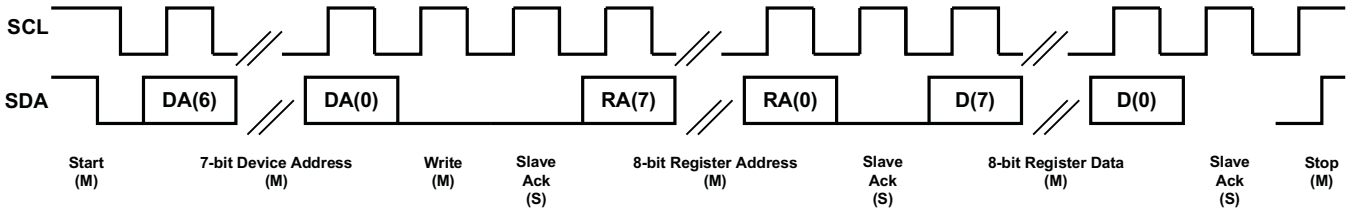


Figure 12. I^2C Write

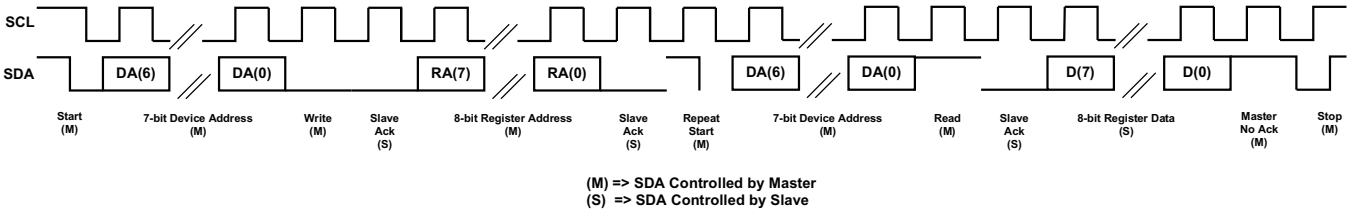


Figure 13. I^2C Read

In the case of an I^2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I^2C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues an ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next 8 clocks the data of the next incremental register.

DIGITAL AUDIO DATA SERIAL INTERFACE

Audio data is transferred between the host processor and the TLV320ADC3101 via the digital audio data serial interface, or audio bus. The audio bus on this device is flexible, including left or right justified data options, support for I2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio serial interface on the TLV320ADC3101 has an extensive IO control to allow for communicating with two independent processors for audio data. Each processor can communicate with the device one at a time. This feature is enabled by register programming of the various pin selections.

The audio bus of the TLV320ADC3101 can be configured for left or right justified, I2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page-0/Register-27/D (5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC sampling frequencies.

The bit clock is used to clock in and out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page-0/Register-30 (see the system clock network figure). The number of bit-clock pulses in a frame may need to be adjusted to accommodate various word-lengths as well as to support the case when multiple TLV320ADC3101's may share the same audio bus.

The TLV320ADC3101 also includes a feature to offset the position of start of data transfer with respect to word-clock. There are two configurations that afford the user to use either a single offset for both channels or to use separate offsets. When Page-0, Register-38, D0 is set to zero, both channel's offset is controlled, in terms of no. of bit-clocks, by the programming in Page-0, Register-28. When Page-0, Register-38, D0 (time-slot-based channel assignment) is set to one, the first channel is controlled, in terms of no. of bit-clocks, by the programming in Page-0, Register-28 and the second channel is controlled, in terms of no. of bit-clocks, by the programming in Page-0, Register-37. Register 37 programs the delay between the 1st word and the 2nd word. The relative order of the two channels can be swapped depending on the programmable register bit (Page-0, Register-38, D4) that enables swapping of the channels.

The TLV320ADC3101 also supports a feature of inverting the polarity of bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of mode of audio interface chosen. This can be configured by writing to Page-0, Register-29, D3.

The TLV320ADC3101 further includes programmability (Page-0/Register-27/D0) to 3-state the DOUT at the end of data transfer (i.e., at the end of the bit-cycle corresponding to the LSB of a channel). By combining this capability with the ability to program at what bit clock in a frame the audio data will begin, time-division multiplexing (TDM) can be accomplished, resulting in multiple ADCs able to use a single audio serial data bus. To further enhance the 3-state capability, the TLV320ADC3101 can be put in high-impedance by a half bit-cycle earlier by setting Page-0, Register-38, D1 to one. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface will be put into a 3-state output condition.

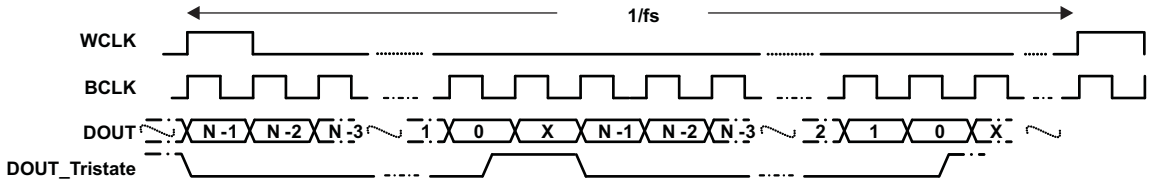


Figure 14. Both Channels Enabled, Early 3-Stating Enabled

Either or both of the two channels can be disabled in LJF, I2S, and DSP modes by using Page-0, Register-38, D3-D2. Figure 33 shows the effect of setting Page-0, Register-38, D2, first channel disabled, and setting Page-0, Register-27, D0 to 1 which enables 3-stating DOUT. If 3-stating was disabled, then the DOUT signal is driven to logic level zero.

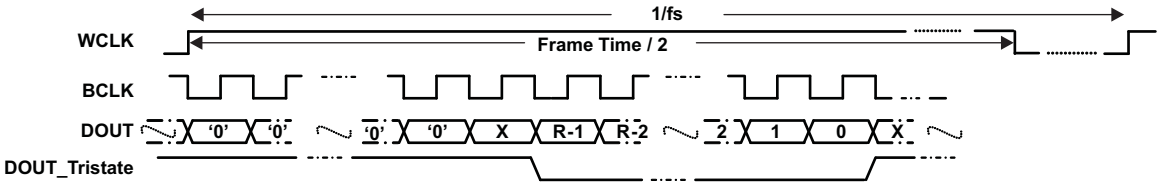


Figure 15. First Channel Disabled, Second Channel Enabled, 3-State Enabled

The sync signal for the ADC filter is not generated based on the disabled channel. The sync signal for the filter corresponds to the beginning of the earlier of the two channels. If the first channel is disabled, the filter sync is generated at the beginning of the second channel, if it is enabled. If both the channels are disabled, there is no output to the serial bus, and the filter sync corresponds to the beginning of the frame.

By default when the word-clocks and bit-clocks are generated by the TLV320ADC3101, these clocks are active only when the ADC is powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This is useful when using the TDM mode with multiple CODECs on the same bus or when word-clock or bit-clocks are used in the system as general purpose clocks.

Right Justified Mode

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

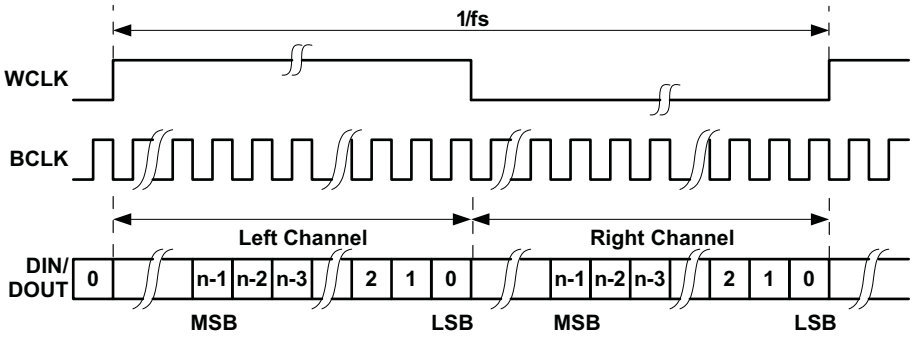


Figure 16. Timing Diagram for Right-Justified Mode

For Right-Justified mode, the number of bit-clock's per frame should be greater than twice the programmed word-length of the data. The time-slot-based mode is not available in the Right-Justified Mode.

Left Justified Mode

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

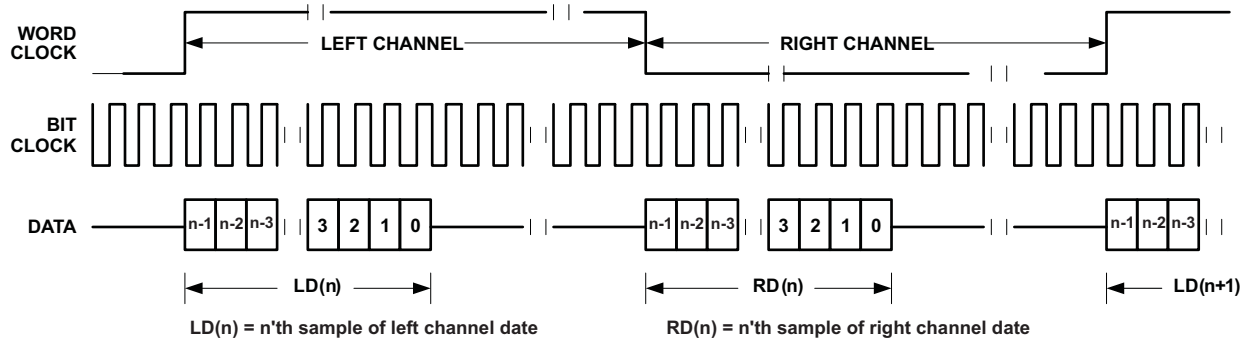


Figure 17. Left-Justified Mode

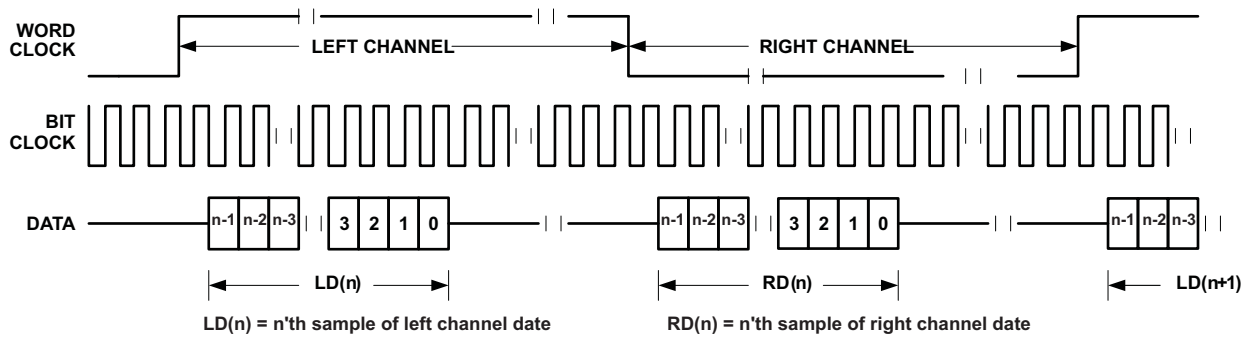


Figure 18. Left-Justified Mode with Offset1=1

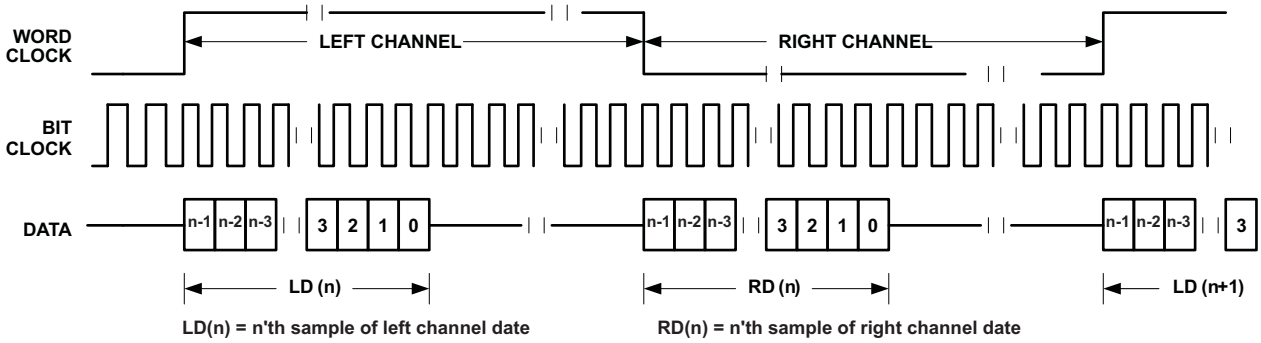


Figure 19. Left-Justified Mode with Offset1=0, Bit Clock Inverted

For Left-Justified mode, the number of bit-clock's per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

When the time-slot-based channel assignment is disabled, the left and right channels have the same offset(Page-0, Register-28), and each edge of the word-clock starts data transfer for one of the two channels, depending on whether or not channel swapping is enabled. Data bits are valid on the rising-edges of bit-clock. With the time-slot-based channel assignment enabled (Page-0, Register-38, D0), the left and right channels have independent offsets, and rising-edge of the word-clock starts data transfer for the first channel after a delay of programmed offset for this channel. Data transfer for the second channel starts after a delay of its programmed offset from the LSB of the first channel's data. The falling-edge of word-clock is not used.

For the purposes of this section Offset1 reference represents the value in Page-0, Register-28 and Offset2 represents the value in Page-0, Register-37.

With no channel swapping, MSB of the left channel is valid on (Offset1+1)th rising-edge of bit-clock following the rising-edge of the word-clock. And, MSB of the right channel is valid on (Offset2+1)th rising-edge of bit-clock following the LSB of the left channel. The operation in this case, with offset of 1, is shown in the timing-diagram of Figure 36. Since, channel swapping is not enabled, left channel data is before the right channel data. With channel swapping enabled, the MSB of the right channel is valid on (Offset1+1)th rising-edge of bit-clock following the rising-edge of the word-clock. And, the MSB of the left channel is valid on (Offset1+1)th rising-edge of bit-clock following the falling-edge of the word-clock. The operation in this case, with offset of 1, is shown in the timing-diagram of Figure 38. As shown in the diagram, right channel data of a frame is before that frame's left channel data, due to channel swapping. Otherwise, the behavior is similar to the case where channel swapping is disabled. The MSB of right channel data is valid on the second rising-edge of bit-clock after the rising-edge of word-clock, due to an offset of 1. Similarly, the MSB of left channel data is valid on the second rising-edge of bit-clock after the falling-edge of word-clock.

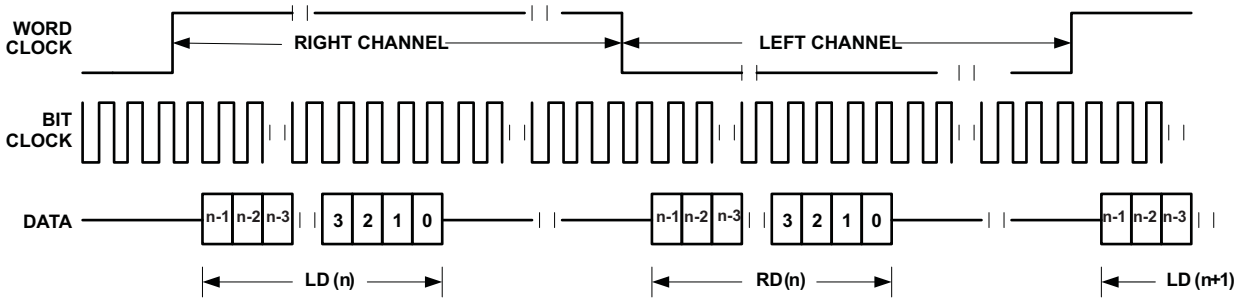


Figure 20. Left-Justified Mode with Offset1=1, Channel Swapping Enabled

When time-based-slot mode is enabled with no channel swapping, MSB of the left channel is valid on (offset1+1)th rising-edge of bit-clock following the rising-edge of the word-clock. And, MSB of the right channel is valid on (offset2+1)th rising-edge of bit-clock following the LSB of the left channel.

Figure 19 shows the operation in this mode. MSB of the left channel is valid on the first rising-edge of bit-clock after the rising-edge of word-clock. Data transfer for the right channel does not wait for the falling-edge of word-clock and the MSB of right channel is valid on the second rising-edge of bit-clock after LSB of the left channel.

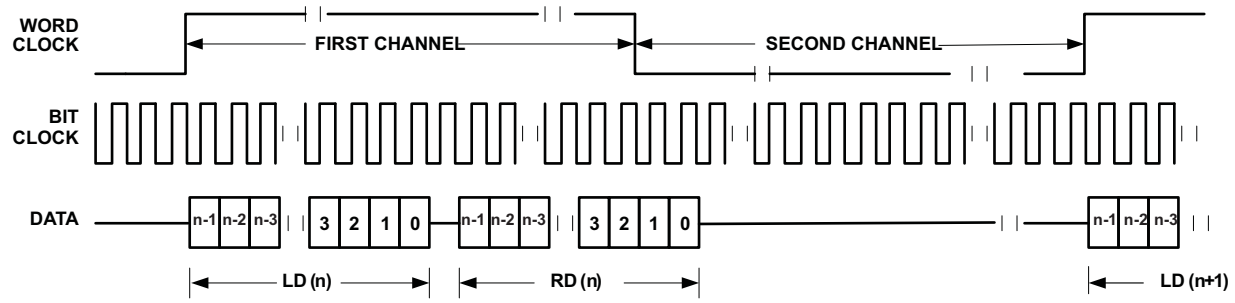


Figure 21. Left-Justified Mode, Time-Based-Slot Mode Enabled, Offset1=0, Offset2=1

For the time-based-slot mode and channel swapping enabled, the MSB of the right channel is valid on (offset1+1)th rising-edge of bit-clock following the rising-edge of the word-clock. And, MSB of the left channel is valid on (offset2+1)th rising-edge of bit-clock following the LSB of the right channel. Figure 40 shows the operation in this mode. MSB of the right channel is valid on the first rising-edge of bit-clock after the rising-edge of word-clock. Data transfer for the left channel starts following the completion of data transfer for the right channel without waiting for the falling-edge of word-clock. MSB of the left channel is valid on the second rising-edge of bit-clock after LSB of the right channel.

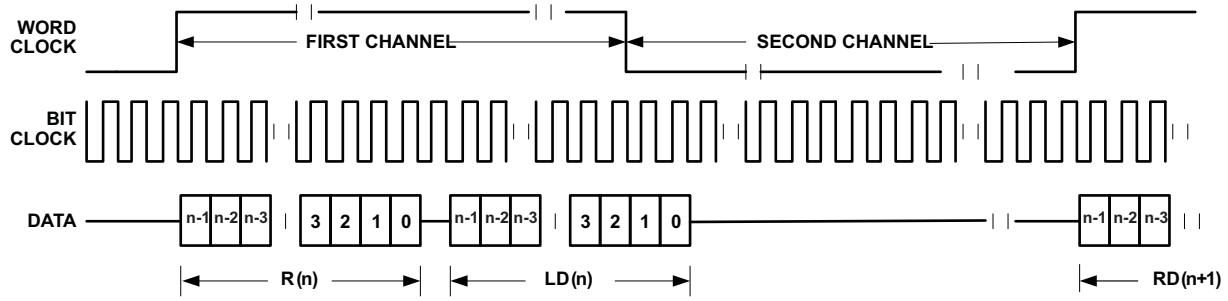


Figure 22. Left-Justified Mode, Time-Based-Slot Mode Enabled, Offset1=0, Offset2=1, Channel Swap Enabled

I2S Mode

In I2S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

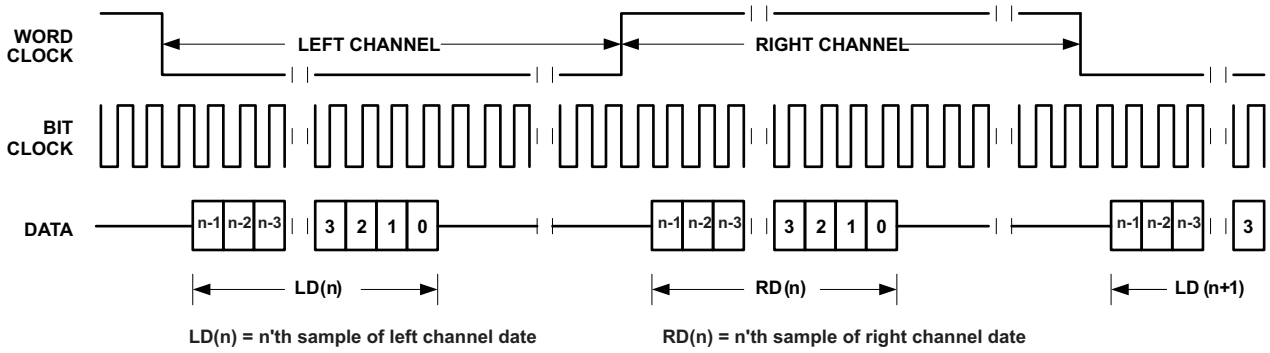


Figure 23. I2S Mode

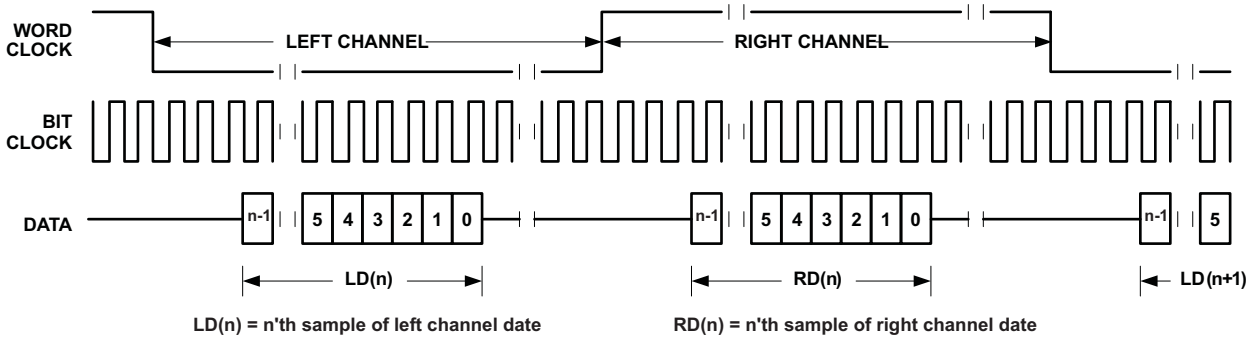


Figure 24. I2S Mode with Offset1=2

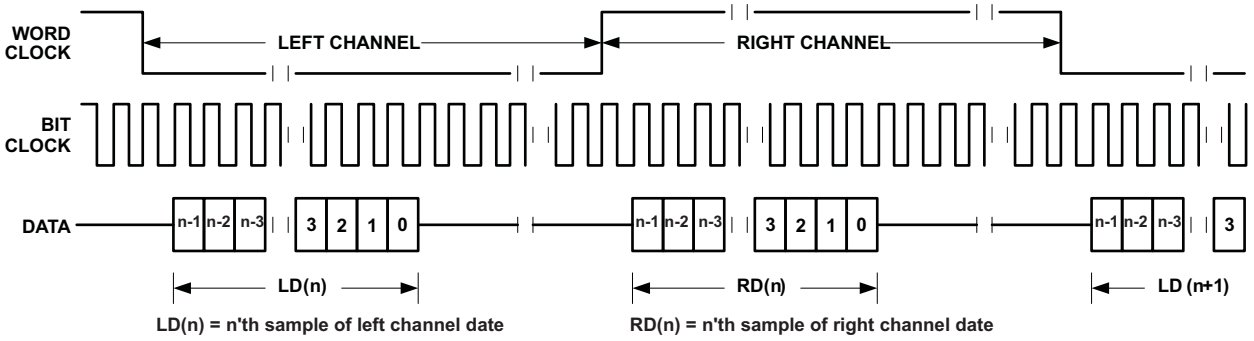


Figure 25. I2S Mode with Offset1=0, Bit Clock Invert

For I2S mode, the number of bit-clock's per channel should be greater than or equal to the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

DSP Mode

In DSP mode, the falling edge of the word clock starts the data transfer with the left channel data first and is immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

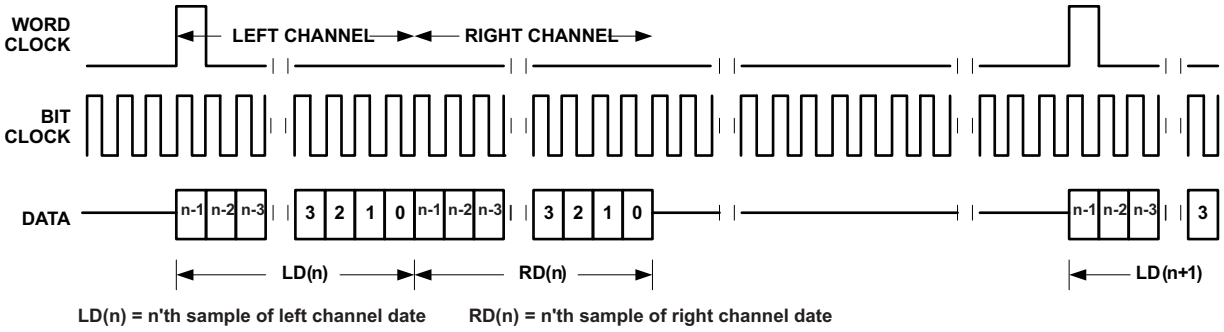


Figure 26. DSP Mode

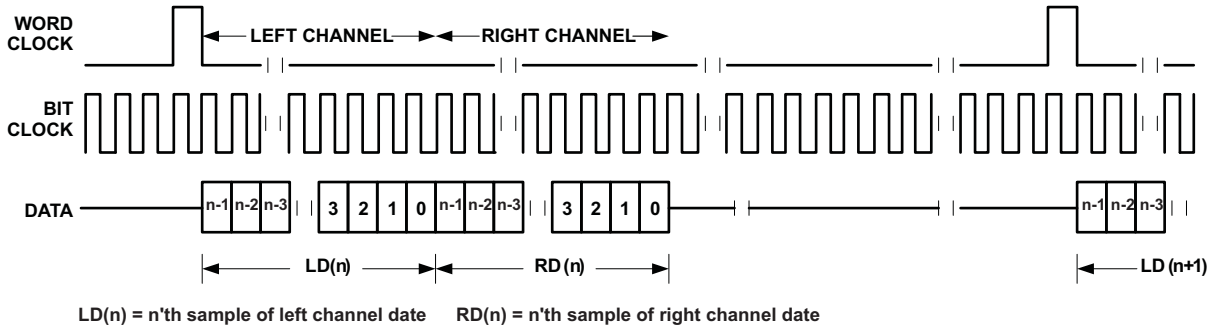


Figure 27. DSP Mode with Offset1=1

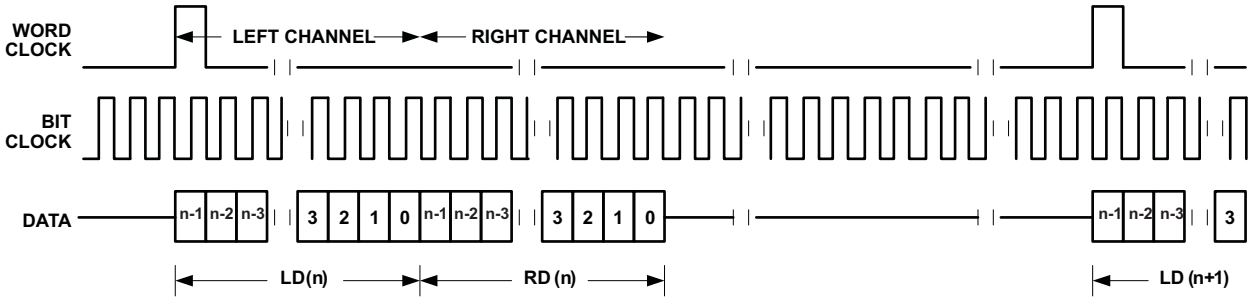


Figure 28. DSP Mode with Offset1=1, Bit Clock Inverted

For DSP mode, the number of bit-clock's per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

Figure 29 shows the time-slot-based mode without channel swapping, and with first channel offset of 0 and second channel offset of 3. The MSB of left channel data is valid on the first falling-edge of bit-clock after rising-edge of word-clock. Since the right channel has an offset of 3 the MSB of its data is valid on the third falling-edge of bit-clock after the LSB of left channel data. As in the case of other modes, serial output bus is put in high-impedance, if tri-stating of output is enabled, during all the extra bit-clock cycles in the frame.

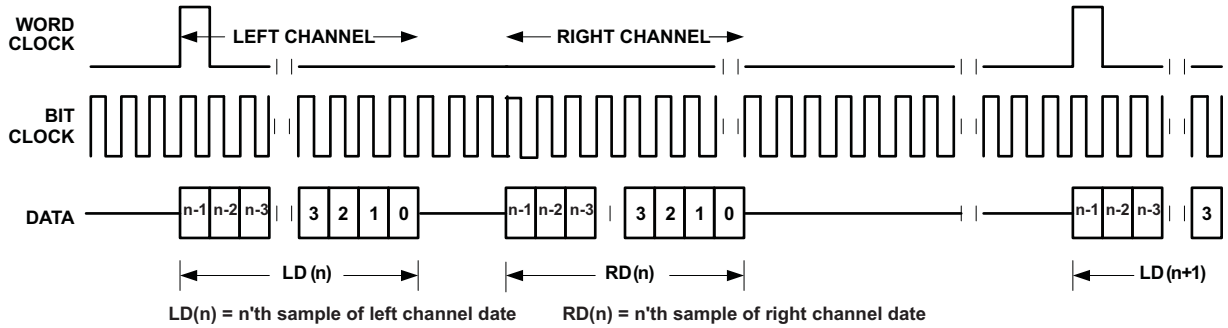


Figure 29. DSP Mode, Time-Slot-Based Mode Enabled, Offset1=0, Offset2=3

Figure 30 shows the timing-diagram for the DSP-mode with left and right channels swapped, first channel offset of 0 and second channel offset of 3. MSB of the right channel is valid on the first falling-edge of bit-clock after the rising-edge of word-clock. And, MSB of the left channel is valid three bit-clock cycles after the LSB of right channel, since the offset for the left channel is 3.

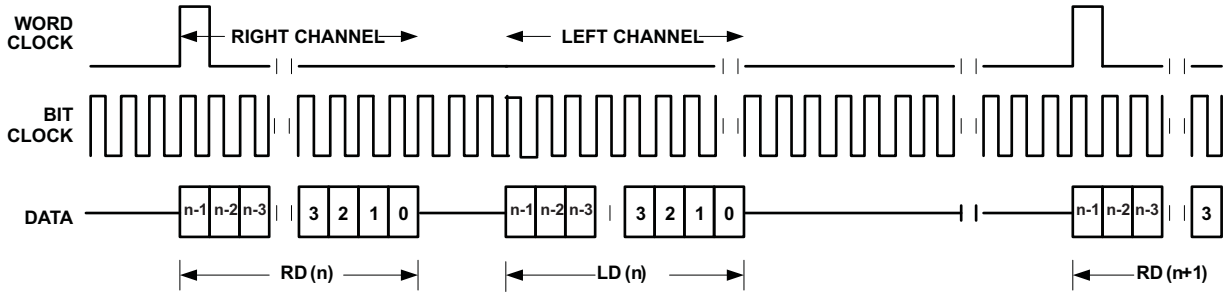


Figure 30. DSP Mode, Time-Slot-Based Mode Enabled, Offset1=0, Offset2=3, Channel Swap Enabled

AUDIO DATA CONVERTERS

The TLV320ADC3101 supports the following standard audio sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz. The converters can also operate at different sampling rates in various combinations, which are described further below.

The TLV320ADC3101 supports a wide range of options for generating clocks for the ADC section as well as the digital interface section and the other control blocks as shown in Figure 31. The clocks for the ADC require a source reference clock. The clock can be provided on device pins MCLK and BCLK. The source reference clock for the ADC section can be chosen by programming ADC_CLKIN value on Page-0, Register-4, D(1:0). The ADC_CLKIN can then be routed through highly flexible clock dividers shown in Figure 31 to generate various clocks required for the ADC and programmable digital filter sections. In the event that the desired audio or programmable digital filter clocks cannot be generated from the external reference clocks on MCLK and BCLK, the TLV320ADC3101 also provides the option of using an on-chip PLL which supports a wide range of fractional multiplication values to generate the required system clocks. Starting from ADC_CLKIN the TLV320ADC3101 provides for several programmable clock dividers to help achieve a variety of sampling rates for the ADC and the clocks for the programmable digital filter section.

AUDIO CLOCK GENERATION

The audio converters in fully programmable filter mode in the TLV320ADC3101 need an internal audio master clock at a frequency of ≥ N×Fs where N = IADC (page 0, register 21) when filter mode (page 0, register 61) equals zero, otherwise N equals the instruction count from Table 5 ADC Processing Blocks. The master clock is obtained from an external clock signal applied to the device.

The part can accept an MCLK input from 512 kHz to 50 MHz, which can then be passed through either a programmable divider or a PLL, to get the proper internal audio master clock needed by the part. The BCLK input can also be used to generate the internal audio master clock.

A primary concern is proper operation of the codec at various sample rates with the limited MCLK frequencies available in the system. This device includes a programmable PLL to accommodate such situations. The integrated PLL can generate audio clocks from a wide variety of possible MCLK inputs, with particular focus paid to the standard MCLK rates already widely used.

When the PLL is enabled,

Fs = (PLLCLK_IN × K × R) / (NADC×MADC×AOSR × P), where

P = 1, 2, 3,…, 8
R = 1, 2, …, 16
K = J.D
J = 1, 2, 3, …, 63
D = 0000, 0001, 0002, 0003, …, 9998, 9999
PLLCLK_IN can be MCLK or BCLK, selected by Page 0, register 4, bits D3-D2

P, R, J, and D are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

Examples:

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied to meet specified performance:

512 kHz ≤ (PLLCLK_IN / P) ≤ 20 MHz
80 MHz ≤ (PLLCLK _IN × K × R / P) ≤ 110 MHz
4 ≤ J ≤ 55

When the PLL is enabled and D≠0000, the following conditions must be satisfied to meet specified performance:

10 MHz ≤ PLLCLK _IN / P ≤ 20 MHz

80 MHz ≤ PLLCLK _IN × K × R / P ≤ 110 MHz
4 ≤ J ≤ 11
R = 1

Example:

For MCLK = 12 MHz, Fs = 44.1 kHz, NADC=8, MADC=2, and AOSR=128:
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example:

For MCLK = 12 MHz, Fs = 48.0 kHz , NADC=8, MADC=2, and AOSR=128:
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

The table below lists several example cases of typical MCLK rates and how to program the PLL to achieve an of Fs = 44.1 kHz or 48 kHz with NADC=8, MADC=2, and AOSR=128.

Fs = 44.1 kHz						
MCLK (MHz)	**P**	**R**	**J**	**D**	**ACHIEVED FS**	**% ERROR**
2.8224	1	1	32	0	44100.00	0.0000
5.6448	1	1	16	0	44100.00	0.0000
12.0	1	1	7	5264	44100.00	0.0000
13.0	1	1	6	9474	44099.71	0.0007
16.0	1	1	5	6448	44100.00	0.0000
19.2	1	1	4	7040	44100.00	0.0000
19.68	1	1	4	5893	44100.30	–0.0007
48.0	4	1	7	5264	44100.00	0.0000
Fs = 48 kHz						
MCLK (MHz)	**P**	**R**	**J**	**D**	**ACHIEVED FS**	**% ERROR**
2.048	1	1	48	0	48000.00	0.0000
3.072	1	1	32	0	48000.00	0.0000
4.096	1	1	24	0	48000.00	0.0000
6.144	1	1	16	0	48000.00	0.0000
8.192	1	1	12	0	48000.00	0.0000
12.0	1	1	8	1920	48000.00	0.0000
13.0	1	1	7	5618	47999.71	0.0006
16.0	1	1	6	1440	48000.00	0.0000
19.2	1	1	5	1200	48000.00	0.0000
19.68	1	1	4	9951	47999.79	0.0004
48.0	4	1	8	1920	48000.00	0.0000

A detailed diagram of the audio clock section of the TLV320ADC3101 is shown in Figure 31.

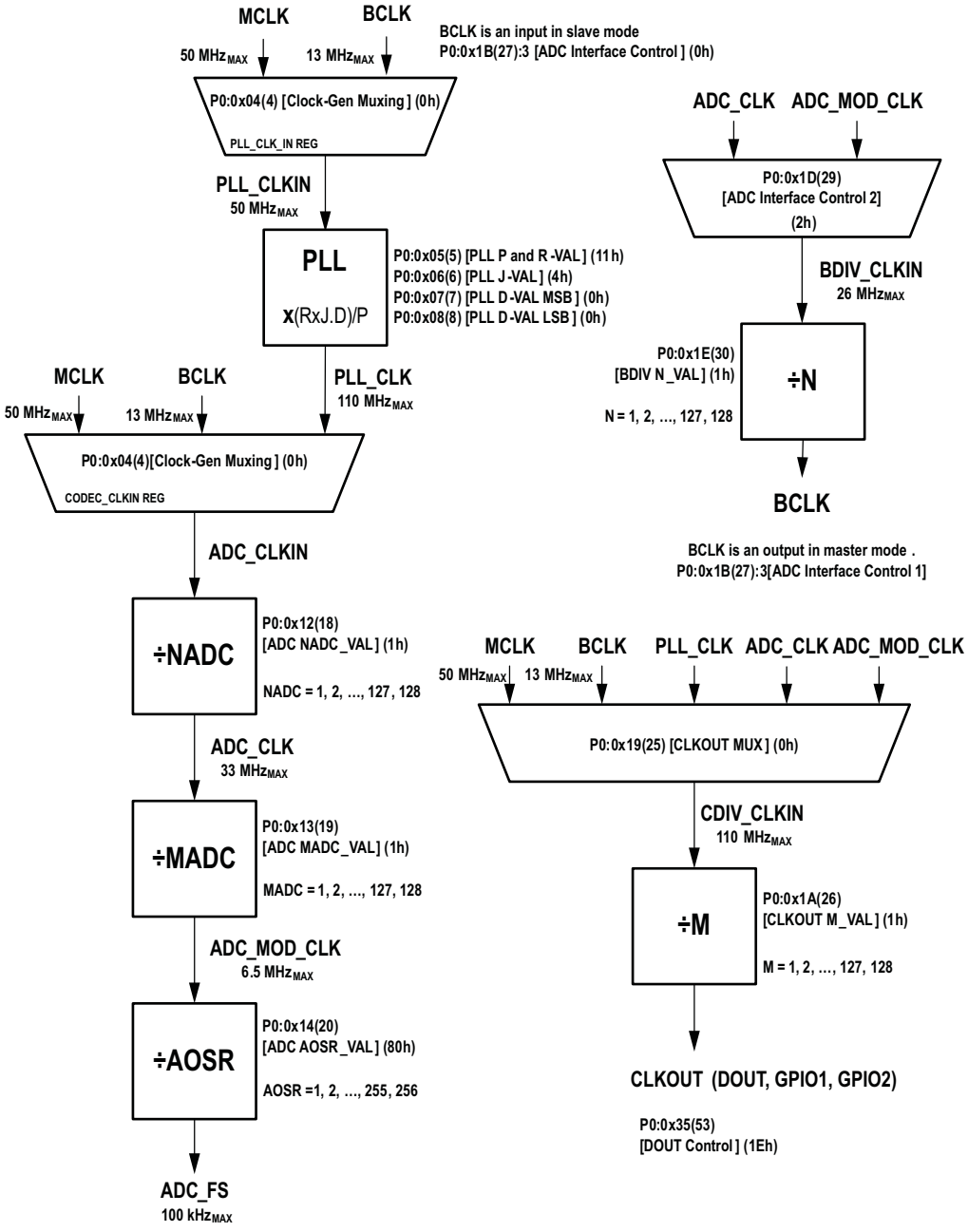


Figure 31. Audio Clock Generation Processing

STEREO AUDIO ADC

The TLV320ADC3101 includes a stereo audio ADC, which uses a delta-sigma modulator with 128-times oversampling in single-rate mode, followed by a digital decimation filter. The ADC supports sampling rates from 8 kHz to 48 kHz in single-rate mode, and up to 96 kHz in dual-rate mode. Whenever the ADC is in operation, the device requires an audio master clock be provided and appropriate audio clock generation be setup within the part.

In order to provide optimal system power dissipation, the stereo ADC can be powered one channel at a time, to support the case where only mono record capability is required. In addition, both channels can be fully or partially powered down.

The integrated digital decimation filter removes high-frequency content and downsamples the audio data from an initial sampling rate of 128 Fs to the final output sampling rate of Fs. The decimation filter provides a linear phase output response with a group delay of 17/Fs. The –3 dB bandwidth of the decimation filter extends to 0.45 Fs and scales with the sample rate (Fs). The filter has minimum 73dB attenuation over the stopband from 0.55 Fs to 64 Fs. Independent digital highpass filters are also included with each ADC channel, with a corner frequency that can be set independently by programmable coefficients or can be disabled entirely.

Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog anti-aliasing filtering are relaxed. The TLV320ADC3101 integrates a second order analog anti-aliasing filter with 20-dB attenuation at 1 MHz. This filter, combined with the digital decimation filter, provides sufficient anti-aliasing filtering without requiring additional external components.

The ADC is preceded by a programmable gain amplifier (PGA), which allows analog gain control from 0 dB to 40 dB in steps of 0.5 dB. The PGA gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register programming (see register page 0 register 81). This soft-stepping specifies that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and upon power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag is set whenever the gain applied by PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming a register bit. When soft stepping is enabled, the audio master clock must be applied to the part after the ADC power down register is written to achieve the soft-stepping to mute has completed. When the ADC powerdown flag is no longer set, the audio master clock can be shut down.

AUDIO ANALOG INPUTS

Digital Volume Control

The TLV320ADC3101 also has a digital volume-control block with a range from -12dB to +20dB in steps of 0.5dB. It is set by programming Page 0, Register 83 and 84 respectively for left and right channels.

Table 1. Digital Volume Control for ADC

Desired Gain dB	Left / Right Channel Page 0, Register 83/84, D(6:0)
–12.0	110 1000
–11.5	110 1001
–11.0	110 1010
..	
–0.5	111 1111
0.0	000 0000 (Default)
+0.5	000 0001
..	
+19.5	010 0111
+20.0	010 1000

During volume control changes, the soft-stepping feature is used to avoid audible artifacts. The soft-stepping rate can be set to either 1 or 2 gain steps per sample. Soft-stepping can also be entirely disabled. This soft-stepping is configured via Page 0, Register 81, D(1:0), and is common to soft-stepping control for the analog PGA. During power-down of an ADC channel, this volume control soft-steps down to -12.0dB before powering down. Due to the soft-stepping control, soon after changing the volume control setting or powering down the ADC channel, the actual applied gain may be different from the one programmed through the control register. The TLV320ADC3101 gives feedback to the user, through read-only flags Page 0, Reg 36, D(7) for Left Channel and Page 0, Reg 36, D(3) for the right channel.

Fine Digital Gain Adjustment

Additionally, the gains in each of the channels is finely adjustable in steps of 0.1dB. This is useful when trying to match the gain between channels. By programming Page 0, Register 82 the gain can be adjusted from 0dB to -0.4dB in steps of 0.1dB. This feature, in combination with the regular digital volume control allows the gains through the left and right channels be matched in the range of -0.5dB to +0.5dB with a resolution of 0.1dB.

AGC

The TLV320ADC3101 includes Automatic Gain Control (AGC) for ADC recording. AGC can be used to maintain a nominally-constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable parameters, including target gain, attack and decay time constants, noise threshold, and max PGA applicable, that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Since the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate.

- **Target Level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320ADC3101 allows programming of eight different target levels, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Since the TLV320ADC3101 reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.
- **Attack Time** determines how quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level due to increase in input signal level. Wide range of attack time programmability is supported in terms of number of samples (i.e. number of ADC sample frequency clock cycles).
- **Decay Time** determines how quickly the PGA gain is increased when the output signal level falls below the target level due to reduction in input signal level. Wide range of decay time programmability is supported in terms of number of samples (i.e., number of ADC sample frequency clock cycles).
- **Noise threshold** determines the level below which if the input signal level falls, the AGC considers it as silence, and thus brings down the gain to 0 dB in steps of 0.5 dB every FS and sets the noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This specifies that noise is not 'gained up' in the absence of speech. Noise threshold level in the AGC algorithm is programmable from -30dB to -90 dB of full-scale. When AGC Noise Threshold is set to –70dB, –80db, or –90dB, the microphone input Max PGA applicable setting must be greater than or equal to 11.5dB, 21.5dB, or 31.5dB respectively. This operation includes hysteresis and debounce to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. The noise (or silence) detection feature can be entirely disabled by the user.
- **Max PGA applicable** allows the designer to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input Max PGA can be programmed from 0 dB to 40dB in steps of 0.5 dB.
- **Hysteresis**, as the name suggests, determines a window around the Noise Threshold which must be exceeded to either detect that the recorded signal is indeed noise or signal. If initially the energy of the recorded signal is greater than the Noise Threshold, then the AGC recognizes it as noise only when the energy of the recorded signal falls below the Noise Threshold by a value given by Hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize it as a signal, its energy must exceed the Noise Threshold by a value given by the Hysteresis setting. In order to prevent the AGC from jumping between noise and signal states, (which can happen when the energy of recorded signal is very close to the Noise threshold) a non-zero hysteresis value should be chosen. The Hysteresis feature can also be disabled.
- **Debounce Time (Noise and Signal)** determines the hysteresis in time domain for noise detection. The AGC

continuously calculates the energy of the recorded signal. If the calculated energy is less than the set Noise Threshold, then the AGC does not increase the input gain to achieve the Target Level. However, to handle audible artifacts which can occur when the energy of the input signal is very close to the Noise Threshold, the AGC checks if the energy of the recorded signal is less than the Noise Threshold for a time greater than the Noise Debounce Time. Similarly the AGC starts increasing the input-signal gain to reach the Target Level when the calculated energy of the input signal is greater than the Noise Threshold. Again, to avoid audible artifacts when the input-signal energy is very close to Noise Threshold, the energy of the input signal needs to continuously exceed the Noise Threshold value for the Signal Debounce Time. If the debounce times are kept very small, then audible artifacts can result by rapid enabling and disabling the AGC function. At the same time, if the Debounce time is kept too large, then the AGC may take time to respond to changes in levels of input signals with respect to Noise Threshold. Both noise and signal debounce time can be disabled.

- The **AGC Noise Threshold Flag** is a read-only flag indicating that the input signal has levels lower than the Noise Threshold, and thus is detected as noise (or silence). In such a condition the AGC applies a gain of 0 dB.
- **Gain Applied by AGC** is a ready-only register setting which gives a real-time feedback to the system on the gain applied by the AGC to the recorded signal. This, along with the Target Setting, can be used to determine the input signal level. In a steady state situation Target Level (dB) = Gain Applied by AGC (dB) + Input Signal Level (dB) When the AGC noise threshold flag is set, then the status of gain applied by AGC should be ignored.
- The **AGC Saturation Flag** is a read-only flag indicating that the ADC output signal has not reached its Target Level. However, the AGC is unable to increase the gain further because the required gain is higher than the Maximum Allowed PGA gain. Such a situation can happen when the input signal has very low energy and the Noise Threshold is also set very low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.
- The **ADC Saturation Flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC Target Level is kept very high and the energy in the input signal increases faster than the Attack Time.
- An **AGC low-pass filter** is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low pass filter is in the form of a first-order IIR filter. Two 8-bit registers are used to form the 16-bit digital coefficient as shown on the register map. In this way, a total of 6 registers are programmed to form the 3 IIR coefficients. The transfer function of the filter implemented for signal level detection is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (1)$$

Where:

Coefficient N0 can be programmed by writing into Page 4, Registers 2 and 3.
Coefficient N1 can be programmed by writing into Page 4, Registers 4 and 5.
Coefficient D1 can be programmed by writing into Page 4, Registers 6 and 7.
N0, N1 and D1 are 16-bit 2's complement numbers and their default values implement a low-pass filter with cut-off at 0.002735 × ADC_FS .

See Table 2 for various AGC programming options. AGC can be used only if analog microphone input is routed to the ADC channel.

Table 2. AGC Parameter Settings

Function	Control Register Left ADC	Control Register Right ADC	Bit
AGC enable	Page 0, Register 86	Page 0,Register 94	D(7)
Target Level	Page 0, Register 86	Page 0, Register 94	D(6:4)
Hysteresis	Page 0, Register 87	Page 0, Register 95	D(7:6)
Noise threshold	Page 0, Register 87	Page 0, Register 95	D(5:1)
Max PGA applicable	Page 0, Register 88	Page 0, Register 96	D(6:0)
Time constants (attack time)	Page 0, Register 89	Page 0, Register 97	D(7:0)
Time constants(decay time)	Page 0, Register 90	Page 0, Register 98	D(7:0)
Debounce time (Noise)	Page 0, Register 91	Page 0, Register 99	D(4:0)

Table 2. AGC Parameter Settings (continued)

Function	Control Register Left ADC	Control Register Right ADC	Bit
Debounce time (Signal)	Page 0, Register 92	Page 0, Register 100	D(3:0)
Gain applied by AGC	Page 0, Register 93	Page 0, Register 101	D(7:0) (Read Only)
AGC Noise Threshold Flag	Page 0, Register 45 (sticky flag), Page 0, Register 47 (non-sticky flag)	Page 0, Register 45 (sticky flag), Page 0, Register 47 (non-sticky flag)	D(6:5) (Read Only)
AGC Saturation flag	Page 0, Register 36 (sticky flag)	Page 0, Register 36 (sticky flag)	D(5), D(1) (Read Only)
ADC Saturation flag	Page 0, Register 42 (sticky flag), Page 0, Register 43 (non-sticky flag)	Page 0, Register 42 (sticky flag), Page 0, Register 43 (non-sticky flag)	D(3:2) (Read Only)

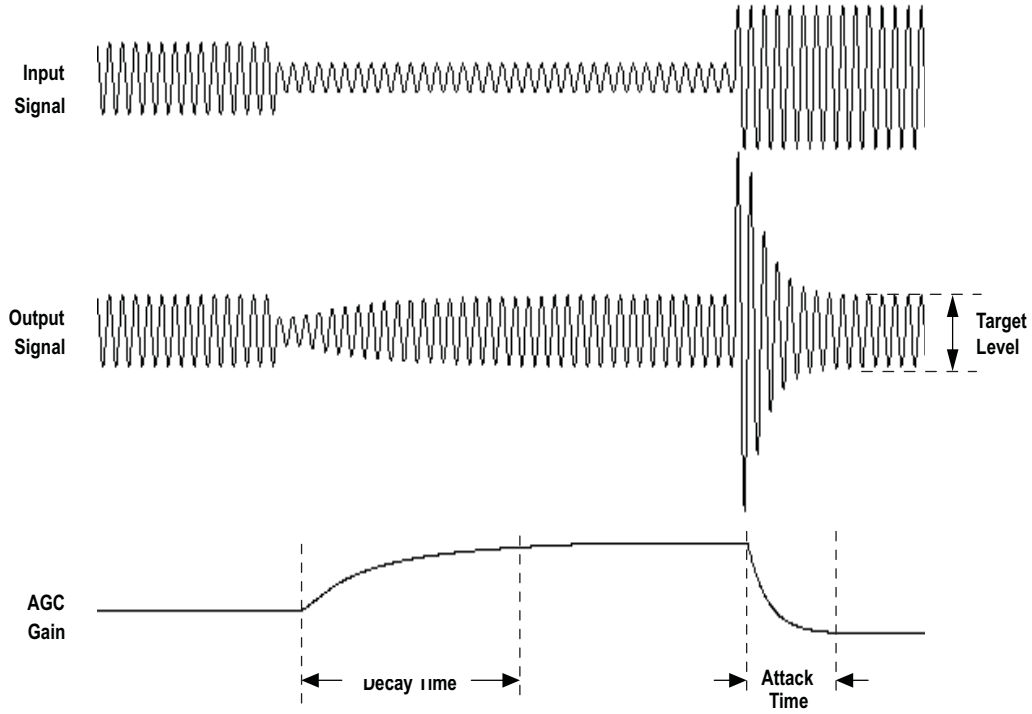


Figure 32. AGC Characteristics

The TLV320ADC3101 includes three analog audio input pins, which can be configured as one fully-differential pair and one single-ended input, or as three single-ended audio inputs. These pins connect through series resistors and switches to the virtual ground terminals of two fully differential operational amplifiers (one per ADC/PGA channel). By selecting to turn on only one set of switches per operational amplifier at a time, the inputs can be effectively muxed to each ADC PGA channel.

By selecting to turn on multiple sets of switches per operational amplifier at a time, mixing can also be achieved. Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal operational amplifiers, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, the user should take adequate precautions to avoid such a saturation case from occurring. In general, the mixed signal should not exceed 2 V_{pp} (single-ended) or 4 V_{pp} (differential).

In most mixing applications, there is also a general need to adjust the levels of the individual signals being mixed. For example, if a soft signal and a large signal are to be mixed and played together, the soft signal generally should be amplified to a level comparable to the large signal before mixing. In order to accommodate this need, the TLV320ADC3101 includes input level control on each of the individual inputs before they are mixed or muxed into the ADC PGAs, with programmable attenuation at 0dB, –6 dB, or off. Note that this input level control is not intended to be a volume control, but instead used for coarse level setting. Finer soft-stepping of the input level is implemented in this device by the ADC PGA.

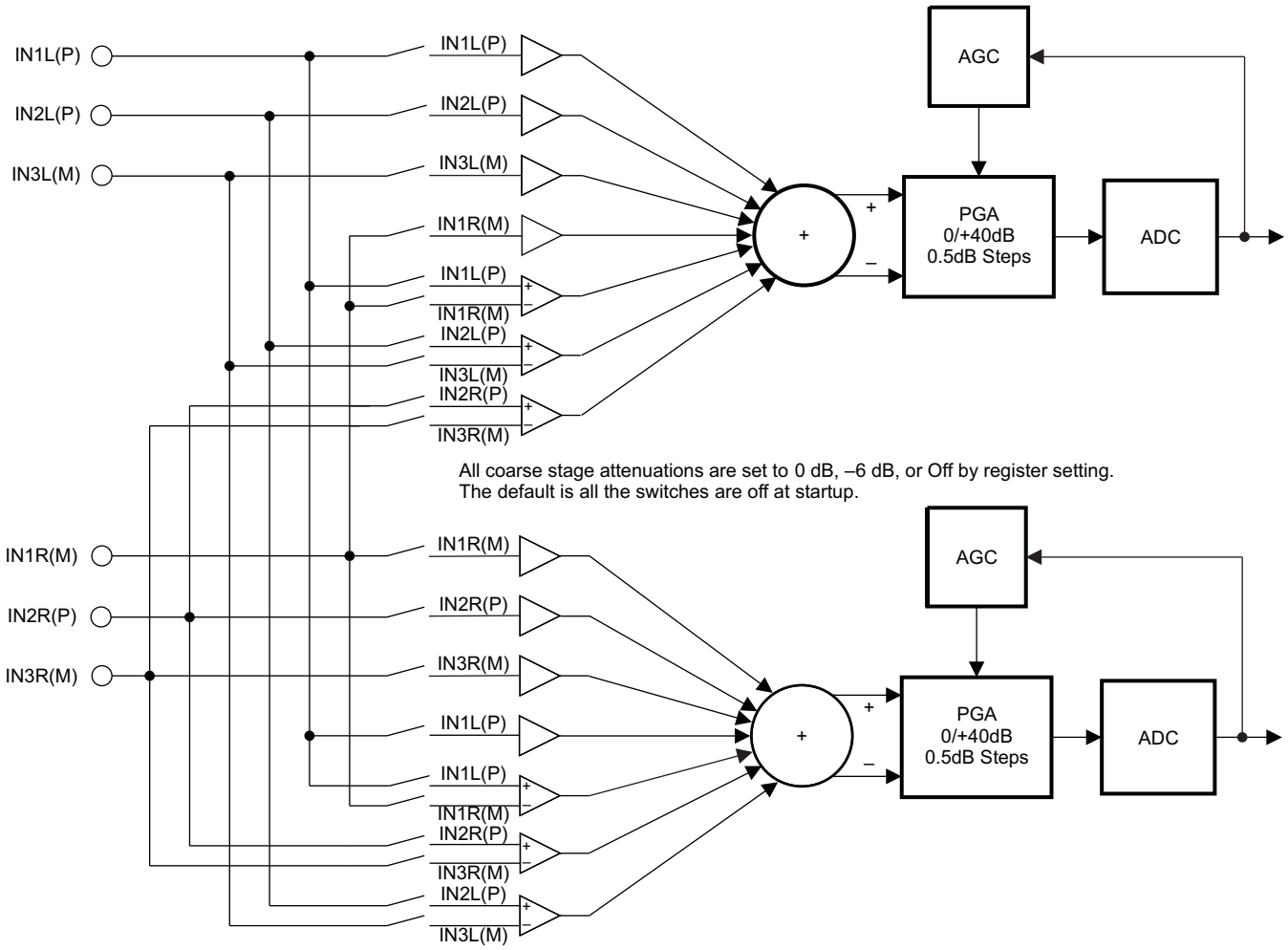


Figure 33. TLV320ADC3101RGE Available Audio Input Path Configurations

Table 3. TLV320ADC3101RGE Audio Signals

Audio Signals Available to Left ADC			Audio Signals Available to Right ADC	
Single Ended Inputs	Differential Inputs		Single Ended Inputs	Differential Inputs
IN1L(P)	IN1L(P), IN1R(M)		IN1R(M)	IN1L(P), IN1R(M)
IN2L(P)	IN2L(P), IN3L(M)		IN2R(P)	IN2R(P), IN3R(M)
IN3L(M)	IN2R(P), IN3R(M)		IN3R(M)	IN2L(P), IN3L(M)
IN1R(M)			IN1L(P)	

Inputs can be selected as single-ended instead of fully-differential, and mixing or muxing into the ADC PGAs is also possible in this mode. It is not possible, however, for an input pair to be selected as fully-differential for connection to one ADC PGA and simultaneously selected as single-ended for connection to the other ADC PGA channel. However, it is possible for an input to be selected or mixed into both left and right channel PGAs, as long as it has the same configuration for both channels (either both single-ended or both fully-differential).

INPUT IMPEDANCE AND VCM CONTROL

The TLV320ADC3101 includes several programmable settings to control analog input pins, particularly when they are not selected for connection to an ADC PGA. The default option allows unselected inputs to be put into a 3-state condition, such that the input impedance seen looking into the device is extremely high. Note, however, that the pins on the device do include protection diode circuits connected to AVDD and AVSS. Thus, if any voltage is driven onto a pin approximately one diode drop (~0.6 V) above AVDD or one diode drop below AVSS, these protection diodes will begin conducting current, resulting in an effective impedance that no longer appears as a 3-state condition.

Another programmable option for unselected analog inputs is to weakly hold them at the common-mode input voltage of the ADC PGA (which is determined by an internal bandgap voltage reference). This is useful to keep the ac-coupling capacitors connected to analog inputs biased up at a normal dc level, thus avoiding the need for them to charge up suddenly when the input is changed from being unselected to selected for connection to an ADC PGA. This option is controlled in Page-1/Reg-52 through 57. The user should make sure this option is disabled when an input is selected for connection to an ADC PGA or selected for the analog input bypass path, since it can corrupt the recorded input signal if left operational when an input is selected.

In most cases, the analog input pins on the TLV320ADC3101 should be ac-coupled to analog input sources, the only exception to this generally being if an ADC is being used for dc voltage measurement. The ac-coupling capacitor will cause a highpass filter pole to be inserted into the analog signal path, so the size of the capacitor must be chosen to move that filter pole sufficiently low in frequency to cause minimal effect on the processed analog signal. The input impedance of the analog inputs when selected for connection to an ADC PGA varies with the setting of the input level control, starting at approximately 35 kΩ with an input level control setting of 0-dB, and 62.5-kΩ when the input level control is set at –6 dB. For example, using a 0.1 μF ac-coupling capacitor at an analog input will result in a highpass filter pole of 45.5 Hz when the 0 dB input level control setting is selected. To set a high pass corner for the application, the following input impedance table has been provided with various mixer gains and microphone PGA ranges.

Table 4. Single-Ended Input Impedance vs PGA Ranges (1)

Mixer Gain (dB)	Microphone PGA Range (dB)	Input Impedance (Ohms)
0	0 - 5.5	35000
0	6 - 11.5	38889
0	12 - 17.5	42000
0	18 - 23.5	44074
0	24 - 29.5	45294
0	30 - 35.5	45960
0	36 - 40	46308
-6	0 - 5.5	62222
-6	6 - 11.5	70000
-6	12 - 17.5	77778
-6	18 - 23.5	84000
-6	24 - 29.5	88148
-6	30 - 35.5	90588
-6	36 - 40	91919

(1) Valid when only one input is enabled.

MICBIAS GENERATION

The TLV320ADC3101 includes two programmable microphone bias outputs (MICBIAS1, MICBIAS2), each capable of providing output voltages of 2 V or 2.5 V (both derived from the on-chip bandgap voltage) with 4-mA output current drive capability. In addition, the MICBIAS outputs may be programmed to be switched to AVDD directly through an on-chip switch, or it can be powered down completely when not needed, for power savings. This function is controlled by register programming in Page-1/Reg-51.

ADC Decimation Filtering and Signal Processing

The TLV320ADC3101 ADC channel includes a built-in digital decimation filter to process the oversampled data from the sigma-delta modulator to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

Processing Blocks

The TLV320ADC3101 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user programmable coefficients.

Table 5. ADC Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Instruction Count
PRB_R1	Stereo	A	Yes	0	No	128,64	188
PRB_R2	Stereo	A	Yes	5	No	128,64	240
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	236
PRB_R4	Right	A	Yes	0	No	128,64	96
PRB_R5	Right	A	Yes	5	No	128,64	120
PRB_R6	Right	A	Yes	0	25-Tap	128,64	120
PRB_R7	Stereo	B	Yes	0	No	64	88
PRB_R8	Stereo	B	Yes	3	No	64	120
PRB_R9	Stereo	B	Yes	0	20-Tap	64	128
PRB_R10	Right	B	Yes	0	No	64	46
PRB_R11	Right	B	Yes	3	No	64	60
PRB_R12	Right	B	Yes	0	20-Tap	64	64
PRB_R13	Right	C	Yes	0	No	32	70
PRB_R14	Stereo	C	Yes	5	No	32	124
PRB_R15	Stereo	C	Yes	0	25-Tap	32	120
PRB_R16	Right	C	Yes	0	No	32	36
PRB_R17	Right	C	Yes	5	No	32	64
PRB_R18	Right	C	Yes	0	25-Tap	32	62

Processing Blocks – Details

1st order IIR, AGC, Filter A

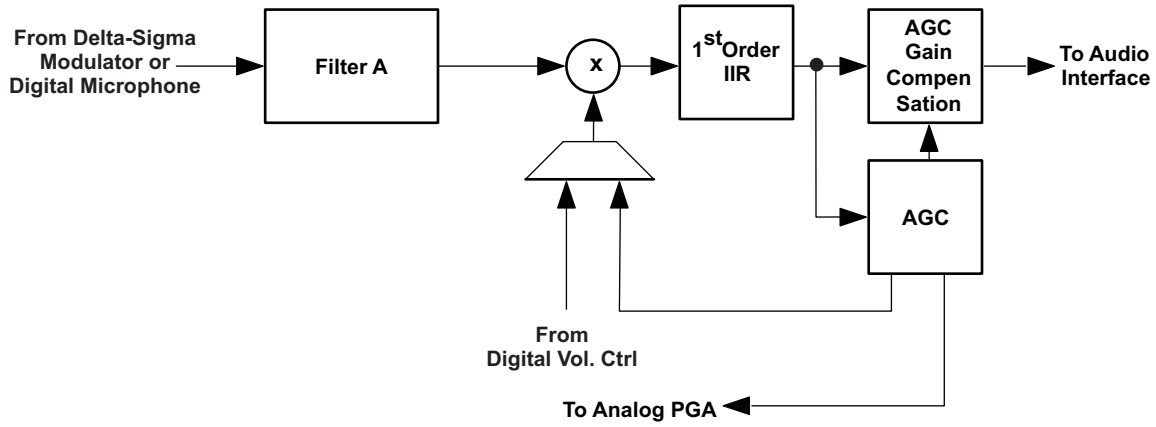


Figure 34. Signal Chain for PRB_R1 and PRB_R4

5 Biquads, 1st order IIR, AGC, Filter A

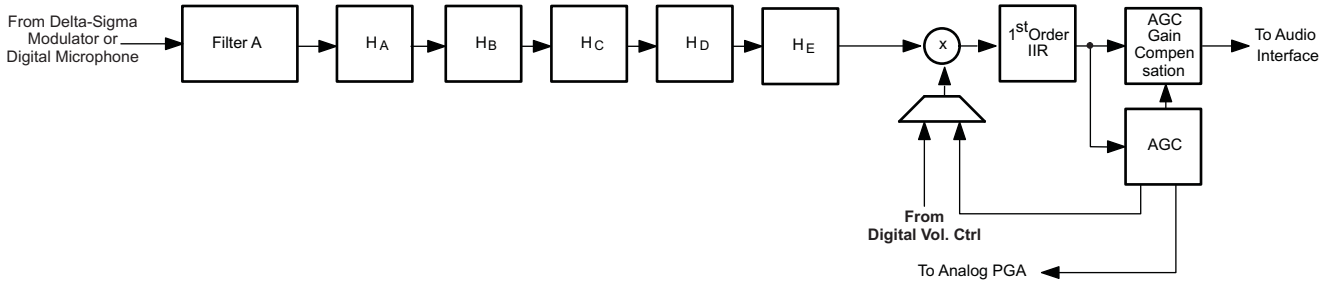


Figure 35. Signal Chain PRB_R2 and PRB_R5

25 Tap FIR, 1st order IIR, AGC, Filter A

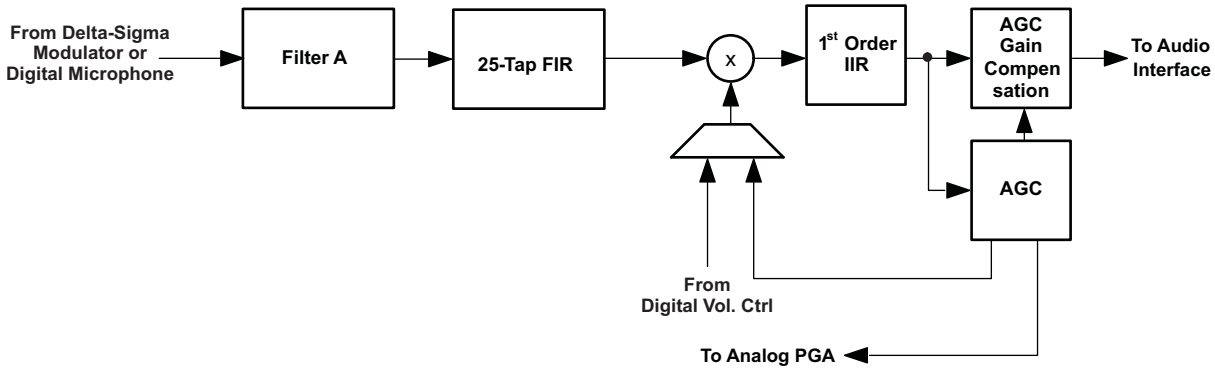


Figure 36. Signal Chain for PRB_R3 and PRB_R6

1st order IIR, AGC, Filter B

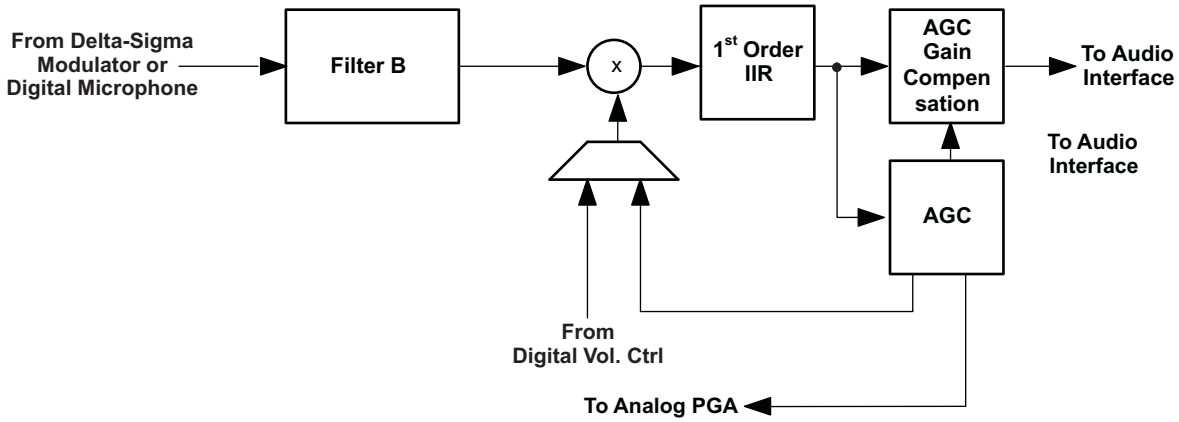


Figure 37. Signal Chain for PRB_R7 and PRB_R10

3 Biquads, 1st order IIR, AGC, Filter B

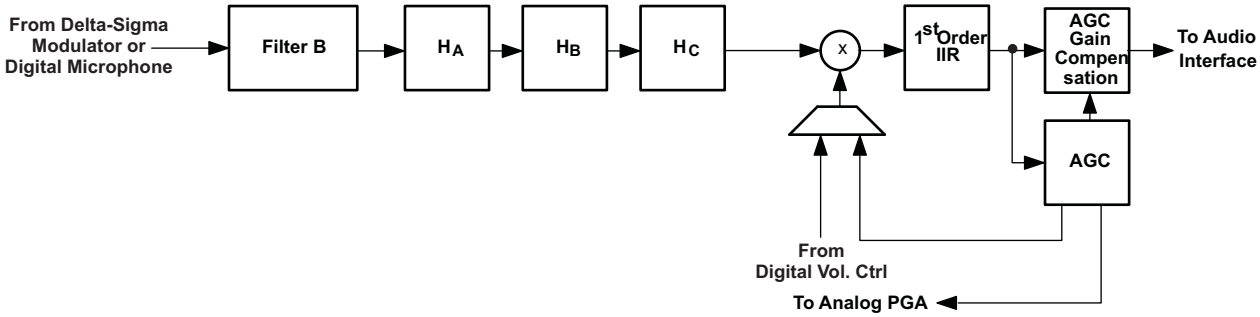


Figure 38. Signal Chain for PRB_R8 and PRB_R11

20 Tap FIR, 1st order IIR, AGC, Filter B

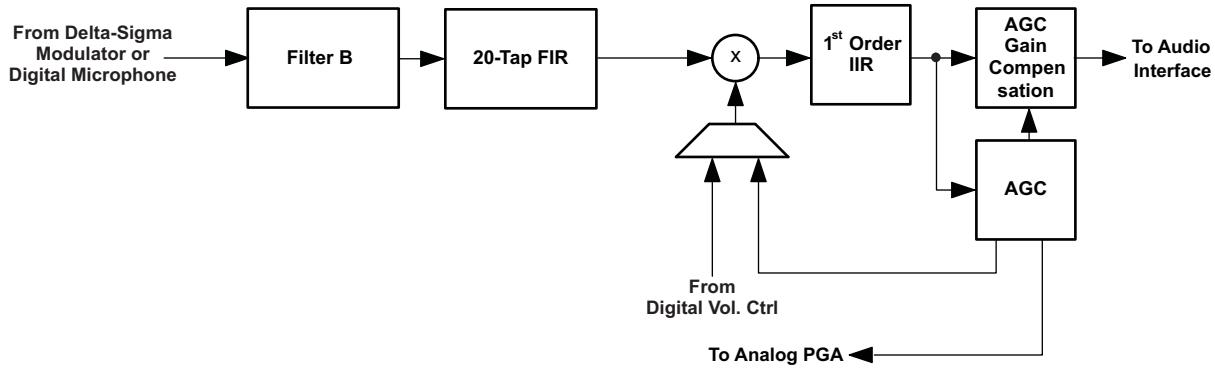


Figure 39. Signal Chain for PRB_R9 and PRB_R12

1st order IIR, AGC, Filter C

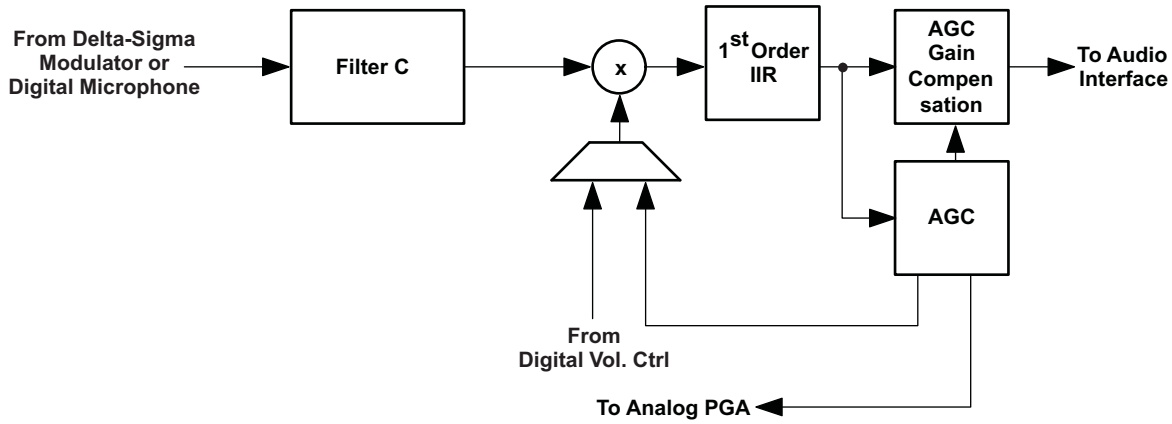


Figure 40. Signal Chain for PRB_R13 and PRB_R16

5 Biquads, 1st order IIR, AGC, Filter C

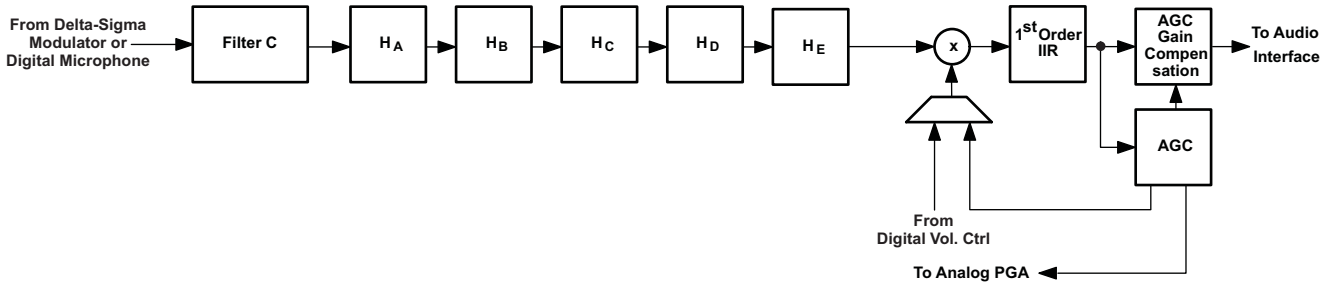


Figure 41. Signal Chain for PRB_R14 and PRB_R17

25 Tap FIR, 1st order IIR, AGC, Filter C

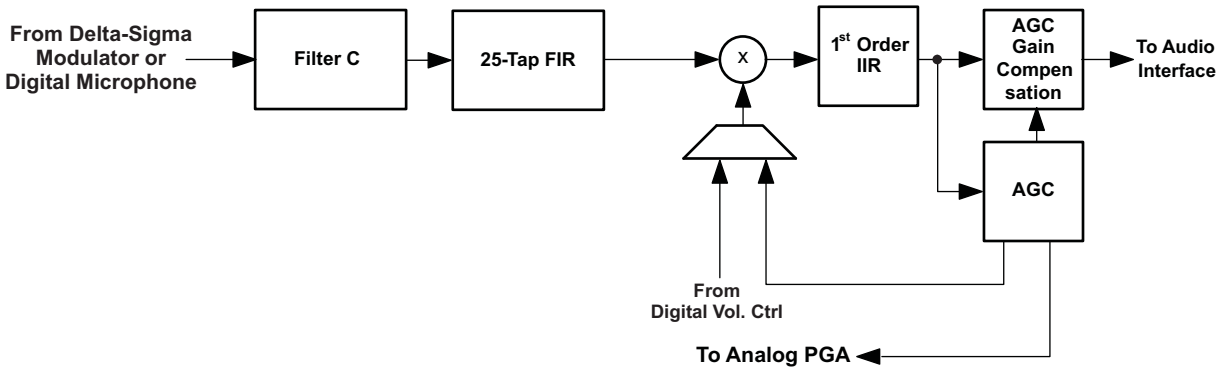


Figure 42. Signal for PRB_R15 and PRB_R18

User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. A 1st-order IIR filter is always available, and is useful to efficiently filter out possible dc components of the signal. Up to 5 biquad section or alternatively up to 25-tap FIR filters are available for specific processing blocks. The coefficients of the available filters are arranged as sequentially indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched on-the-fly.

The coefficients of these filters are each 16-bits wide, in 2s-complement and occupy two consecutive 8-bit registers in the register space. Table 6.

1st Order IIR Section

The transfer function for the first order IIR Filter is given by Equation 2.

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (2)$$

The frequency response for the 1st order IIR Section with default coefficients is flat at a gain of 0dB.

Table 6. ADC 1st order IIR Filter Coefficients

Filter	FIlter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
1st Order IIR	N0	C4 (Pg 4, Reg 8, 9)	C36 (Pg 4,Reg 72, 73)
	N1	C5 (Pg 4, Reg 10, 11)	C37 (Pg 4,Reg 74, 75)
	D1	C6 (Pg 4, Reg 12, 13)	C38 (Pg 4,Reg 76, 77)

Biquad Section

The transfer function of each of the Biquad Filters is given by Equation 3.

$$H(z) = \frac{N_0 + 2 \times N_1 z^{-1} + N_2 z^{-2}}{2^{15} - 2 \times D_1 z^{-1} - D_2 z^{-2}} \quad (3)$$

The frequency response for each of the biquad sections with default coefficients is flat at a gain of 0dB.

Table 7. ADC Biquad Filter Coefficients

Filter	FIlter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
BIQUAD A	N0	C7 (Pg 4, Reg 14, 15)	C39 (Pg 4, Reg 78, 79)
	N1	C8 (Pg 4, Reg 16, 17)	C40 (Pg 4, Reg 80, 81)
	N2	C9 (Pg 4, Reg 18, 19)	C41 (Pg 4, Reg 82, 83)
	D1	C10 (Pg 4, Reg 20, 21)	C42 (Pg 4, Reg 84, 85)
	D2	C11 (Pg 4, Reg 22, 23)	C43 (Pg 4, Reg 86, 87)
BIQUAD B	N0	C12 (Pg 4, Reg 24, 25)	C44 (Pg 4, Reg 88, 89)
	N1	C13 (Pg 4, Reg 26, 27)	C45 (Pg 4, Reg 90, 91)
	N2	C14 (Pg 4, Reg 28, 29)	C46 (Pg 4, Reg 92, 93)
	D1	C15 (Pg 4, Reg 30, 31)	C47 (Pg 4, Reg 94, 95)
	D2	C16 (Pg 4, Reg 32, 33)	C48 (Pg 4, Reg 96, 97)
BIQUAD C	N0	C17 (Pg 4, Reg 34, 35)	C49 (Pg 4, Reg 98, 99)
	N1	C18 (Pg 4, Reg 36, 37)	C50 (Pg 4, Reg 100, 101)
	N2	C19 (Pg 4, Reg 38, 39)	C51 (Pg 4, Reg 102, 103)
	D1	C20 (Pg 4, Reg 40, 41)	C52 (Pg 4, Reg 104, 105)
	D2	C21 (Pg 4, Reg 42, 43)	C53 (Pg 4, Reg 106, 107)
BIQUAD D	N0	C22 (Pg 4, Reg 44, 45)	C54 (Pg 4, Reg 108, 109)
	N1	C23 (Pg 4, Reg 46, 47)	C55 (Pg 4, Reg 110, 111)
	N2	C24 (Pg 4, Reg 48, 49)	C56 (Pg 4, Reg 112,113)
	D1	C25 (Pg 4, Reg 50, 51)	C57 (Pg 4, Reg 114, 115)
	D2	C26 (Pg 4, Reg 52, 53)	C58 (Pg 4, Reg 116, 117)
BIQUAD E	N0	C27 (Pg 4, Reg 54, 55)	C59 (Pg 4, Reg 118, 119)
	N1	C28 (Pg 4, Reg 56, 57)	C60 (Pg 4, Reg 120, 121)
	N2	C29 (Pg 4, Reg 58, 59)	C61 (Pg 4, Reg 122,123)
	D1	C30 (Pg 4, Reg 60, 61)	C62 (Pg 4, Reg 124, 125)
	D2	C31 (Pg 4, Reg 62, 63)	C63 (Pg 4, Reg 126, 127)

FIR Section

Six of the available ADC processing blocks offer FIR filters for signal processing. PRB_R9 and PRB_R12 feature a 20-tap FIR filter while the processing blocks PRB_R3, PRB_R6, PRB_R15 and PRB_R18 feature a 25-tap FIR filter

$$H(z) = \sum_{n=0}^{M} Fir_n z^{-n}$$

$$M = 24, \text{for PRB\_R3, PRB\_R6, PRB\_R15 and PRB\_R18}$$

$$M = 19, \text{for PRB\_R9 and PRB\_R12} \quad (4)$$

The coefficients of the FIR filters are 16-bit 2's complement format and correspond to the ADC coefficient space as listed below. There is no default transfer function for the FIR filter. When the FIR filter gets used all applicable coefficients must be programmed.

Table 8. ADC FIR Filter Coefficients

Filter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
Fir0	C7 (Pg 4, Reg 14, 15)	C39 (Pg 4, Reg 78, 79)
Fir1	C8 (Pg 4, Reg 16, 17)	C40 (Pg 4, Reg 80, 81)
Fir2	C9 (Pg 4, Reg 18, 19)	C41 (Pg 4, Reg 82, 83)
Fir3	C10 (Pg 4, Reg 20, 21)	C42 (Pg 4, Reg 84, 85)
Fir4	C11 (Pg 4, Reg 22, 23)	C43 (Pg 4, Reg 86, 87)
Fir5	C12 (Pg 4, Reg 24, 25)	C44 (Pg 4, Reg 88, 89)
Fir6	C13 (Pg 4, Reg 26, 27)	C45 (Pg 4, Reg 90, 91)
Fir7	C14 (Pg 4, Reg 28, 29)	C46 (Pg 4, Reg 92, 93)
Fir8	C15 (Pg 4, Reg 30, 31)	C47 (Pg 4, Reg 94, 95)
Fir9	C16 (Pg 4, Reg 32, 33)	C48 (Pg 4, Reg 96, 97)
Fir10	C17 (Pg 4, Reg 34, 35)	C49 (Pg 4, Reg 98, 99)
Fir11	C18 (Pg 4, Reg 36, 37)	C50 (Pg 4, Reg 100, 101)
Fir12	C19 (Pg 4, Reg 38, 39)	C51 (Pg 4, Reg 102, 103)
Fir13	C20 (Pg 4, Reg 40, 41)	C52 (Pg 4, Reg 104, 105)
Fir14	C21 (Pg 4, Reg 42, 43)	C53 (Pg 4, Reg 106, 107)
Fir15	C22 (Pg 4, Reg 44, 45)	C54 (Pg 4, Reg 108, 109)
Fir16	C23 (Pg 4, Reg 46, 47)	C55 (Pg 4, Reg 110, 111)
Fir17	C24 (Pg 4, Reg 48, 49)	C56 (Pg 4, Reg 112,113)
Fir18	C25 (Pg 4, Reg 50, 51)	C57 (Pg 4, Reg 114, 115)
Fir19	C26 (Pg 4, Reg 52, 53)	C58 (Pg 4, Reg 116, 117)
Fir20	C27 (Pg 4, Reg 54, 55)	C59 (Pg 4, Reg 118, 119)
Fir21	C28 (Pg 4, Reg 56, 57)	C60 (Pg 4, Reg 120, 121)
Fir22	C29 (Pg 4, Reg 58, 59)	C61 (Pg 4, Reg 122, 123)
Fir23	C30 (Pg 4, Reg 60, 61)	C62 (Pg 4, Reg 124, 125)
Fir24	C31 (Pg 4, Reg 62, 63)	C63 (Pg 4, Reg 126, 127)

Decimation Filter

The TLV320ADC3101 offers 3 different types of decimation filters. The integrated digital decimation filter removes high-frequency content and down samples the audio data from an initial sampling rate of AOSR × Fs to the final output sampling rate of Fs. The decimation filtering is achieved using a higher-order CIC filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself, it is implicitly set through the chosen processing block.

The following subsections describe the properties of the available filters A, B and C.

Decimation Filter A

This filter is intended for use at sampling rates up to 48kHz. When configuring this filter, the oversampling ratio of the ADC can either be 128 or 64. For highest performance the oversampling ratio must be set to 128. Filter A can also be used for 96kHz at an AOSR of 64.

Table 9. ADC Decimation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
AOSR = 128			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…64Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.18 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
AOSR = 64			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…32Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.18 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.1	dB

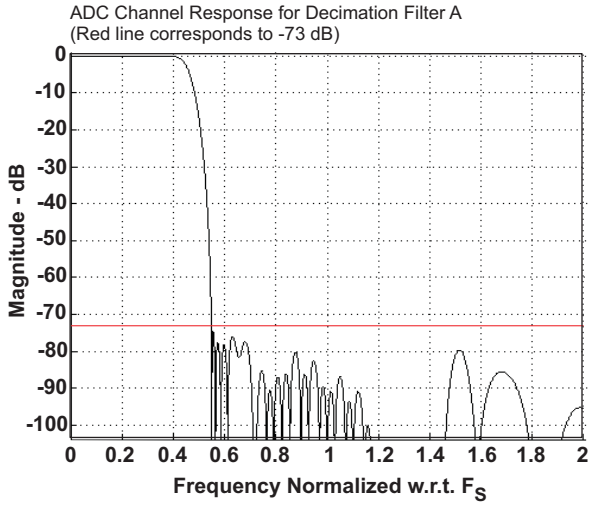


Figure 43. ADC Decimation Filter A, Frequency Response

Decimation Filter B

Filter B is intended to support sampling rates up to 96kHz at a oversampling ratio of 64.

Table 10. ADC Decimation Filter B, Specifications

Parameter	Condition	Value (Typical)	Units
AOSR = 64			
Filter Gain Pass Band	0…0.39Fs	±0.077	dB
Filter Gain Stop Band	0.60Fs…32Fs	–46	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39Fs	0.076	dB
Pass Band Ripple, 44.18 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 48 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.11	dB

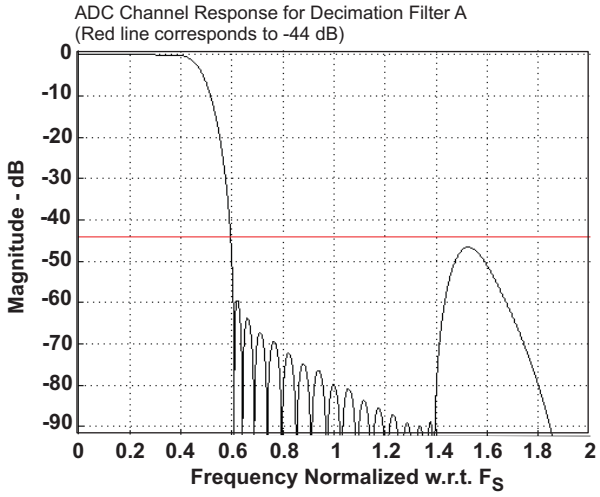


Figure 44. ADC Decimation Filter B, Frequency Response

Decimation Filter C

Filter type C along with AOSR of 32 is specially designed for 192ksps operation for the ADC. The pass band which extends up to 0.11 × Fs (corresponds to 21kHz), is suited for audio applications.

Table 11. ADC Decimation Filter C, Specifications

Parameter	Condition	Value (Typical)	Units
Filter Gain from 0 to 0.11Fs	0…0.11Fs	±0.033	dB
Filter Gain from 0.28Fs to 16Fs	0.28Fs…16Fs	–60	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 44.18 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 48 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 96 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 192 ksps	0…20kHz	0.086	dB

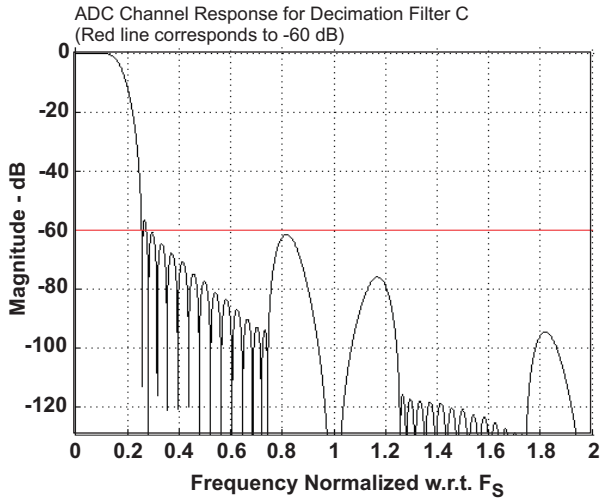


Figure 45. ADC Decimation Filter C, Frequency Response

ADC Data Interface

The decimation filter and signal processing block in the ADC channel passes 32-bit data words to the audio serial interface once every cycle of Fs, ADC. During each cycle of Fs,ADC, a pair of data words (for left and right channel) are passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data as per the different modes for audio serial interface.

Digital Microphone Function

In addition to supporting analog microphones, the TLV320ADC3101 also interfaces to digital microphones.

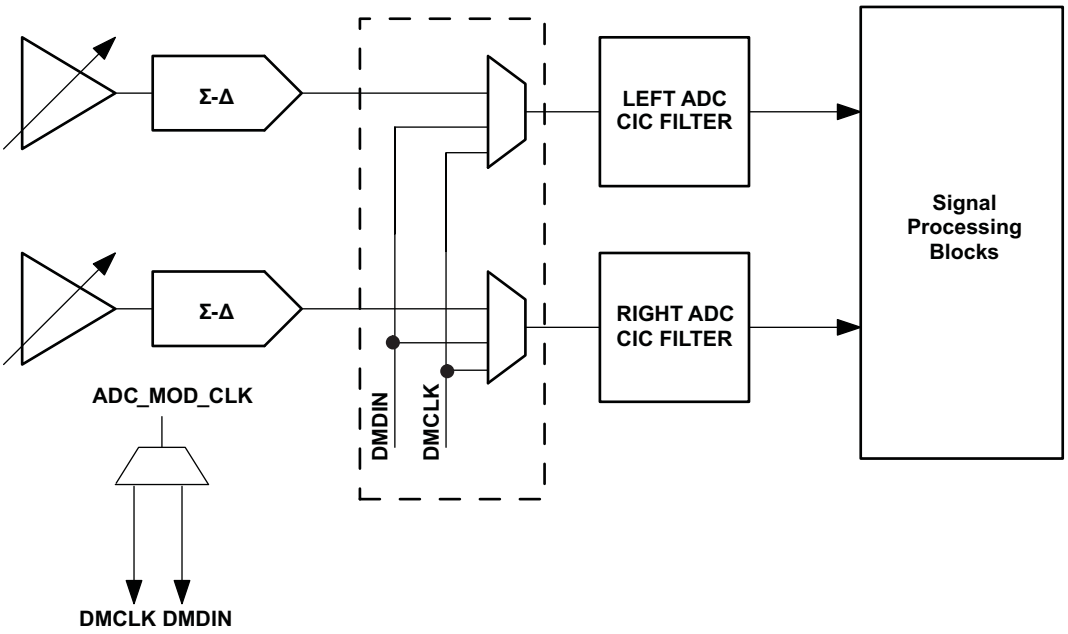


Figure 46. Digital Microphone in TLV320ADC3101

The TLV320ADC3101 outputs internal clock ADC_MOD_CLK on the DMCLK pin (Page 0, Register 51, D(5:2)) or DMDIN pin (Page 0, Register 52, D(5:2)). This clock can be connected to the external digital microphone device. The single-bit output of the external digital microphone device can be connected to DMDIN or DMCLK pins. Internally the TLV320ADC3101 latches the steady value of data on a selectable edge (Page 0, Register 80, D(1)) of ADC_MOD_CLK for the Left ADC channel, and the steady value of data on a selectable edge (Page 0, Register 80, D(0)) for the Right ADC channel.

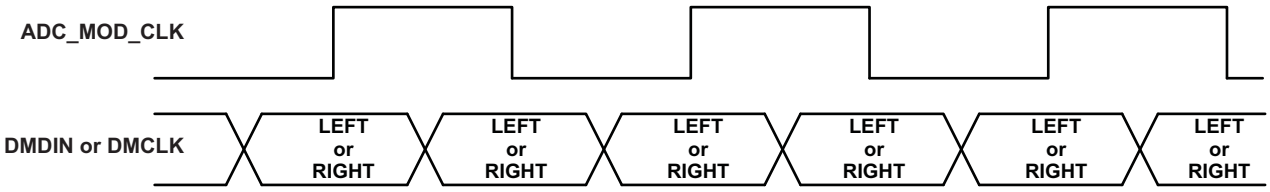


Figure 47. Timing Diagram for Digital Microphone Interface

The digital-microphone mode can be selectively enabled for only-left, only-right, or stereo channels. When the digital microphone mode is enabled, the analog section of the ADC can be powered down and bypassed for power efficiency. The AOSR value for the ADC channel must be configured to select the desired decimation ratio to be achieved based on the external digital microphone properties.

CONTROL REGISTERS

The control registers for the TLV320ADC3101 are described in detail as follows. All registers are 8 bits in width, with D7 referring to the most-significant bit of each register, and D0 referring to the least-significant bit.

Pages 0, 1, 4, 5, and 32 - 47 are available. All other pages are Reserved. Do not read or write to reserved pages.

Page/Register Map

PAGE0: (Clock Multipliers and Dividers, Serial Interfaces, Flags, Interrupts and GPIO's related programmability's)	
Reg No.	***Reg Name***
0	Page Control Register
1	S/W RESET
2	Revision and PG ID
3	Reserved
4	Clock-Gen Muxing
5	PLL P and R-VAL
6	PLL J-VAL
7	PLL D-VAL MSB
8	PLL D-VAL LSB
9 - 17	Reserved
18	ADC NADC_VAL
19	ADC MADC_VAL
20	ADC AOSR_VAL
21	ADC IADC_VAL
22	ADC MAC Engine Decimation
23 and 24	Reserved
25	CLKOUT MUX
26	CLKOUT M_VAL
27	ADC INTERFACE CONTROL1
28	DATA SLOT OFFSET PROGRAMMABILITY
29	ADC INTERFACE CONTROL2
30	BCLK N_VAL
31	CODEC Secondary Interface Control 1
32	CODEC Secondary Interface Control 2
33	CODEC Secondary Interface Control 3
34	I2S Sync
35	Reserved
36	ADC Flag Register
37	Data Slot Offset Progammability
38	I2S TDM Control Register
39 - 41	Reserved
42	Interrupt Flags (Overflow)
43	Interrupt Flags (Overflow)
44	Reserved
45	Interrupt Flags-ADC
46	Reserved
47	Interrupt Flags-ADC
48	INT1 Interrupt Control
49	INT2 Interrupt Control
50	Reserved
51	DMCLK/GPIO2 Control
52	DMDIN/GPIO1 Control
53	DOUT (OUT PIN) CONTROL
54 - 56	Reserved
57	ADC Sync Control 1

Page/Register Map (continued)

58	ADC Sync Control 2
59	ADC CIC Filter Gain Control
60	Reserved
61	ADC Instruction Set
62	Programmable Instruction mode control bits
63 - 79	Reserved
80	Digital Microphone Polarity Control
81	ADC Digital
82	ADC Volume Control
83	Left ADC Volume Control
84	Right ADC Volume Control
85	ADC Phase Compensation
86	Left AGC Control 1
87	Left AGC Control 2
88	Left AGC Maximum Gain
89	Left AGC Attack Time
90	Left AGC Decay Time
91	Left AGC Noise Debounce
92	Left AGC Signal Debounce
93	Left AGC Gain
94	Right AGC Control 1
95	Right AGC Control 2
96	Right AGC Maximum Gain
97	Right AGC Attack Time
98	Right AGC Decay Time
99	Right AGC Noise Debounce
100	Right AGC Signal Debounce
101	Right AGC Gain
102 - 127	Reserved
PAGE1: (ADC Routing, PGA, Power-Controls and MISC logic related programmabilities)	
Reg No.	**Reg Name**
0	Page Control Register
1 - 25	Reserved
26	Dither Control
27 - 50	Reserved
51	MICBIAS Control
52	Left ADC Input selection for Left PGA
53	Reserved
54	Left ADC Input selection for Left PGA
55	Right ADC Input selection for Right PGA
56	Reserved
57	Right ADC Input selection for Right PGA
58	Reserved
59	Left Analog PGA setting
60	Right Analog PGA setting
61	ADC low current modes
62	ADC Analog PGA Flags

Page/Register Map (continued)

63 - 127	Reserved
PAGE 2: Reserved. Do not read or write to this page.	
PAGE 3: Reserved. Do not read or write to this page.	
ADC Digital Filter RAM and Instruction Pages:	
PAGE 4: ADC Programmable Coefficients RAM (1:63)	
PAGE 5: ADC Programmable Coefficients RAM (65:127)	
PAGES 6-31: Reserved. Do not read or write to these pages.	
PAGES 32-47: ADC Programmable Instruction RAM (0:511)	
Page 32 Instruction Instr0(0:31)	
Page 33 Instruction Instr1(32:63)	
Page 34 Instruction Instr2(64:95)	
...	
Page 47 Instruction Instr15(479:511)	
PAGES 48-255: Reserved. Do not read or write to these pages.	

Page 0/Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0	Valid pages are 0,1,4, 5, 32-47

Page 0/Register 1: Software Reset

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	0000 000	Reserved. Write only zeros to these bits.
D0	R/W	0	0: Don't care 1: Self-clearing software reset for control register

Page 0/Register 2: Revision ID

BIT	Reset Value	Values	DESCRIPTION
D7	0	All values	Reserved don't write any value other than reset value.
D6–D4 (1)	2	All values	Revision ID
D3–D0	0	All values	Reserved don't write any value other than reset value.

(1) Read Only Bits…Writing any value to this will not be used anywhere.

Page 0/Register 3: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 0/Register 4: Clock-Gen Muxing(1)

BIT	Reset Value	Values	DESCRIPTION
D7–D4	0	All values	Reserved don't write any value other than reset value.
D3-D2	0	0	PLL_CLKIN = MCLK (Device Pin)
		1	PLL_CLKIN = BCLK (Device Pin)
		2	Reserved. Do not use.
		3	PLL_CLKIN = Logic Level 0
D1-D0	0	0	CODEC_CLKIN = MCLK (Device Pin)
		1	CODEC_CLKIN = BCLK (Device Pin)
		2	Reserved. Do not use.
		3	CODEC_CLKIN = PLL_CLK (Generated On-Chip)

(1) Refer to Sheet "Clock Generation Logic" for more details on clock generation muxing and dividers.

Page 0/Register 5: PLL P and R-VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: PLL is powered down. 1: PLL is powered up.
D6–D4	R/W	010	000: PLL divider P = 8 001: PLL divider P = 1 010: PLL divider P = 2 ... 110: PLL divider P = 6 111: PLL divider P = 7
D3–D0	R/W	0001	0000: PLL multiplier R = 16 0001: PLL multiplier R = 1 0010: PLL multiplier R = 2 ... 1110: PLL multiplier R = 14 1111: PLL multiplier R = 15

Page 0/Register 6: PLL J-VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only zeros to these bits.
D5–D0	R/W	00 1111	00 0000: Don't use (reserved) 00 0001: PLL multiplier J = 1 00 0010: PLL multiplier J = 2 ... 11 1110: PLL multiplier J = 62 11 1110: PLL multiplier J = 63

Page 0/Register 7: PLL D-VAL MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only zeros to these bits.
D5–D0	R/W	00 0000	PLL fractional multiplier D(13:8)

Page 0/Register 8: PLL D-VAL LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	PLL fractional multiplier D(7:0)

Page 0/Registers 9–17: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to these registers.

Page 0/Register 18: ADC NADC_VAL

Bit	Reset Value	Values	Description
D7	0	0	ADC NADC divider is powered down
		1	ADC NADC divider is powered up
D6–D0	1	0	ADC divider NADC = 128
		1	ADC divider NADC = 1
		2	ADC divider NADC = 2
		126	ADC divider NADC = 126
		127	ADC divider NADC = 127

Page 0/Register 19: ADC MADC_VAL

Bit	Reset Value	Values	Description
D7	0	0	ADC MADC divider is powered down
		1	ADC MADC divider is powered up
D6–D0	1	0	ADC divider MADC = 128
		1	ADC divider MADC = 1
		2	ADC divider MADC = 2
		126	ADC divider MADC = 126
		127	ADC divider MADC = 127

Page 0/Register 20: ADC AOSR_VAL

BIT	Reset Value	Values	DESCRIPTION
D7–D0	128	0	ADC OSR AOSR = 256
		1	ADC OSR AOSR = 1
		2	ADC OSR AOSR = 2
		254	ADC OSR AOSR = 254
		255	ADC OSR AOSR = 255

Page 0/Register 21: ADC IADC_VAL

BIT	Reset Value	Values	DESCRIPTION
D7–D0	128	0	Reserved. Do not use.
		1	Number of instruction for ADC MAC Engine, IADC = 2
		2	Number of instruction for ADC MAC Engine, IADC = 4
		191	Number of instruction for ADC MAC Engine, IADC = 382
		192	Number of instruction for ADC MAC Engine, IADC = 384
		193 to 255	Number of instruction for ADC MAC Engine, IADC = Up to 510

Page 0/Register 22: ADC MAC Engine Decimation

BIT	Reset Value	Values	DESCRIPTION
D7–D4	0	All values	Reserved don't write any value other than reset value.
D3–D0	4	0	Decimation Ratio in ADC MAC Engine = 16
		1	Decimation Ratio in ADC MAC Engine = 1
		2	Decimation Ratio in ADC MAC Engine = 2
		13	Decimation Ratio in ADC MAC Engine = 13
		14	Decimation Ratio in ADC MAC Engine = 14
		15	Decimation Ratio in ADC MAC Engine = 15

Page 0/Registers 23–24: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to these registers.

Page 0/Register 25: CLKOUT MUX

BIT	Reset Value	Values	DESCRIPTION
D7–D3	0	All values	Reserved don't write any value other than reset value.
D2-D0	0	0	CDIV_CLKIN = MCLK (Device Pin)
		1	CDIV_CLKIN = BCLK (Device Pin)
		2	Reserved. Do not use.
		3	CDIV_CLKIN = PLL_CLK (Generated On-Chip)
		4	Reserved. Do not use.
		5	Reserved. Do not use.
		6	CDIV_CLKIN = ADC_CLK (Generated On-Chip)
		7	CDIV_CLKIN = ADC_MOD_CLK (Generated On-Chip)

Page 0/Register 26: CLKOUT M_VAL

BIT	Reset Value	Values	DESCRIPTION
D7	0	0	CLKOUT M divider is powered down
		1	CLKOUT M divider is powered up
D6–D0	1	0	CLKOUT divider M = 128
		1	CLKOUT divider M = 1
		2	CLKOUT divider M = 2
		126	CLKOUT divider M = 126
		127	CLKOUT divider M = 127

Page 0/Register 27: ADC Interface Control1

Bit	Reset Value	Values	Description
D7–D6	0	0	ADC Interface = I2S
		1	ADC Interface = DSP
		2	ADC interface = RJF
		3	ADC interface = LJF
D5–D4	0	0	ADC interface word length = 16 bits
		1	ADC interface word length = 20 bits
		2	ADC interface word length = 24 bits
		3	ADC interface word length = 32 bits
D3	0	0	BCLK is Input
		1	BCLK is Output
D2	0	0	WCLK is Input
		1	WCLK is Output
D1	0	All values	Reserved don't write any value other than reset value.
D0	0	0	3-stating of DOUT: Disabled
		1	3-stating of DOUT: Enabled

Page 0/Register 28: Data Slot Offset Programmability 1

Bit	Reset Value	Values	Description
D7–D0	0	0	Offset = 0BCLK's. Offset is measured with respect to WCLK-rising edge in DSP Mode(1)
		1	Offset = 1BCLK's
		2	Offset = 2BCLK's
		254	Offset = 254BCLK's
		255	Offset = 255BCLK's

(1) Usage controlled by Page 0/Register 38 (D0)

Page 0/Register 29: ADC Interface Control2

Bit	Reset Value	Values	Description
D7–D4	0	All values	Reserved don't write any value other than reset value.
D3	0	0	BCLK is not inverted (Valid for both Primary and Secondary BCLK)
		1	BCLK is inverted (Valid for both Primary and Secondary BCLK)
D2	0	0	BCLK and WCLK active even with Codec powered down : Disabled (Valid for both Primary and Secondary BCLK)
		1	BCLK and WCLK active even with Codec powered down : Enabled (Valid for both Primary and Secondary BCLK)
D1–D0	2	0	Reserved. Do not use.
		1	Reserved. Do not use.
		2	BDIV_CLKIN = ADC_CLK (Generated On-Chip)
		3	BDIV_CLKIN = ADC_MOD_CLK (Generated On-Chip)

Page 0/Register 30: BCLK N_VAL

BIT	Reset Value	Values	DESCRIPTION
D7–D0	0	0	BCLK N divider is powered down
		1	BCLK N divider is powered up
D6–D0	1	0	BCLK divider N = 128
		1	BCLK divider N = 1
		2	BCLK divider N = 2
		126	BCLK divider N = 126
		127	BCLK divider N = 127

Page 0/Register 31: CODEC Secondary Interface Control 1

BIT	Reset Value	Values	DESCRIPTION
D7	0	All values	Reserved don't write any value other than reset value.
D6–D5	0	0	Secondary BCLK is obtained from GPIO1 pin
		1	Secondary BCLK is obtained from GPIO2 pin
		2	Reserved. Do not use.
		3	Reserved. Do not use.
D4–D3	0	0	Secondary WCLK is obtained from GPIO1 pin
		1	Secondary WCLK is obtained from GPIO2 pin
		2	Reserved. Do not use.
		3	Reserved. Do not use.
D2–D0	0	All values	Reserved don't write any value other than reset value.

Page 0/Register 32: CODEC Secondary Interface Control 2

BIT	Reset Value	Values	DESCRIPTION
D7–D4	0	All values	Reserved don't write any value other than reset value.
D3	0	0	Primary BCLK is used for Audio Interface and Clocking
		1	Secondary BCLK is used for Audio Interface and Clocking
D2	0	0	Primary WCLK is used for Audio Interface and Clocking
		1	Secondary WCLK is used for Audio Interface and Clocking
D1–D0	0	All values	Reserved don't write any value other than reset value.

Page 0/Register 33: CODEC Secondary Interface Control 3

BIT	Reset Value	Values	DESCRIPTION
D7	0	0	Primary BCLK Output = Internally generated BCLK Clock
		1	Primary BCLK Output = Secondary BCLK
D6	0	0	Secondary BCLK Output = Primary BCLK
		1	Secondary BCLK Output = Internally generated BCLK Clock
D5–D4	0	0	Reserved. Do not use.
		1	Primary WCLK Output = Internally generated ADC_FS Clock
		2	Primary WCLK Output = Secondary WCLK
		3	Reserved. Do not use.
D3–D2	0	0	Secondary WCLK Output = Primary WCLK
		1	Reserved. Do not use.
		2	Secondary WCLK Output = Internally generated ADC_FS Clock
		3	Reserved. Do not use.
D2–D0	0	All values	Reserved don't write any value other than reset value.

Page 0/Register 34: I2S Sync

Bit	Reset Value	Values	Description
D7	0	0	Internal logic is enabled to detect the I2C hang and react accordingly.
		1	Internal logic is disabled to detect the I2C hang.
D6(1)	0	0	I2C hang is not detected.
		1	I2C hang detected flag. Once set get cleared only after reading this register.
D5	0	0	I2C general call address will be ignored.
		1	Device will accept I2C general call address.
D4	0	All values	Reserved don't write any value other than reset value.
D3	0	All values	Reserved don't write any value other than reset value.
D2	0	All values	Reserved don't write any value other than reset value.
D1	0	0	Re-sync logic is Disabled for ADC
		1	Re-Sync Stereo ADC with Codec Interface if the group delay changed by more than ±ADCFS/4.
D0	0	0	Re-Sync is done without soft-muting the channel for ADC
		1	Re-Sync is done by internally soft-muting the channel for ADC

(1) Read Only Bits...Writing any value to this will not be used anywhere.

Page 0/Register 35: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 0/Register 36: ADC Flag Register

Bit	Reset Value	Values	Description
D7(1)	0	0	Left ADC PGA , Applied Gain not = Programmed Gain
		1	Left ADC PGA , Applied Gain = Programmed Gain
D6(1)	0	0	Left ADC Powered Down
		1	Left ADC Powered Up
D5(2)	0	0	Left AGC not Saturated
		1	Left AGC Applied Gain = Maximum Applicable Gain by Left AGC
D4	0	All values	Reserved don't write any value other than reset value.
D3(1)	0	0	Right ADC PGA , Applied Gain not = Programmed Gain
		1	Right ADC PGA , Applied Gain = Programmed Gain
D2(1)	0	0	Right ADC Powered Down
		1	Right ADC Powered Up
D1(2)	0	0	Right AGC not Saturated
		1	Right AGC Applied Gain = Maximum Applicable Gain by Right AGC
D0	0	All values	Reserved don't write any value other than reset value.

(1) Read Only Bits…Writing any value to this will not be get used anywhere.
(2) Sticky Flag BIts....These are read-only bits. They are automatically cleared once they are read and are set only if the source trigger occurs freshly again.

Page 0/Register 37: Data Slot Offset Programmability 2

Bit	Reset Value	Values	Description
D7–D0	0	0	Offset = 0BCLK's. Offset is measured with respect to the end of the first channel(1)
		1	Offset = 1BCLK's
		2	Offset = 2BCLK's
		254	Offset = 254BCLK's
		255	Offset = 255BCLK's

(1) Usage controlled by Page 0/Register 38 (D0) time_slot_mode_enable

Page 0/Register 38: I2S TDM Control Register

Bit	Reset Value	Values	Description
D7–D5	0	All values	Reserved don't write any value other than reset value.
D4	0	0	Channel Swap Disabled.
		1	Channel Swap Enabled.
D3–D2	0	0	Both left and right channels enabled
		1	Left channel enabled
		2	Right channel enabled
		3	Both left and right channels disabled
D1	1	0	early_3-state disabled
		1	early_3-state enabled
D0	0	0	time_slot_mode disabled (Both Channels offset controlled by Page 0/Register 28)
		1	time_slot_mode enabled (Channel 1 offset controlled by Page 0/Register 28 and Channel 2 offset controlled by Page 0/Register 37)

Page 0/Registers 39–41: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to these registers.

Page 0/Register 42: Interrupt Flags (Overflow)

Bit	Reset Value	Values	Description
D7–D4	0		Reserved.
D3(1)	0		Left ADC Overflow Flag
D2(1)	0		Right ADC Overflow Flag
D1(1)	0		ADC Barrel Shifter Output Overflow Flag
D0	0		Reserved.

(1) Sticky Flag BIts....These are read-only bits. They are automatically cleared once they are read and are set only if the source trigger occurs freshly again.

Page 0/Register 43: Interrupt Flags (Overflow)

Bit	Reset Value	Values	Description
D7–D4	0		Reserved.
D3	0		Left ADC Overflow Flag
D2	0		Right ADC Overflow Flag
D1	0		ADC Barrel Shifter Output Overflow Flag
D0	0		Reserved.

Page 0/Registers 44: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 0/Register 45: Interrupt Flags—ADC

Bit	Reset Value	Values	Description(1)
D7	0		Reserved.
D6	0	0	Left ADC Signal Power Greater than Noise Threshold for Left AGC.
		1	Left ADC Signal Power Lesser than Noise Threshold for Left AGC.
D5	0	0	Right ADC Signal Power Greater than Noise Threshold for Right AGC.
		1	Right ADC Signal Power Lesser than Noise Threshold for Right AGC.
D4	0		ADC MAC Engine Standard Interrupt Port Output
D3	0		ADC MAC Engine Auxilliary Interrupt Port Output
D2 - D0	0		Reserved.

(1) Sticky Flag BIts....These are read-only bits. They are automatically cleared once they are read and are set only if the source trigger occurs freshly again.

Page 0/Register 46: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 0/Register 47: Interrupt Flags—ADC

Bit	Reset Value	Values	Description
D7	0		Reserved.
D6	0	0	Left ADC Signal Power Greater than Noise Threshold for Left AGC.
		1	Left ADC Signal Power Lesser than Noise Threshold for Left AGC.
D5	0	0	Right ADC Signal Power Greater than Noise Threshold for Right AGC.
		1	Right ADC Signal Power Lesser than Noise Threshold for Right AGC.
D4	0	0	ADC MAC Engine Standard Interrupt Port Output
D3	0	0	ADC MAC Engine Auxilliary Interrupt Port Output
D2 - D0	0		Reserved.

Page 0/Register 48: INT1 Interrupt Control

Bit	Reset Value	Values	Description
D7–D5	0	All values	Reserved don't write any value other than reset value.
D4	0	0	ADC AGC Noise Interrupt is not used in the generation of INT1 Interrupt
		1	ADC AGC Noise Interrupt is used in the generation of INT1 Interrupt
D3	0	All values	Reserved don't write any value other than reset value.
D2	0	0	Engine generated Interrupts and Overflow Flags are not used in the generation of INT1 Interrupt
		1	Engine generated Interrupts and Overflow Flags are used in the generation of INT1 Interrupt
D1	0	0	ADC Data-Available Interrupt is not used in the generation of INT1 Interrupt
		1	ADC Data-Available Interrupt is used in the generation of INT1 Interrupt
D0	0	0	INT1 will be only one pulse(active high) of duration typical 2ms
		1	INT1 will be multiple pulses(active high) of duration typical 2ms and period 4ms, untill the flag register 42 or 45 is read by the USER

Page 0/Register 49: INT2 Interrupt Control

Bit	Reset Value	Values	Description
D7–D5	0	All values	Reserved don't write any value other than reset value.
D4	0	0	ADC AGC Noise Interrupt is not used in the generation of INT2 Interrupt
		1	ADC AGC Noise Interrupt is used in the generation of INT2 Interrupt
D3	0	All values	Reserved don't write any value other than reset value.
D2	0	0	Engine generated Interrupts and Overflow Flags are not used in the generation of INT2 Interrupt
		1	Engine generated Interrupts and Overflow Flags are used in the generation of INT2 Interrupt
D1	0	0	ADC Data-Available Interrupt is not used in the generation of INT2 Interrupt
		1	ADC Data-Available Interrupt is used in the generation of INT2 Interrupt
D0	0	0	INT2 will be only one pulse(active high) of duration typical 2ms
		1	INT2 will be multiple pulses(active high) of duration typical 2ms and period 4ms, untill the flag register 42 or 45 is read by the USER

Page 0/Register 50: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 0/Register 51: DMCLK/GPIO2 Control

Bit	Reset Value	Values	Description
D7–D6	0	All values	Reserved don't write any value other than reset value.
D5–D2	0	0	DMCLK Disabled (Input and Output buffers powered down)
		1	DMCLK is in Input mode (can be used as Secondary BCLK input ,Secondary WCLK input, Dig_Mic_In or in ClockGen Block)
		2	DMCLK is used as General Purpose Input (GPI)
		3	DMCLK Output = General Purpose Output
		4	DMCLK Output = CLKOUT Output (source determined by cdiv_clkin_reg; Page 0 Register 25)
		5	DMCLK Output = INT1 Output
		6	DMCLK Output = INT2 Output
		7	Reserved. Do not use.
		8	DMCLK Output = Secondary BCLK Output for CODEC Interface
		9	DMCLK Output = Secondary WCLK Output for CODEC Interface
		10	DMCLK Output = ADC_MOD_CLK Output for the digital microphone
		11 to 15	Reserved. Do not use.
D1	0		DMCLK Input Buffer Value
D0	0	0	DMCLK Value = 0 when D5-D2 is programmed to 3
		1	DMCLK Value = 1 when D5-D2 is programmed to 3

Page 0/Register 52: DMDIN/GPIO1 Control

Bit	Reset Value	Values	Description
D7–D6	0	All values	Reserved don't write any value other than reset value.
D5–D2	0	0	DMDIN Disabled (Input and Output buffers powered down)
		1	DMDIN is in Input mode (can be used as Secondary BCLK input ,Secondary WCLK input, Dig_Mic_In or in ClockGen Block)
		2	DMDIN is used as General Purpose Input (GPI)
		3	DMDIN Output = General Purpose Output
		4	DMDIN Output = CLKOUT Output (source determined by cdiv_clkin_reg; Page 0 Register 25)
		5	DMDIN Output = INT1 Output
		6	DMDIN Output = INT2 Output
		7	Reserved. Do not use.
		8	DMDIN Output = Secondary BCLK Output for CODEC Interface
		9	DMDIN Output = Secondary WCLK Output for CODEC Interface
		10	DMDIN Output = ADC_MOD_CLK Output for the digital microphone
		11 to 15	Reserved. Do not use.
D1	0		DMDIN Input Buffer Value
D0	0	0	DMDIN Value = 0 when D5-D2 is programmed to 3
		1	DMDIN Value = 1 when D5-D2 is programmed to 3

Page 0/Register 53: DOUT (OUT Pin) Control

Bit	Reset Value	Values	Description
D7–D5	0	All values	Reserved don't write any value other than reset value.
D4	1	0	DOUT Bus Keeper Enabled
		1	DOUT Bus Keeper Disabled
D3–D1	1	0	DOUT Disabled (Output buffer powered down)
		1	DOUT = Primary DOUT Output for CODEC Interface
		2	DOUT = General Purpose Output
		3	DOUT = CLKOUT Output
		4	DOUT = INT1 Output
		5	DOUT = INT2 Output
		6	DOUT = Secondary BCLK Output for CODEC Interface
		7	DOUT = Secondary WCLK Output for CODEC Interface
D0	0	0	DOUT Value = 0 when D3-D1 is programmed to 2
		1	DOUT Value = 1 when D3-D1 is programmed to 2

Page 0/Register 54 – 56: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write

Page 0/Register 57: ADC Sync Control 1

Bit	Reset Value	Values	Description
D7	0	0	Default Synchronization
		1	Custom Synchronization
D6–D0	0	0	Custom Synchronization Window Size = 0 instructions
		1	Custom Synchronization Window Size = 2 instructions (+/- 1 instruction)
		2	Custom Synchronization Window Size = 4 instructions (+/- 2 instructions)
		127	Custom Synchronization Window Size = 254 instructions (+/- 127 instructions)

Page 0/Register 58: ADC Sync Control 2

Bit	Reset Value	Values	Description
D7–D0	0	0	Custom Synchronization Target = instruction 0
		1	Custom Synchronization Target = instruction 2
		2	Custom Synchronization Target = instruction 4
		255	Custom Synchronization Target = instruction 510

Page 0/Register 59: ADC CIC Filter Gain Control(1)

Bit	Reset Value	Values	Description
D7–D4	4	See note below	Left CIC Filter Gain
D3–D0	4	See note below	Right CIC Filter Gain

(1) For proper operation, CIC gain must be ≤ 1.
If AOSR {Page 0; Reg 20} = 64 and (1 ≤ Filter Mode {Page 0; Reg 61} ≤ 6), then the reset value of 4 results in CIC gain = 1.
Otherwise, the CIC gain = $(AOSR/ (64 \times MAC\ Engine\ Decimation))^4 \times 2^{(CIC\ Filter\ Gain\ Control)}$ for 0 ≤ CIC Filter Gain Control ≤ 12, and if CIC Filter Gain Control = 15, CIC gain is automatically set such that for 7 ≤ (AOSR/MAC Engine Decimation) ≤ 64, 0.5 < CIC gain ≤ 1.

Page 0/Register 60: Reserved

Bit	Reset Value	Values	Description
D7–D0	0	All values	Reserved don't write to this register.

Page 0/Register 61: ADC Instruction Set

Bit	Reset Value	Values	Description
D7–D5	0	All values	Reserved don't write any value other than reset value.
D4–D0	1	0	ADC Programmable Instruction Mode Enabled.
		1	Default Instruction Set for Stereo-ADC with 4x-Decimation + 1-Programmable First Order IIR per channel
		2	Default Instruction Set for Stereo-ADC with 4x-Decimation + 1-Programmable First Order IIR per channel + 5-Programmable Biquads per channel
		3	Default Instruction Set for Stereo-ADC with 4x-Decimation + 1-Programmable First Order IIR per channel +25-tap Programmable FIR(Adaptive) per channel
		4	Default Instruction Set for Mono-ADC with 4x-Decimation + 1-Programmable First Order IIR per channel
		5	Default Instruction Set for Mono-ADC with 4x-Decimation + 1-Programmable First Order IIR per channel + 5-Programmable Biquads per channel
		6	Default Instruction Set for Mono-ADC with 4x-Decimation + 1-Programmable First Order IIR per channel +25-tap Programmable FIR(Adaptive) per channel
		7	Default Instruction Set for Stereo-ADC with 2x-Decimation + 1-Programmable First Order IIR per channel
		8	Default Instruction Set for Stereo-ADC with 2x-Decimation + 1-Programmable First Order IIR + 3-Programmable Biquads(Adaptive) per channel
		9	Default Instruction Set for Stereo-ADC with 2x-Decimation + 1-Programmable First Order IIR +20-tap Programmable FIR(Adaptive) per channel
		10	Default Instruction Set for Mono-ADC with 2x-Decimation + 1-Programmable First Order IIR per channel
		11	Default Instruction Set for Mono-ADC with 2x-Decimation + 1-Programmable First Order IIR + 3-Programmable Biquads(Adaptive) per channel
		12	Default Instruction Set for Mono-ADC with 2x-Decimation + 1-Programmable First Order IIR +20-tap Programmable FIR(Adaptive) per channel
		13	Default Instruction Set for Stereo-ADC with no Decimation + 1-Programmable First Order IIR per channel
		14	Default Instruction Set for Stereo-ADC with no Decimation + 1-Programmable First Order IIR + 5-Programmable Biquads(Adaptive) per channel
		15	Default Instruction Set for Stereo-ADC with no Decimation + 1-Programmable First Order IIR +25-tap Programmable FIR(Adaptive) per channel
		16	Default Instruction Set for Mono-ADC with no Decimation + 1-Programmable First Order IIR per channel
		17	Default Instruction Set for Mono-ADC with no Decimation + 1-Programmable First Order IIR + 5-Programmable Biquads(Adaptive) per channel
		18	Default Instruction Set for Mono-ADC with no Decimation + 1-Programmable First Order IIR +25-tap Programmable FIR(Adaptive) per channel
		19 to 31	Reserved. Do not use.

Page 0/Register 62: Programmable Instruction Mode Control bits

Bit	Reset Value	Values	Description
D7	0	All values	Reserved don't write any value other than reset value.
D6	0	0	ADC MAC Engine Auxilliary Control bit A, which can be used for conditional instructions like JMP
D5	0	0	ADC MAC Engine Auxilliary Control bit B, which can be used for conditional instructions like JMP
D4	0	0	ADC Instructions counter reset at the start of the new frame is enabled.
		1	ADC Instructions counter reset at the start of the new frame is disabled.
D3–D0	0	All values	Reserved don't write any value other than reset value.

Page 0/Register 63–79: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to these registers.

Page 0/Register 80: ADC Digital Microphone Polarity Select

Bit	Reset Value	Values	Description
D7–D2	0	All values	Reserved don't write any value other than reset value.
D1	0	0	Capture Left Channel Digital Microphone data on rising edge of ADC Modulator Clock.
		1	Capture Left Channel Digital Microphone data on falling edge of ADC Modulator Clock.
D0	0	0	Capture Right Channel Digital Microphone data on rising edge of ADC Modulator Clock.
		1	Capture Right Channel Digital Microphone data on falling edge of ADC Modulator Clock.

Page 0/Register 81: ADC Digital

Bit	Reset Value	Values	Description
D7	0	0	Left-channel ADC is powered down.
		1	Left-channel ADC is powered up.
D6	0	0	Right-channel ADC is powered down.
		1	Right-channel ADC is powered up.
D5	0	0	Left Channel Digital Microphone Input is obtained from DMDIN pin
		1	Left Channel Digital Microphone Input is obtained from DMCLK pin
D4	0	0	Right Channel Digital Microphone Input is obtained from DMDIN pin
		1	Right Channel Digital Microphone Input is obtained from DMCLK pin
D3	0	0	Digital Microphone is not Enabled for Left ADC Channel
		1	Digital Microphone is Enabled for Left ADC Channel
D2	0	0	Digital Microphone is not Enabled for Right ADC Channel
		1	Digital Microphone is Enabled for Right ADC Channel
D1–D0	0	0	ADC channel volume control soft-stepping is enabled for one-step/Fs
		1	ADC channel volume control soft-stepping is enabled for one-step/2Fs
		2	ADC channel volume control soft-stepping is disabled
		3	Reserved. Do not use.

Page 0/Register 82: ADC Volume Control

Bit	Reset Value	Values	Description
D7	1	0	Left ADC Channel not Muted
		1	Left ADC Channel Muted
D6–D4	0	0	Left ADC Channel Fine Gain = 0 dB
		-1	Left ADC Channel Fine Gain = -0.1 dB
		-2	Left ADC Channel Fine Gain = -0.2 dB
		-3	Left ADC Channel Fine Gain = -0.3 dB
		-4	Left ADC Channel Fine Gain = -0.4 dB
		others	Reserved. Do not use.
D3	1	0	Right ADC Channel not Muted
		1	Right ADC Channel Muted
D2–D0	0	0	Right ADC Channel Fine Gain = 0 dB
		-1	Right ADC Channel Fine Gain = -0.1 dB
		-2	Right ADC Channel Fine Gain = -0.2 dB
		-3	Right ADC Channel Fine Gain = -0.3 dB
		-4	Right ADC Channel Fine Gain = -0.4 dB
		others	Reserved. Do not use.

Page 0/Register 83: Left ADC Volume Control

Bit	Reset Value	Values(1)	Description
D7	0	All values	Reserved don't write any value other than reset value.
D6–D0	0	-64 to -25	Left ADC Channel Gain = 0dB
		-24	Left ADC Channel Gain = -12dB
		-23	Left ADC Channel Gain = -11.5dB
		39	Left ADC Channel Gain = 19.5dB
		40	Left ADC Channel Gain = 20dB
		41 to 63	Reserved. Do not use.

(1) Values in 2s complement decimal format

Page 0/Register 84: Right ADC Volume Control

Bit	Reset Value	Values(1)	Description
D7	0	All values	Reserved don't write any value other than reset value.
D6–D0	0	-64 to -25	Right ADC Channel Gain = 0dB
		-24	Right ADC Channel Gain = -12dB
		-23	Right ADC Channel Gain = -11.5dB
		39	Right ADC Channel Gain = 19.5dB
		40	Right ADC Channel Gain = 20dB
		41 to 63	Reserved. Do not use.

(1) Values in 2s complement decimal format

Page 0/Register 85: Left ADC Phase Compensation

Bit	Reset Value	Values	Description
D7–D6	0	-128	Left ADC has a phase shift of -128 ADC_MOD_CLK cycles with respect to Right ADC
		-127	Left ADC has a phase shift of -127 ADC_MOD_CLK cycles with respect to Right ADC
		...	...
		-2	Left ADC has a phase shift of -2 ADC_MOD_CLK cycles with respect to Right ADC
		-1	Left ADC has a phase shift of -1 ADC_MOD_CLK cycles with respect to Right ADC
		0	No phase shift between stereo ADC channel.
		1	Left ADC has a phase shift of 1 ADC_MOD_CLK cycles with respect to Right ADC
		2	Left ADC has a phase shift of 2 ADC_MOD_CLK cycles with respect to Right ADC
		...	...
		126	Left ADC has a phase shift of 126 ADC_MOD_CLK cycles with respect to Right ADC
		127	Left ADC has a phase shift of 127 ADC_MOD_CLK cycles with respect to Right ADC

Page 0/Register 86: Left AGC Control 1

Bit	Reset Value	Values	Description
D7	0	0	Left AGC Disabled
		1	Left AGC Enabled
D6–D4(1)	0	0	Left AGC Target Level = –5.5dB
		1	Left AGC Target Level = –8dB
		2	Left AGC Target Level = –10dB
		3	Left AGC Target Level = –12dB
		4	Left AGC Target Level = –14dB
		5	Left AGC Target Level = –17dB
		6	Left AGC Target Level = –20dB
		7	Left AGC Target Level = –24dB
D3–D0	0	All values	Reserved don't write any value other than reset value.

(1) Values are approximate and their actual values have to be characterized.

Page 0/Register 87: Left AGC Control 2

Bit	Reset Value	Values	Description
D7–D6	0	0	Left AGC hysteresis Setting of 1dB
		1	Left AGC Hysteresis Setting of 2dB
		2	Left AGC Hysteresis Setting of 4dB
		3	Left AGC Hysteresis Disabled
D5–D1	0	0	Left AGC Noise/Silence detection is Disabled.
		1	Left AGC Noise Threshold = –30dB
		2	Left AGC Noise Threshold = –32dB
		3	Left AGC Noise Threshold = –34dB
		29	Left AGC Noise Threshold = –86dB
		30	Left AGC Noise Threshold = –88dB
		31	Left AGC Noise Threshold = –90dB
D0	0	0	Disable Clip Stepping for AGC
		1	Enable Clip Stepping for AGC

Page 0/Register 88: Left AGC Maximum Gain

Bit	Reset Value	Values	Description
D7	0	All values	Reserved don't write any value other than reset value.
D6–D0	127	0	Left AGC Max Gain=0.0dB
		1	Left AGC Max Gain=0.5dB
		2	Left AGC Max Gain=1.0dB
		80	Left AGC Max Gain=40.0dB

Page 0/Register 89: Left AGC Attack Time

Bit	Reset Value	Values	Description
D7–D3	0	0	Left AGC Attack Time=1 × (32/Fs)
		1	Left AGC Attack Time=3 × (32/Fs)
		2	Left AGC Attack Time=5 × (32/Fs)
		3	Left AGC Attack Time=7 × (32/Fs)
		4	Left AGC Attack Time=9 × (32/Fs)
		30	Left AGC Attack Time=61 × (32/Fs)
		31	Left AGC Attack Time=63 × (32/Fs)
D2–D0	0	0	Multiply factor for the programmed Left AGC Attack Time = 1
		1	Multiply factor for the programmed Left AGC Attack Time = 2
		2	Multiply factor for the programmed Left AGC Attack Time = 4
		7	Multiply factor for the programmed Left AGC Attack Time = 128

Page 0/Register 90: Left AGC Decay Time

Bit	Reset Value	Values	Description
D7–D3	0	0	Left AGC Decay Time=1 × (512/Fs)
		1	Left AGC Decay Time=3 × (512/Fs)
		2	Left AGC Decay Time=5 × (512/Fs)
		3	Left AGC Decay Time=7 × (512/Fs)
		4	Left AGC Decay Time=9 × (512/Fs)
		30	Left AGC Decay Time=61 × (512/Fs)
		31	Left AGC Decay Time=63 × (512/Fs)
D2–D0	0	0	Multiply factor for the programmed Left AGC Decay Time = 1
		1	Multiply factor for the programmed Left AGC Decay Time = 2
		2	Multiply factor for the programmed Left AGC Decay Time = 4
		7	Multiply factor for the programmed Left AGC Decay Time = 128

Page 0/Register 91: Left AGC Noise Debounce

Bit	Reset Value	Values	Description
D7–D5	0	All values	Reserved don't write any value other than reset value.
D4–D0	0	0	Left AGC Noise Debounce = 0/Fs
		1	Left AGC Noise Debounce = 4/Fs
		2	Left AGC Noise Debounce = 8/Fs
		3	Left AGC Noise Debounce = 16/Fs
		4	Left AGC Noise Debounce = 32/Fs
		5	Left AGC Noise Debounce = 64/Fs
		6	Left AGC Noise Debounce = 128/Fs
		7	Left AGC Noise Debounce = 256/Fs
		8	Left AGC Noise Debounce = 512/Fs
		9	Left AGC Noise Debounce = 1024/Fs
		10	Left AGC Noise Debounce = 2048/Fs
		11	Left AGC Noise Debounce = 4096/Fs
		12	Left AGC Noise Debounce = 2 × 4096/Fs
		13	Left AGC Noise Debounce = 3 × 4096/Fs
		14	Left AGC Noise Debounce = 4 × 4096/Fs
		30	Left AGC Noise Debounce = 20 × 4096/Fs
		31	Left AGC Noise Debounce = 21 × 4096/Fs

Page0 /Register 92: Left AGC Signal Debounce

Bit	Reset Value	Values	Description
D7–D4	0	All values	Reserved don't write any value other than reset value.
D3–D0	0	0	Left AGC Signal Debounce = 0/Fs
		1	Left AGC Signal Debounce = 4/Fs
		2	Left AGC Signal Debounce = 8/Fs
		3	Left AGC Signal Debounce = 16/Fs
		4	Left AGC Signal Debounce = 32/Fs
		5	Left AGC Signal Debounce = 64/Fs
		6	Left AGC Signal Debounce = 128/Fs
		7	Left AGC Signal Debounce = 256/Fs
		8	Left AGC Signal Debounce = 512/Fs
		9	Left AGC Signal Debounce = 1024/Fs
		10	Left AGC Signal Debounce = 2048/Fs
		11	Left AGC Signal Debounce = 2 × 2048/Fs
		12	Left AGC Signal Debounce = 3 × 2048/Fs
		13	Left AGC Signal Debounce = 4 × 2048/Fs
		14	Left AGC Signal Debounce = 5 × 2048/Fs
		15	Left AGC Signal Debounce = 6 × 2048/Fs

Page 0/Register 93: Left AGC Gain Applied

Bit(1)	Reset Value	Values	Description
D7–D0	0	–24	Gain Applied by Left AGC= –12.0dB
		–23	Gain Applied by Left AGC= –11.5dB
		0	Gain Applied by Left AGC=0.0dB
		80	Gain Applied by Left AGC=40.0dB

(1) These are read-only bits.

Page 0/Register 94: Right AGC Control 1

Bit	Reset Value	Values	Description
D7	0	0	Right AGC Disabled
		1	Right AGC Enabled
D6–D4(1)	0	0	Right AGC Target Level = -5.5dB
		1	Right AGC Target Level = -8dB
		2	Right AGC Target Level = -10dB
		3	Right AGC Target Level = -12dB
		4	Right AGC Target Level = -14dB
		5	Right AGC Target Level = -17dB
		6	Right AGC Target Level = -20dB
		7	Right AGC Target Level = -24dB
D3–D0	0	All values	Reserved don't write any value other than reset value.

(1) Values are approximate and their actual values have to be characterized.

Page 0/Register 95: Right AGC Control 2

Bit	Reset Value	Values(1)	Description
D7–D6	0	0	Right AGC Hysteresis Setting of 1dB
		1	Right AGC Hysteresis Setting of 2dB
		2	Right AGC Hysteresis Setting of 4dB
		3	Right AGC Hysteresis Disabled
D5–D1	0	0	Right AGC Noise/Silence detection is Disabled.
		1	Right AGC Noise Threshold = -30dB
		2	Right AGC Noise Threshold = -32dB
		3	Right AGC Noise Threshold = -34dB
		29	Right AGC Noise Threshold = -86dB
		30	Right AGC Noise Threshold = -88dB
		31	Right AGC Noise Threshold = -90dB
D0	0	1	Disable Clip Stepping for Right AGC
		2	Enable Clip Stepping for Right AGC

(1) Values in 2s complement decimal format

Page 0/Register 96: Right AGC Maximum Gain

Bit	Reset Value	Values	Description
D7	0	All values	Reserved don't write any value other than reset value.
D6–D0	127	0	Right AGC Max Gain=0.0dB
		1	Right AGC Max Gain=0.5dB
		2	Right AGC Max Gain=1.0dB
		80	Right AGC Max Gain=40.0dB

Page 0/Register 97: Right AGC Attack Time

Bit	Reset Value	Values	Description
D7–D3	0	0	Right AGC Attack Time=1 × (32/Fs)
		1	Right AGC Attack Time=3 × (32/Fs)
		2	Right AGC Attack Time=5 × (32/Fs)
		3	Right AGC Attack Time=7 × (32/Fs)
		4	Right AGC Attack Time=9 × (32/Fs)
		30	Right AGC Attack Time=61 × (32/Fs)
		31	Right AGC Attack Time=63 × (32/Fs)
D2–D0	0	0	Multiply factor for the programmed Right AGC Attack Time = 1
		1	Multiply factor for the programmed Right AGC Attack Time = 2
		2	Multiply factor for the programmed Right AGC Attack Time = 4
		7	Multiply factor for the programmed Right AGC Attack Time = 128

Page 0/Register 98: Right AGC Decay Time

Bit	Reset Value	Values	Description
D7–D3	0	0	Right AGC Decay Time=1 × (512/Fs)
		1	Right AGC Decay Time=3 × (512/Fs)
		2	Right AGC Decay Time=5 × (512/Fs)
		3	Right AGC Decay Time=7 × (512/Fs)
		4	Right AGC Decay Time=9 × (512/Fs)
		30	Right AGC Decay Time=61 × (512/Fs)
		31	Right AGC Decay Time=63 × (512/Fs)
D2–D0	0	0	Multiply factor for the programmed Right AGC Decay Time = 1
		1	Multiply factor for the programmed Right AGC Decay Time = 2
		2	Multiply factor for the programmed Right AGC Decay Time = 4
		7	Multiply factor for the programmed Right AGC Decay Time = 128

Page 0/Register 99: Right AGC Noise Debounce

Bit	Reset Value	Values	Description
D7–D5	0	All values	Reserved don't write any value other than reset value.
D4–D0	0	0	Right AGC Noise Debounce = 0/Fs
		1	Right AGC Noise Debounce = 4/Fs
		2	Right AGC Noise Debounce = 8/Fs
		3	Right AGC Noise Debounce = 16/Fs
		4	Right AGC Noise Debounce = 32/Fs
		5	Right AGC Noise Debounce = 64/Fs
		6	Right AGC Noise Debounce = 128/Fs
		7	Right AGC Noise Debounce = 256/Fs
		8	Right AGC Noise Debounce = 512/Fs
		9	Right AGC Noise Debounce = 1024/Fs
		10	Right AGC Noise Debounce = 2048/Fs
		11	Right AGC Noise Debounce = 4096/Fs
		12	Right AGC Noise Debounce = 2 × 4096/Fs
		13	Right AGC Noise Debounce = 3 × 4096/Fs
		14	Right AGC Noise Debounce = 4 × 4096/Fs
		30	Right AGC Noise Debounce = 20 × 4096/Fs
		31	Right AGC Noise Debounce = 21 × 4096/Fs

Page0 /Register 100: Right AGC Signal Debounce

Bit	Reset Value	Values	Description
D7–D4	0	All values	Reserved don't write any value other than reset value.
D3–D0	0	0	Right AGC Signal Debounce = 0/Fs
		1	Right AGC Signal Debounce = 4/Fs
		2	Right AGC Signal Debounce = 8/Fs
		3	Right AGC Signal Debounce = 16/Fs
		4	Right AGC Signal Debounce = 32/Fs
		5	Right AGC Signal Debounce = 64/Fs
		6	Right AGC Signal Debounce = 128/Fs
		7	Right AGC Signal Debounce = 256/Fs
		8	Right AGC Signal Debounce = 512/Fs
		9	Right AGC Signal Debounce = 1024/Fs
		10	Right AGC Signal Debounce = 2048/Fs
		11	Right AGC Signal Debounce = 2 × 2048/Fs
		12	Right AGC Signal Debounce = 3 × 2048/Fs
		13	Right AGC Signal Debounce = 4 × 2048/Fs
		14	Right AGC Signal Debounce = 5 × 2048/Fs
		15	Right AGC Signal Debounce = 6 × 2048/Fs

Page 0/Register 101: Right AGC Gain Applied

Bit(1)	Reset Value	Values	Description
D7–D0	0	–24	Gain Applied by Right AGC= –12.0dB
		–23	Gain Applied by Right AGC= –11.5dB
		0	Gain Applied by Right AGC=0.0dB
		80	Gain Applied by Right AGC=40.0dB

(1) These are read-only bits.

Page 0/Registers 102–127: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to these registers.

CONTROL REGISTERS Page1: ADC Routing, PGA, Power-Controls and MISC Logic Related Programmabilities

Page 1/Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0	Valid pages are 0,1,4, 94, and 95

Page 1/Registers 1–25: Reserved

Bit	Reset Value	Values	Description
D7–D4	X	All values	Reserved don't write to these registers.

Page 1/Registers 26: Dither Control

Bit	Reset Value	Values	Description
D7–D4	0		DC Offset into input of Left ADC; signed magnitude number offering +/-15mV steps
		-7	-105 mV
		...	...
		-3	-60 mV
		-2	-30 mV
		-1	-15 mV
		0	0 mV
		1	15 mV
		2	30 mV
		3	60 mV
		....	....
		7	105 mV
D3-D0	0		DC Offset into input of Right ADC; signed magnitude number offering +/-15mV steps
		-7	-105 mV
		...	...
		-3	-60 mV
		-2	-30 mV
		-1	-15 mV
		0	0 mV
		1	15 mV
		2	30 mV
		3	60 mV
		....	....
		7	105 mV

Page 1/Registers 27–50: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to these registers.

Page 1/Register 51: MICBIAS Control

Bit	Reset Value	Values	Description
D7	0	All values	Reserved don't write any value other than the reset value.
D6 – D5	0	0	MICBIAS1 is powered down.
		1	MICBIAS1 is powered to 2.0V.
		2	MICBIAS1 is powered to 2.5V.
		3	MICBIAS1 is connected to AVDD.
D4 – D3	0	0	MICBIAS2 is powered down.
		1	MICBIAS2 is powered to 2.0V.
		2	MICBIAS2 is powered to 2.5V.
		3	MICBIAS2 is connected to AVDD.
D2–D0	0	All values	Reserved don't write any value other than the reset value.

Page 1/Register 52: Left ADC Input selection for Left PGA

Bit	Reset Value	Values	Description(1)
D7–D6	3		LCH_SEL4; Differential Pair using the IN2L(P) as PLUS and IN3L(M) as MINUS inputs.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Left ADC PGA.
		3	Is not connected to the Left ADC PGA.
D5–D4	3		LCH_SEL3; Used for the IN3L(M) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Left ADC PGA.
		3	Is not connected to the Left ADC PGA.
D3–D2	3		LCH_SEL2; Used for the IN2L(P) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Left ADC PGA.
		3	Is not connected to the Left ADC PGA.
D1–D0	3		LCH_SEL1; Used for the IN1L(P) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Left ADC PGA.
		3	Is not connected to the Left ADC PGA.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs will have a 2X gain applied.

Page 1/Registers 53: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 1/Register 54: Left ADC Input selection for Left PGA

Bit	Reset Value	Values	Description(1)
D7	0	0	Don't Bypass Left PGA.
		1	Bypass Left PGA, Unbuffered Differential Pair using the IN2L(P) as PLUS and IN3L(M) as MINUS inputs.
D6	0		LCH_SELCM
		0	Left ADC channel unselected inputs are not biased weakly to the ADC common-mode voltage.
		1	Left ADC channel unselected inputs are biased weakly to the ADC common-mode voltage.
D5–D4	3		LCH_SEL3X; Differential Pair using the IN1L(P) as PLUS and IN1R(M) as MINUS inputs.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Left ADC PGA.
		3	Is not connected to the Left ADC PGA.
D3–D2	3		LCH_SEL2X; Differential Pair using the IN2R(P) as PLUS and IN3R(M) as MINUS inputs.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Left ADC PGA.
		3	Is not connected to the Left ADC PGA.
D1–D0	3		LCH_SEL1X; Used for the IN1R(M) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Left ADC PGA.
		3	Is not connected to the Left ADC PGA.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs will have a 2X gain applied.

Page 1/Register 55: Right ADC Input selection for Right PGA

Bit	Reset Value	Values	Description(1)
D7–D6	3		RCH_SEL4; Differential Pair using the IN2R(P) as PLUS and IN3R(M) as MINUS inputs.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Right ADC PGA.
		3	Is not connected to the Right ADC PGA.
D5–D4	3		RCH_SEL3; Used for the IN3R(M) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Right ADC PGA.
		3	Is not connected to the Right ADC PGA.
D3–D2	3		RCH_SEL2; Used for the IN2R(P) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Right ADC PGA.
		3	Is not connected to the Right ADC PGA.
D1–D0	3		RCH_SEL1; Used for the IN1R(M) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Right ADC PGA.
		3	Is not connected to the Right ADC PGA.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs will have a 2X gain applied.

Page 1/Register 56: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 1/Register 57: Right ADC Input selection for Right PGA

Bit	Reset Value	Values	Description(1)
D7	0	0	Don't Bypass Right PGA.
		1	Bypass Right PGA, Unbuffered Differential Pair using the IN2R(P) as PLUS and IN3R(M) as MINUS inputs.
D6	0		RCH_SELCM
		0	Right ADC channel unselected inputs are not biased weakly to the ADC common-mode voltage.
		1	Right ADC channel unselected inputs are biased weakly to the ADC common-mode voltage.
D5–D4	3		RCH_SEL3X; Differential Pair using the IN1L(P) as PLUS and IN1R(M) as MINUS inputs.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Right ADC PGA.
		3	Is not connected to the Right ADC PGA.
D3–D2	3		RCH_SEL2X; Differential Pair using the IN2L(P) as PLUS and IN3L(M) as MINUS inputs.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Right ADC PGA.
		3	Is not connected to the Right ADC PGA.
D1–D0	3		RCH_SEL1X; Used for the IN1L(P) pin which is single ended.
		0	0 dB setting is chosen
		1	-6 dB setting is chosen
		2	Is not connected to the Right ADC PGA.
		3	Is not connected to the Right ADC PGA.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs will have a 2X gain applied.

Page 1/Register 58: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

Page 1/Register 59: Left Analog PGA Settings

Bit	Reset Value	Values	Description
D7	1	0	Left PGA is not muted
		1	Left PGA is muted
D6–D0	0	0	Left PGA Gain = 0dB
		1	Left PGA Gain = 0.5dB
		2	Left PGA Gain = 1dB
		80	Left PGA Gain = 40dB
		81 – 127	Reserved. Do not use.

Page 1/Register 60: Right Analog PGA Settings

Bit	Reset Value	Values	Description
D7	1	0	Right PGA is not muted
		1	Right PGA is muted
D6–D0	0	0	Right PGA Gain = 0dB
		1	Right PGA Gain = 0.5dB
		2	Right PGA Gain = 1dB
		80	Right PGA Gain = 40dB
		81 – 127	Reserved. Do not use.

Page 1/Register 61: ADC Low Current Modes

BIT	Reset Value	Values	DESCRIPTION
D7–D1	0	All values	Reserved. Write only zeros to these bits.
D0	0	0	1x ADC modulator current used.
		1	0.5x ADC modulator current used.

Page 1/Register 62: ADC Analog PGA Flags

Bit	Reset Value	Values	Description
D7–D2	0	All values	Reserved, don't write any value other than reset value
D1	0	0	Left ADC PGA , Applied Gain not = Programmed Gain
		1	Left ADC PGA , Applied Gain = Programmed Gain
D0	0	0	Right ADC PGA , Applied Gain not = Programmed Gain
		1	Right ADC PGA , Applied Gain = Programmed Gain

Page 1/Registers 63–127: Reserved

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to these registers.

CONTROL REGISTERS Page 2:

Page 2/Register 0: Page Control Register

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

CONTROL REGISTERS Page 3:

Page 3/Register 0: Page Control Register

Bit	Reset Value	Values	Description
D7–D0	X	All values	Reserved don't write to this register.

CONTROL REGISTERS Page4: ADC Programmable Coefficients RAM (1:63)

Page 4/Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0	Valid pages are 0,1,4, 5, 32 - 47

Page 4/Register 1: ADC

Bit	Reset Value	Values	Description
D6–D2	0	All values	Reserved don't write any value other than reset value.
D1	0	1	No effect
		2	Toggle the MSB Bit of the Coefficient Address generated by the ADC MAC Engine.
D0(1)	0	All values	ADC MAC Engine Generated Flag for Toggling MSB Bit of the Coefficient Address

(1) Read Only Bits…Writing any value to this will not be get used anywhere

Page 4/Register 2: C1_MSB

Bit	Reset Value	Values	Description
D7–D0	1	All values	Coefficient C1(15:8) of ADC

Page 4/Register 3: C1_LSB

Bit	Reset Value	Values	Description
D7–D0	23	All values	Coefficient C1(7:0) of ADC

Page 4/Register 4: C2_MSB

Bit	Reset Value	Values	Description
D7–D0	1	All values	Coefficient C2(15:8) of ADC

Page 4/Register 5: C2_LSB

Bit	Reset Value	Values	Description
D7–D0	23	All values	Coefficient C2(7:0) of ADC

Page 4/Register 6: C3_MSB

Bit	Reset Value	Values	Description
D7–D0	125	All values	Coefficient C3(15:8) of ADC

Page 4/Register 7: C3_LSB

Bit	Reset Value	Values	Description
D7–D0	211	All values	Coefficient C3(7:0) of ADC

Page 4/Register 8: C4_MSB

Bit	Reset Value	Values	Description
D7–D0	127	All values	Coefficient C4(15:8) of ADC

Page 4/Register 9: C4_LSB

Bit	Reset Value	Values	Description
D7–D0	255	All values	Coefficient C4(7:0) of ADC

Page 4/Register 10: C5_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C5(15:8) of ADC

Page 4/Register 11: C5_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C5(7:0) of ADC

Page 4/Register 12: C6_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C6(15:8) of ADC

Page 4/Register 13: C6_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C6(7:0) of ADC

Page 4/Register 14: C7_MSB

Bit	Reset Value	Values	Description
D7–D0	127	All values	Coefficient C7(15:8) of ADC

Page 4/Register 15: C7_LSB

Bit	Reset Value	Values	Description
D7–D0	255	All values	Coefficient C7(7:0) of ADC

Page 4/Register 16: C8_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C8(15:8) of ADC

Page 4/Register 17: C8_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C8(7:0) of ADC

Page 4/Register 18: C9_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C9(15:8) of ADC

Page 4/Register 19: C9_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C9(7:0) of ADC

Page 4/Register 20: C10_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C10(15:8) of ADC

Page 4/Register 21: C10_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C10(7:0) of ADC

Page 4/Register 22: C11_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C11(15:8) of ADC

Page 4/Register 23: C11_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C11(7:0) of ADC

Page 4/Register 24: C12_MSB

Bit	Reset Value	Values	Description
D7–D0	127	All values	Coefficient C12(15:8) of ADC

Page 4/Register 25: C12_LSB

Bit	Reset Value	Values	Description
D7–D0	255	All values	Coefficient C12(7:0) of ADC

Page 4/Register 26: C13_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C13(15:8) of ADC

Page 4/Register 27: C13_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C13(7:0) of ADC

Page 4/Register 28: C14_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C14(15:8) of ADC

Page 4/Register 29: C14_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C14(7:0) of ADC

Page 4/Register 30: C15_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C15(15:8) of ADC

Page 4/Register 31: C15_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C15(7:0) of ADC

Page 4/Register 32: C16_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C16(15:8) of ADC

Page 4/Register 33: C16_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C16(7:0) of ADC

Page 4/Register 34: C17_MSB

Bit	Reset Value	Values	Description
D7–D0	127	All values	Coefficient C17(15:8) of ADC

Page 4/Register 35: C17_LSB

Bit	Reset Value	Values	Description
D7–D0	255	All values	Coefficient C17(7:0) of ADC

Page 4/Register 36: C18_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C18(15:8) of ADC

Page 4/Register 37: C18_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C18(7:0) of ADC

Page 4/Register 38: C19_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C19(15:8) of ADC

Page 4/Register 39: C19_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C19(7:0) of ADC

Page 4/Register 40: C20_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C20(15:8) of ADC

Page 4/Register 41: C20_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C20(7:0) of ADC

Page 4/Register 42: C21_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C21(15:8) of ADC

Page 4/Register 43: C21_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C21(7:0) of ADC

Page 4/Register 44: C22_MSB

Bit	Reset Value	Values	Description
D7–D0	127	All values	Coefficient C22(15:8) of ADC

Page 4/Register 45: C22_LSB

Bit	Reset Value	Values	Description
D7–D0	255	All values	Coefficient C22(7:0) of ADC

Page 4/Register 46: C23_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C23(15:8) of ADC

Page 4/Register 47: C23_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C23(7:0) of ADC

Page 4/Register 48: C24_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C24(15:8) of ADC

Page 4/Register 49: C24_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C24(7:0) of ADC

Page 4/Register 50: C25_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C25(15:8) of ADC

Page 4/Register 51: C25_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C25(7:0) of ADC

Page 4/Register 52: C26_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C26(15:8) of ADC

Page 4/Register 53: C26_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C26(7:0) of ADC

Page 4/Register 54: C27_MSB

Bit	Reset Value	Values	Description
D7–D0	127	All values	Coefficient C27(15:8) of ADC

Page 4/Register 55: C27_LSB

Bit	Reset Value	Values	Description
D7–D0	255	All values	Coefficient C27(7:0) of ADC

Page 4/Register 56: C28_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C28(15:8) of ADC

Page 4/Register 57: C28_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C28(7:0) of ADC

Page 4/Register 58: C29_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C29(15:8) of ADC

Page 4/Register 59: C29_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C29(7:0) of ADC

Page 4/Register 60: C30_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C30(15:8) of ADC

Page 4/Register 61: C30_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C30(7:0) of ADC

Page 4/Register 62: C31_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C31(15:8) of ADC

Page 4/Register 63: C31_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C31(7:0) of ADC

Page 4/Register 64: C32_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C32(15:8) of ADC

Page 4/Register 65: C32_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C32(7:0) of ADC

Page 4/Register 66: C33_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C33(15:8) of ADC

Page 4/Register 67: C33_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C33(7:0) of ADC

Page 4/Register 68: C34_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C34(15:8) of ADC

Page 4/Register 69: C34_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C34(7:0) of ADC

Page 4/Register 70: C35_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C35(15:8) of ADC

Page 4/Register 71: C35_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C35(7:0) of ADC

Page 4/Register 72: C36_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C36(15:8) of ADC

Page 4/Register 73: C36_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C36(7:0) of ADC

Page 4/Register 74: C37_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C37(15:8) of ADC

Page 4/Register 75: C37_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C37(7:0) of ADC

Page 4/Register 76: C38_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C38(15:8) of ADC

Page 4/Register 77: C38_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C38(7:0) of ADC

Page 4/Register 78: C39_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C39(15:8) of ADC

Page 4/Register 79: C39_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C39(7:0) of ADC

Page 4/Register 80: C40_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C40(15:8) of ADC

Page 4/Register 81: C40_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C40(7:0) of ADC

Page 4/Register 82: C41_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C41(15:8) of ADC

Page 4/Register 83: C41_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C41(7:0) of ADC

Page 4/Register 84: C42_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C42(15:8) of ADC

Page 4/Register 85: C42_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C42(7:0) of ADC

Page 4/Register 86: C43_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C43(15:8) of ADC

Page 4/Register 87: C43_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C43(7:0) of ADC

Page 4/Register 88: C44_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C44(15:8) of ADC

Page 4/Register 89: C44_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C44(7:0) of ADC

Page 4/Register 90: C45_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C45(15:8) of ADC

Page 4/Register 91: C45_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C45(7:0) of ADC

Page 4/Register 92: C46_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C46(15:8) of ADC

Page 4/Register 93: C46_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C46(7:0) of ADC

Page 4/Register 94: C47_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C47(15:8) of ADC

Page 4/Register 95: C47_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C47(7:0) of ADC

Page 4/Register 96: C48_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C48(15:8) of ADC

Page 4/Register 97: C48_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C48(7:0) of ADC

Page 4/Register 98: C49_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C49(15:8) of ADC

Page 4/Register 99: C49_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C49(7:0) of ADC

Page 4/Register 100: C50_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C50(15:8) of ADC

Page 4/Register 101: C50_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C50(7:0) of ADC

Page 4/Register 102: C51_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C51(15:8) of ADC

Page 4/Register 103: C51_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C51(7:0) of ADC

Page 4/Register 104: C52_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C52(15:8) of ADC

Page 4/Register 105: C52_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C52(7:0) of ADC

Page 4/Register 106: C53_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C53(15:8) of ADC

Page 4/Register 107: C53_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C53(7:0) of ADC

Page 4/Register 108: C54_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C54(15:8) of ADC

Page 4/Register 109: C54_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C54(7:0) of ADC

Page 4/Register 110: C55_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C55(15:8) of ADC

Page 4/Register 111: C55_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C55(7:0) of ADC

Page 4/Register 112: C56_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C56(15:8) of ADC

Page 4/Register 113: C56_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C56(7:0) of ADC

Page 4/Register 114: C57_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C57(15:8) of ADC

Page 4/Register 115: C57_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C57(7:0) of ADC

Page 4/Register 116: C58_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C58(15:8) of ADC

Page 4/Register 117: C58_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C58(7:0) of ADC

Page 4/Register 118: C59_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C59(15:8) of ADC

Page 4/Register 119: C59_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C59(7:0) of ADC

Page 4/Register 120: C60_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C60(15:8) of ADC

Page 4/Register 121: C60_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C60(7:0) of ADC

Page 4/Register 122: C61_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C61(15:8) of ADC

Page 4/Register 123: C61_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C61(7:0) of ADC

Page 4/Register 124: C62_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C62(15:8) of ADC

Page 4/Register 125: C62_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C62(7:0) of ADC

Page 4/Register 126: C63_MSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C63(15:8) of ADC

Page 4/Register 127: C63_LSB

Bit	Reset Value	Values	Description
D7–D0	0	All values	Coefficient C63(7:0) of ADC

PACKAGING INFORMATION

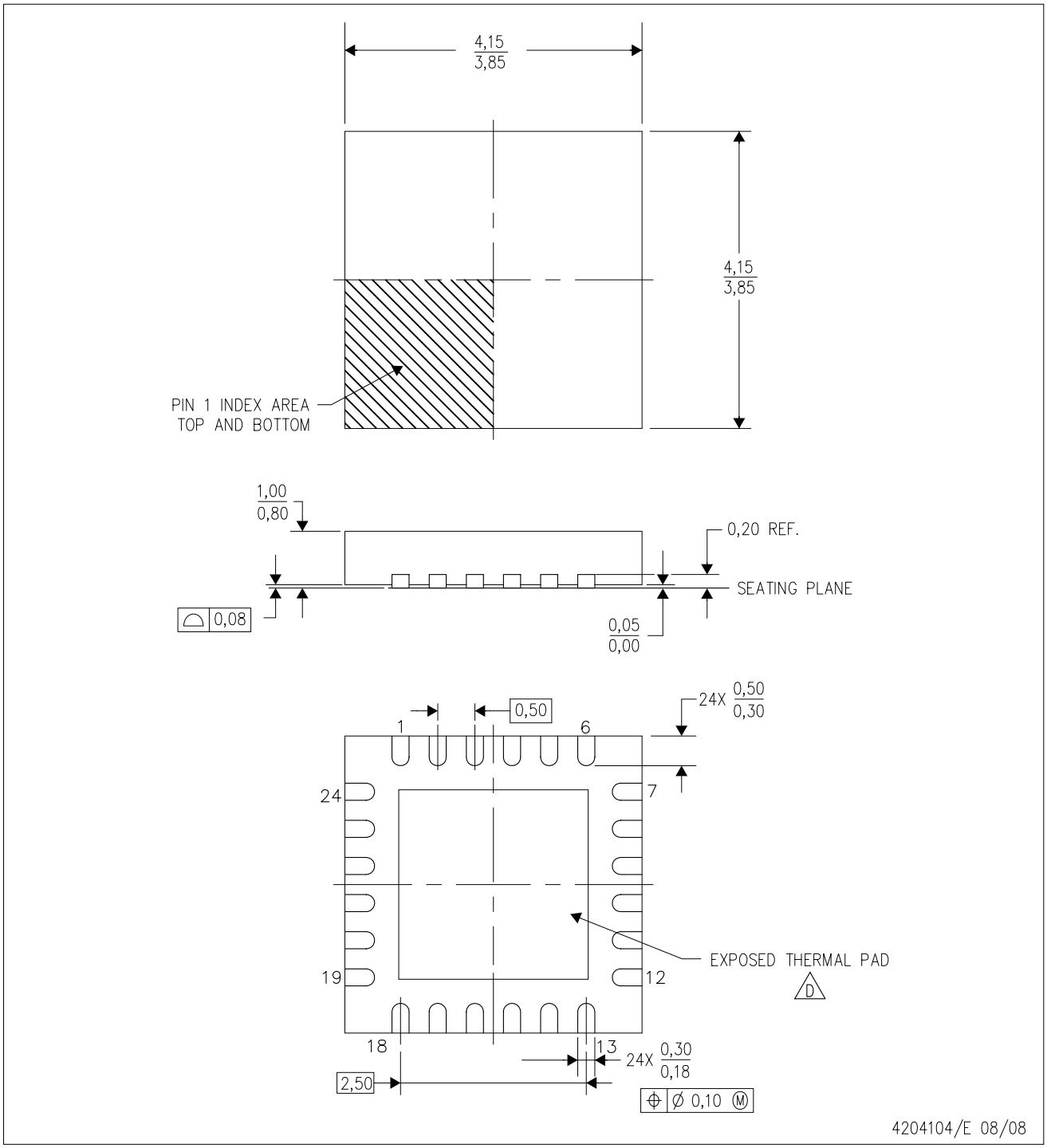
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV320ADC3101IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV320ADC3101IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

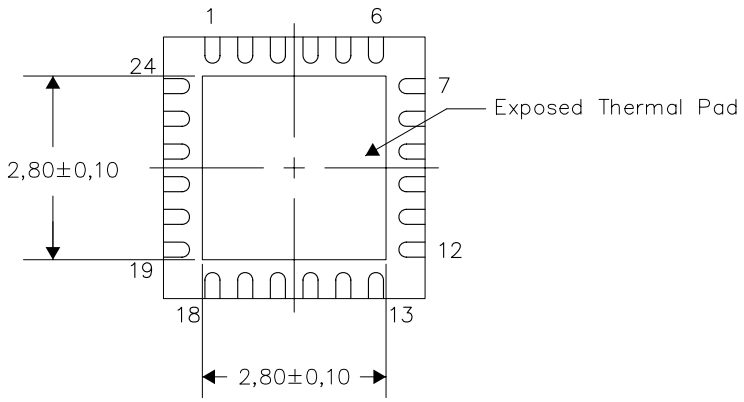
RGE (S–PVQFN–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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