

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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## SWITCHING N-CHANNEL POWER MOS FET

### DESCRIPTION

The 2SK3480 is N-channel MOS Field Effect Transistor designed for high current switching applications.

### FEATURES

- Super low on-state resistance:  
 $R_{DS(on)1} = 31 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 25 \text{ A)}$   
 $R_{DS(on)2} = 36 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 25 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 3600 \text{ pF TYP.}$
- Built-in gate protection diode

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	100	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 50$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 100$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	84	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	34	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	116	mJ

**Notes** 1.  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

2. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

### THERMAL RESISTANCE

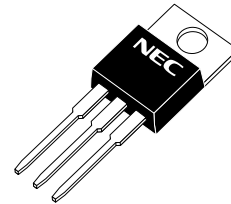
Channel to Case	$R_{th(ch-C)}$	1.48	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

### ORDERING INFORMATION

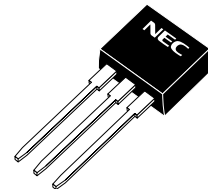
PART NUMBER	PACKAGE
2SK3480	TO-220AB
2SK3480-S	TO-262
2SK3480-ZJ	TO-263
2SK3480-Z	TO-220SMD <sup>Note</sup>

**Note** TO-220SMD package is produced only in Japan.

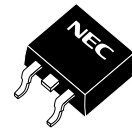
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)

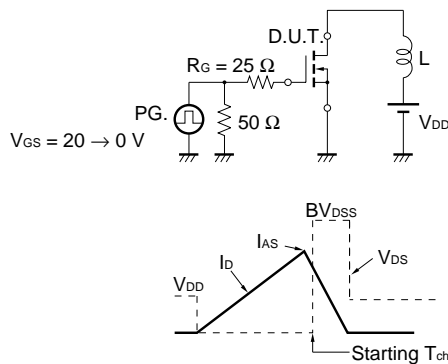


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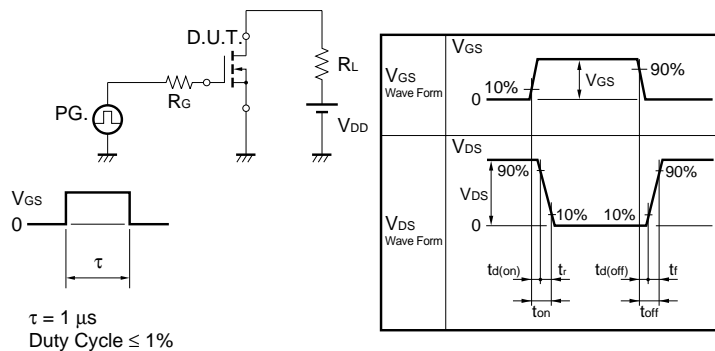
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 25 A	17	34		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A		25	31	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 25 A		27	36	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		3600		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		360		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		190		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 25 A		15		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		11		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		68		ns
Fall Time	t <sub>f</sub>			6.0		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 80 V		74		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		10		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 50 A		20		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		70		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		180		nC

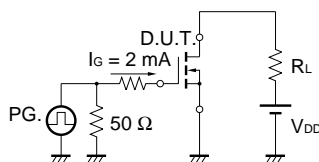
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



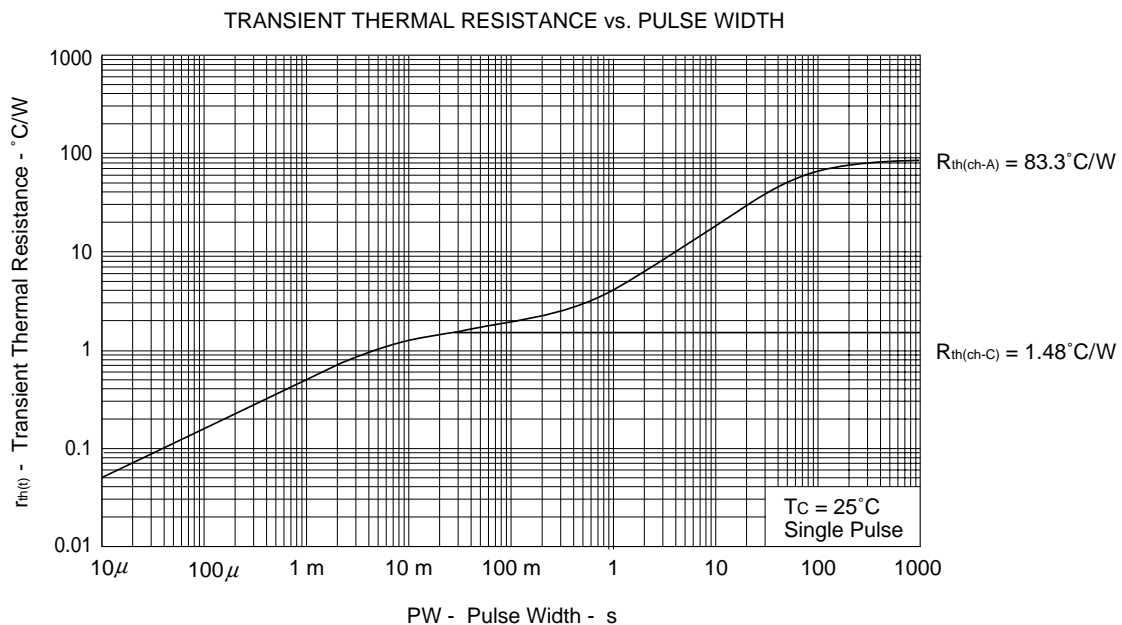
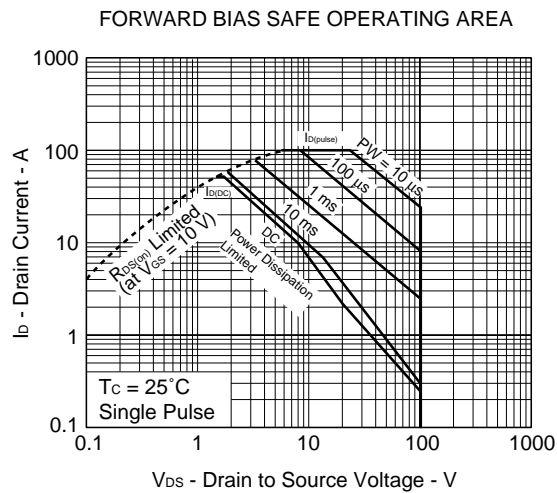
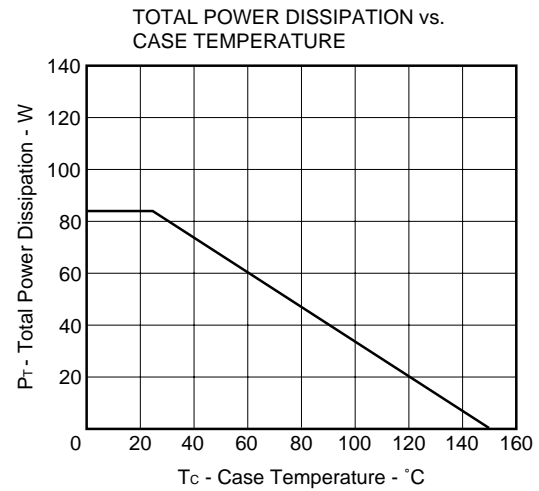
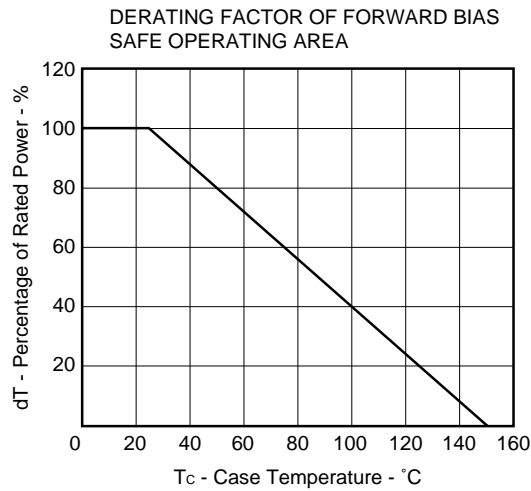
**TEST CIRCUIT 2 SWITCHING TIME**



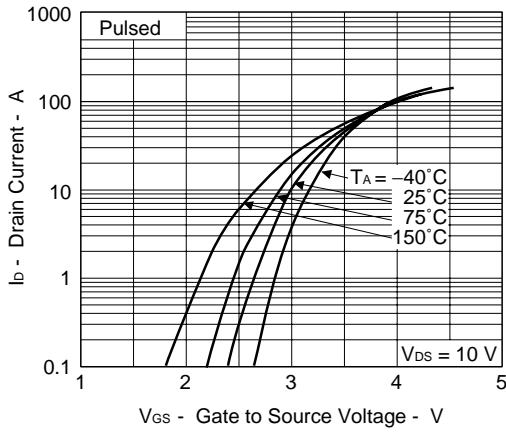
**TEST CIRCUIT 3 GATE CHARGE**



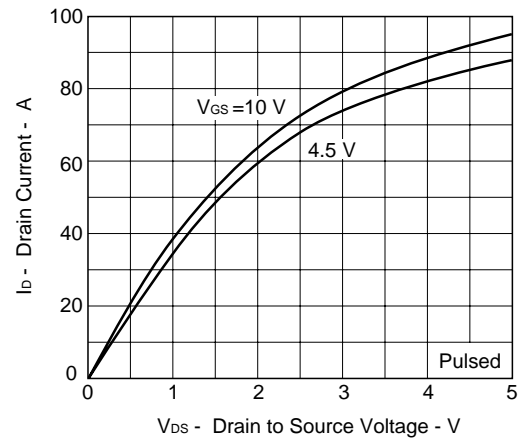
TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



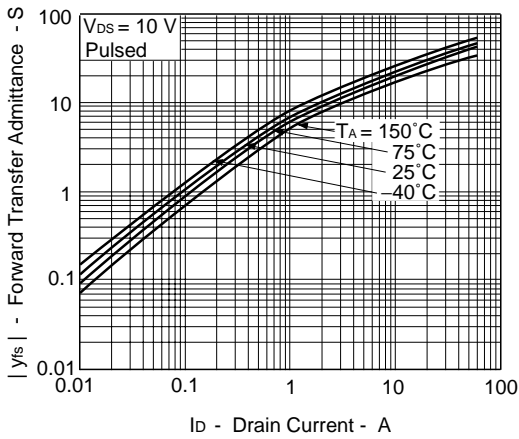
FORWARD TRANSFER CHARACTERISTICS



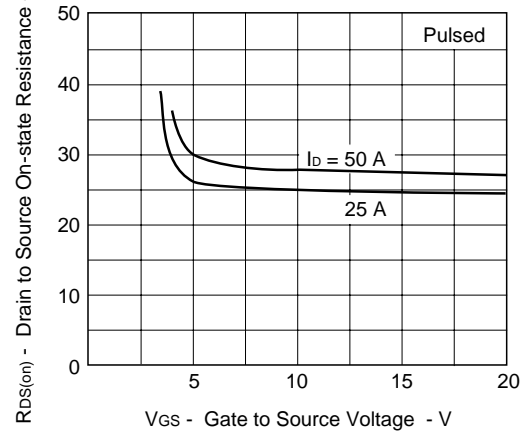
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



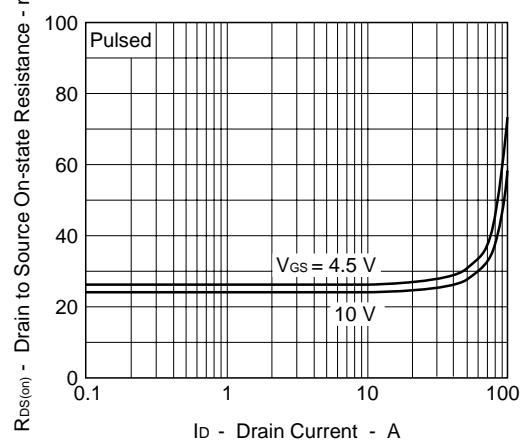
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



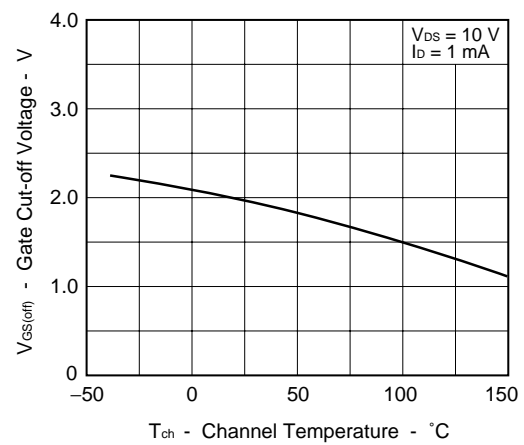
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



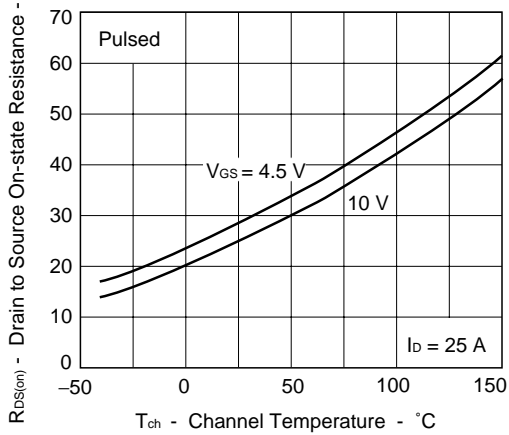
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



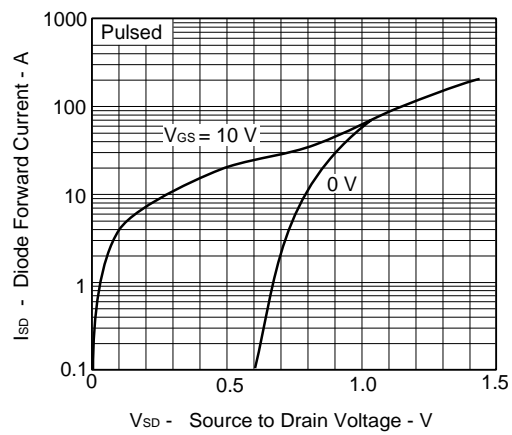
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



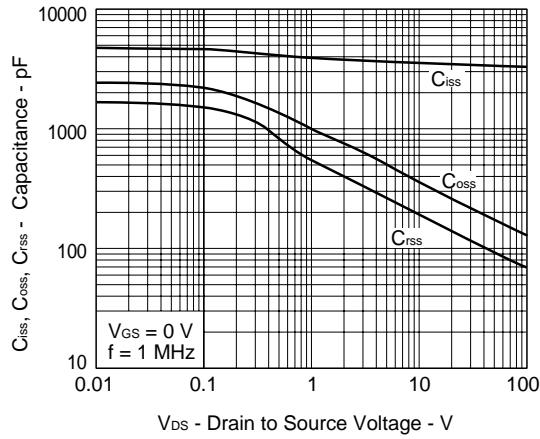
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



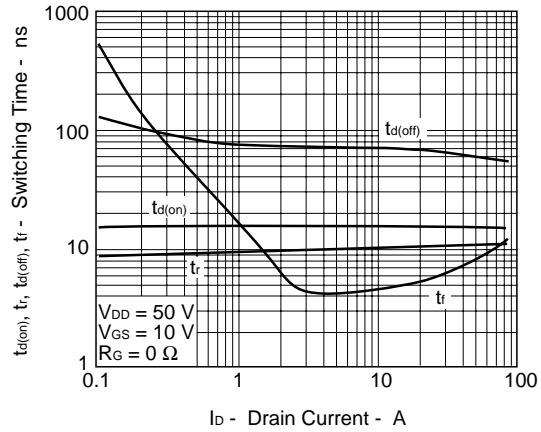
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



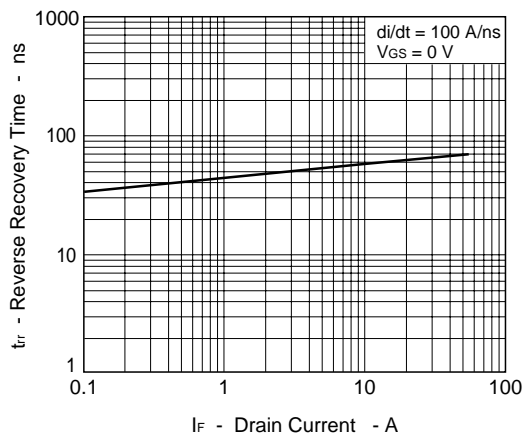
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



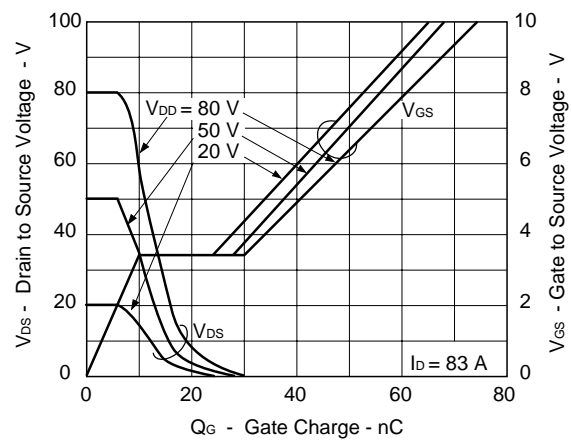
SWITCHING CHARACTERISTICS

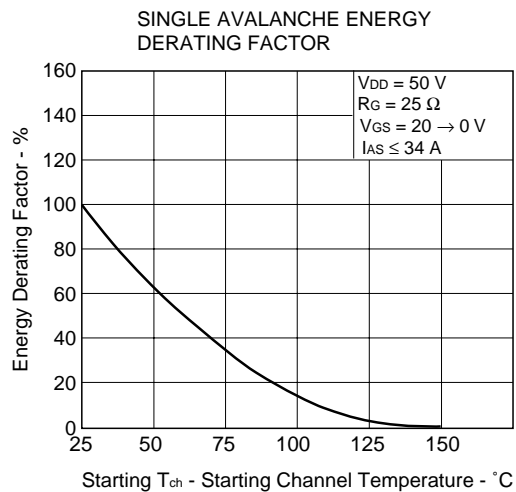
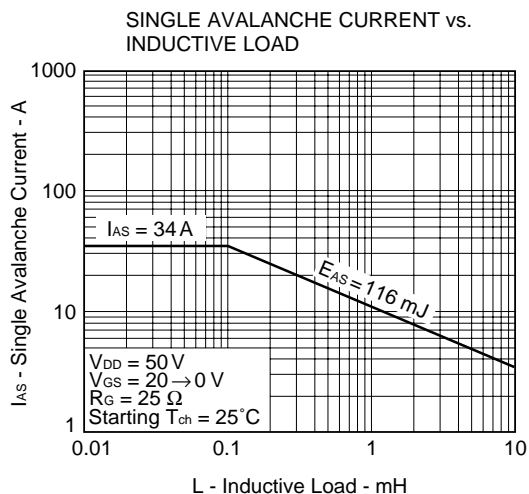


REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

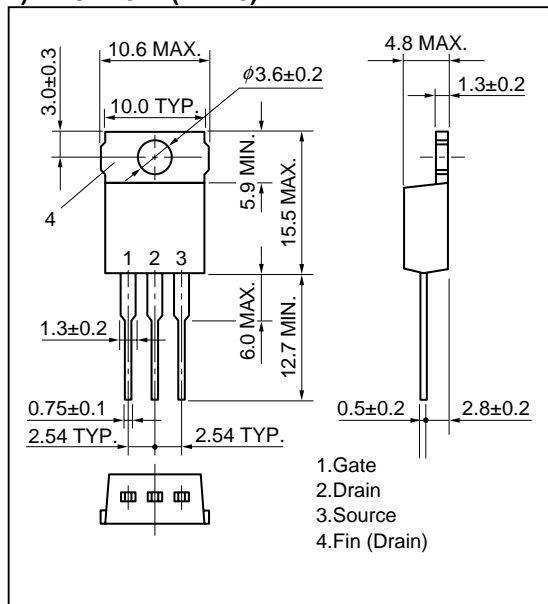




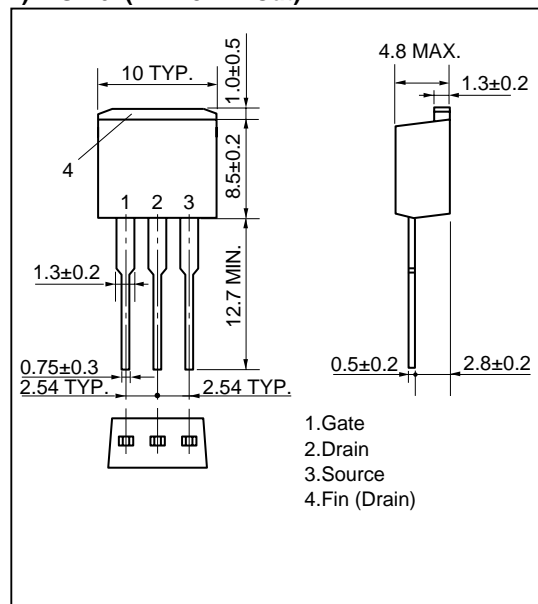


PACKAGE DRAWINGS (Unit: mm)

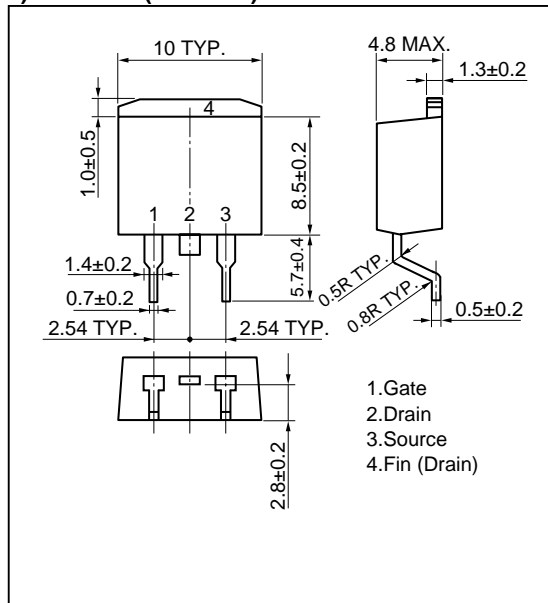
1) TO-220AB(MP-25)



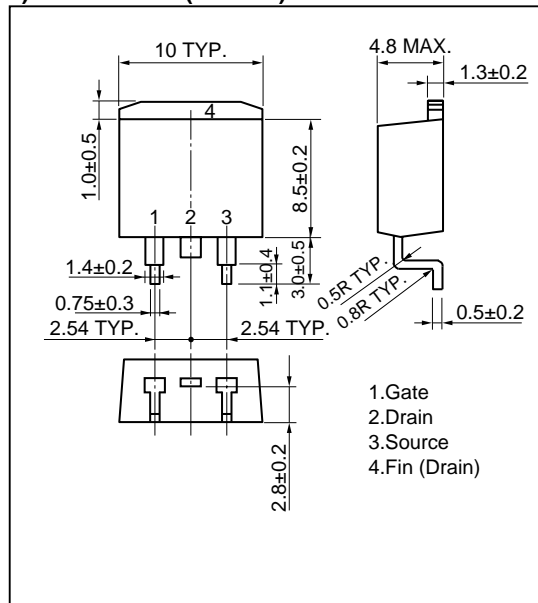
2) TO-262(MP-25 Fin Cut)



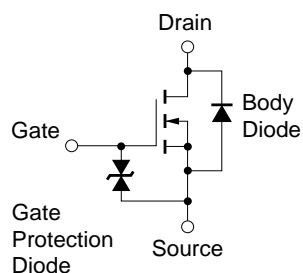
3) TO-263 (MP-25ZJ)



4) TO-220SMD(MP-25Z)<sup>Note</sup>



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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