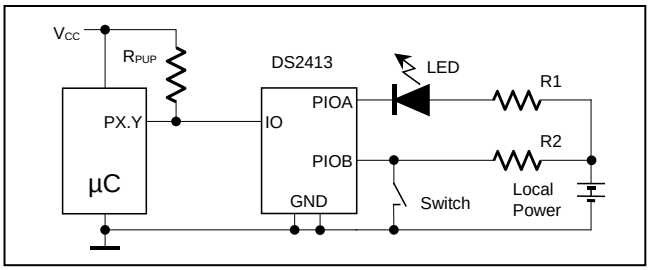
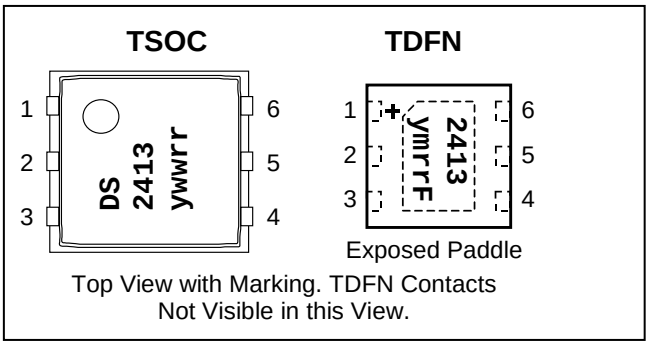
19-5316; 3/15

DS2413
1-Wire Dual Channel Addressable Switch

GENERAL DESCRIPTION
The DS2413 is a dual-channel programmable I/O 1-Wire® chip. The PIO outputs are configured as open-drain and provide up to 20mA continuous sink capability and off-state operating voltage up to 28V. Control and sensing of the PIO pins is performed with a dedicated device-level command protocol. To provide a high level of fault tolerance in the end application, the 1-Wire IO and PIO pins are all capable of withstanding continuous application of voltages up to 28V max. Communication and operation of the DS2413 is performed with the single contact Maxim/Dallas 1-Wire serial interface.

APPLICATIONS
- LED Control
- Accessory Identification and Control
- General Purpose Input/Output
- Key-Pick Systems
- Industrial Controllers
- System Monitoring

TYPICAL OPERATING CIRCUIT


PIN CONFIGURATION


BENEFITS AND FEATURES
- Controls Dual Programmable High Voltage, High Current I/O Port Pins from a Single Micro Port Pin
  - Open-Drain Programmable I/O Pins Support 20mA max Continuous Current Sink
  - 28V (max) PIO Pin Operating Voltage
  - On-Resistance of PIO Pulldown Transistor 20Ω max; OFF Resistance 1MΩ min
  - Parasitic Power Supply Through 1-Wire
- Minimalist 1-Wire Interface Lowers Cost and Interface Complexity
  - Communicates to Host with a Single Digital Signal at 14.9kb or 100kbps
  - Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise
  - 1-Wire IO Pin Supports 28V Absolute Maximum DC Level for Fault Conditions
  - Unique 64-bit ROM Serial Number Factory Lasered Into Each Device
  - High ESD Immunity of 1-Wire IO Pin: 8kV HBM Typical
  - TSOC and TDFN Packages Available
- Wide Voltage and Temperature Operating Ranges Enables Robust System Performance
  - 2.8V to 5.25V
  - 0°C to +70°C

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2413P+	0°C to +70°C	TSOC
DS2413P+T&R	0°C to +70°C	TSOC
DS2413Q+T&R	0°C to +70°C	TDFN

+ Denotes a lead(Pb)-free package/RoHS-compliant package.
T&R = Tape and reel.

Commands, Registers, and Modes are capitalized for clarity.

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin to GND	-0.5V, +30V
Maximum Current into IO Pin	±25mA
Maximum Current into PIO Pin	±30mA
Maximum Current Through GND Pins (Both Pins Tied Together)	±60mA
Operating Temperature Range	0°C to +70°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN GENERAL DATA						
1-Wire Pullup Voltage (Note 1)	V_{PUP}	Standard speed	2.8		5.25	V
		Overdrive speed	2.9		5.25	
		DC only; no 1-Wire communication			28	
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)	1.5		2.2	kΩ
Input Load Current	I_L	$V_{PUP} \le 5.25V$	3.5		70	µA
		$V_{PUP} \le 3.30V$	3.5		15	
		V(IO) = 28V (Note 3)	400		950	
Input Capacitance	C_{IO}	At 25°C (Notes 4, 5)			800	pF
Input Low Voltage	V_{IL}	(Notes 1, 6)			0.4	V
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 7, 8)	0.4		3.2	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 7, 9)	0.7		3.6	V
Switching Hysteresis	V_{HY}	(Notes 5, 10)	0.2			V
Output Low Voltage	V_{OL}	At 4mA Current Load (Note 11)			0.4	V
Recovery Time (Notes 1, 12)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Time slot Duration (Note 1, 5)	t_{SLOT}	Standard speed, $V_{PUP} \ge 4.5V$	65			µs
		Standard speed (Note 14)	67			
		Overdrive speed, $V_{PUP} \ge 4.5V$ (Note 14)	9			
		Overdrive speed (Note 14)	10			
IO PIN, 1-Wire RESET, PRESENCE DETECT CYCLE						
Reset Low Time (Note 1)	t_{RSTL}	Standard speed, $V_{PUP} \ge 4.5V$	480		960	µs
		Standard speed (Note 14)	600		960	
		Overdrive speed, $V_{PUP} \ge 4.5V$	48		80	
		Overdrive speed (Note 14)	63		80	
Presence Detect High Time (Notes 14, 15)	t_{PDH}	Standard speed, $V_{PUP} \ge 4.5V$	15		66	µs
		Standard speed	15		68	
		Overdrive speed, $V_{PUP} \ge 4.5V$	2		7.0	
		Overdrive speed	2		8.2	
Presence Detect Fall Time (Notes 5, 16)	t_{FPD}	Standard speed, $V_{PUP} > 4.5V$	0.24		1.4	µs
		Standard speed	0.24		1.6	
		Overdrive speed, $V_{PUP} \ge 4.5V$	0		0.7	
		Overdrive speed	0		0.9	
Presence Detect Low Time (Note 15)	t_{PDL}	Standard speed, $V_{PUP} > 4.5V$	60		240	µs
		Standard speed (Note 14)	60		260	
		Overdrive speed, $V_{PUP} \ge 4.5V$ (Note 14)	8		25	
		Overdrive speed (Note 14)	8		32	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Presence Detect Sample Time (Notes 1, 20)	t_{MSP}	Standard speed, V_{PUP} > 4.5V	67.4		75	µs
		Standard speed	69.6		75	
		Overdrive speed, $V_{PUP} \geq 4.5V$	7.7		10	
		Overdrive speed	9.1		10	
IO PIN, 1-Wire WRITE						
Write-0 Low Time (Notes 1, 17)	t_{W0L}	Standard speed, V_{PUP} > 4.5V	60		120	µs
		Standard speed (Note 14)	62		120	
		Overdrive speed, $V_{PUP} \geq 4.5V$ (Note 14)	7		16	
		Overdrive speed (Note 14)	8		16	
Write-1 Low Time (Notes 1, 17)	t_{W1L}	Standard speed	5		15	µs
		Overdrive speed	1		2	
IO PIN, 1-Wire READ						
Read Low Time (Notes 1, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 1, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
PIO Pins						
Leakage Current	I_{LP}	Pin at 28V (Note 19)	8.5		24	µA
Input Capacitance	C_P	(Note 5)		100		pF
Output low voltage	V_{OLP}	20mA load current			0.4	V
Input Low Voltage	V_{ILP}	(Note 1)			0.8	V
Input High Voltage (Note 21)	V_{IHP}	(Note 1)	V_{PUP} – 0.3V		28	V

Note 1: System requirement.

Note 2: Full R_{PUP} range guaranteed by design and simulation. not production tested. Production testing performed at a fixed R_{PUP} value. Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00 or DS2480B may be required. The DS2482-x00 may not always detect the DS2413 presence pulse. For proper operation it may be necessary to disregard (force to 1) the PPD bit in the DS2482-x00 status register.

Note 3: The I-V characteristic is linear for voltages greater than 10V.

Note 4: Capacitance on the data pin could be 800pF when V_{PUP} is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied the parasite capacitance will not affect normal communications.

Note 5: Guaranteed by design and simulation. Not production tested.

Note 6: The voltage on IO needs to be less than or equal to V_{ILMAX} whenever the master drives the line low.

Note 7: V_{TL} and V_{TH} are functions of the internal supply voltage, which is a function of V_{PUP} and the 1-Wire Recovery Times. The V_{TH} and V_{TL} maximum specifications are valid at V_{PUPmax} (5.25V). In any case, $V_{TL} < V_{TH} < V_{PUP}$.

Note 8: Voltage below which, during a falling edge on IO, a logic 0 is detected.

Note 9: Voltage above which, during a rising edge on IO, a logic 1 is detected.

Note 10: After V_{TH} is crossed during a rising edge on IO, the voltage on IO has to drop by at least V_{HY} to be detected as logic '0'.

Note 11: The I-V characteristic is linear for voltages less than 1V.

Note 12: Applies to a single DS2413 attached to a 1-Wire line.

Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.

Note 14: Highlighted numbers are NOT in compliance with legacy 1-Wire product standards. See comparison table below.

Note 15: t_{PDH} is deemed to have ended when the voltage on IO drops below 80% of V_{PUP} on the leading edge of the presence-detect low pulse. t_{PDL} is deemed to have begun when the voltage on IO drops below 20% of V_{PUP} on the leading edge of the pulse.

Note 16: Interval during the negative edge on IO at the beginning of a Presence Detect pulse between the time at which the voltage is 80% of V_{PUP} and the time at which the voltage is 20% of V_{PUP}.

Note 17: ε in Figure 12 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1Lmax} + t_F - \varepsilon$ and $t_{W0Lmax} + t_F - \varepsilon$ respectively.

Note 18: δ in Figure 12 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLmax} + t_F$.

Note 19: The I-V characteristic is linear for voltages greater than 7V.

Note 20: t_{MSP} is a system required sample point and not directly production tested. Production testing is performed on related parameters t_{PDH} and t_{PDL}. Parameter t_{FPD} is guaranteed by design and simulation, not production tested.

Note 21: Production tested for $V_{IHP(min)}$. $V_{IHP(max)}$ is guaranteed by design and simulation, not production tested.

PARAMETER	LEGACY VALUES				DS2413 VALUES			
	STANDARD SPEED		OVERDRIVE SPEED		STANDARD SPEED		OVERDRIVE SPEED	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (incl. t_{REC})	61µs	(undef.)	7µs	(undef.)	67µs	(undef.)	10µs	(undef.)
t_{RSTL}	480µs	(undef.)	48µs	80µs	600µs	960µs	63µs	80µs
t_{PDH}	15µs	60µs	2µs	6µs	15µs	68µs	2µs	8.2µs
t_{PDL}	60µs	240µs	8µs	24µs	60µs	260µs	8µs	32µs
t_{W0L}	60µs	120µs	6µs	16µs	62µs	120µs	8µs	16µs

PIN DESCRIPTION

NAME	TSOC PIN #	TDFN PIN #	FUNCTION
IO	2	2	1-Wire bus interface. Open-drain, requires external pullup resistor.
PIOA	6	4	Programmable I/O pin, open-drain with weak pulldown, power-on default is off (PIOA = 1).
PIOB	4	6	Programmable I/O pin, open-drain with weak pulldown, power-on default is off (PIOB = 1).
GND1	1	3	Ground reference 1
GND2	5	5	Ground reference 2; both GND pins must be connected in the application.
NC	3	1	Not connected
GND	—	EP	Exposed Paddle (TDFN only). Solder evenly to the board's ground plane for proper operation. See Application Note 3273 for additional information.

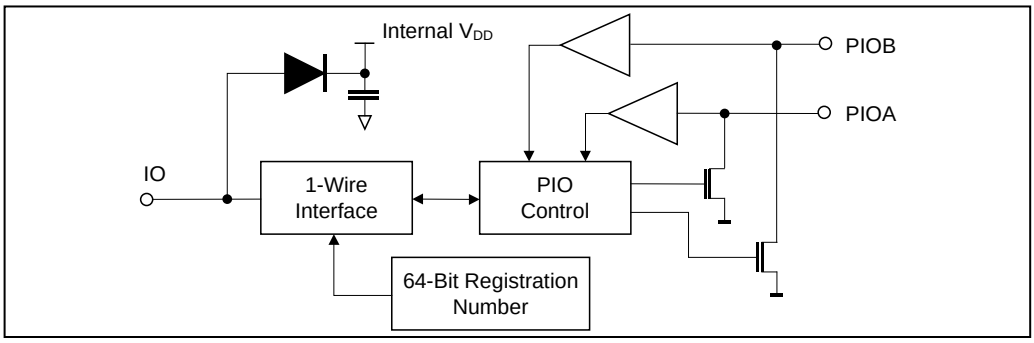
DESCRIPTION

The DS2413 combines two PIO pins and a fully featured 1-Wire interface in a single chip. PIO outputs are open-drain, operate at up to 28V and provide an on resistance of 20Ω max. A robust communication protocol ensures that PIO output changes occur error-free. Each DS2413 has a Registration Number that is 64 bits long. The Registration Number guarantees unique identification and is used to address the device in a multidrop 1-Wire network environment, where multiple devices reside on a common 1-Wire bus and operate independently of each other. Device power is supplied parasitically from the 1-Wire bus. The DS2413's applications of include accessory identification and control, system monitoring, and general-purpose input/output.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major sections of the DS2413. The DS2413 has two main components: 64-bit Registration Number, and PIO Control. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Resume, 6) Overdrive-Skip ROM or 7) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 10. After a ROM function command is successfully executed, the PIO functions become accessible and the master may provide one of the two PIO Function commands. The protocol for these commands is described in Figure 6. **All data is read and written least significant bit first.**

Figure 1. Block Diagram



64-BIT LASERED ROM

Each DS2413 has a unique ROM Registration Number that is 64 bits long, as shown in Figure 3. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC (Cyclic Redundancy Check) of the first 56 bits. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire CRC is available in *Application Note 27*. The shift register bits are initialized to zero. Then starting with the LSB of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

Figure 2. Hierarchical Structure for 1-Wire Protocol

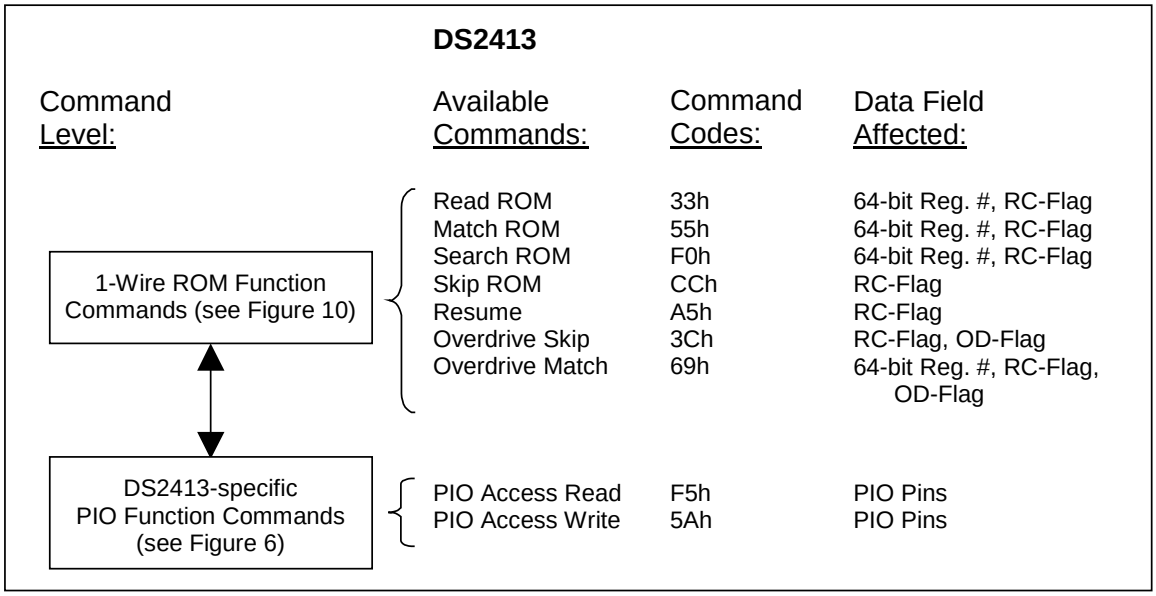


Figure 3. 64-Bit LASERED ROM

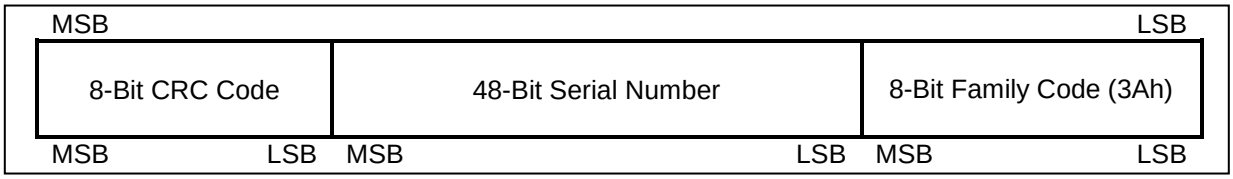
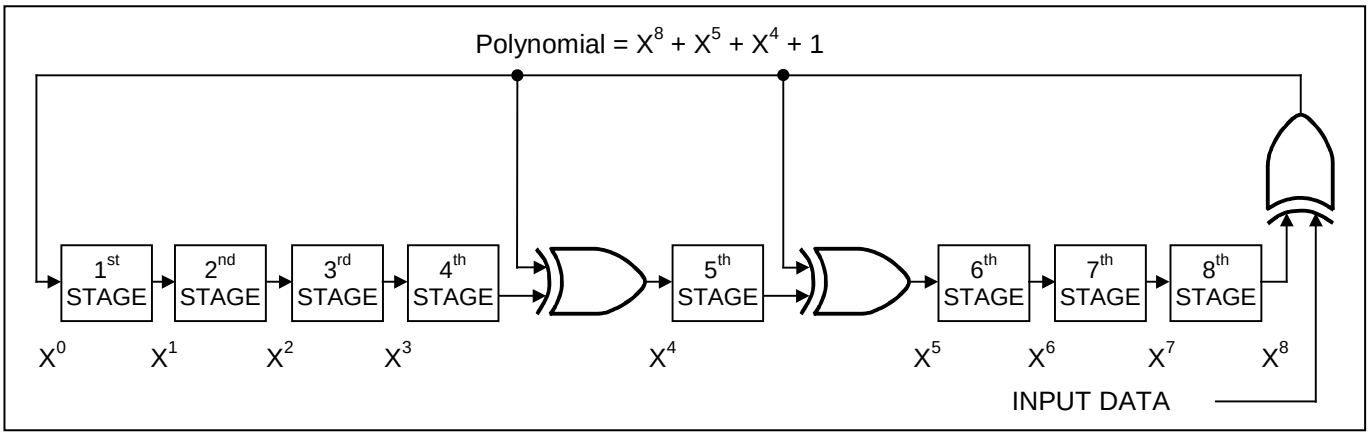


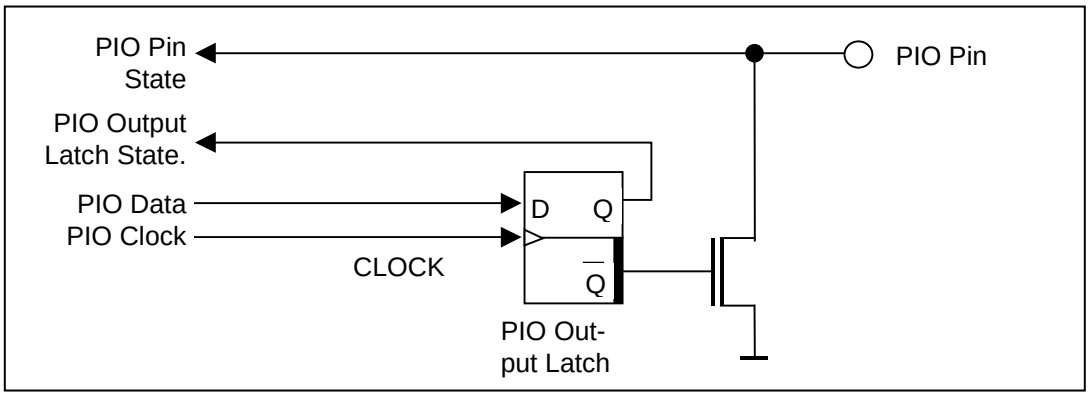
Figure 4. 1-Wire CRC Generator



PIO STUCTURE

Each PIO consists of an open-drain pulldown transistor with 28V capability. The transistor is controlled by the PIO Output Latch, as shown in Figure 5. The PIO Control unit connects the PIOs to the 1-Wire interface.

Figure 5. PIO Simplified Logic Diagram



PIO FUNCTION COMMANDS

The *PIO Function Flow Chart* (Figure 6) describes the protocols necessary to access the PIO pins of the DS2413. Examples on how to use these functions are included at the end of this document. The communication between master and DS2413 takes place either at standard speed (default, OD = 0) or at Overdrive Speed (OD = 1). If not explicitly set into the Overdrive Mode, the DS2413 powers up in standard speed.

PIO ACCESS READ [F5h]

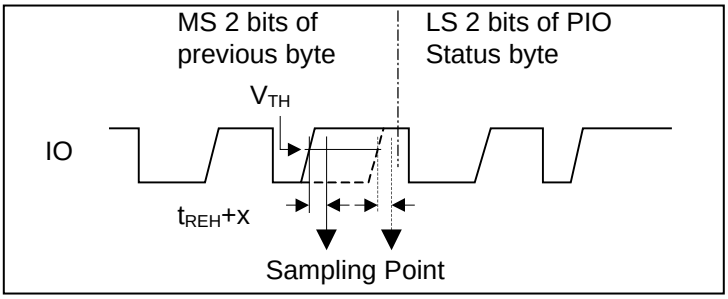
This command reads the PIO logical status and reports it together with the state of the PIO Output Latch in an endless loop. A PIO Access Read can be terminated at any time with a 1-Wire Reset.

PIO Status Bit Assignment

b7	b6	b5	b4	b3	b2	b1	b0
Complement of b3 to b0				PIOB Output Latch State	PIOB Pin State	PIOA Output Latch State	PIOA Pin State

The state of both PIO channels is sampled at the same time. The first sampling occurs during the last (most significant) bit of the command code F5h. The PIO status is then reported to the bus master. While the master receives the last (most significant) bit of the PIO status byte, the next sampling occurs and so on until the master generates a 1-Wire Reset. The sampling occurs with a delay of $t_{REH}+x$ from the rising edge of the MS bit of the previous byte, as shown in Figure 7. The value of "x" is approximately 0.2µs.

Figure 7. PIO Access Read Timing Diagram

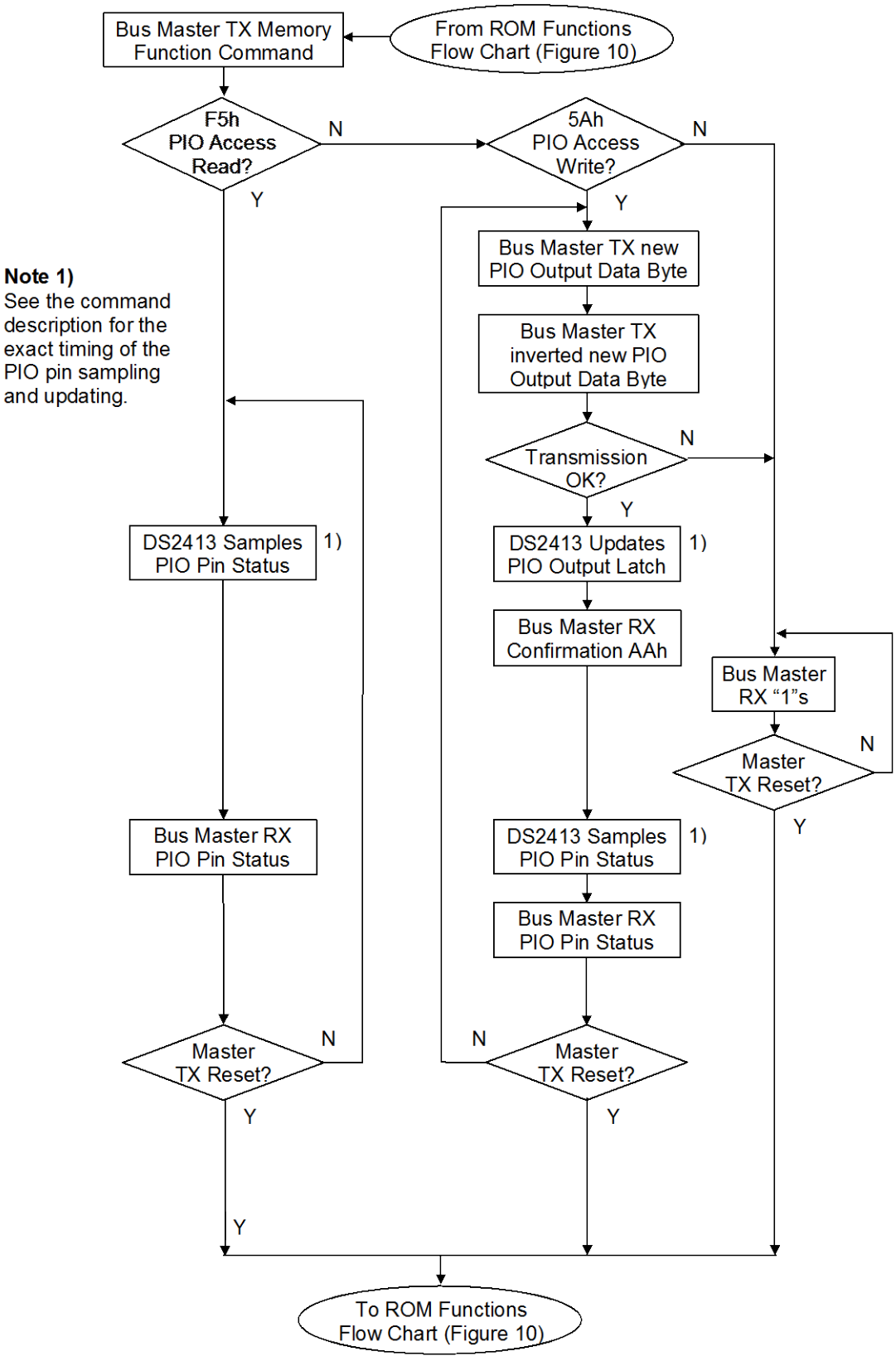


Notes:

1 The "previous byte" could be the command code or the data byte resulting from the previous PIO sample.

2 The sample point timing also applies to the PIO Access Write command, with the "previous byte" being the write confirmation byte (AAh).

Figure 6. PIO Function Flow Chart



PIO ACCESS WRITE [5Ah]

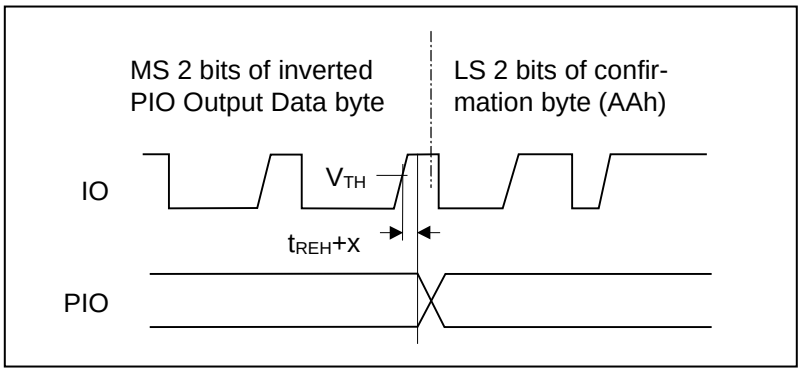
The PIO Access Write command writes to the PIO output latches, which control the pulldown transistors of the PIO channels. In an endless loop this command first writes new data to the PIO and then reads back the PIO status. This implicit read-after-write can be used by the master for status verification. A PIO Access Write can be terminated at any time with a 1-Wire Reset.

PIO Output Data Bit Assignment

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	PIOB	PIOA

After the command code the master transmits a PIO Output Data byte that determines the new state of the PIO output transistors. The first (least significant) bit is associated to PIOA; the next bit affects PIOB. The other 6 bits of the new state byte do not have corresponding PIO pins. These bits should always be transmitted as "1"s. To switch the output transistor on, the corresponding bit value is 0. To switch the output transistor off (non-conducting) the bit must be 1. This way the bit transmitted as the new PIO output state arrives in its true form at the PIO pin. To protect the transmission against data errors, the master must repeat the PIO Output Data byte in its inverted form. Only if the transmission was error-free will the PIO status change. The actual PIO transition to the new state occurs with a delay of t_{REH}+x from the rising edge of the MS bit of the inverted PIO byte, as shown in Figure 8. The value of "x" is approximately 0.2µs. To inform the master about the successful communication of the PIO byte, the DS2413 transmits a confirmation byte with the data pattern AAh. While the MS bit of the confirmation byte is transmitted, the DS2413 samples the state of the PIO pins, as shown in Figure 7, and sends it to the master. The master can either continue writing more data to the PIO or issue a 1-Wire Reset to end the command.

Figure 8. PIO Access Write Timing Diagram



1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS2413 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

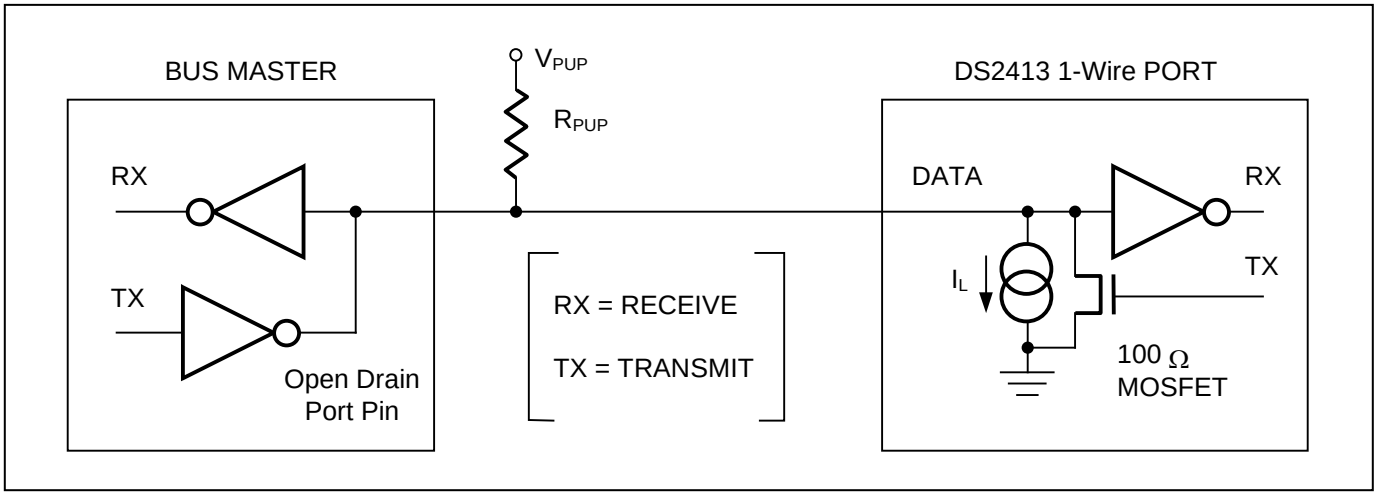
HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or tri-state outputs. The 1-Wire port of the DS2413 is open drain with an internal circuit equivalent to that shown in Figure 9.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS2413 supports both a Standard and Overdrive communication speed of 14.9kbps (max) and 100kbps (max), respectively. Note that legacy 1-Wire products support a standard communication speed of 16.3kbps and Overdrive of 142kbps. The value of the pullup resistor primarily depends on the network size and load conditions. The DS2413 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (Overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset.

Figure 9. Hardware Configuration



TRANSACTION SEQUENCE

The protocol for accessing the DS2413 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- PIO Function Command
- Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2413 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS2413 supports. All ROM function commands are 8 bits long. A list of these commands follows (refer to the flow chart in Figure 10).

READ ROM [33h]

This command allows the bus master to read the DS2413's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

MATCH ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2413 on a multidrop bus. Only the DS2413 that exactly matches the 64-bit ROM sequence, including the external address, responds to the following PIO Function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their device ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the device ID numbers of all slave devices. For each bit of the device ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its device ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its device ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the device ID number of a single device. Additional passes identify the device ID numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example.

SKIP ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the PIO functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

RESUME [A5h]

To maximize the data throughput in a multidrop environment, the Resume function is available. This function checks the status of the RC bit and, if it is set, directly transfers control to the PIO functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume Command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume Command function.

OVERDRIVE SKIP ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the PIO functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS2413 in the Overdrive mode (OD = 1). All communication following this command has to occur at Overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

OVERDRIVE MATCH ROM [69h]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at Overdrive Speed allows the bus master to address a specific DS2413 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS2413 that exactly matches the 64-bit ROM sequence responds to the subsequent PIO Function command. Slaves already in Overdrive mode from a previous Overdrive Skip or successful Overdrive Match command remain in Overdrive mode. All overdrive-capable slaves return to standard speed at the next Reset Pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

Figure 10-1. ROM Functions Flow Chart

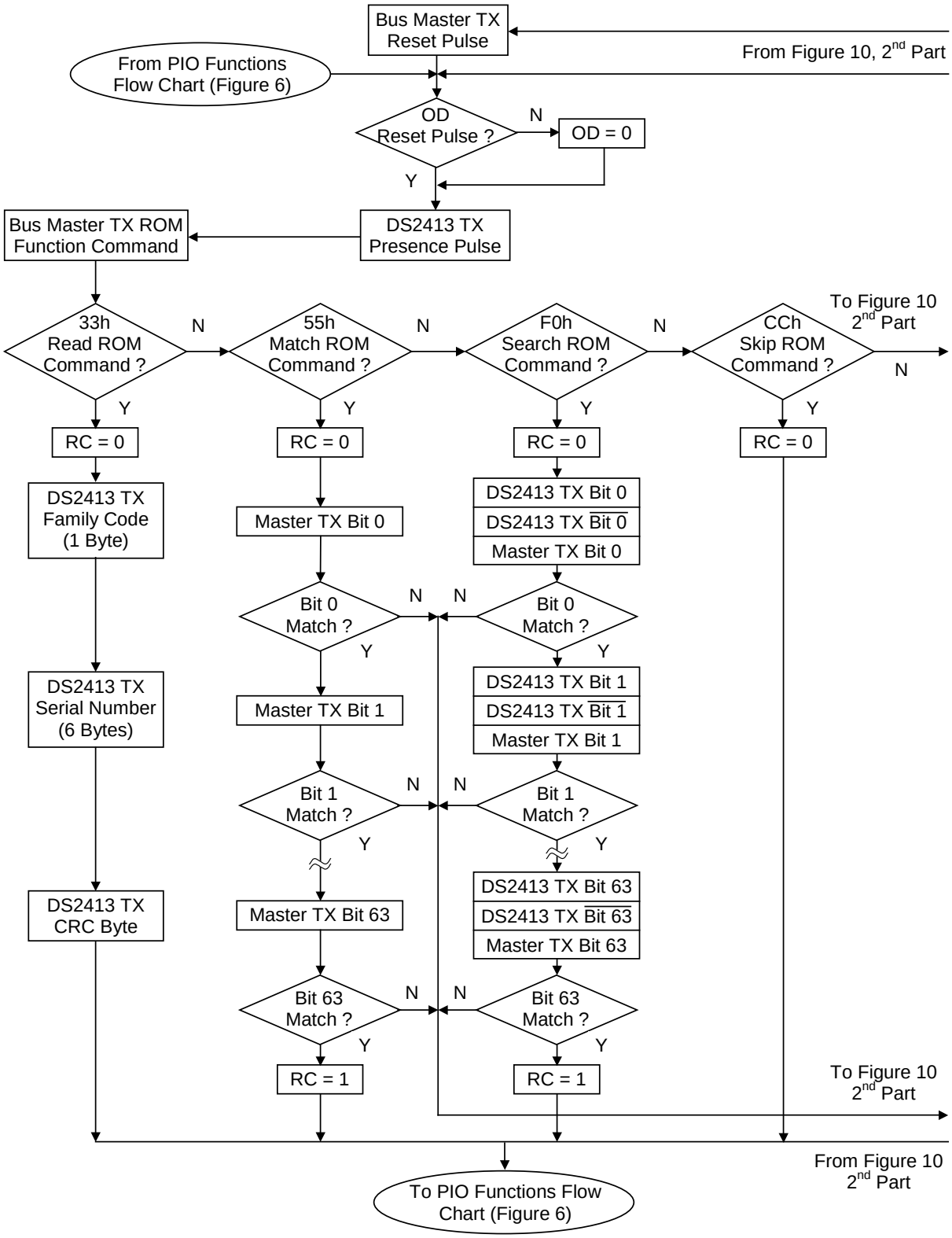
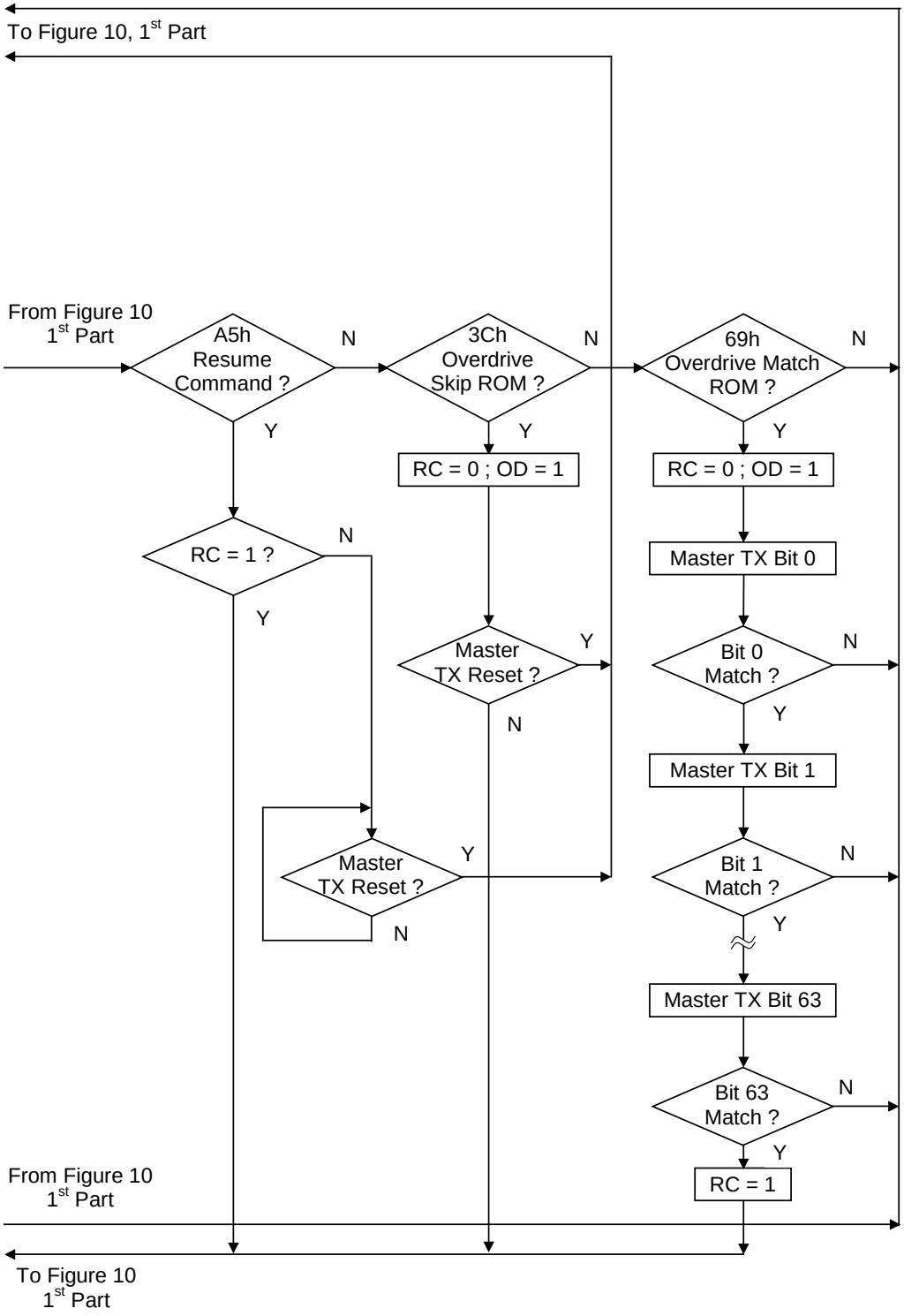


Figure 10-2. ROM Functions Flow Chart (continued)



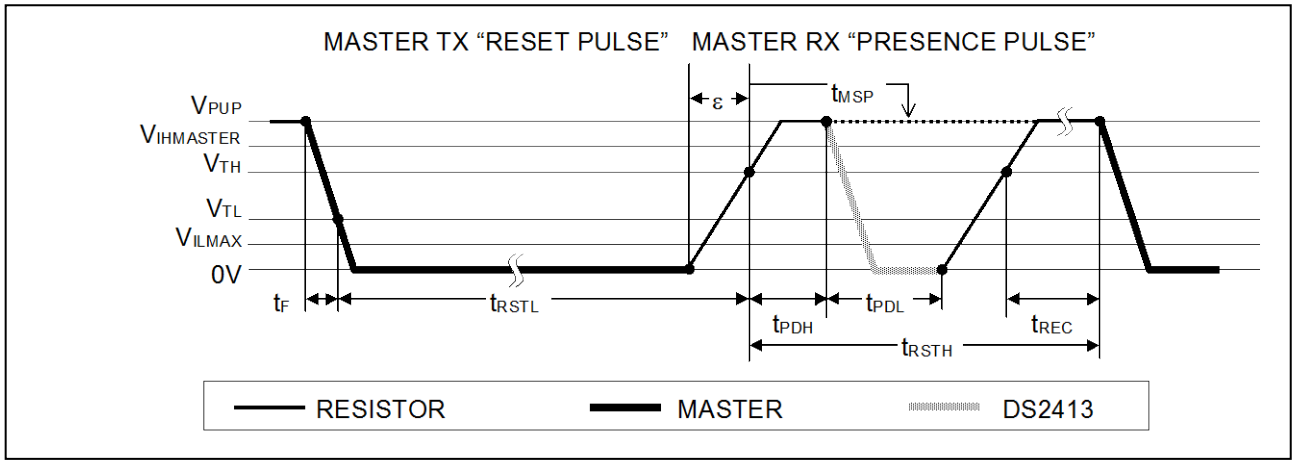
1-Wire SIGNALING

The DS2413 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write-Zero, Write-One, and Read-Data. Except for the Presence pulse, the bus master initiates all falling edges. The DS2413 can communicate at two different speeds, standard speed, and Overdrive Speed. If not explicitly set into the Overdrive mode, the DS2413 communicates at standard speed. While in Overdrive Mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 11 as 'ε' and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS2413 when determining a logical level, not triggering any events.

Figure 11 shows the initialization sequence required to begin any communication with the DS2413. A Reset Pulse followed by a Presence Pulse indicates the DS2413 is ready to receive data, given the correct ROM and PIO Function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for t_{RSTL} + t_F to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the Overdrive Mode, returning the device to standard speed. If the DS2413 is in Overdrive Mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive Mode. If the device is in Overdrive Mode and t_{RSTL} is *between* 80µs and 480µs, the device will reset, but the communication speed is undetermined.

Figure 11. Initialization Procedure: Reset and Presence Pulse



After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor, or in case of a DS2482-x00 or DS2480B driver, by active circuitry. When the threshold V_{TH} is crossed, the DS2413 waits for t_{PDH} and then transmits a Presence Pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

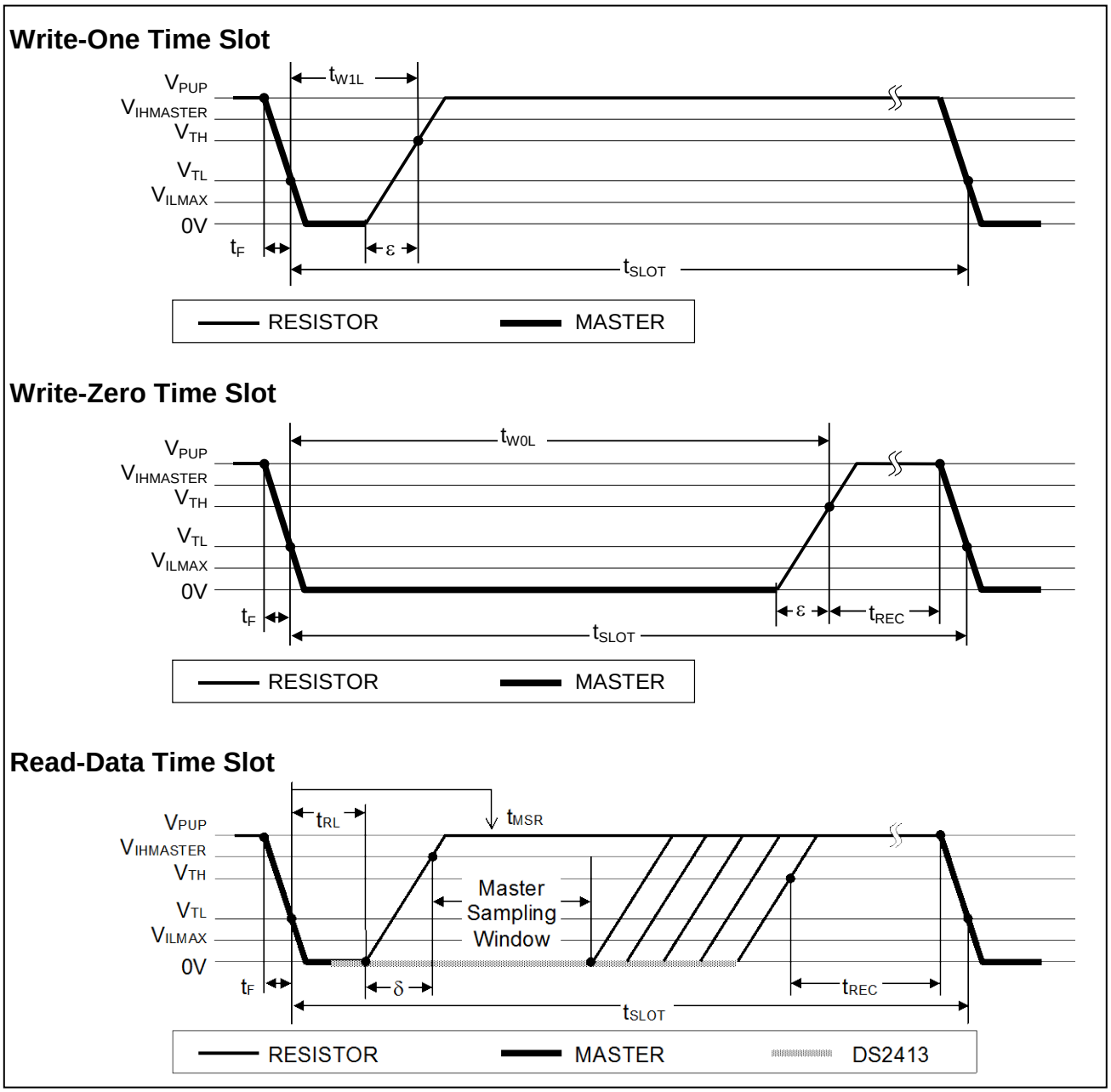
The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS2413 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at Overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS2413 takes place in time slots, which carry a single bit each. Write-time slots transport data from bus master to slave. Read-time slots transfer data from slave to master. Figure 12 illustrates the definitions of the write- and read-time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS2413 starts its internal timing generator that determines when the data line is sampled during a write-time slot and how long data is valid during a read-time slot.

Figure 12. Read/Write Timing Diagram



Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS2413 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS2413 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS2413 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of $t_{RL} + \delta$ (rise time) on one side and the internal timing generator of the DS2413 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS2413 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS2413 attached to a 1-Wire line. For multidevice configurations, t_{REC} needs to be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

IMPROVED NETWORK BEHAVIOR (SWITCHPOINT HYSTERESIS)

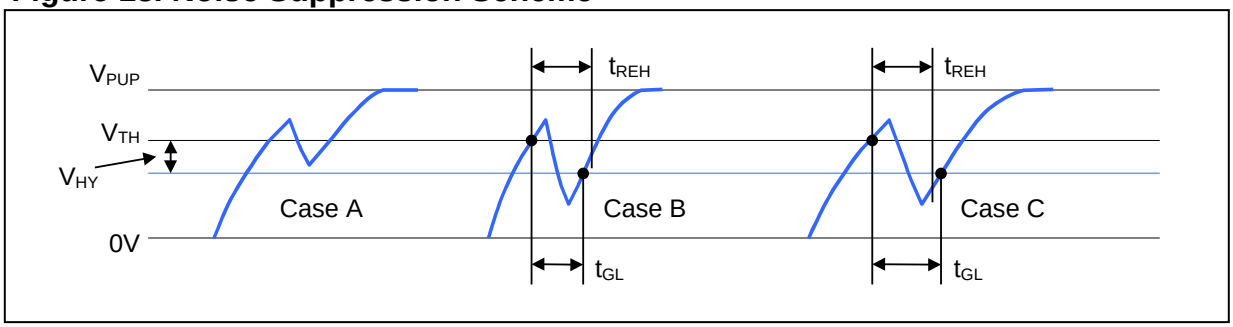
In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up, or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS2413 uses a new 1-Wire front end, which makes it less sensitive to noise and also reduces the magnitude of noise injected by the slave device itself.

The 1-Wire front end of the DS2413 differs from traditional slave devices in four characteristics.

1) The falling edge of the presence pulse has a controlled slew rate. This provides a better match to the line impedance than a digitally switched transistor, converting the high-frequency ringing known from traditional devices into a smoother low-bandwidth transition. The slew-rate control is specified by the parameter t_{FPD}, which has different values for standard and Overdrive speed.
2) There is additional low-pass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at Overdrive speed.
3) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below $V_{TH} - V_{HY}$, it will not be recognized (Figure 13, Case A). The hysteresis is effective at any 1-Wire speed.
4) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below $V_{TH} - V_{HY}$ threshold (Figure 13, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 13, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters t_{FPD}, V_{HY}, and t_{REH} specified in their electrical characteristics use the improved 1-Wire front end.

Figure 13. Noise Suppression Scheme



COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—LEGEND

SYMBOL	DESCRIPTION
RST	1-Wire Reset Pulse generated by master.
PD	1-Wire Presence Pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol.
PIOR	Command "PIO Access Read".
PIOW	Command "PIO Access Write".
FF loop	Indefinite loop where the master reads FF bytes.

COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—COLOR CODES

Master to slave	Slave to master

PIO ACCESS READ (CANNOT FAIL)

RST	PD	Select	PIOR	<PIO Status Byte>

Continues until master sends Reset Pulse

PIO ACCESS WRITE (SUCCESS)

RST	PD	Select	PIOW	<PIO Output data>	<PIO Output data>	<AAh>	<PIO Status Byte>

Loop until master sends Reset Pulse

PIO ACCESS WRITE (INVALID DATA BYTE)

RST	PD	Select	PIOW	<PIO Output data>	<invalid data byte>	FF loop

PIO ACCESS READ EXAMPLE

Read the state of the PIOs 3 times.
With only a single DS2413 connected to the bus master, the communication looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	F5h	Issue “PIO Access Read” command
RX	<3 data bytes>	Read 3 PIO samples
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse

PIO ACCESS WRITE EXAMPLE

Set both PIOs to 0 and then set PIOA to 1. Both PIOs are pulled high to V_{CC} or V_{PUP} by a resistor.
With only a single DS2413 connected to the bus master, the communication looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	5Ah	Issue “PIO Access Write” command
TX	FCh	Write new PIO output state
TX	03h	Write inverted new PIO output state
RX	AAh	Read confirmation byte
RX	F0h	Read new PIO pin status
TX	FDh	Write new PIO output state
TX	02h	Write inverted new PIO output state
RX	AAh	Read confirmation byte
RX	C3h	Read new PIO pin status
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse

Note: Usually, the PIO pin state and PIO Output Latch State are the same. To read from a PIO, the PIO Output Latch must be 1. If the PIO pin is then pulled low by a switch or external circuitry, the output latch state and pin state are different.

PACKAGE INFORMATION

For the latest package outline information, go to www.maxim-ic.com/packages. Note that a “+”, “#”, or “-“ in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN
6 TSOC	D6+1	**21-0382**	**90-0321**
6 TDFN	T633+2	**21-0137**	**90-0058**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
11/07	• Remove epsilon from the tW1L spec in the EC table. • Apply EC table note 17 also to tWOL. • Add to EC table notes 17 and 18 the reference to Figure 12 and the text "The actual maximum duration...." • Show epsilon also in the write zero time slot graphic. • Add note that the V_{TH} and V_{TL} maximum spec values apply at V_{PUP} max (V_{TH} and V_{TL} are GBD, not tested). • Added 3mm x 3mm x 0.8mm TDFN package. • LF update, delete standard versions (with lead) from ordering info. • Added Package Information Table.	1, 3, 4, 14, 17, 18
11/08	• Added “TDFN Packages Available” within the *Features* section. • Added new TDFN part number “DS2413Q+T&R,” and information to the *Ordering Information* table. • Removed the note to “Contact factory for availability of the TDFN package” from the *Ordering Information* table.	1
07/10	• Changed soldering temperature from JEDEC reference to explicit values. • Added DS2482-related application hints to EC table, Note 2. • Removed reference to the DS2490. • Added land pattern reference.	2–3, 17
11/14	• Updated *SEARCH ROM [F0h]* section	10
3/15	• Updated *Benefits and Features* section	1

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