Data Sheet | August 25, 2005 | FN2979.2

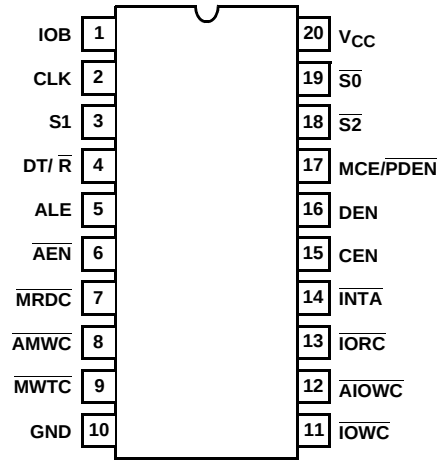
CMOS Bus Controller

The Intersil 82C88 is a high performance CMOS Bus Controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C88 provides the control and command timing signals for 80C86, 80C88, 8086, 8088, 8089, 80186, and 80188 based systems. The high output drive capability of the 82C88 eliminates the need for additional bus drivers.

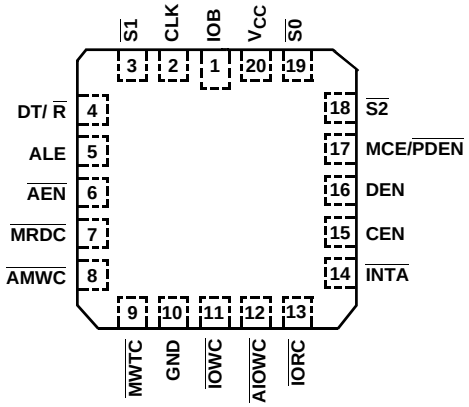
Static CMOS circuit design insures low operating power. The Intersil advanced SAJI process results in performance equal to or greater than existing equivalent products at a significant power savings.

Pinouts

20 LD PDIP, CERDIP
TOP VIEW



20 LD PLCC, CLCC
TOP VIEW



Features

- Compatible with Bipolar 8288
- Performance Compatible with:
  - 80C86/80C88 . . . . . (5/8MHz)
  - 80186/80188. . . . . (6/8MHz)
  - 8086/8088. . . . . (5/8MHz)
  - 8089
- Provides Advanced Commands for Multi-Master Busses
- Three-State Command Outputs
- Bipolar Drive Capability
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Power Operation
  - ICCSB. . . . . .10µA (Max)
  - ICCOP . . . . . 1mA/MHz (Max)
- Operating Temperature Ranges
  - C82C88 . . . . . 0°C to +70°C
  - I82C88 . . . . . .-40°C to +85°C
  - M82C88 . . . . . .-55°C to +125°C
- Pb-Free Plus Anneal Available (RoHS Compliant)

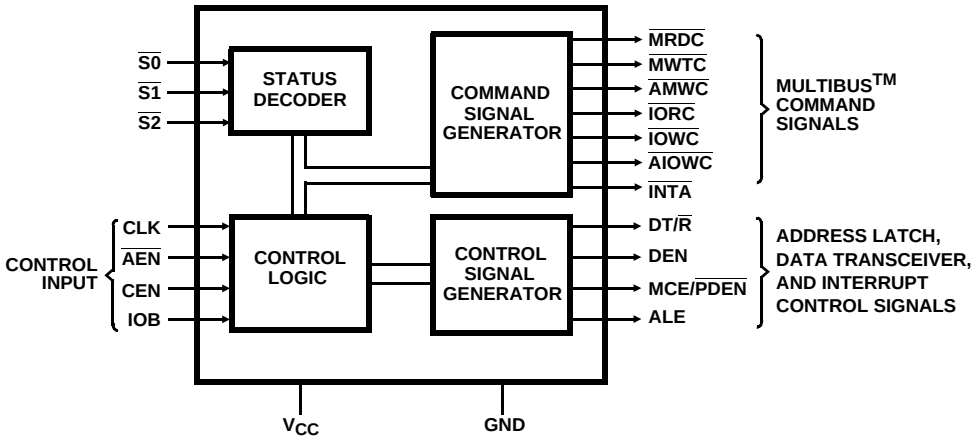
Ordering Information

PART NUMBER	PART MARKING	PACKAGE	TEMP RANGE (°C)	PKG. DWG. #
CP82C88	CP82C88	20 Ld PDIP	0 to +70	E20.3
CP82C88Z (Note)	CP82C88Z	20 Ld PDIP (Pb-free)	0 to +70	E20.3
CP82C88-10	CP82C88-10	20 Ld PDIP	0 to +70	E20.3
IP82C88	IP82C88		-40 to +85	E20.3
CS82C88	CS82C88	20 Ld PLCC	0 to +70	N20.35
IS82C88	IS82C88		-40 to +85	N20.35
CD82C88	CD82C88	20 Ld CERDIP	0 to +70	F20.3
ID82C88	ID82C88		-40 to +85	F20.3
MD82C88/B	MD82C88/B		-55 to +125	F20.3
8406901RA	8406901RA	SMD#		F20.3
MR82C88/B	MR82C88/B	20 Pad CLCC	-55 to +125	J20.A
84069012A	84069012A	SMD#		J20.A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Diagram



Pin Description

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
V_{CC}	20		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins 10 and 20 is recommended for decoupling.
GND	10		GROUND.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	19, 3, 18	I	STATUS INPUT PINS: These pins are the input pins from the 80C86, 80C88,8086/88, 8089 processors. The 82C88 decodes these inputs to generate command and control signals at the appropriate time. When Status pins are not in use (passive), command outputs are held HIGH (See Table1).
CLK	2	I	CLOCK: This is a CMOS compatible input which receives a clock signal from the 82C84A or 82C85 clock generator and serves to establish when command/control signals are generated.
ALE	5	O	ADDRESS LATCH ENABLE: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches, such as the 82C82 and 82C83H.
DEN	16	O	DATA ENABLE: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	4	O	DATA TRANSMIT/RECEIVE: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (read from I/O or memory).
$\overline{AEN}$	6	I	ADDRESS ENABLE: $\overline{AEN}$ enables command outputs of the 82C88 Bus Controller a minimum of 110ns (250ns maximum) after it becomes active (LOW). $\overline{AEN}$ going inactive immediately three-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the 82C88 is in the I/O Bus mode (IOB tied HIGH).
CEN	15	I	COMMAND ENABLE: When this signal is LOW all 82C88 command outputs and the DEN and PDEN control outputs are forced to their Inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	1	I	INPUT/OUTPUT BUS MODE: When the IOB pin is strapped HIGH, the 82C88 functions in the I/O Bus mode. When it is strapped LOW, the 82C88 functions in the System Bus mode (See I/O Bus and System Bus sections).
$\overline{AIOWC}$	12	O	ADVANCED I/O WRITE COMMAND: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	11	O	I/O WRITE COMMAND: This command line instructs an I/O device to read the data on the data bus. The signal is active LOW.
$\overline{IORC}$	13	O	I/O READ COMMAND: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.

Pin Description (Continued)

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
$\overline{AMWC}$	8	O	ADVANCED MEMORY WRITE COMMAND: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	MEMORY WRITE COMMAND: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	7	O	MEMORY READ COMMAND: This command line instructs the memory to drive its data onto the data bus. $\overline{MRDC}$ is active LOW.
$\overline{INTA}$	14	O	INTERRUPT ACKNOWLEDGE: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	17	O	This is a dual function pin. MCE (IOB IS TIED LOW) Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master 82C59A Priority Interrupt Controller onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB IS TIED HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

Functional Description

The command logic decodes the three 80C86, 8086, 80C88, 8088, 80186, 80188 or 8089 status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) to determine what command is to be issued (see Table 1).

TABLE 1. COMMAND DECODE DEFINITION

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	PROCESSOR STATE	82C88 COMMAND
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O Bus Mode

The 82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode, all I/O command lines $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a “Bus Ready” signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode

The 82C88 is in the System Bus mode if the IOB pin is strapped LOW. In this mode, no command is issued until a specified time period after the $\overline{AEN}$ line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

The command outputs are:

$\overline{MRDC}$ - Memory Read Command

$\overline{MWTC}$ - Memory Write Command

$\overline{IORC}$ - I/O Read Command

$\overline{IOWC}$ - I/O Write Command

$\overline{AMWC}$ - Advanced Memory Write Command

$\overline{AIOWC}$ - Advanced I/O Write Command

$\overline{INTA}$ - Interrupt Acknowledge

Control Outputs

The control outputs of the 82C88 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/ Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the 82C88. When the 82C88 is in the IOB mode (IOB HIGH), the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the 82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence, there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case, the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the 82C82/82C83H address latches. ALE also serves to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the 82C88. If the CEN pin is high, the 82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not three-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C88 . . . . . 0°C to +70°C
I82C88 . . . . . -40°C to +85°C
M82C88 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	18
CLCC Package	85	22
PDIP Package	75	N/A
PLCC Package	75	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 100 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ± 10%;
T_A = 0°C to +70°C (C82C88);
T_A = -40°C to +85°C (I82C88);
T_A = -55°C to +125°C (M82C88)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	- -	V V	C82C88, I82C88 M82C88
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
VIHC	CLK Logical One Input Voltage	V_{CC} -0.8	-	V	
VILC	CLK Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Output High Voltage Command Outputs	3.0 V_{CC} -0.4	-	V V	I_{OH} = -8.0mA I_{OH} = -2.5mA
	Output High Voltage Control Outputs	3.0 V_{CC} -0.4	-	V V	I_{OH} = -4.0mA I_{OH} = -2.5mA
V_{OL}	Output Low Voltage Command Outputs	-	0.5	V	I_{OL}= +12.0mA
	Output Low Voltage Control Outputs	-	0.4	V	I_{OL} = +8.0mA
I_I	Input Leakage Current	-1.0	1.0	µA	V_{IN} = GND or V_{CC}, except $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, DIP Pins 1-2, 6, 15
IBHH	Input Leakage Current-Status Bus	-50	-300	µA	V_{IN} = 2.0V, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ (See Note 1)
IO	Output Leakage Current	-10.0	10.0	µA	V_O = GND or V_{CC}, IOB = GND, $\overline{AEN}$ = V_{CC}, DIP Pins 7-9, 11-14
ICCSB	Standby Power Supply	-	10	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	V_{CC} = 5.5V, Outputs Open (See Note 2)

NOTES:

1. IBHH should be measured after raising the V_{IN} on $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ to V_{CC} and then lowering to valid input high level of 2.0V.
2. ICCOP = 1mA/MHz of CLK cycle time (TCLCL)

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	10	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT	Output Capacitance	17	pF	

AC Electrical Specifications

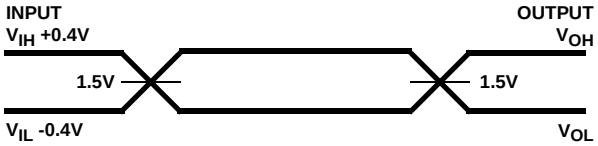
V_{CC} = 5.0V ± 10%;
T_A = 0°C to +70°C (C82C88);
T_A = -40°C to +85°C (I82C88);
T_A = -55°C to +125°C (M82C88)

SYMBOL	PARAMETER	8MHz		10MHz		12MHz		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS									
(1) TCLCL	CLK Cycle Period	125	-	100	-	83	-	ns	
(2) TCLCH	CLK Low Time	55	-	50	-	34	-	ns	
(3) TCHCL	CLK High Time	40	-	37	-	34	-	ns	
(4) TSVCH	Status Active Setup Time	35	-	35	-	35	-	ns	
(5) TCHSV	Status Inactive Hold Time	10	-	10	-	5	-	ns	
(6) TSHCL	Status Inactive Setup Time	35	-	35	-	35	-	ns	
(7) TCLSH	Status Active Hold Time	10	-	10	-	5	-	ns	
TIMING RESPONSES									
(8) TCVNV	Control Active Delay	5	45	5	45	5	45	ns	1
(9) TCVNX	Control Inactive Delay	10	45	10	45	10	35	ns	1
(10) TCLLH	ALE Active Delay (from CLK)	-	20	-	20	-	20	ns	1
(11) TCLMCH	MCE Active Delay (from CLK)	-	25	-	23	-	23	ns	1
(12) TSVLH	ALE Active Delay (from Status)	-	20	-	20	-	20	ns	1
(13) TSVMCH	MCE Active Delay (from Status)	-	30	-	23	-	23	ns	1
(14) TCHLL	ALE Inactive Delay	4	18	4	18	4	18	ns	1
(15) TCLML	Command Active Delay	5	35	5	35	5	35	ns	2
(16) TCLMH	Command Inactive Delay	5	35	5	35	5	35	ns	2
(17) TCHDTL	Direction Control Active Delay	-	50	-	50	-	50	ns	1
(18) TCHDTH	Direction Control Inactive Delay	-	30	-	30	-	30	ns	1
(19) TAELCH	Command Enable Time (Note 1)	-	40	-	40	-	40	ns	3
(20) TAEHCZ	Command Disable Time (Note 2)	-	40	-	40	-	40	ns	4
(21) TAELCV	Enable Delay Time	110	250	110	250	110	250	ns	2
(22) TAEVNV	$\overline{AEN}$ to DEN	-	25	-	25	-	25	ns	1
(23) TCEVNV	CEN to DEN, $\overline{PDEN}$	-	25	-	25	-	25	ns	1
(24) TCELRH	CEN to Command	-	TCLML +10	-	TCLML	-	TCLML	ns	2
(25) TLHLL	ALE High Time	TCLCH - 10	-	TCLCH - 10	-	TCLCH - 10	n	ns	1

NOTES:

1. TAELCH measurement is between 1.5V and 2.5V.
2. TAEHCZ measured at 0.5V change in VOUT.

AC Testing Input, Output Waveform



A.C. Testing: All input signals (other than CLK) must switch between V_{IL} -0.4V and V_{IH} +0.4. CLK must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times are driven at 1ns/V.

A.C. Test Circuit

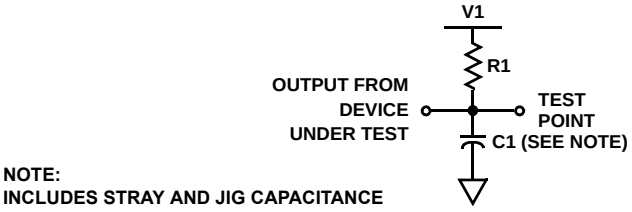
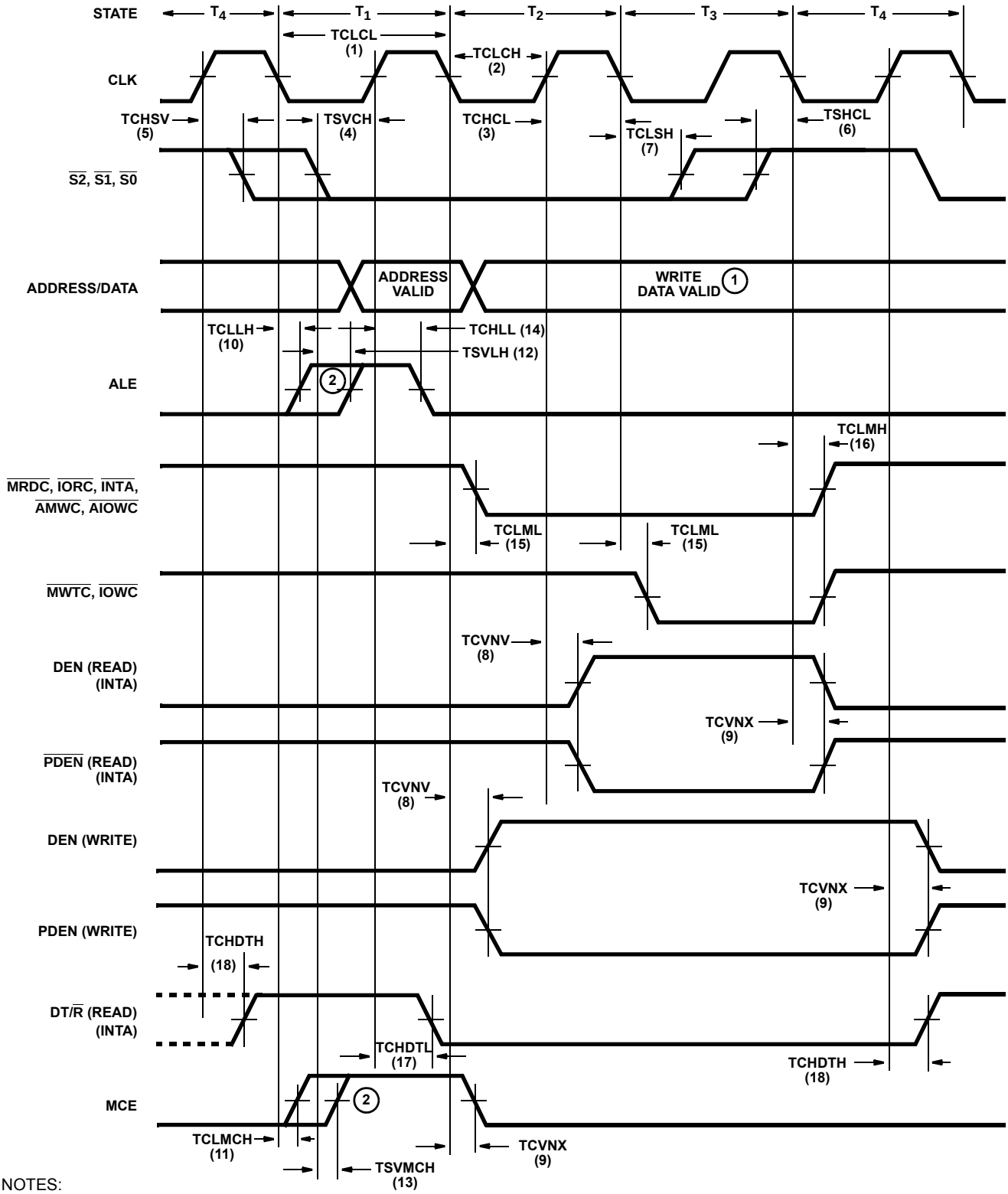


TABLE 2. TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	C1
1	2.13V	220Ω	80pF
2	2.29V	91Ω	300pF
3	1.5V	187Ω	300pF
4	1.5V	187Ω	50pF

Timing Waveforms (Note 3)



NOTES:

1. Address/Data Bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active. Whichever occurs last.
3. All timing measurements are made at 1.5V unless otherwise specified.

FIGURE 1.

Timing Waveforms (Note 3) **(Continued)**

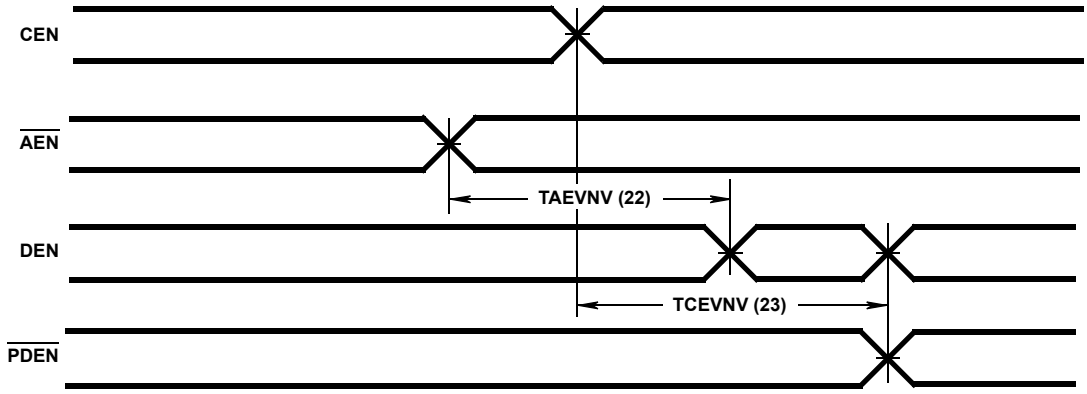
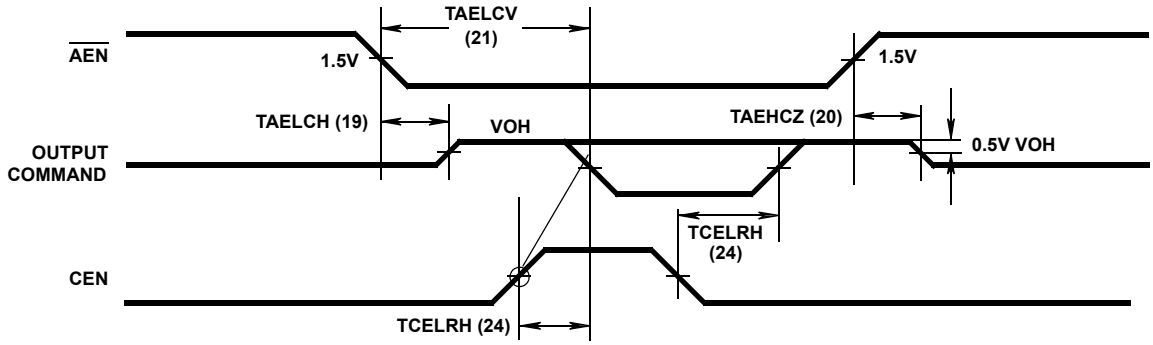


FIGURE 2. DEN, $\overline{\text{PDEN}}$ QUALIFICATION TIMING



CEN MUST BE LOW OR INVALID PRIOR TO T2 TO PREVENT THE COMMAND FROM BEING GENERATED.

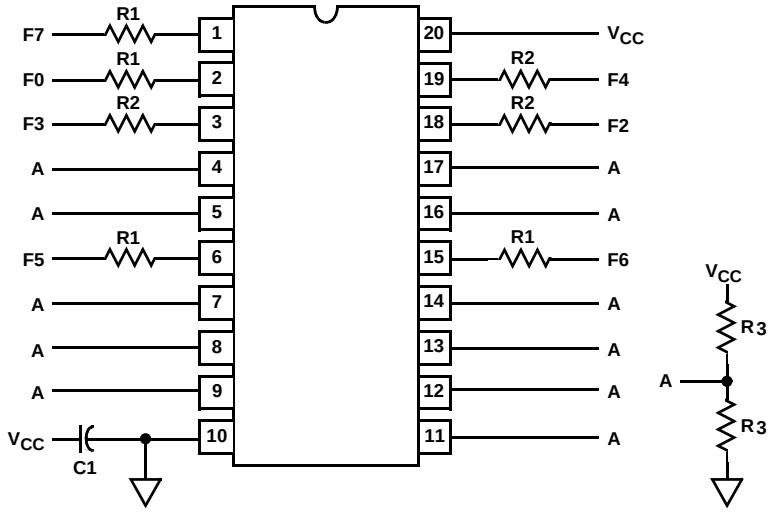
FIGURE 3. ADDRESS ENABLE ($\overline{\text{AEN}}$) TIMING (THREE-STATE ENABLE/DISABLE)

NOTES:

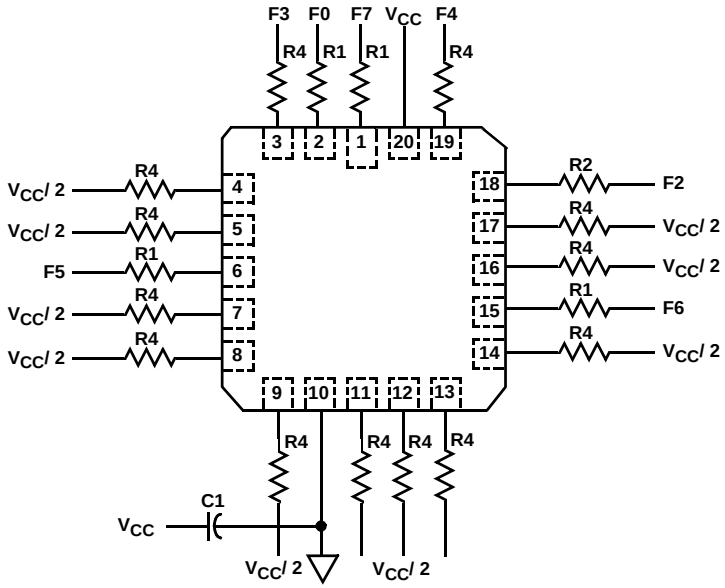
1. Address/Data Bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active. Whichever occurs last.
3. All timing measurements are made at 1.5V unless otherwise specified.

Burn-In Circuits

MD82C88 CERDIP



MR82C88 CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V
   GND = 0V
2. V_{IH} = 4.5V ± 10%
   V_{IL} = -0.2V to +0.4V
3. Component Values:
   R1 = 47kΩ, 1/4W, 5%
   R2 = 1.5kΩ, 1/4W, 5%
   R3 = 10kΩ, 1/4W, 5%
   R4 = 1.2kΩ, 1/4W, 5%
   C1 = 0.01μF (Min)
   F0 = 100kHz ± 10%
   F1 = F0/2
   F2 = F1/2 . . . F7 = F6/2

Die Characteristics

DIE DIMENSIONS:
103.5 x 116.5 x 19 ± 1mils

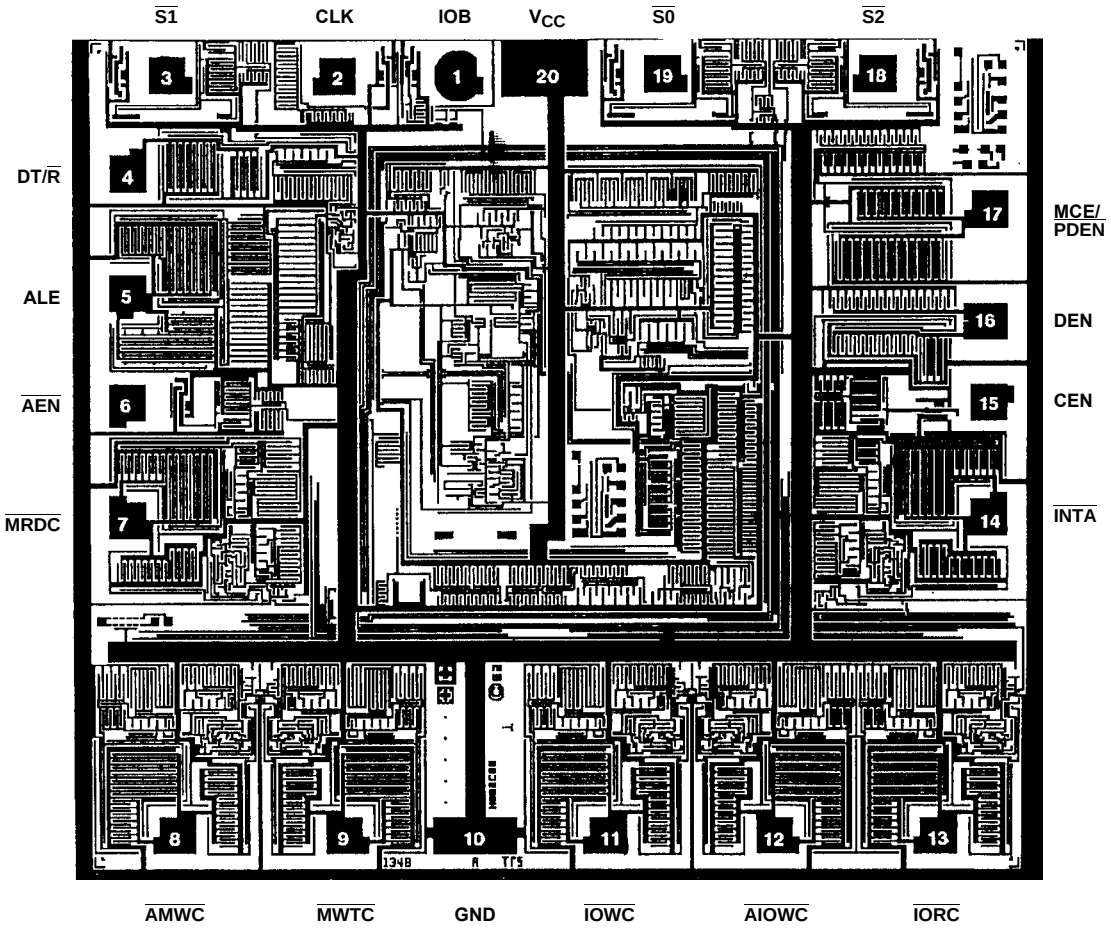
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
1.9×10^5 A/cm^2

Metallization Mask Layout

82C88



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