

DATA SHEET

CLA Series: Silicon Limiter Diodes, Packaged and Bondable Chips

Applications

- Limiters

Features

- Established Skyworks limiter diode process
- High power, mid-range, and cleanup designs
- Low insertion loss: 0.1 dB @ 10 GHz
- Power handling to +66 dBm
- Tight control of I layer base width
- Mesa and planar chip designs

NEW



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Description

Skyworks CLA series of silicon limiter diodes provides passive receiver protection over a wide range of frequencies from 100 MHz to over 30 GHz. These devices use Skyworks well-established silicon technology resulting in high resistivity and tightly controlled base width PIN limiter diodes. Limiter circuits using these devices perform with strong limiting action and low loss.

The CLA series consists of nine individual chip designs of different intrinsic region base widths and capacitances designed to accommodate multi-stage limiter applications. The mesa-constructed, thin base width, low capacitance CLA4601-000, CLA4602-000, CLA4604-000, and CLA4605-000 are designed for low-level and cleanup applications. The CLA4603-000 and CLA4606-000 through CLA4608-000 are planar designs designated for high-power and mid-range applications.

The CLA4609-000 thick base width mesa diode is designed for coarse limiter-stage applications.

The absolute maximum ratings of the CLA diode series are provided in Table 1. Electrical specifications are specified in Table 2. Typical performance characteristics are provided in Table 3 and Figures 1 through 5. Table 4 identifies the die part numbers with their corresponding top contact diameters and die outline drawings. Table 5 identifies the hermetic part numbers together with their thermal resistance specifications and hermetic outline drawings.

Table 1. CLA Series Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power dissipation	P_{DIS}			$\frac{\text{Maximum } T_J - \text{Case Temp}}{\text{Thermal Resistance}_{\text{junction-to-case}}}$	W
Reverse voltage	V_R			Minimum rated breakdown voltage	V
Forward current	I_F			200	mA
Junction temperature	T_J	-65		+175	°C
Storage temperature	T_{STG}	-65		+200	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 2. CLA Series Electrical Specifications (Note 1)

($T_{OP} = +25\text{ °C}$, C_J Measured at 1 MHz, R_S Measured at 500 MHz, CW Thermal Resistance for Infinite Heat Sink, Pulse Thermal Resistance for Single 1 μs Pulse, Unless Otherwise Noted)

Part Number	Breakdown Voltage (V)	I Region (μm)	Junction Capacitance (C_J) @ 0 V (pF)	Junction Capacitance (C_J) @ 6 V (pF)	Series Resistance (R_S) @ 10 mA (Ω)	Minority Carrier Lifetime (T_L) @ 10 mA (ns)	Thermal Impedance (θ)	
							Average (°C/W)	1 μs Pulse (°C/W)
	Min – Max	Nominal	Typical	Maximum	Maximum	Typical	Maximum	Typical
CLA4601-000	15 – 30	1	0.12	0.10	2.5	5	120	15
CLA4602-000	15 – 30	1	0.20	0.15	2.0	5	80	10
CLA4603-000	20 – 45	1.5	0.20	0.15	2.0	5	100	10
CLA4604-000	30 – 60	2.0	0.12	0.10	2.5	7	100	10
CLA4605-000	30 – 60	2.0	0.20	0.15	2.0	7	70	7.0
CLA4606-000	45 – 75	2.5	0.20	0.15	2.0	10	80	7.0
CLA4607-000	120 – 180	7.0	0.20	0.15 @ 50 V	2.0	50	40	1.2
CLA4608-000	120 – 180	7.0	0.80	0.50 @ 50 V	1.2	100	15	0.3
CLA4609-000	250 (Min.)	28	0.26	0.14	1.5	1175	15	0.3

Note 1: Performance is guaranteed only under the conditions listed in this Table and is not guaranteed over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.

Table 3. Typical Performance @ 25 °C

Part Number	Insertion Loss @ -10 dBm (dB)	Input Power for 1 dB Loss (dBm)	Maximum Pulsed Input Power (dBm)	Output @ Maximum Pulsed Input (dBm)	Maximum CW Input power (W)	Recovery Time (ns)
CLA4601-000	0.1	7	47	21	2	5
CLA4602-000	0.1	7	50	24	3	5
CLA4603-000	0.1	10	50	22	2	10
CLA4604-000	0.1	12	47	24	3	10
CLA4605-000	0.1	12	50	27	4	10
CLA4606-000	0.1	15	53	27	3	20
CLA4607-000	0.1	20	60	39	6	50
CLA4608-000	0.2	20	66	44	15	100
CLA4609-000	0.3	38	70	50	20	1000

Notes:

Insertion loss for CLA4601-000 through CLA4607-000 @ 10 GHz. Insertion loss for CLA4608-000 @ 5 GHz. Insertion loss for CLA4609-000 @ 2.1 GHz.

Limiter power results @ 1 GHz for shunt connected, single limiter diode and DC return in 50 Ω line.

Maximum pulsed power for 1 μs pulse and 0.1% duty factor with chip @ 25 °C heat sink. Derate linearly to 0 W @ 175 °C.

Maximum CW input power @ 25 °C heat sink. Derate linearly to 0 W @ 175 °C.

Recovery time to insertion loss from limiting state.

Table 4. CLA Series Parts – Die Packages

Part Number	Typical Top Contact Diameter (mils/mm)	Die Drawing
CLA4601-000	1.10/0.028	150-806
CLA4602-000	1.25/0.032	150-806
CLA4603-000	2.00/0.050	149-815
CLA4604-000	1.65/0.042	150-806
CLA4605-000	2.05/0.052	150-813
CLA4606-000	2.25/0.057	149-815
CLA4607-000	3.50/0.089	149-815
CLA4608-000	7.50/0.190	149-815
CLA4609-000	6.50/0.165	150-813

Table 5. Hermetic Packages

Hermetic Stripline Drawing	Typical θ_{JC} (°C/W)	Hermetic Pill Drawing	Typical θ_{JC} (°C/W)	Hermetic Pill Drawing	Typical θ_{JC} (°C/W)	Hermetic Pill Drawing	Typical θ_{JC} (°C/W)
CLA4601-240	200	CLA4601-203	150	CLA4601-219	200	CLA4601-210	140
CLA4602-240	160	CLA4602-203	110	CLA4602-219	160	CLA4602-210	100
CLA4603-240	180	CLA4603-203	130	CLA4603-219	180	CLA4603-210	120
CLA4604-240	160	CLA4604-203	130	CLA4604-219	180	CLA4604-210	120
CLA4605-240	150	CLA4605-203	100	CLA4605-219	150	CLA4605-210	90
CLA4606-240	160	CLA4606-203	110	CLA4606-219	160	CLA4606-210	100
CLA4607-240	120	CLA4607-203	70	CLA4607-219	120	CLA4607-210	60
CLA4608-240	100	CLA4608-203	45	CLA4608-219	100	CLA4608-210	35
CLA4609-240	100	CLA4609-203	45	CLA4609-219	100	CLA4609-210	35

Typical Performance Characteristics at 25 °C

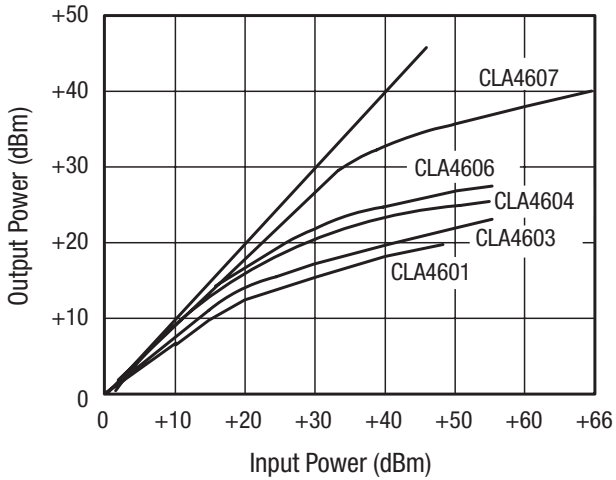


Figure 1. Typical Peak Leakage Power @ 1 GHz



Figure 2. Normalized Pulsed Thermal Impedance

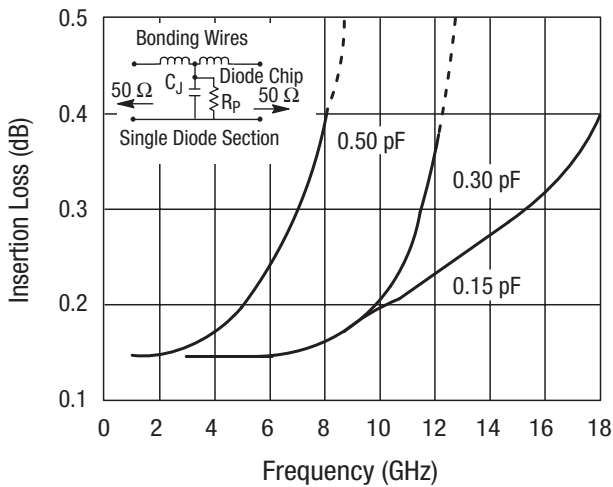


Figure 3. Typical Diode Insertion Loss vs Frequency



Figure 4. Typical Peak Leakage Power @ 1 GHz

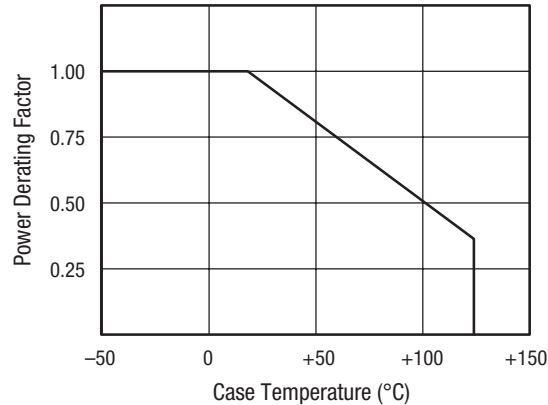


Figure 5. Power Handling Capability vs Temperature

Technical Description

The CLA4603 and CLA4606 limiter diodes are constructed in a passivated flat-chip configuration and are available in a basic chip form or encapsulated in several Skyworks hermetic ceramic packages.

Limiter diodes with lower capacitance values to 0.08 pF and constructed with a passivated mesa configuration are available in the CLA4601 and CLA4605 series. The mesa devices offer low capacitance and, therefore, broader bandwidth, lower loss, and faster response at reduced power. These diodes are also available in chip package form and represent the ultimate in limiter performance not approached by other manufacturers.

The CLA4607 diodes (highest power) are available in both planar and mesa construction.

Figures 6 and 7 illustrate the fundamental structures of diodes mounted in a 50 Ω microstrip circuit.

Additional bonding and handling methods are contained in the Skyworks Application Notes, *Waffle Pack Chip Carrier Handling/Opening Procedure* (document #200146) and *Diode Chips, Beam-Lead Diodes, Capacitors: Bonding Methods and Packaging* (document #200146).

Basic Applications

In microstrip limiters, the bonding wire length and diameter together with the chip capacitance, form a low-pass filter (see Figure 8). Line lengths (X1 and X2) are varied to provide broadband matching and flat leakage characteristics. Typically, X1 and X2 are on the order of 0.1 wavelength. In Figure 9, the CLA4607 chip provides about 20 dB attenuation, reducing a 1 kW input signal to a 10 W output signal. The CLA4606 reduces this to 100 mW and the CLA4603 to about 20 mW.

During the rise time of the incident pulse, the diodes behave in the following manner. The CLA4603, due to its thin I region, is the first to change to a low impedance. Experiments indicate that the CLA4603 reaches the 10 dB isolation point in about 1 ns and 20 dB in 1.5 ns with an incident power of 10 W.

The CLA4606 takes about 4 ns and the CLA4607 about 50 ns to achieve 10 dB isolation. Consequently, the CLA4603 provides protection during the initial stages of pulse rise time with the thicker diodes progressively “turning on” as the power increases. With proper spacing (X1 and X2), the “on” diodes reflect high impedances to the upstream diodes, reducing the turn-on time for those diodes and ensuring that essentially all of the incident power is reflected by the input diode, preventing burnout of the thinner diodes.

At the end of the pulse the process reverses and the diodes “recover” to their high impedance states; the free charge that was injected into their I regions by the high-incident power signal leaks off through the ground return and is also reduced by internal recombination. With a ground return, recovery time is on the order of 50 ns. With a high impedance return (for example, the circuit shown in Figure 10), the Schottky diode (such as the CDF7621-000) recovers or “opens” in practically zero time. Internal recombination on the order of several diode lifetimes is the only available mechanism for recovery of the limiter diodes. This recovery time can be long – on the order of 1 ms for the CLA4607 series. The shunt resistor (R_R) minimizes the problem. One hundred Ohms approximately doubles the recovery time compared to a short circuit.

When the Schottky diode is directly coupled to the transmission line in cascade after the coarse limiter, the leakage power is less than if a 0 Ω ground return were used. If the Schottky is decoupled too much, the leakage power increases due to the high DC impedance of a Schottky. Similarly, a 3 Ω ground return causes an increase of about 3 dB in leakage power compared to a 0 Ω return.

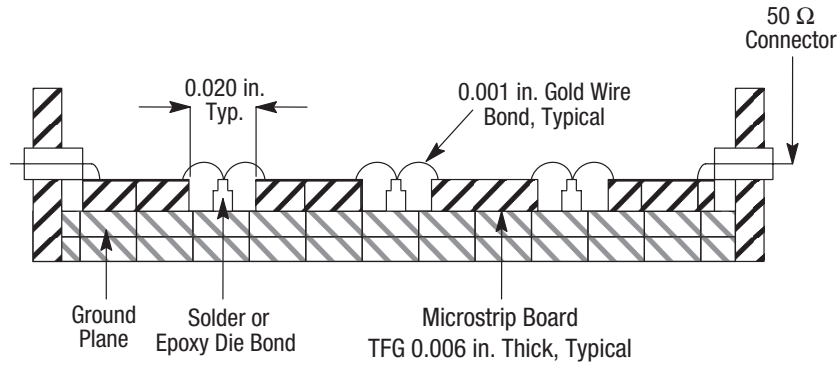


Figure 6. Diodes in 50 Ω Microstrip Circuit (Side View)



Figure 7. Diodes in 50 Ω Microstrip Circuit (Top View)

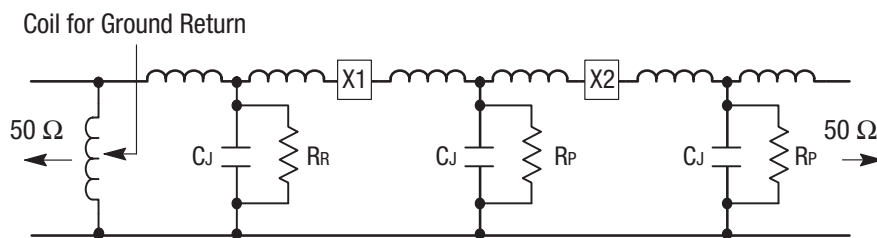


Figure 8. Low-Level Equivalent Circuit



Figure 9. Cascaded Limiter Design



Figure 10. Quasi-Active Limiter Design



Figure 11. High-Power Equivalent Circuit

Package Outline Drawings

Package outline die drawings for the CLA diode series are shown in Figures 12, 13, and 14. Hermetic package outlines are shown in Figures 15 through 18.

Die Packages



Figure 12. 149-815 Package



Figure 13. 150 Series Package

Die Packages (Continued)



Figure 14. 150-813 Package

Hermetic Packages



Figure 15. -203 Package



Figure 16. -210 Package

Hermetic Packages (Continued)



Figure 17. -219 Package



Figure 18. -240 Package

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