

ISL85403DEMO1Z

Demonstration Board

AN1960
Rev 1.00
Mar 13, 2015

Description

The ISL85403DEMO1Z board allows quick evaluation of the ISL85403 in the synchronous buck configuration. It also demonstrates the compact size solution for the wide input voltage range point-of-load DC/DC converter using ISL85403.

Specifications

The design specifications of the ISL85403DEMO1Z are shown in [Table 1](#).

TABLE 1. SPECIFICATIONS

PARAMETERS	VALUES
Input Voltage (V_{IN})	7V to 40V
Output Voltage (V_{OUT})	5.0V
Max. Output Current (I_{OUT_MAX})	2.5A
Switching Frequency	500kHz
Output Ripple	50mV at 2.5A Load
Peak Efficiency	93% at 50% Load, 12V Input

Key Features

- Small, compact design
- V_{IN} range of 7V to 40V
- V_{OUT} adjustable from 0.8V to 5V
- Convenient power connection

References

[ISL85403](#) Datasheet

Ordering Information

PART NUMBER	DESCRIPTION
ISL85403DEMO1Z	ISL85403 Evaluation kit, synchronous buck configuration 5V output

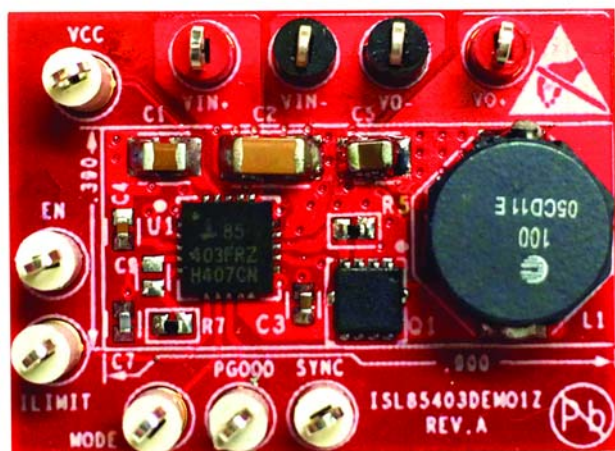


FIGURE 1. TOP VIEW

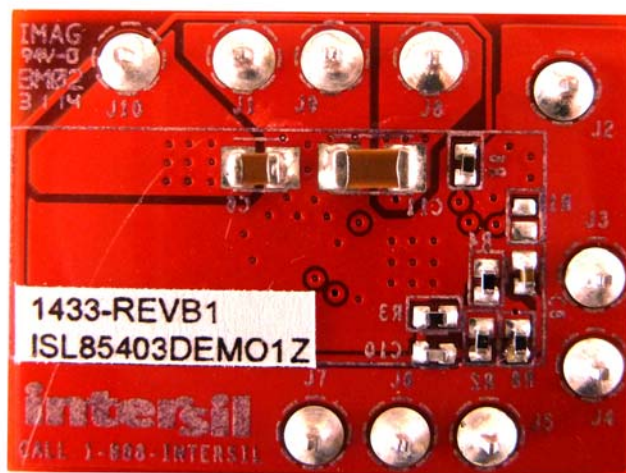


FIGURE 2. BOTTOM VIEW

Functional Description

The ISL85403 is a flexible switching regulator with an integrated 127mΩ high-side MOSFET. It can be used as a synchronous buck converter, a 2-stage boost-buck converter, or a noninverting buck-boost converter.

The ISL85403DEMO1Z board demonstrates the compact size and operations of the ISL85403 in the synchronous buck configuration. The ISL85403DEMO1Z board is shown in [Figures 1](#) and [2](#).

The schematic is shown on [page 3](#), bill of materials on [page 4](#), and PCB layers for reference start on [page 7](#). [Figures 4](#) through [12](#) show performance data taken from the demo board.

Operating Range

The board input voltage range is 7V to 40V. The output voltage is set to 5V and can be changed by voltage feedback resistors R_3 and R_4 , as shown in [Equation 1](#):

$$R_4 = R_3 \cdot \frac{V_{ref}}{V_{out} - V_{ref}} \quad (EQ. 1)$$

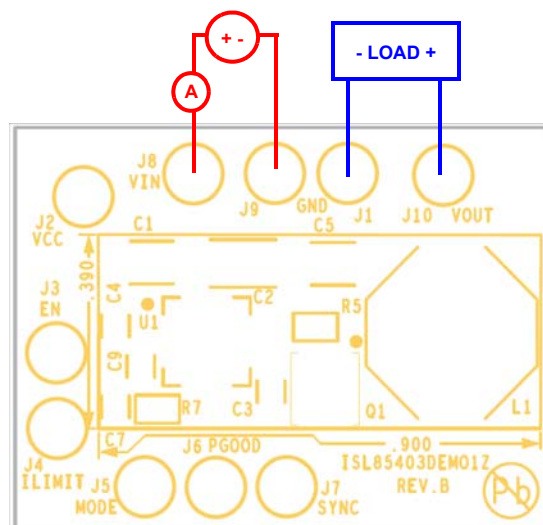
NOTE: In order to change to a higher output voltage, the output capacitors have to be changed for the higher voltage rating.

The board is set to a default frequency of 500kHz (FS pin/ R_1 is open). The switching frequency can be programmed to other values by a resistor at R_1 . Refer to the [ISL85403](#) datasheet for the resistor value and the switching frequency. The switching frequency can also be synchronized to external clock by connecting the external clock to the SYNC terminal (J7).

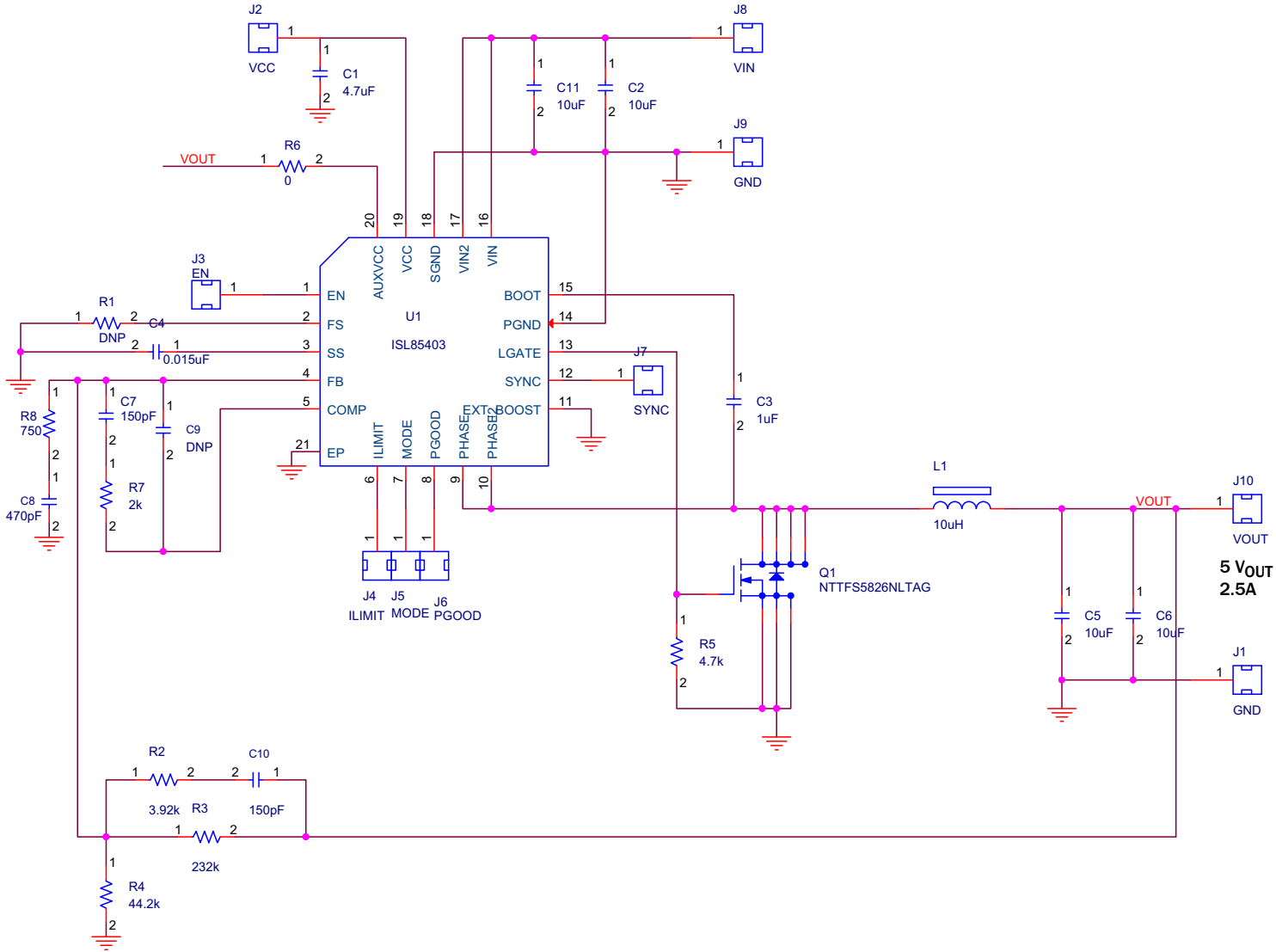
PCB Layout Guidelines

1. Place the input ceramic capacitors as closely as possible to the IC VIN pin and power ground connecting to the power MOSFET or Diode. Keep this loop (input ceramic capacitor, IC VIN pin and MOSFET/Diode) as tiny as possible to minimize the voltage spikes induced by the trace parasitic inductance.
2. Keep the phase node copper area small but large enough to handle the load current.
3. Place the output ceramic and aluminum capacitors close to the power stage components as well.
4. Place vias (at least 9) in the bottom pad of the IC. The bottom pad should be placed in ground copper plane with an area as large as possible in multiple layers to effectively reduce the thermal impedance.
5. Place the 4.7μF ceramic decoupling capacitor at the VCC pin (the closest place to the IC). Put multiple vias close to the ground pad of this capacitor.
6. Keep the bootstrap capacitor close to the IC.
7. Keep the LGATE drive trace as short as possible and try to avoid using via in the LGATE drive path to achieve the lowest impedance.
8. Place the output voltage sense trace close to the place that is to be strictly regulated.
9. Place all the peripheral control components close to the IC.

Quick Test Setup



ISL85403DEMO1Z Circuit Schematic



Bill of Materials

REF DES	PART NUMBER	QTY	DESCRIPTION	MANUFACTURER
C9		0	DNP	
C7, C10	VARIOUS	2	CAP, SMD, 0402, 150pF, 50V, 10%, C0G, ROHS	VARIOUS
C3	ECJ-OEB0J105M	1	CAP, SMD, 0402, 1μF, 6.3V, 20%, X5R, ROHS	PANASONIC
C4	VARIOUS	1	CAP, SMD, 0402, 0.015μF, 16V, 10%, X7R, ROHS	VARIOUS
C8	VARIOUS	1	CAP, SMD, 0402, 470pF, 50V, 10%, X7R, ROHS	VARIOUS
C5, C6	GRM21BR71A106KE51K	2	CAP, SMD, 0805, 10μF, 10V, 10%, X7R, ROHS	Murata
C1	GRM21BR71A475KA73L	1	CAP, SMD, 0805, 4.7μF, 10V, 10%, X7R, ROHS	Murata
C2, C11	C3216X5R1H106K	2	CAP, SMD, 1206, 10μF, 50V, 10%, X5R, ROHS	TDK
L1	SD8350-100-R	1	COIL-PWR INDUCTOR, SMD, 9.5x8.3, 10μH, 20%, 4A, 31.4mΩ, ROHS	COILTRONICS
U1	ISL85403IRZ	1	IC-SWITCHING REGULATOR, 20P, QFN, 4X4, ROHS	INTERSIL
Q1	NTTFS5826NLTAG	1	TRANSIST-MOS, N-CHANNEL, 8P, PG-TSDSON-8, 60V, 8A, ROHS	ON SEMI
R2	VARIOUS	1	RES, SMD, 0402, 3.92k, 1/16W, 1%, TF, ROHS	VARIOUS
R3	VARIOUS	1	RES, SMD, 0402, 232k, 1/16W, 1%, TF, ROHS	VARIOUS
R7	VARIOUS	1	RES, SMD, 0402, 2k, 1/16W, 1%, TF, ROHS	VARIOUS
R4	ERJ-2RK4422X	1	RES, SMD, 0402, 44.2k, 1/16W, 1%, TF, ROHS	VARIOUS
R5	VARIOUS	1	RES, SMD, 0402, 4.7k, 1/16W, 1%, TF, ROHS	VARIOUS
R6	VARIOUS	1	RES, SMD, 0402, 0Ω, 1/16W, 1%, TF, ROHS	VARIOUS
R1	N/A	0	Do not populate	N/A

Typical Performance Curves

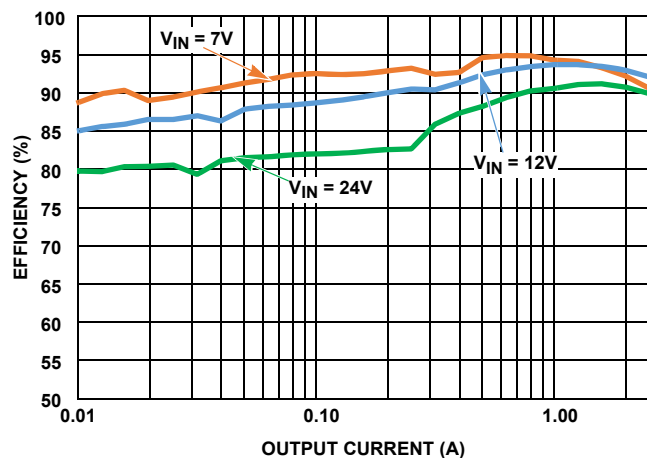


FIGURE 4. EFFICIENCY vs LOAD

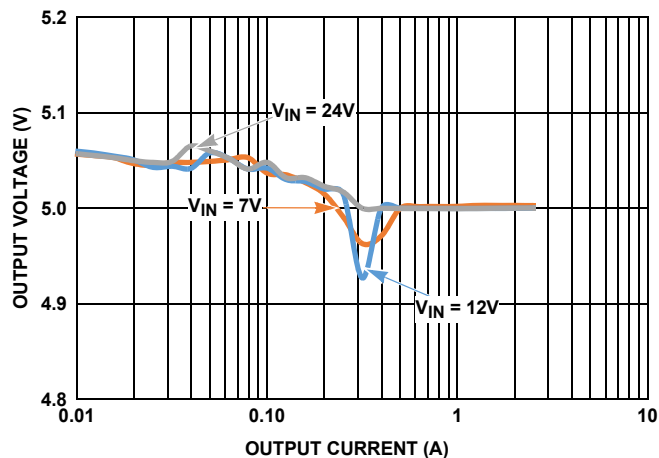


FIGURE 5. LINE REGULATION

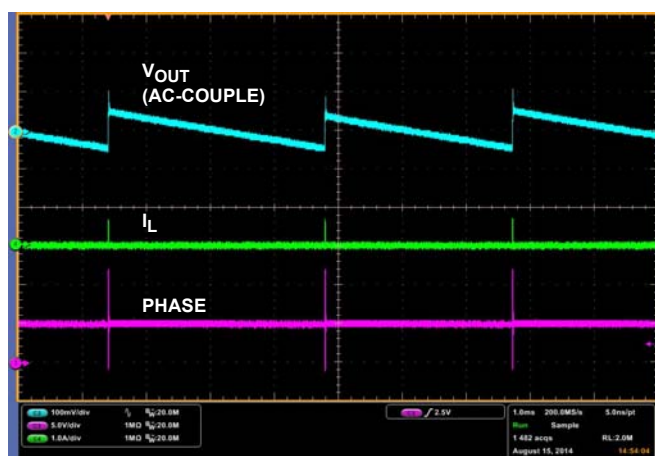


FIGURE 6. OUTPUT RIPPLE AT 0A LOAD

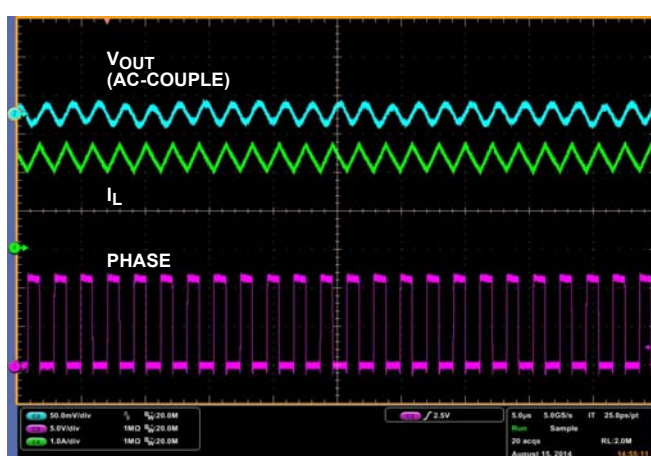


FIGURE 7. OUTPUT RIPPLE AT 2.5A LOAD

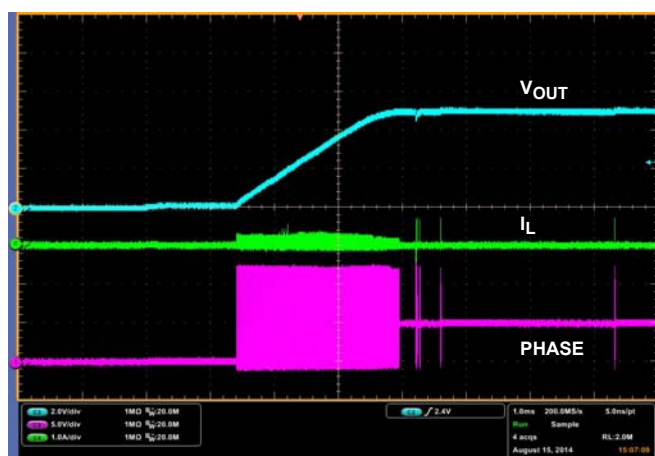


FIGURE 8. SOFT-START AT 0A LOAD

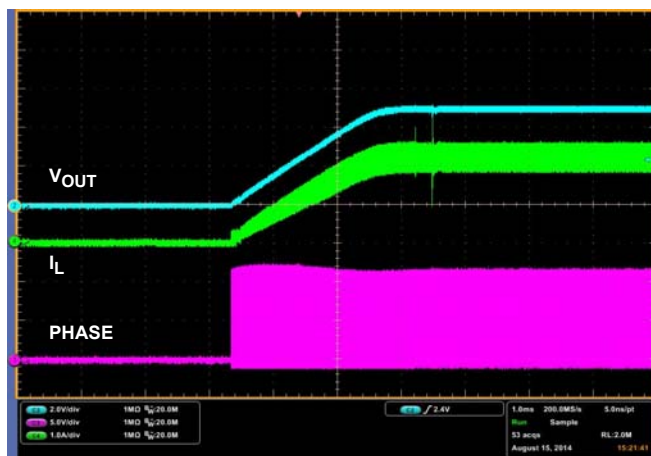


FIGURE 9. SOFT-START AT 2.5A LOAD

Oscilloscope screenshot showing three waveforms:

- V_{OUT} (AC-COUPLE)** (Blue trace): Shows a small transient spike.
- I_L** (Green trace): Shows a rectangular pulse.
- PHASE** (Magenta trace): Shows a noisy baseline.

Oscilloscope settings at the bottom:

- V_{OUT} Scale:** 1.6V/div
- I_L Scale:** 1.8V/div
- PHASE Scale:** 1.8A/div
- Time Scale:** 1.0ms
- Sample Rate:** 200.0MS/s
- Resolution:** 148 bits
- Math:** RL-2.0M
- Date:** August 15, 2014
- Time:** 10:03

V_{OUT}
(AC-COUPLE)

I_L

PHASE

500mV/div I_L 5.0V/div 1.8A/div

25.0µs 5.0GS/s IT 100ps/div

75.0mV RL 2.0M

August 15, 2014 10:00

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Board Layout

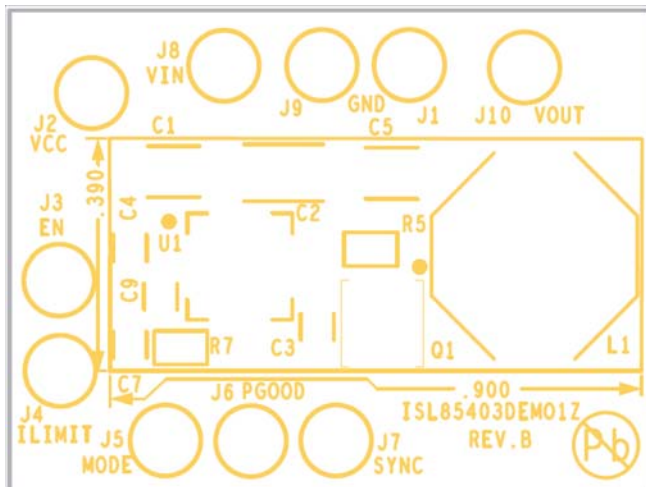


FIGURE 13. SILKSCREEN TOP COMPONENTS

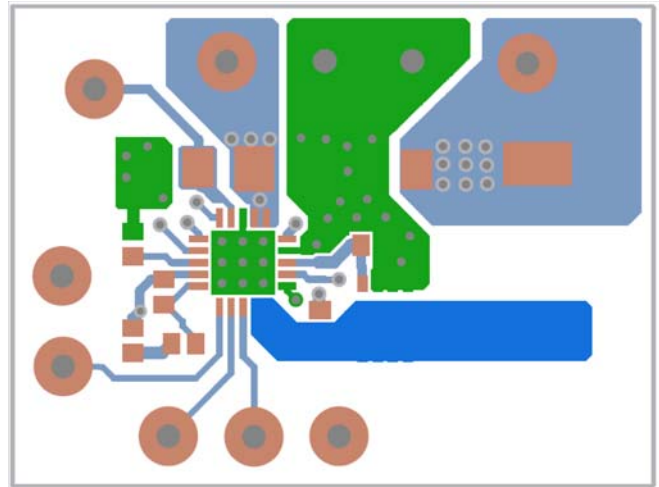


FIGURE 14. TOP LAYER

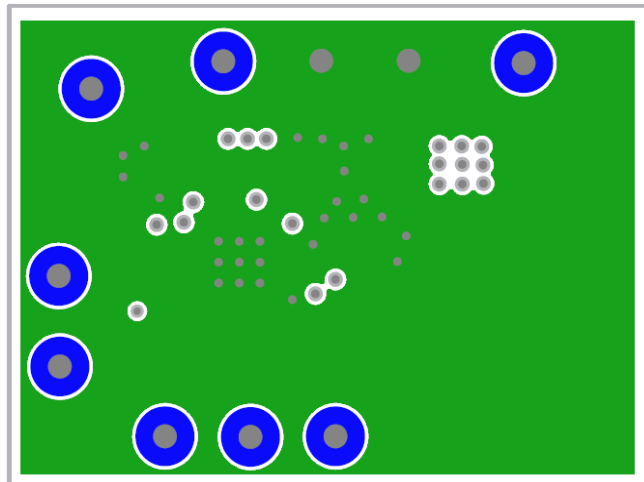


FIGURE 15. 2nd LAYER

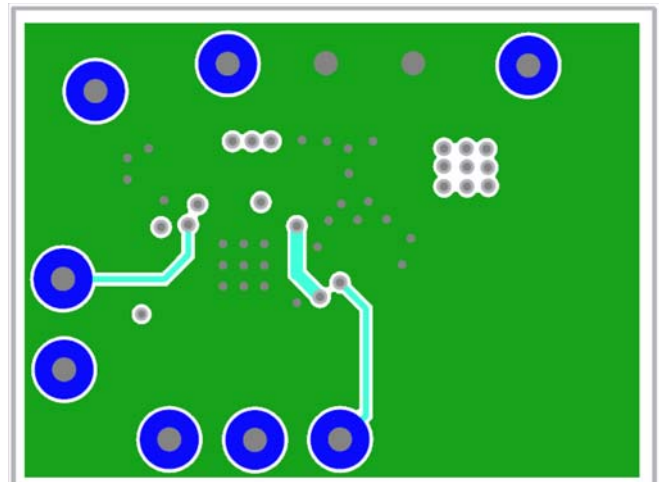


FIGURE 16. 3rd LAYER

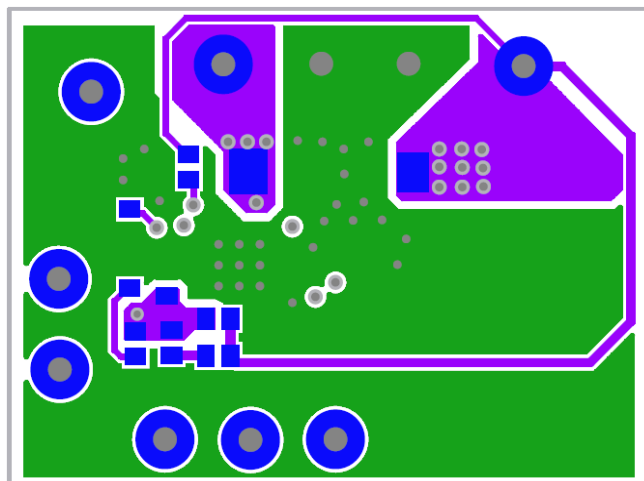


FIGURE 17. BOTTOM LAYER

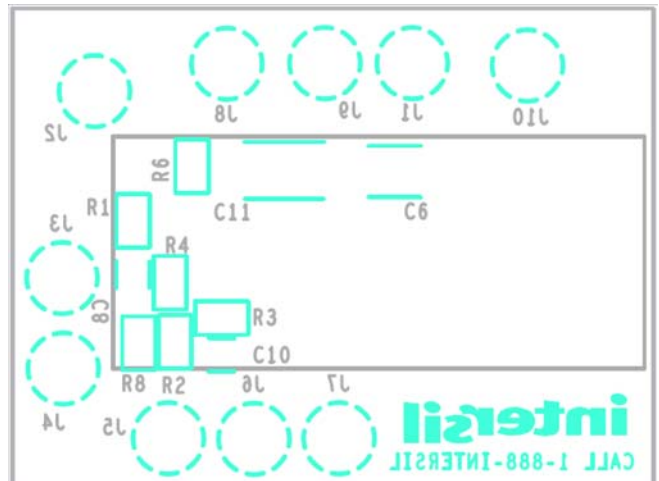


FIGURE 18. SILKSCREEN BOTTOM COMPONENTS

Board Layout (Continued)

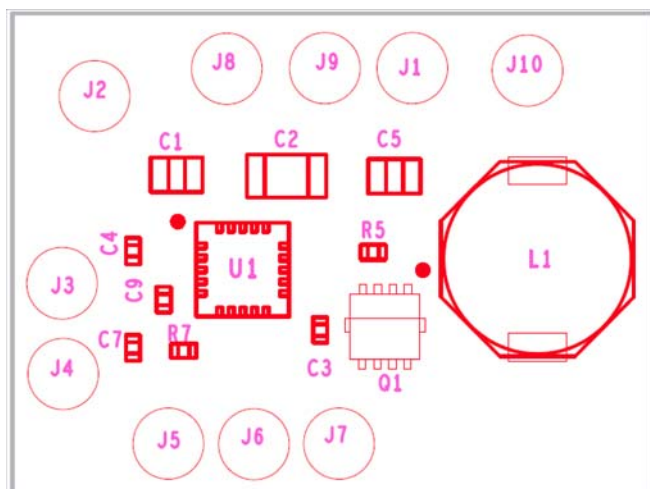


FIGURE 19. TOP COMPONENT ASSEMBLY

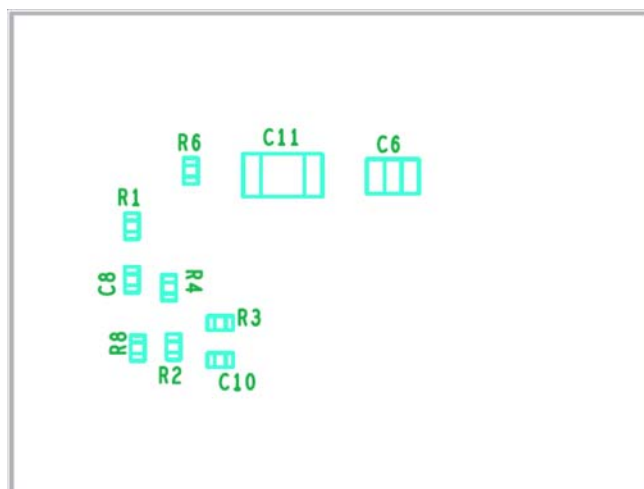


FIGURE 20. BOTTOM COMPONENT ASSEMBLY (MIRRORED)

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

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80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
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Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

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