

*RoHS Compliant*

# **Industrial Secure Digital Card**

*Specifications*

January 2<sup>nd</sup>, 2013

*Version 1.3*



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## FEATURES:

- **Fully compatible with SD card standard specification**
  - SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 2.00
  - SD Memory Card Specifications, Part 2, File System Specification, Version 2.00
  - SD Memory Card Specifications, Part 3, Security Specification, Version 2.00
- **Capacity**
  - Standard: 256, 512 MB  
1, 2 GB
  - SDHC: 4, 8, 16, 32 GB
- **Performance**
  - Sustained read: Up to 19 MB/sec
  - Sustained write: Up to 14 MB/sec
- **SD-protocol compatible**
- **Support SPI mode**
- **NAND Flash Type: SLC**
- **Variable clock rate 0-50MHz**
- **Intelligent endurance design**
  - Built-in BCH-ECC supports correction up to 24 bits data error per 1K bytes data automatically
  - Implements global wear-leveling algorithms to substantially increase longevity of flash media
  - Flash bad-block management
  - S.M.A.R.T utility
- **Temperature ranges**

|          |              |
|----------|--------------|
| Standard | 0°C ~ 70°C   |
| Extended | -40°C ~ 85°C |

  - Operating temperature
  - Storage temperature: -40°C ~ 85°C
- **Power consumption**
  - Standby: 110  $\mu$  A
  - Read: 45 mA
  - Write: 55 mA
- **Operation voltage: 2.7V ~ 3.6V**
- **Physical dimension: 24mm x 32mm x 2.1mm**
- **RoHS Compliant**

Note: The performance and the power consumption addressed here are typical and may vary from capacities, flash configurations or host system settings.

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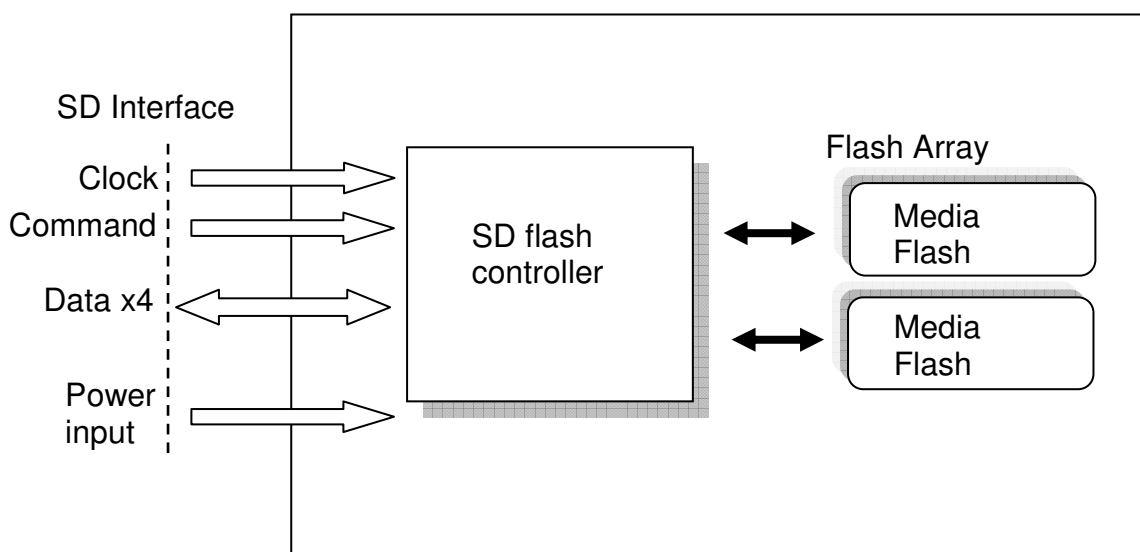
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## 1. General Description

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's embedded SD card is designed specifically for rigorous applications by offering maximum endurance, reliability, and agility, where extreme traceability, enhanced data integrity, and exceptionally velocity are required.

### 1.1 Product Function Block

The embedded SD contains a flash controller and flash media with SD standard interface.



### 1.2 Functional description

The embedded SD device contains a high level, intelligent subsystem that provides many capabilities including:

- Powerful ECC algorithms
- Global wear-leveling algorithms
- Power management

---

### **1.2.1 Flash Management**

The SD controller contains logic/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The embedded SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the embedded SD replaces this bad bit with a spare bit within the sector header. If necessary, the embedded SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

### **1.2.2 Powerful ECC Algorithms**

The powerful ECC algorithms will enhance flash block use rate and whole device life. The SD controller has an innovative algorithm to recover the data. Built-in BCH-ECC supports correction up to 24 bits data error per 1K bytes data automatically

### **1.2.3 Power Management**

A power saving feature of the embedded SD is automatic entrance and exit from sleep mode. Upon completion of an operation, the embedded SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The embedded SD is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the embedded SD will cause it to exit sleep mode and response to the master.

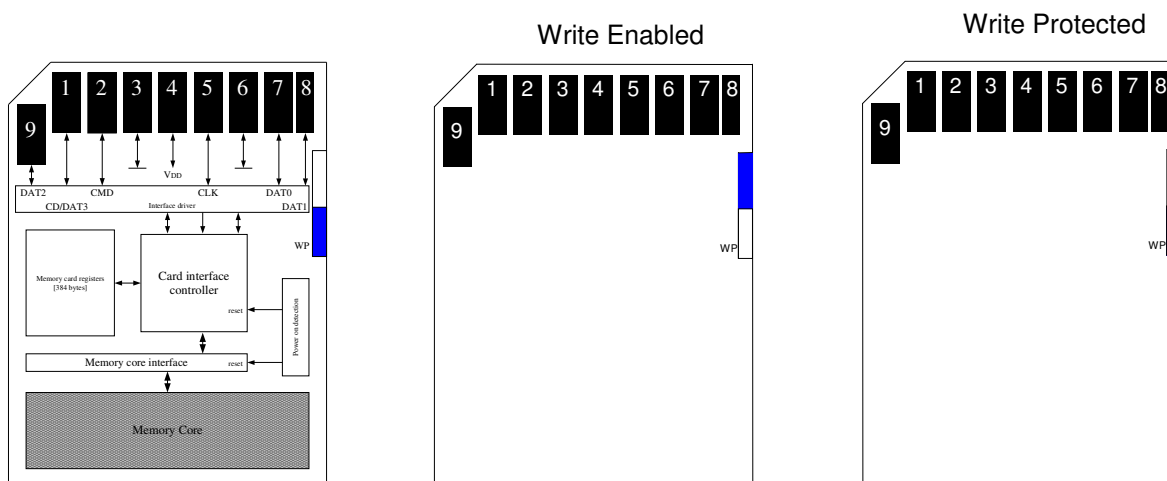
### **1.2.4 S.M.A.R.T**

S.M.A.R.T. (SMART), an acronym stands for Self-Monitoring, Analysis and Reporting Technology, is an open standard allowing an individual disk drive in the ATA/IDE or SCSI interface to automatically monitor its own health and report potential problems in order to prevent data loss. This failure warning technology provides predictions from unscheduled downtime by observing and storing critical drive performance and calibration parameters. Ideally, this should allow taking hands-on actions to keep from impending drive failure.

Failures are divided into two categories: those that can be predicted and those that cannot. Predictable failures occur gradually over time, and the decline in performance can be detected; on the other hand, unpredictable failures happen very sudden without any warning. These failures may be caused by power surges or related to electronic components. The purpose of the SMART implementation is to predict near-term failures of each individual disk drive and generate a warning to prevent unfortunate loss.

## 2. Electrical characteristics

### 2.1 Card Architecture



### 2.2 Pin Assignment

| Pin | SD Mode |                              | SPI Mode |                       |
|-----|---------|------------------------------|----------|-----------------------|
|     | Name    | Description                  | Name     | Description           |
| 1   | CD/DAT3 | Card detect/Data line[Bit 3] | CS       | Chip select           |
| 2   | CMD     | Command/Response             | DI       | Data in               |
| 3   | VSS1    | Supply voltage ground        | VSS      | Supply voltage ground |
| 4   | VDD     | Supply voltage               | VDD      | Supply voltage        |
| 5   | CLK     | Clock                        | SCLK     | Clock                 |
| 6   | VSS2    | Supply voltage ground        | VSS2     | Supply voltage ground |
| 7   | DAT0    | Data line[Bit 0]             | DO       | Data out              |
| 8   | DAT1    | Data line[Bit 1]             | Reserved |                       |
| 9   | DAT2    | Data line[Bit 2]             | Reserved |                       |

## 2.3 Capacity Specification

The following table shows the out-of-box capacity. (Follow SDA rule to do format)

| Capacity | Total (LBA) Sectors | Total Partition Sectors | User Data Sectors | User Data Bytes |
|----------|---------------------|-------------------------|-------------------|-----------------|
| 256 MB   | 499,712             | 499,611                 | 499,456           | 255,721,472     |
| 512 MB   | 985,088             | 984,851                 | 984,576           | 504,102,912     |
| 1 GB     | 2,000,896           | 2,000,651               | 2,000,128         | 1,024,065,536   |
| 2 GB     | 4,009,984           | 4,009,739               | 4,009,216         | 2,052,718,592   |
| 4 GB     | 8,019,968           | 8,011,776               | 8,003,584         | 4,097,835,008   |
| 8 GB     | 16,039,936          | 16,031,744              | 16,023,552        | 8,204,025,856   |
| 16 GB    | 31,719,424          | 31,711,232              | 31,703,040        | 16,231,923,712  |
| 32 GB    | 63,438,848          | 63,430,656              | 63,414,272        | 32,468,074,496  |

Note: the statistics may vary depending on file systems of various OS. User data bytes do not indicate total useable bytes. LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

## 2.4 Performance

Performances of Embedded SD are shown in the table below.

| Capacity               | 256 MB | 512 MB | 1 GB | 2 GB | 4 GB | 8 GB | 16 GB | 32 GB |
|------------------------|--------|--------|------|------|------|------|-------|-------|
| Performance            |        |        |      |      |      |      |       |       |
| Sustained Read (MB/s)  | 18     | 19     | 19   | 19   | 19   | 19   | 19    | 19    |
| Sustained Write (MB/s) | 7      | 13     | 11   | 12   | 14   | 14   | 11    | 12    |

Note: Performances vary from flash configurations or host device settings.

## 2.5 DC Power Supply

| Symbol          | Parameter            | Min. | Typ. | Max. | Unit |
|-----------------|----------------------|------|------|------|------|
| V <sub>DD</sub> | Power Supply Voltage | 2.7  | 3.3  | 3.6  | V    |

## 2.6 Power consumption

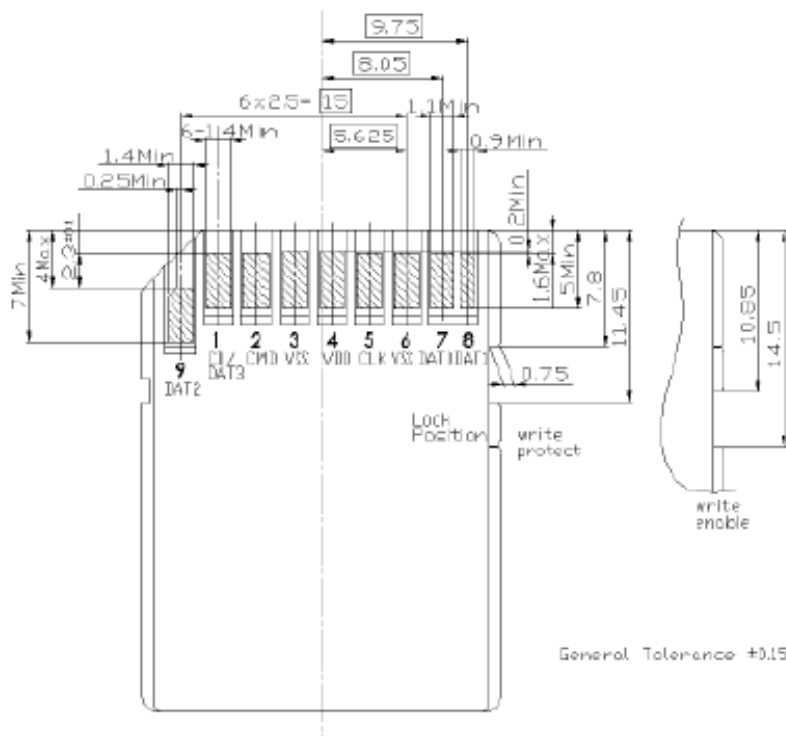
| Mode    | Value | Unit    | Condition |
|---------|-------|---------|-----------|
| Standby | 110   | $\mu$ A | Typical   |
| Read    | 45    | mA      | Typical   |
| Write   | 55    | mA      | Typical   |

Note: results are measured under 3.3V

## 3. Physical Characteristics

### 3.1 Physical Dimension

|                         |                                                                   |
|-------------------------|-------------------------------------------------------------------|
| Dimensions Card Package | 24 mm x 32 mm<br>Min. 23.9 mm x 31.9 mm<br>Max. 24.1 mm x 32.1 mm |
| Thickness               | 2.1 mm ± 0.15 mm                                                  |
| Surface                 | Plain (except contact area)                                       |
| Edges                   | Smooth edges                                                      |



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## 3.2 Environmental Specifications

| Climatic Testing       |           |                              |
|------------------------|-----------|------------------------------|
| Test Item              | DUT State | Test Condition (Gold Series) |
|                        |           | Temperature                  |
| High Temperature       | Storage   | 85°C                         |
|                        | Operation | 70°C                         |
| Low Temperature        | Storage   | - 40°C                       |
|                        | Operation | 0°C                          |
| Moisture and Corrosion | Storage   | 40°C 93%                     |
|                        | Operation | 25°C 95%                     |
| Junction temperature   |           | Max. 95°C                    |

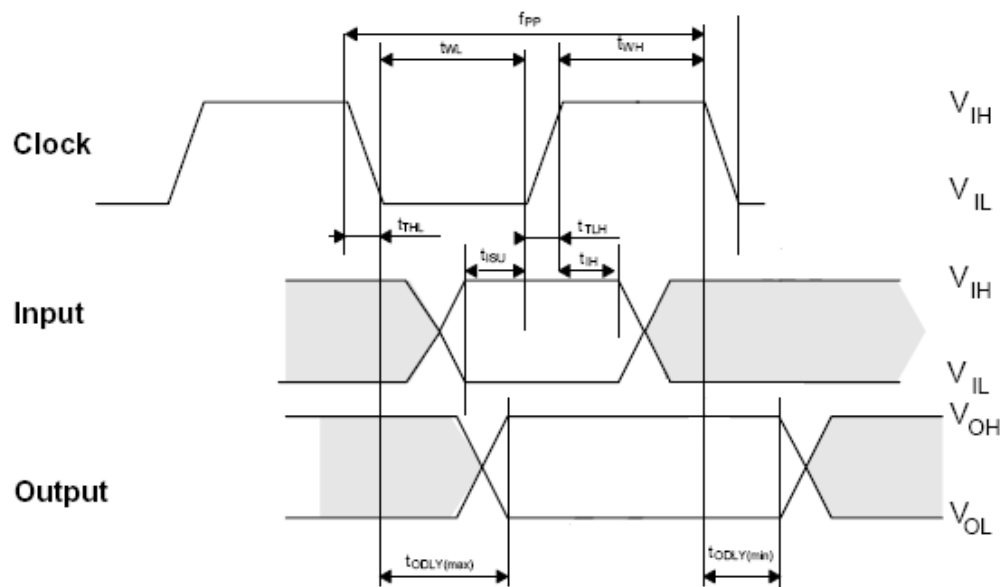
| Reliability & Durability Testing |                      |
|----------------------------------|----------------------|
| Test Item                        | Descriptions         |
| Durability                       | 10,000 mating cycles |

**Industrial Secure Digital Card**  
**AP-ISDxxxXXXX-3X**

|                                  |                                                                                                                                                                     |
|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bending                          | 10 N                                                                                                                                                                |
| UV light exposure                | UV:254 nm, 15 Ws/cm <sup>2</sup> according to ISO 7816-1                                                                                                            |
| Visual inspection shape and form | No warpage; no mold skin; complete form; no cavities surface smoothness $\leq -0.1$ mm/cm <sup>2</sup> within contour; no cracks; no pollution (fat, oil dust, etc) |
| Drop                             | 1.5 m free fall                                                                                                                                                     |
| Salt Water Spray                 | 3 $\pm$ 1%NaCl; 35°C; 24hrs accumulated (MIL STD Method 1009)                                                                                                       |
| Torque                           | 0.15N.m or +/- 2.5 degree                                                                                                                                           |
| WP (Write Protect) switch cycles | Minimum 1000 cycles (@ slide force 0.4 N to 5N)                                                                                                                     |

## 4. AC Characteristics

### 4.1 SD Interface Timing (Default)



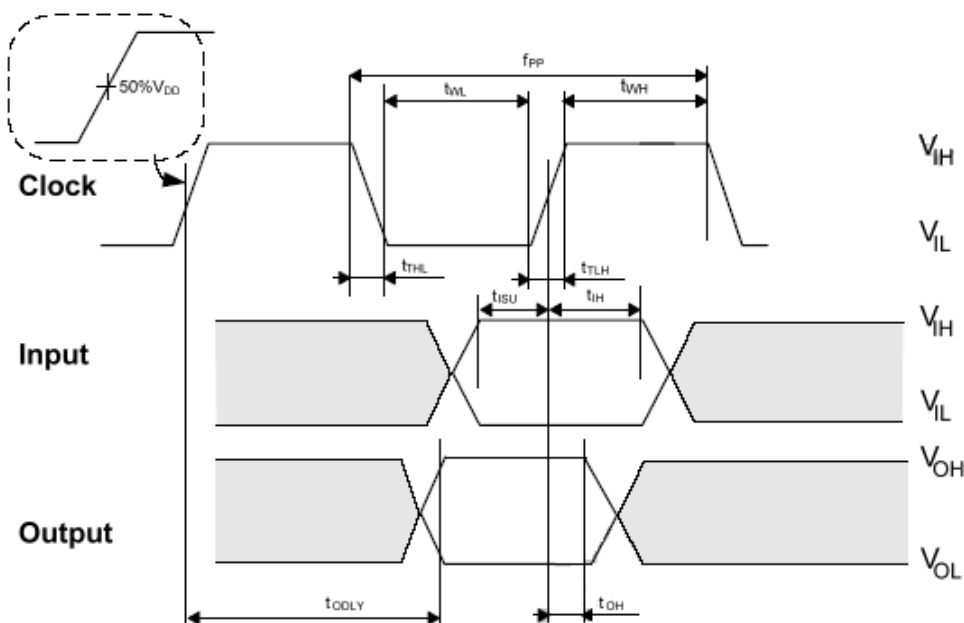
Shaded areas are not valid

| SYMBOL                                                                                              | PARAMETER                           | MIN                   | MAX | UNIT | Note                              |
|-----------------------------------------------------------------------------------------------------|-------------------------------------|-----------------------|-----|------|-----------------------------------|
| <b>Clock CLK (All values are referred to min(<math>V_{IH}</math>) and max(<math>V_{IL}</math>))</b> |                                     |                       |     |      |                                   |
| $f_{PP}$                                                                                            | Clock frequency Data Transfer Mode  | 0                     | 25  | MHz  | $C_{card} \leq 10$ pF<br>(1 card) |
| $f_{OD}$                                                                                            | Clock frequency Identification Mode | 0 <sub>(1)</sub> /100 | 400 | kHz  | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{WL}$                                                                                            | Clock low time                      | 10                    | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{WH}$                                                                                            | Clock high time                     | 10                    | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{TLH}$                                                                                           | Clock rise time                     | -                     | 10  | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{THL}$                                                                                           | Clock fall time                     | -                     | 10  | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{ISU}$                                                                                           | Input setup time                    | 5                     | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{IH}$                                                                                            | Input hold time                     | 5                     | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{ODLY}$                                                                                          | Output delay time                   | 0                     | 14  | ns   | $C_L \leq 40$ pF<br>(1 card)      |

|            |                                              |   |    |    |                              |
|------------|----------------------------------------------|---|----|----|------------------------------|
| $t_{ODLY}$ | Output Delay time during Identification Mode | 0 | 50 | ns | $C_L \leq 40$ pF<br>(1 card) |
|------------|----------------------------------------------|---|----|----|------------------------------|

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases that requires the clock to be continued.

## 4.2 SD Interface Timing (High Speed Mode)



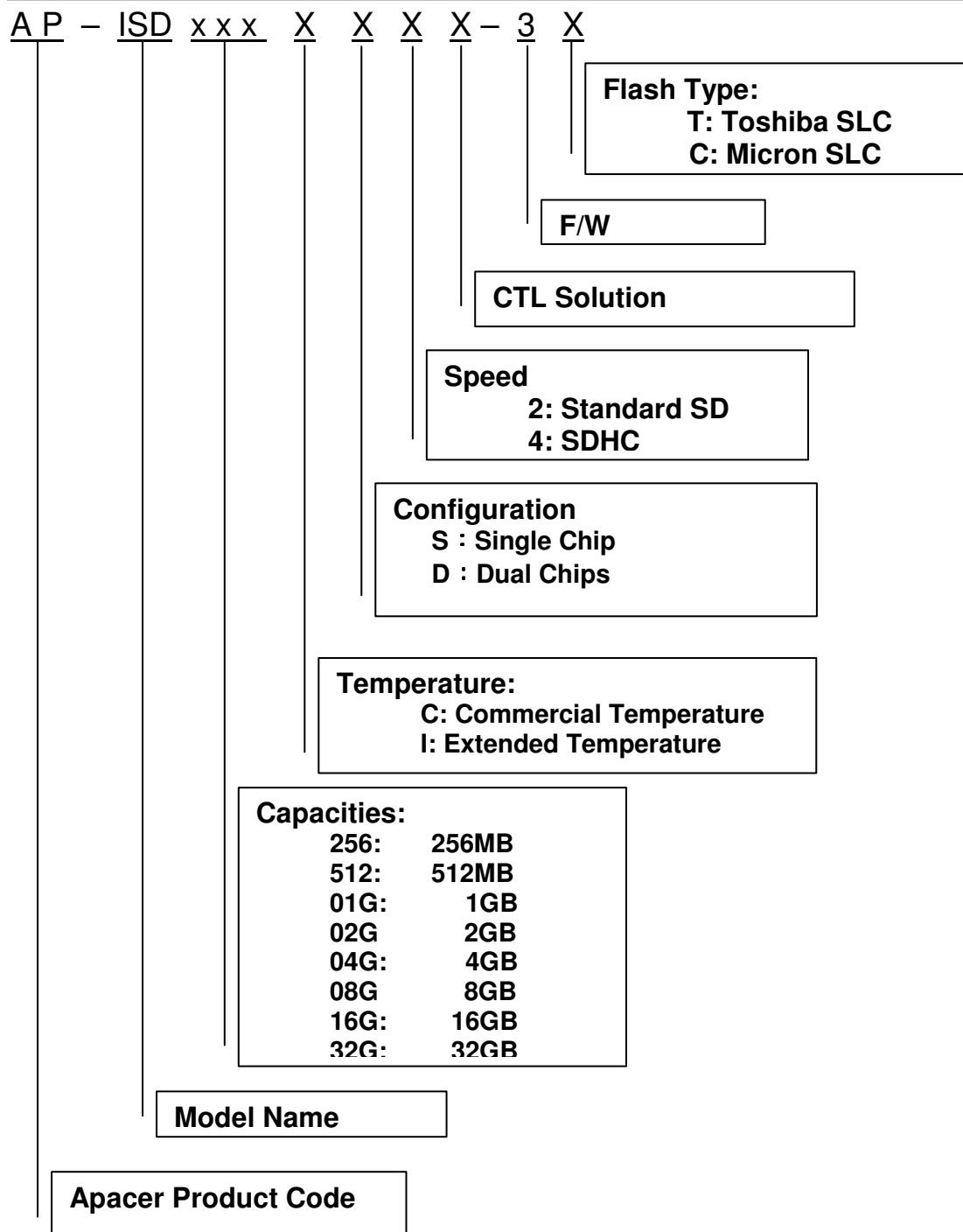
Shaded areas are not valid

| SYMBOL     | PARAMETER                          | MIN | MAX | UNIT | Note                              |
|------------|------------------------------------|-----|-----|------|-----------------------------------|
| $f_{PP}$   | Clock frequency data transfer mode | 0   | 50  | MHz  | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{WL}$   | Clock low time                     | 7   | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{WH}$   | Clock high time                    | 7   | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{TLH}$  | Clock rise time                    | -   | 3   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{THL}$  | Clock fall time                    | -   | 3   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{ISU}$  | Input setup time                   | 6   | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{IH}$   | Input hold time                    | 2   | -   | ns   | $C_{card} \leq 10$ pF<br>(1 card) |
| $t_{ODLY}$ | Output delay time                  |     | 14  | ns   | $C_L \leq 40$ pF<br>(1 card)      |
| $T_{OH}$   | Output hold time                   | 2.5 |     | ns   | $C_L \leq 15$ pF<br>(1 card)      |
| $C_L$      | System capacitance of each line*   |     | 40  | pF   | $C_L \leq 15$ pF<br>(1 card)      |

\*In order to satisfy severe timing, host shall run on only one card

## 5. Product Ordering Information

### 5.1 Product Code Designations



## 5.2 Valid Combinations

### 5.2.1 Standard Temperature

| <b>Capacity</b> | <b>AP/N</b>      |
|-----------------|------------------|
| 256MB           | AP-ISD256CS2A-3T |
| 512MB           | AP-ISD512CS2A-3T |
| 1GB             | AP-ISD01GCS2A-3T |
| 2GB             | AP-ISD02GCS2A-3T |
| 4GB             | AP-ISD04GCS4A-3T |
| 8GB             | AP-ISD08GCD4A-3T |
| 16GB            | AP-ISD16GCD4A-3C |
| 32GB            | AP-ISD32GCD4A-3C |

### 5.2.2 Extended Temperature

| <b>Capacity</b> | <b>AP/N</b>      |
|-----------------|------------------|
| 256MB           | AP-ISD256IS2B-3T |
| 512MB           | AP-ISD512IS2B-3T |
| 1GB             | AP-ISD01GIS2B-3T |
| 2GB             | AP-ISD02GIS2B-3T |
| 4GB             | AP-ISD04GIS4B-3T |
| 8GB             | AP-ISD08GID4B-3T |
| 16GB            | AP-ISD16GID4B-3C |
| 32GB            | AP-ISD32GID4B-3C |

**Note:** Please consult with Apacer sales representatives for availabilities.

## Revision History

| Revision | Description                                                                                                                                          | Date       |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| 1.0      | Official release                                                                                                                                     | 06/14/2011 |
| 1.1      | Updated operating voltage information<br>- Add a short note of +/- 10% tolerance and lowest at 1.8V                                                  | 02/17/2012 |
| 1.2      | Updated Product Ordering Information due to firmware upgrade                                                                                         | 10/23/2012 |
| 1.3      | Corrected the mistake in Product Ordering Information:<br>from single/dual channels to single/dual chips as SD card is<br>designed in single channel | 01/02/2013 |

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## Global Presence

|                              |                                                                                                                                                                                                                                                     |
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