1:2 Single-Ended, Low Cost, Active RF Splitter

ADA4304-2

FEATURES

- **Ideal for CATV and terrestrial applications**
- **Excellent frequency response**
  - **1.6 GHz, −3 dB bandwidth**
  - **1 dB flatness to 1.0 GHz**
- **Low noise figure: 4.0 dB**
- **Low distortion**
  - **Composite second order (CSO): −62 dBc**
  - **Composite triple beat (CTB): −72 dBc**
  - **1 dB compression point of 8.25 dBm**
- **2.8 dB of gain per output channel**
- **25 dB output-to-output isolation, 50 MHz to 1000 MHz**
- **75 Ω input and outputs**
- **Integrated output resistors**
- **Small package size: 16-lead, 3 mm × 3 mm LFCSP**

APPLICATIONS

- **Set-top boxes**
- **Residential gateways**
- **CATV distribution systems**
- **Splitter modules**
- **Digital cable ready (DCR) TVs**

FUNCTIONAL BLOCK DIAGRAM

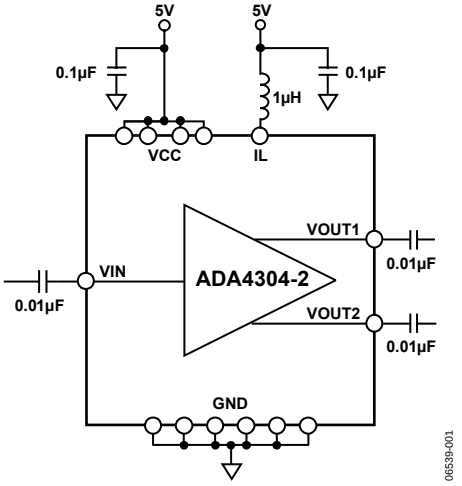

Figure 1.

GENERAL DESCRIPTION

The ADA4304-2 is a 75 Ω active splitter for use in applications where a lossless signal split is required. Typical applications include multituner digital set-top boxes, cable splitter modules, multituner/digital cable ready (DCR) televisions, and home gateways where traditional solutions require discrete passive splitter modules with separate fixed gain amplifiers.

The ADA4304-2 is fabricated using Analog Devices, Inc. proprietary silicon-germanium (SiGe), complementary bipolar process, enabling it to achieve very low levels of distortion with a noise figure of 4 dB. The part provides a low cost alternative that simplifies designs and improves system performance by integrating a signal splitter element and a gain block into a single IC. The ADA4304-2 is available in a 16-lead LFCSP and operates in the extended industrial temperature range of −40°C to +85°C.

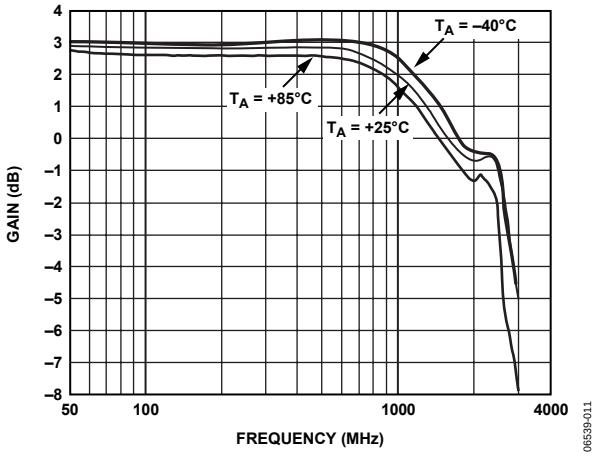

Figure 2. Gain (S_{21}, S_{31}) vs. Frequency

Rev. 0

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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V, 75 Ω system, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth (−3 dB)			1600		MHz
Specified Frequency Range		54		865	MHz
Gain (S_{21}, S_{31})	f = 100 MHz; see Figure 17 and Figure 18		2.8		dB
1 dB Gain Flatness			1000		MHz
NOISE/DISTORTION PERFORMANCE					
Noise Figure[1]	@ 54 MHz		4.0		dB
	@ 550 MHz		4.5		dB
	@ 865 MHz		4.6		dB
Output IP3	f_1 = 97.25 MHz, f_2 = 103.25 MHz		26		dBm
Output IP2	f_1 = 97.25 MHz, f_2 = 103.25 MHz		44.5		dBm
Composite Triple Beat (CTB)	135 channels, 15 dBmV/channel, f = 865 MHz		−72		dBc
Composite Second Order (CSO)	135 channels, 15 dBmV/channel, f = 865 MHz		−62		dBc
Cross Modulation (CXM)	135 channels, 15 dBmV/channel, 100% modulation @ 15.75 kHz, f = 865 MHz		−69		dBc
INPUT CHARACTERISTICS	See Figure 17, Figure 18, and Figure 19				
Input Return Loss (S_{11})	@ 54 MHz		−15	−11	dB
	@ 550 MHz		−35.5	−22	dB
	@ 865 MHz		−13.3	−8	dB
Output-to-Input Isolation (S_{12}, S_{13})	Either output, 54 MHz to 865 MHz				
	@ 54 MHz		−32	−30	dB
	@ 550 MHz		−32	−29	dB
	@ 865 MHz		−33	−31	dB
OUTPUT CHARACTERISTICS	See Figure 17, Figure 18, and Figure 19				
Output Return Loss (S_{22}, S_{33})	Either output, 54 MHz to 865 MHz				
	@ 54 MHz		−26.7	−21	dB
	@ 550 MHz		−22	−15	dB
	@ 865 MHz		−20	−12	dB
Output-to-Output Isolation (S_{23}, S_{32})	Either output, 54 MHz to 865 MHz				dB
	@ 54 MHz		−26.7		dB
	@ 550 MHz		−25.1		dB
	@ 865 MHz		−25		dB
1 dB Compression (P_{1dB})	Output referred, f = 100 MHz		8.25		dBm
POWER SUPPLY					
Nominal Supply Voltage		4.75	5.0	5.25	V
Quiescent Supply Current			88	105	mA

[1] Characterized with 50 Ω noise figure analyzer.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD 51-7.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	98	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4304-2 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4304-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is essentially equal to the quiescent power dissipation; the supply voltage (V_S) times the quiescent current (I_S). In Table 1, the maximum power dissipation of the ADA4304-2 can be calculated as

$$P_{D\,(MAX)} = 5.25\ \text{V} \times 105\ \text{mA} = 551\ \text{mW}$$

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through-holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP (98°C/W) on a JEDEC standard 4-layer board.

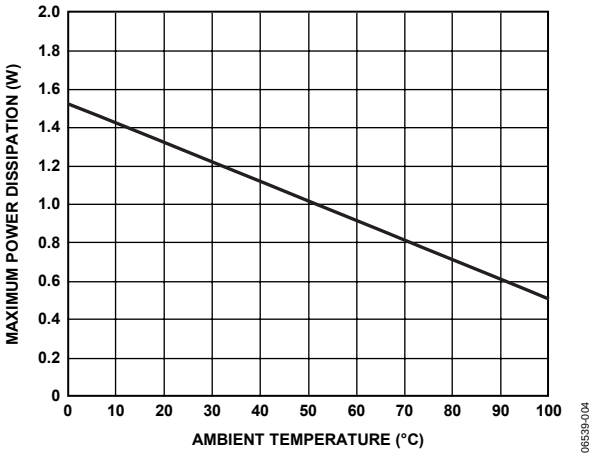


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

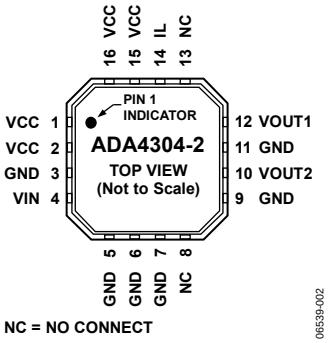


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 15, 16	VCC	Supply Pin
3, 5 to 7, 9, 11	GND	Ground
4	VIN	Input
8, 13	NC	No Connection
10	VOUT2	Output 2
12	VOUT1	Output 1
14	IL	Bias Pin

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5 V, 75 Ω system, T_A = 25°C, unless otherwise noted.

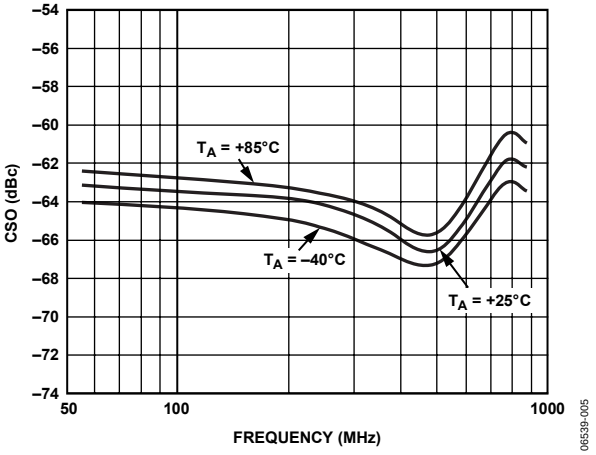


Figure 5. Composite Second Order (CSO) vs. Frequency

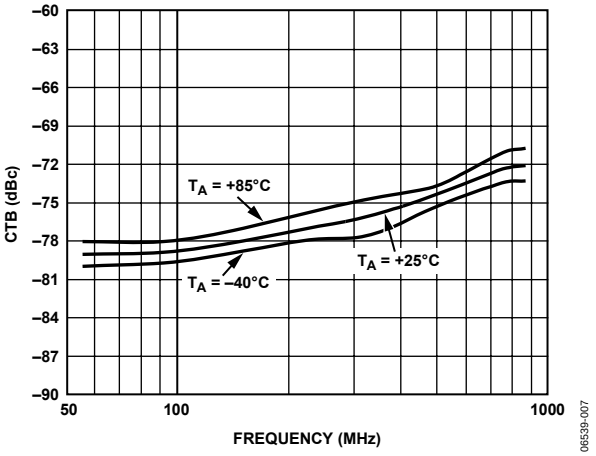


Figure 6. Composite Triple Beat (CTB) vs. Frequency

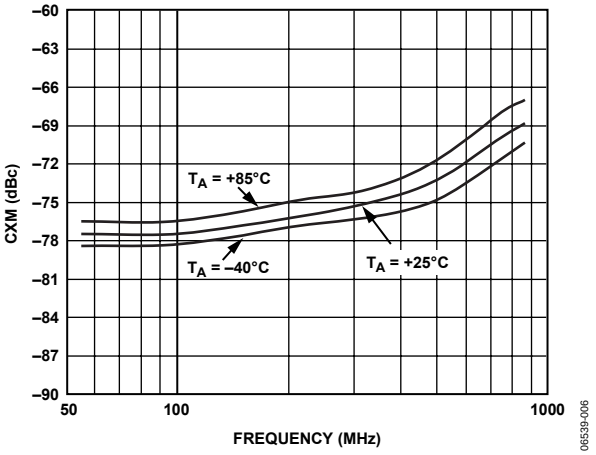


Figure 7. Cross Modulation (CXM) vs. Frequency

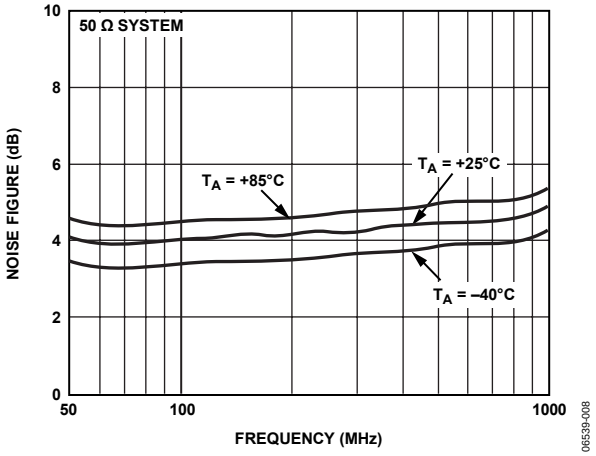


Figure 8. Noise Figure vs. Frequency

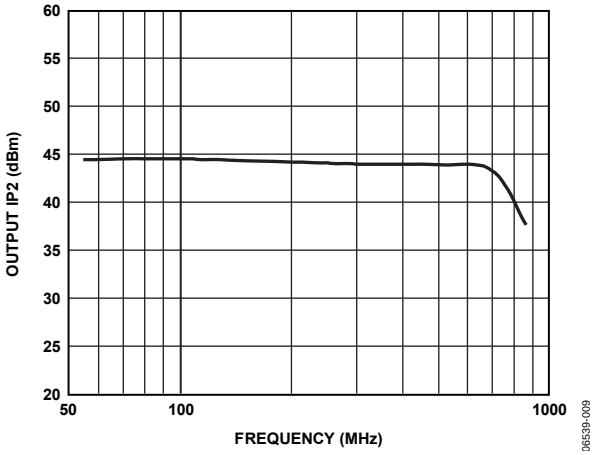


Figure 9. Output IP2 vs. Frequency

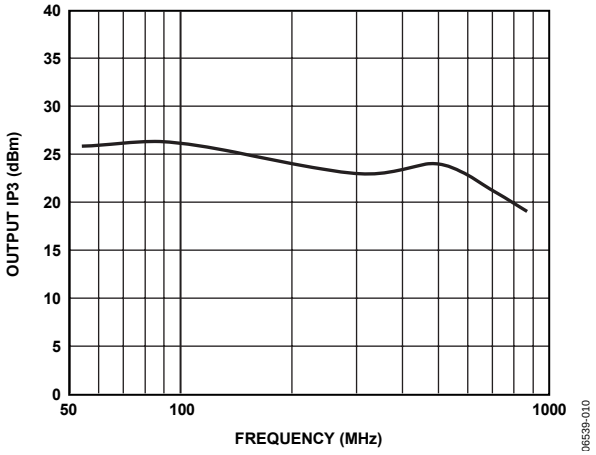


Figure 10. Output IP3 vs. Frequency

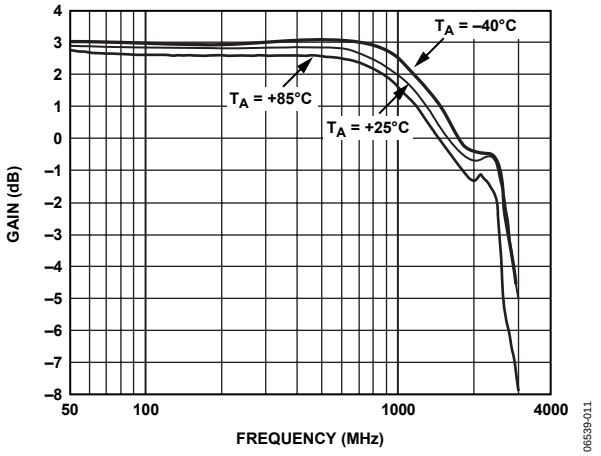


Figure 11. Gain (S_{21}, S_{31}) vs. Frequency

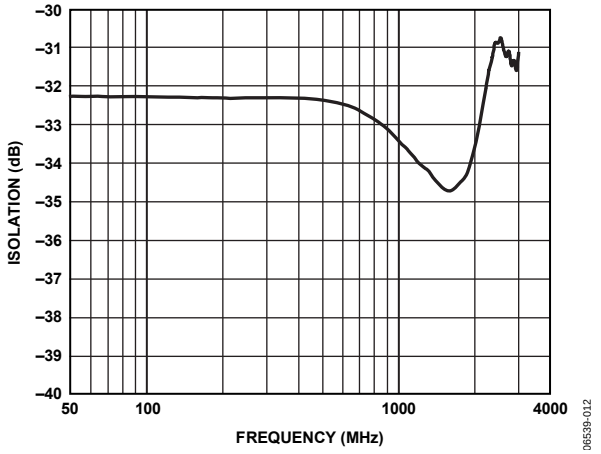
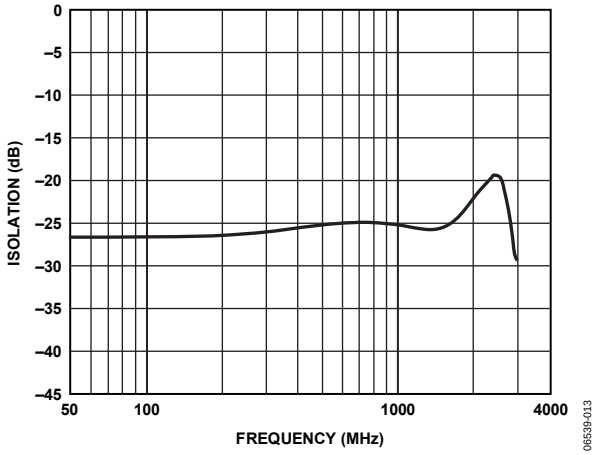


Figure 12. Output-to-Input Isolation (S_{12}, S_{13}) vs. Frequency



`Figure 13. Output-to-Output Isolation (S_{23}, S_{32}) vs. Frequency

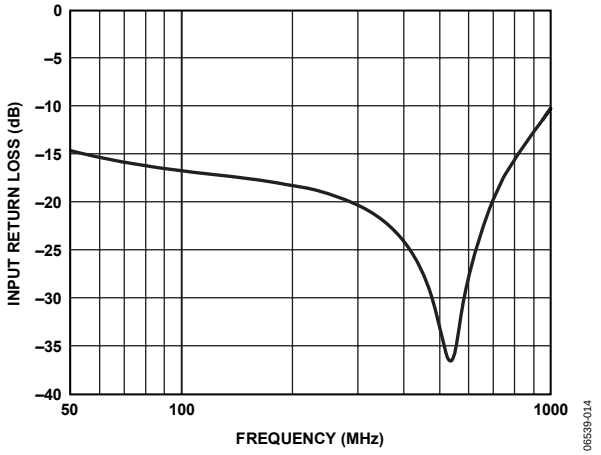


Figure 14. Input Return Loss (S_{11}) vs. Frequency

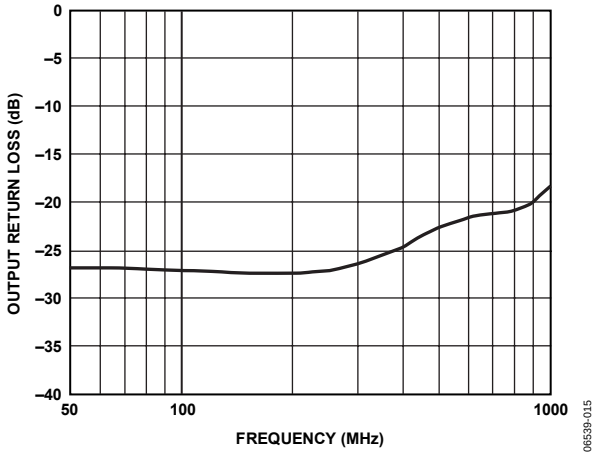


Figure 15. Output Return Loss (S_{22}, S_{33}) vs. Frequency

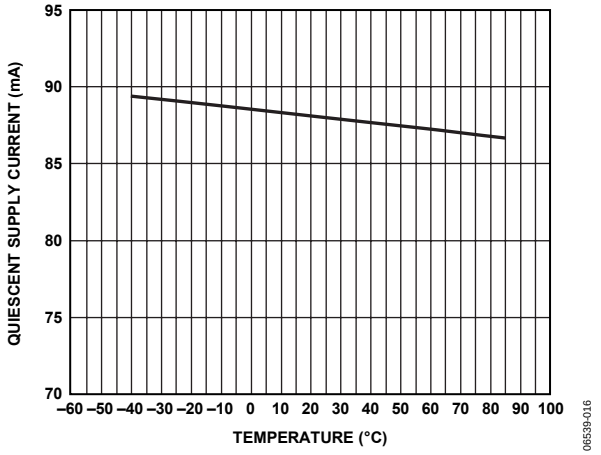


Figure 16. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

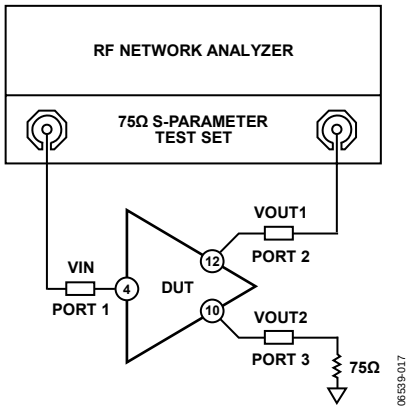


Figure 17. Test Circuit for S_{11}, S_{12}, S_{21}, S_{22} Measurements

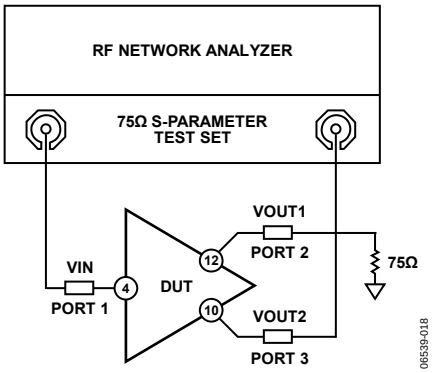


Figure 18. Test Circuit for S_{13}, S_{31}, S_{33} Measurements

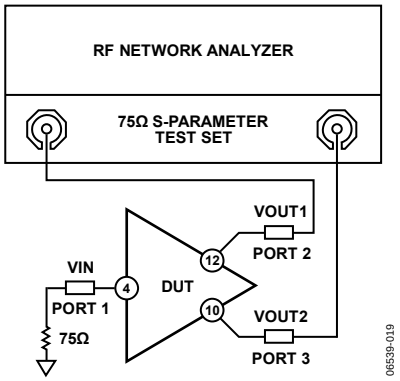


Figure 19. Test Circuit for S_{23}, S_{32} Measurements

APPLICATIONS

The ADA4304-2 active splitter is primarily intended for use in the downstream path of television set-top boxes (STBs) that contain multiple tuners. It is typically located directly after the diplexer in a bidirectional CATV customer premise unit. The ADA4304-2 provides a single-ended input and two single-ended outputs that allow the delivery of the RF signal to two different signal paths. These paths can include, but are not limited to, a main picture tuner, the picture-in-picture (PIP) tuner, an out-of-band (OOB) tuner, a digital video recorder (DVR), and a cable modem (CM).

The ADA4304-2 exhibits composite second order (CSO) and composite triple beat (CTB) products that are −62 dBc and −72 dBc, respectively. The use of the SiGe bipolar process also allows the ADA4304-2 to achieve a noise figure (NF) of 4 dB.

CIRCUIT DESCRIPTION

The ADA4304-2 consists of a low noise buffer amplifier followed by a resistive power divider. This arrangement provides 2.8 dB of gain relative to the RF signal present at the input of the device. The input and each output must be properly matched to a 75 Ω environment for distortion and noise performance to match the data sheet specifications. AC coupling capacitors of 0.01 µF are recommended for the input and outputs.

A 1 µH RF choke (Coilcraft chip inductor 0805LS-102X) is required to correctly bias internal nodes of the ADA4304-2. It should be connected between the 5 V supply and the IL pin (Pin 14). The choke should be placed as close as possible to the ADA4304-2 to minimize parasitic capacitance on the IL pin, which is critical for achieving the specified bandwidth and flatness.

EVALUATION BOARDS

The ADA4304-2 evaluation board allows designers to assess the performance of the parts in their particular application. The board includes 75 Ω coaxial connectors and 75 Ω controlled-impedance signal traces that carry the input and output signals. Power (5 V) is applied to the red VCC loop connector, and ground is connected to the black GND loop connector. Figure 20 is a schematic of the ADA4304-2 evaluation board. On the ADA4304-2 evaluation board, connectors VO1 and VO4 are not populated.

RF LAYOUT CONSIDERATIONS

Appropriate impedance matching techniques are mandatory when designing circuit boards for the ADA4304-2. Improper characteristic impedances on traces can cause reflections that can lead to poor linearity. The characteristic impedance of the signal trace to the input and from each output should be 75 Ω. Any ground metal on the top surface near signal lines should be stitched with vias to the internal ground plane, as shown in Figure 21.

POWER SUPPLY

The 5 V supply should be applied to each of the VCC pins and RF choke via a low impedance power bus. The power bus should be decoupled to ground using a 10 µF tantalum capacitor and a 0.1 µF ceramic chip capacitor located close to the ADA4304-2. In addition, the VCC pins should be decoupled to ground with a 0.1 µF ceramic chip capacitor located as close to each of the pins as possible.

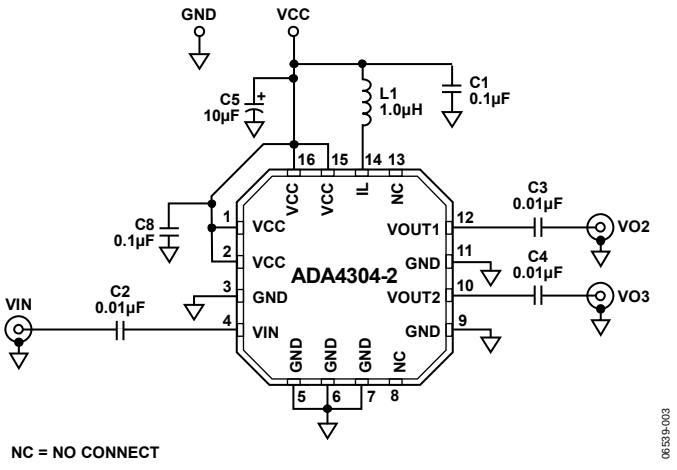


Figure 20. Evaluation Board Schematic

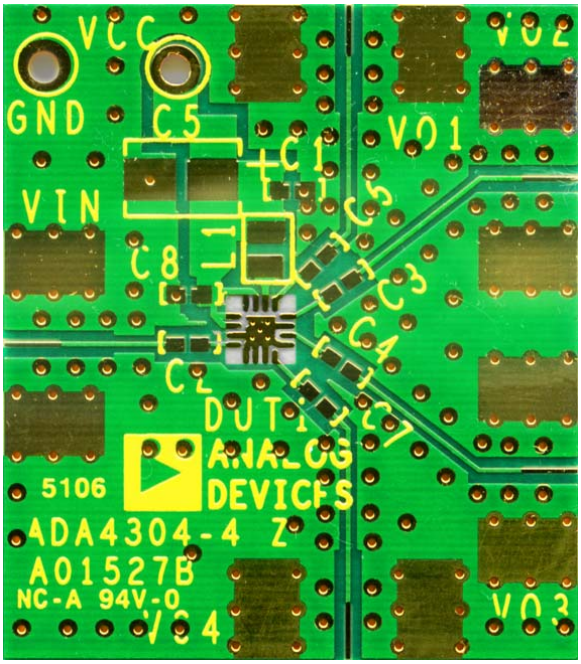


Figure 21. ADA4304-2 Evaluation Board

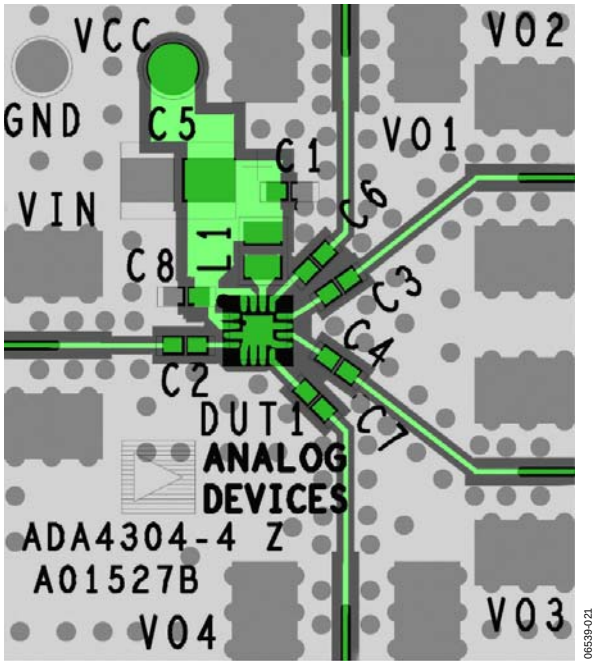


Figure 22. Evaluation Board Component Layout

OUTLINE DIMENSIONS

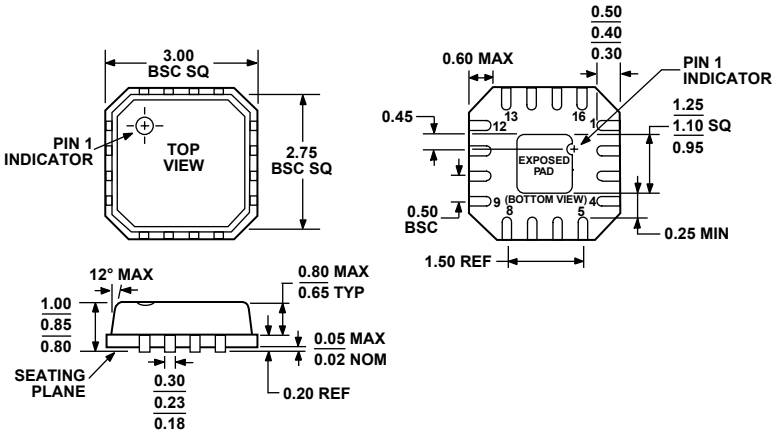


Figure 23. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4304-2ACPZ-RL[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-1	5,000	H0Z
ADA4304-2ACPZ-R7[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-1	1,500	H0Z
ADA4304-2ACPZ-R2[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-1	250	H0Z

[1] Z = RoHS Compliant Part.

NOTES

D06539-0-5/07(0)

Стандарт Электрон Связь

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