Charge-Pump, Parallel Backlight Driver with Image Content PWM Input

Data Sheet

ADP8870

FEATURES

- Charge pump with automatic gain selection of 1×, 1.5×, and 2× for maximum efficiency
- Two high accuracy (±5%) phototransistor inputs for automated ambient light sensing (ALS)
- 5 programmable ambient light-sensing zones for optimal backlight power savings
- Independent ALS control of D7, for automated response of keypad lighting to ambient light levels
- PWM input can be used for content adaptive brightness control (CABC) of any, or all, of the LEDs
- PWM input scales the LED output current
- 7 independent, programmable LED drivers
  - 6 drivers capable of 30 mA (maximum)
  - 1 driver capable of 60 mA (maximum)
- Programmable maximum current limit (128 levels)
- Standby mode for <1 µA current consumption
- 16 programmable fade-in and fade-out times (0.1 sec to 5.5 sec) with choice of square or cubic rates
- Fading override
- I²C-compatible interface for all programming
- Dedicated reset pin and built-in power-on reset (POR)
- Short-circuit, overvoltage, and overtemperature protection
- Internal soft start to limit inrush currents
- Input-to-output isolation during faults or shutdown
- Operates down to V_{IN} = 2.5 V, with undervoltage lockout (UVLO) at 2.0 V.
- Available in a small, 2.15 mm × 2.36 mm × 0.6 mm wafer level chip scale package (WLCSP) or a 4 mm × 4 mm × 0.75 mm lead frame chip scale package (LFCSP)

APPLICATIONS

- Mobile display backlighting
- Mobile phone keypad backlighting
- RGB LED lighting
- LED indication
- General backlighting of small format displays

TYPICAL OPERATING CIRCUIT

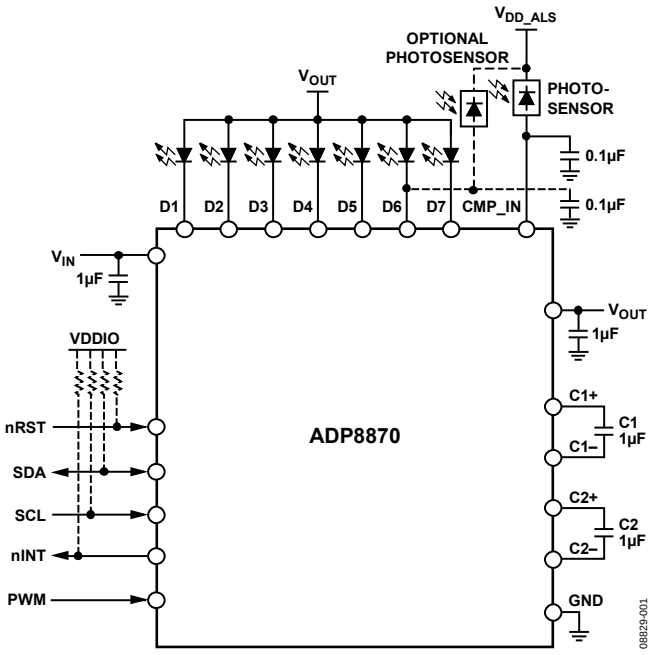

Figure 1.

GENERAL DESCRIPTION

The ADP8870 combines a programmable backlight LED charge-pump driver with automatic phototransistor control of the brightness (LED current) and a PWM input to control the scale of the output current. This combination allows significant power savings because it automatically changes the current intensity based on the sensed ambient lighting levels and the display image content. It performs this function automatically, eliminating the need for a processor to monitor the phototransistor. The light intensity thresholds are fully programmable via the I²C interface.

The ADP8870 allows up to six LEDs to be independently driven up to 30 mA (maximum). An additional seventh LED can be driven to 60 mA (maximum). All LEDs are individually programmable for minimum/maximum current and fade-in/fade-out times through an I²C interface. These LEDs can also be combined into groups to reduce the processor instructions during fade-in and fade-out.

Driving these components is a two-capacitor charge pump with gains of 1×, 1.5×, and 2×. This setup is capable of driving a maximum I_{OUT} of 240 mA from a supply of 2.5 V to 5.5 V. A full suite of safety features, including short-circuit, overvoltage, and overtemperature protection, allows easy implementation of a safe and robust design. Additionally, input inrush currents are limited via an integrated soft start combined with controlled input-to-output isolation.

Rev. C

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REVISION HISTORY

10/2017—Rev. B to Rev. C

Changed CP-20-10 to CP-20-8 ... Throughout
Updated Outline Dimensions ... 57
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1/2014—Rev. A to Rev. B

Change to Figure 35 ... 17

8/2012—Revision A: Initial Version

SPECIFICATIONS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nINT = open, nRST = 2.7 V, CMP_IN = 0 V, $V_{D1:D7}$ = 0.4 V, C1 = 1 µF, C2 = 1 µF, C_{OUT} = 1 µF, typical values are at T_J = 25°C and are not guaranteed, minimum and maximum limits are guaranteed from T_J = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage						
Operating Range	V_{IN}		2.5		5.5	V
Start-Up Level	$V_{IN(START)}$	V_{IN} increasing		2.02	2.3	V
Low Level	$V_{IN(STOP)}$	V_{IN} decreasing	1.6	1.94		V
$V_{IN(START)}$ Hysteresis	$V_{IN(HYS)}$	After startup		80		mV
Quiescent Current	I_Q					
During Standby	$I_{Q(STBY)}$	V_{IN} = 3.6 V, Bit nSTBY = 0, SCL = SDA = 0 V		0.3	1.5	µA
I_Q Active at Gain = 1×	$I_{Q(1×)}$	V_{IN} = 3.6 V, Bit nSTBY = 1, I_{OUT} = 0 mA		1.4	2.0	mA
I_Q Active at Gain = 1.5×	$I_{Q(1.5×)}$	V_{IN} = 3.6 V, Bit nSTBY = 1, I_{OUT} = 0 mA		3.9	5.1	mA
I_Q Active at Gain = 2×	$I_{Q(2×)}$	V_{IN} = 3.6 V, Bit nSTBY = 1, I_{OUT} = 0 mA		4.6	6.2	mA
OSCILLATOR		Charge-pump gain = 2×				
Switching Frequency	f_{SW}		0.90	1.00	1.10	MHz
Duty Cycle	D			50		%
OUPUT CURRENT CONTROL						
Maximum Drive Current	$I_{D1:D7(MAX)}$	$V_{D1:D7}$ = 0.4 V				
D1 to D7		Bit SCR = 0 in the ISC7 register				
T_J = 25°C			28.0	30.0	32.0	mA
T_J = −40°C to +105°C			27.0		33.0	mA
D7 (60 mA Setting)	$I_{D7(60\ mA)}$	V_{D7} = 0.4 V, Bit SCR = 1 in the ISC7 register				
T_J = 25°C			55.0	60.0	65.0	mA
T_J = −40°C to +105°C			52.5		67.0	mA
LED Current Source Matching[1]	I_{MATCH}	$V_{D1:D7}$ = 0.4 V		1	2.5	%
Leakage Current on LED Pins	$I_{D1:D7(LKG)}$	V_{IN} = 5.5 V, $V_{D1:D7}$ = 2.5 V, Bit nSTBY=1			0.5	µA
Equivalent Output Resistance	R_{OUT}					
Gain = 1×		V_{IN} = 3.6 V, I_{OUT} = 100 mA		0.5	1.0	Ω
Gain = 1.5×		V_{IN} = 3.1 V, I_{OUT} = 100 mA		3.0		Ω
Gain = 2×		V_{IN} = 2.5 V, I_{OUT} = 100 mA		3.8		Ω
Regulated Output Voltage	$V_{OUT(REG)}$	V_{IN} = 3 V, gain = 2×, I_{OUT} = 10 mA	4.3	4.7	5.1	V
AUTOMATIC GAIN SELECTION						
Headroom Voltage Threshold for Gain Increase	$V_{HR(UP)}$	Decrease V_{Dx} until the gain switches up	115	180	245	mV
Minimum Current Sink Headroom Voltage	$V_{HR(MIN)}$	I_{Dx} = $I_{Dx(MAX)}$ × 95%		50		mV
Gain Delay	t_{GAIN}	The delay after gain has changed and before gain is allowed to change again		100		µs
AMBIENT LIGHT-SENSING COMPARATORS						
Ambient Light Sensor Current	I_{ALS}					
T_J = 25°C			1.05	1.10	1.15	mA
T_J = −40°C to +105°C			1.00		1.20	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DAC Bit Step						
Threshold for Level 2	I_{L2BIT}	$I_{L2BIT} = I_{ALS}/250$		4.4		µA
Threshold for Level 3	I_{L3BIT}	$I_{L3BIT} = I_{ALS}/500$		2.2		µA
Threshold for Level 4	I_{L4BIT}	$I_{L4BIT} = I_{ALS}/1000$		1.1		µA
Threshold for Level 5	I_{L5BIT}	$I_{L5BIT} = I_{ALS}/2000$		0.55		µA
Ambient Light Sensor Threshold Voltage	V_{ALS}			0.95	1.12	V
PWM SPECIFICATIONS						
V_{DDIO} Voltage Operating Range	V_{DDIO}				5.5	V
Logic Low Input[2]	V_{PWMIL}	V_{IN} = 2.5 V			0.5	V
Logic High Input[3]	V_{PWMIH}	V_{IN} = 5.5 V	1.45			V
Minimum PWM Clock Frequency	$f_{PWM(MIN)}$				140	Hz
Maximum PWM Clock Frequency	$f_{PWM(MAX)}$		60			kHz
PWM Pulse Width	$t_{PWM(MIN)}$	PWM on time for valid detection of PWM input	2			µs
PWM to Output Current Linearity		Maximum deviation in output current vs. PWM duty cycle from 100% to 25%		1.4		%
Response Time of PWM Controlled Output		f_{PWM} < 2 kHz		$1/f_{PWM}$		sec
Response Time of PWM Controlled Output		f_{PWM} > 2 kHz			1.3	ms
PWM Accuracy		BLMX = 0x7F (30 mA), PWM duty cycle = 50%		1.0		%
FAULT PROTECTION						
Start-Up Charging Current Source	I_{SS}	V_{IN} = 3.6 V, $V_{OUT} = 0.8 \times V_{IN}$	3.5	7.0	11.0	mA
Output Voltage Threshold	V_{OUT}					
Exit Soft Start	$V_{OUT(START)}$	V_{OUT} rising		$0.92 \times V_{IN}$		V
Short-Circuit Protection	$V_{OUT(SC)}$	V_{OUT} falling		$0.55 \times V_{IN}$		V
Output Overvoltage Protection Activation Level	V_{OVP}			5.7		V
Thermal Shutdown						
Threshold	TSD			150		°C
Hysteresis	$TSD_{(HYS)}$			20		°C
Isolation from Input to Output During Fault	I_{OUTLKG}	V_{IN} = 5.5 V, V_{OUT} = 0 V, Bit nSTBY = 0			1	µA
Time to Validate a Fault	t_{FAULT}			2		µs
I²C INTERFACE						
V_{DDIO} Voltage Operating Range	V_{DDIO}				5.5	V
Logic Low Input[2]	V_{IL}	V_{IN} = 2.5 V			0.5	V
Logic High Input[3]	V_{IH}	V_{IN} = 5.5 V	1.45			V
I²C TIMING SPECIFICATIONS		Guaranteed by design				
Delay from Reset Deassertion to I²C Access	t_{RESET}				20	µs
SCL Clock Frequency	f_{SCL}				400	kHz
SCL High Time	t_{HIGH}		0.6			µs
SCL Low Time	t_{LOW}		1.3			µs
Setup Time						
Data	$t_{SU, DAT}$		100			ns
Repeated Start	$t_{SU, STA}$		0.6			µs
Stop Condition	$t_{SU, STO}$		0.6			µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hold Time						
Data	$t_{HD, DAT}$		0		0.9	µs
Start/Repeated Start	$t_{HD, STA}$		0.6			µs
Bus-Free Time (Stop and Start Conditions)	t_{BUF}		1.3			µs
Rise Time (SCL and SDA)	t_R		20 + 0.1 C_B		300	ns
Fall Time (SCL and SDA)	t_F		20 + 0.1 C_B		300	ns
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Capacitive Load Per Bus Line	C_B				400	pF

[1] Matching is calculated by dividing the difference between the maximum and minimum current from the sum of the maximum and minimum.
[2] V_{IL} is a function of the V_{IN} voltage. See Figure 19 in the Typical Performance Characteristics section for typical values over operating ranges.
[3] V_{IH} is a function of the V_{IN} voltage. See Figure 19 in the Typical Performance Characteristics section for typical values over operating ranges.

Timing Diagram

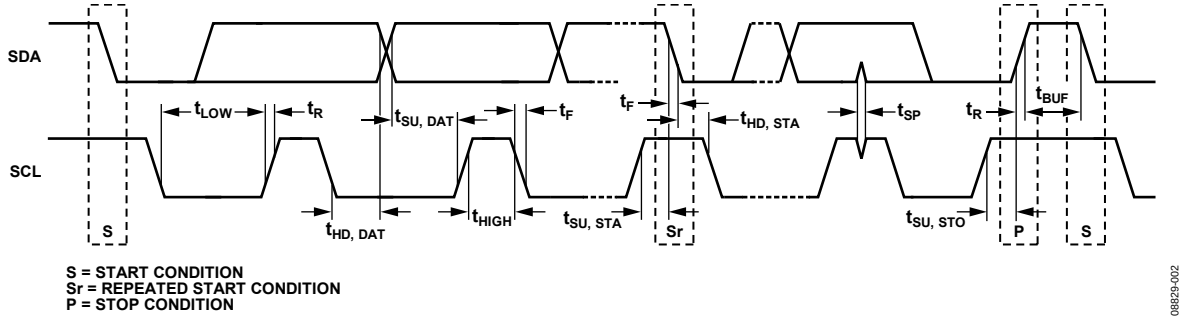


Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, VOUT to GND	−0.3 V to +6 V
D1, D2, D3, D4, D5, D6, and D7 to GND	−0.3 V to +6 V
CMP_IN to GND	−0.3 V to +6 V
nINT, nRST, SCL, and SDA to GND	−0.3 V to +6 V
Output Short-Circuit Duration	Indefinite
Operating Ambient Temperature Range[1]	−40°C to +85°C
Operating Junction Temperature Range[1]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
ESD (Electrostatic Discharge)	
Human Body Model (HBM)	±2.0 kV
Charged Device Model (CDM)	±1.5 kV

[1] The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). See the Maximum Temperature Ranges section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to GND.

MAXIMUM TEMPERATURE RANGES

The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). Therefore, in situations where the ADP8870 is exposed to poor thermal resistance and a high power dissipation (P_D), the maximum ambient temperature may need to be derated. In these cases, the ambient temperature maximum can be calculated with the following equation:

$$T_{A(MAX)} = T_{J(MAX)} - (\theta_{JA} \times P_{D(MAX)}).$$

THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA}, θ_{JB} (junction to board), and θ_{JC} (junction to case) are determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling. For the LFCSP package, the exposed pad must be soldered to GND.

Table 3. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
WLCSP	48	9	N/A	°C/W
LFCSP	49.5	N/A	5.3	°C/W

[1] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

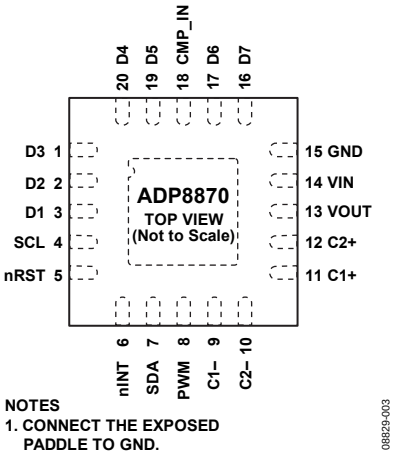


Figure 3. LFCSP Pin Configuration

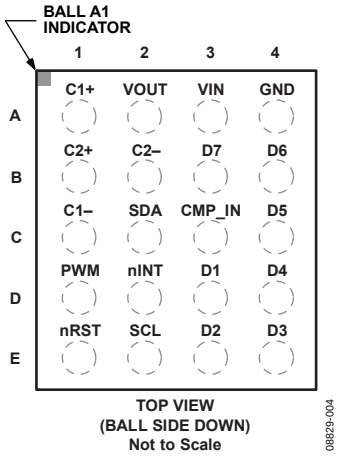


Figure 4. WLCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
LFCSP	**WLCSP**	**Mnemonic**	**Description**
14	A3	VIN	Input Voltage (2.5 V to 5.5 V).
3	D3	D1	LED Sink 1.
2	E3	D2	LED Sink 2.
1	E4	D3	LED Sink 3.
20	D4	D4	LED Sink 4.
19	C4	D5	LED Sink 5.
17	B4	D6	LED Sink 6 and optional comparator input for second phototransistor. When this pin is used as a second phototransistor input, a capacitor (0.1 µF recommended) must be connected from this pin to ground.
16	B3	D7	LED Sink 7.
18	C3	CMP_IN	Comparator Input for Phototransistor. When this pin is used, a capacitor (0.1 µF recommended) must be connected from this pin to ground.
13	A2	VOUT	Charge-Pump Output.
11	A1	C1+	Charge-Pump C1+.
9	C1	C1−	Charge-Pump C1−.
12	B1	C2+	Charge-Pump C2+.
10	B2	C2−	Charge-Pump C2−.
15	A4	GND	Ground.
8	D1	PWM	PWM Input for LED Dimming.
6	D2	nINT	Processor Interrupt (Active Low). Requires an external pull-up resistor. If this pin is not used, it can be left floating.
5	E1	nRST	Hardware Reset (Active Low). This bit resets the device to the default conditions. If this pin is not used, it must be tied above $V_{IH(MAX)}$.
7	C2	SDA	I^2C Serial Data. Requires an external pull-up resistor.
4	E2	SCL	I^2C Clock. Requires an external pull-up resistor.
EP		EP	Exposed Paddle. The exposed paddle must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nRST = 2.7 V, $V_{D1:D7}$ = 0.4 V, C_{IN} = 1 µF, C1 = 1 µF, C2 = 1 µF, C_{OUT} = 1 µF, T_A= 25°C, unless otherwise noted.

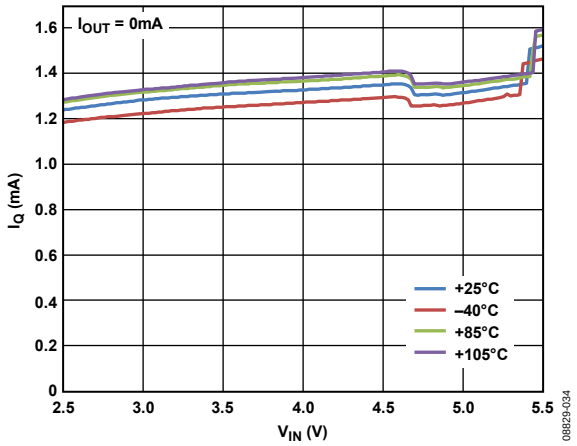


Figure 5. Typical Operating Current, G = 1×

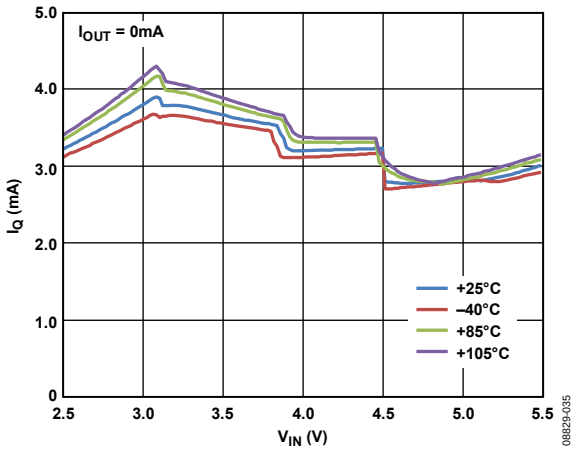


Figure 6. Typical Operating Current, G = 1.5×

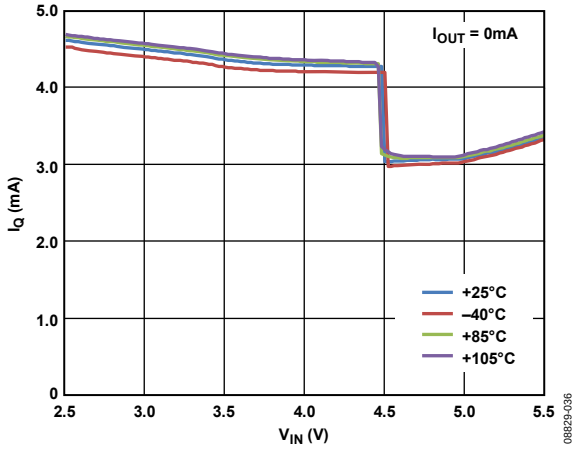


Figure 7. Typical Operating Current, G = 2×

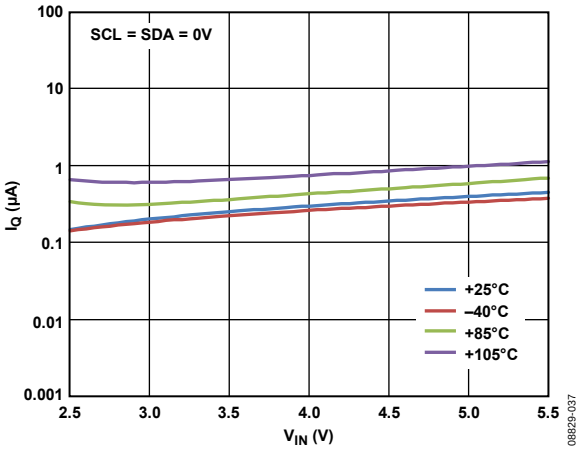


Figure 8. Typical Standby I_Q

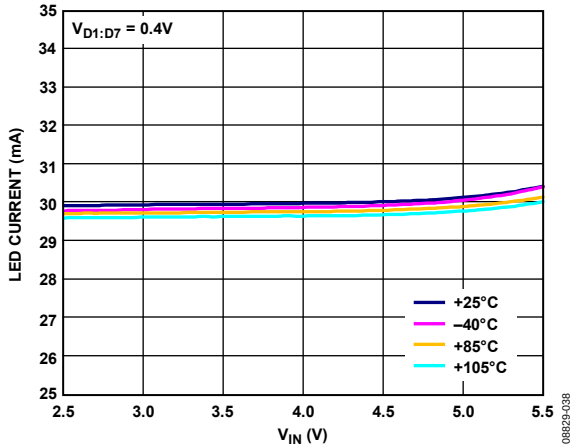


Figure 9. Typical Diode Current vs. V_{IN}

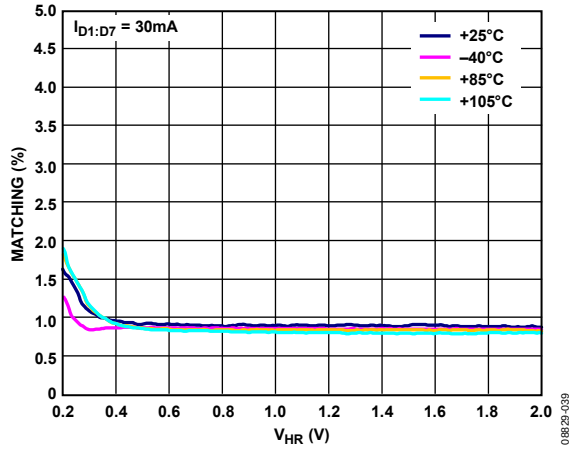


Figure 10. Typical Diode Matching vs. Current Sink Headroom Voltage (V_{HR})

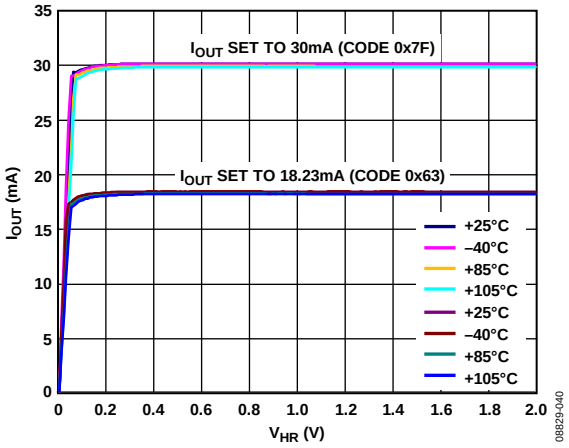


Figure 11. Typical Diode Current vs. Current Sink Headroom Voltage (V_{HR})

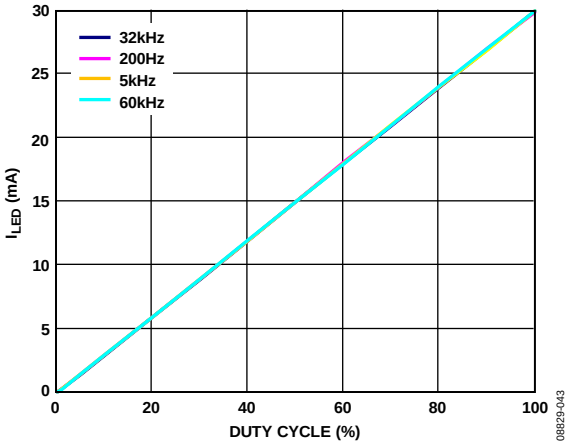


Figure 14. PWM Current Scaling Across PWM Frequency

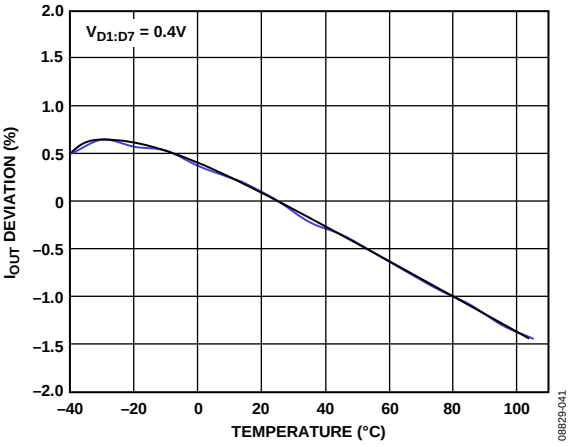


Figure 12. Typical Change In Diode Current vs. Temperature

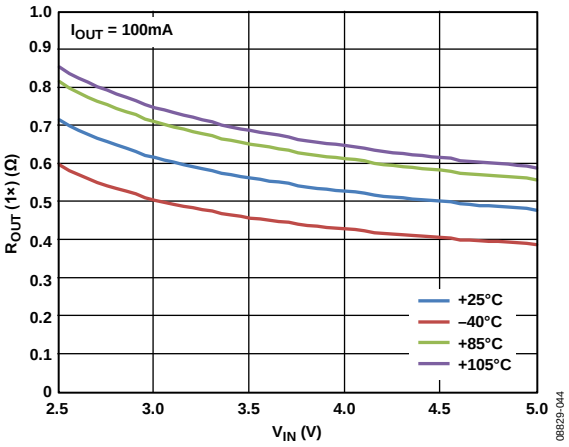


Figure 15. Typical R_{OUT} (G = 1×) vs. V_{IN}

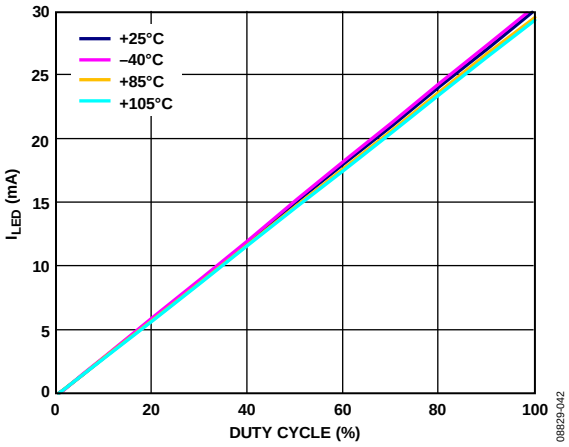


Figure 13. PWM Current Scaling Across Temperature

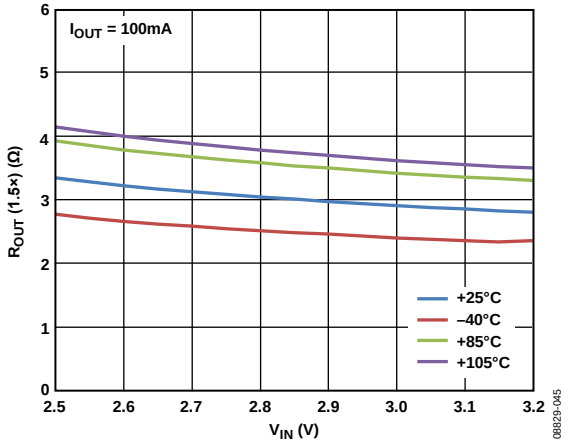


Figure 16. Typical R_{OUT} (G = 1.5×) vs. V_{IN}

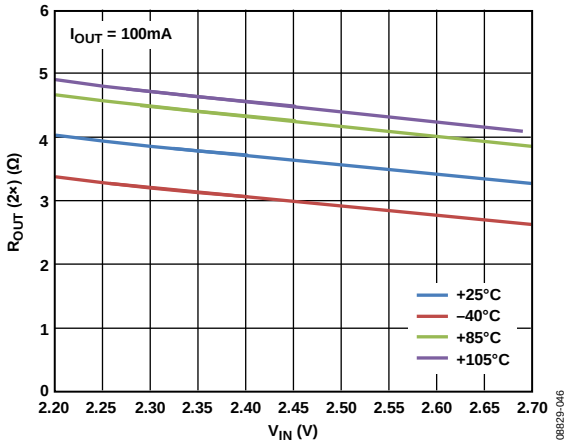


Figure 17. Typical R_{OUT} ($G = 2\times$) vs. V_{IN}

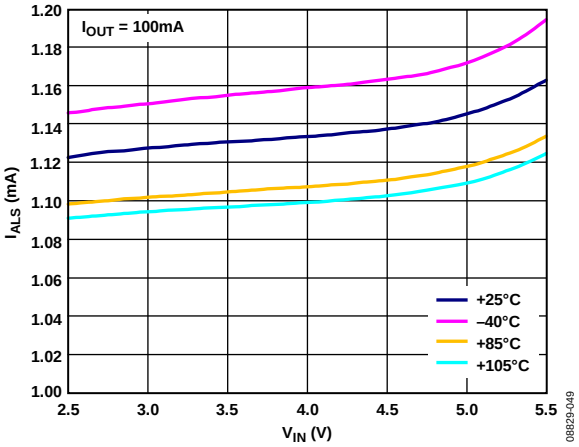


Figure 20. Typical ALS Current (I_{ALS})

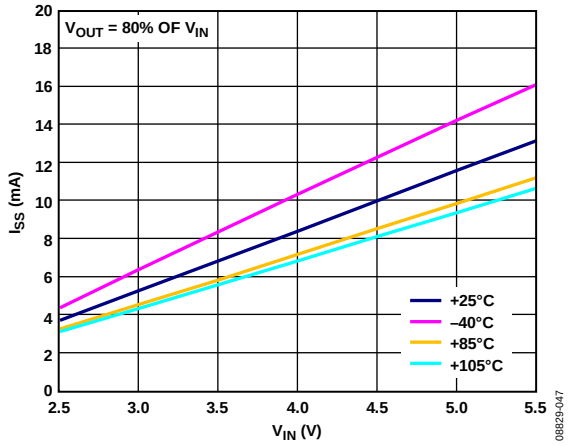


Figure 18. Typical Output Soft Start Current (I_{SS})

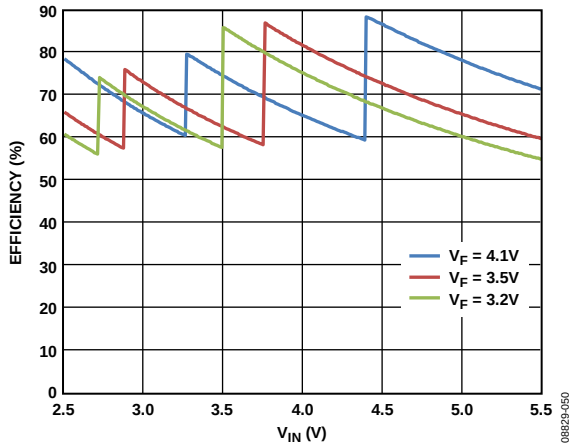


Figure 21. Typical Efficiency (Seven LEDs, 30 mA per LED)

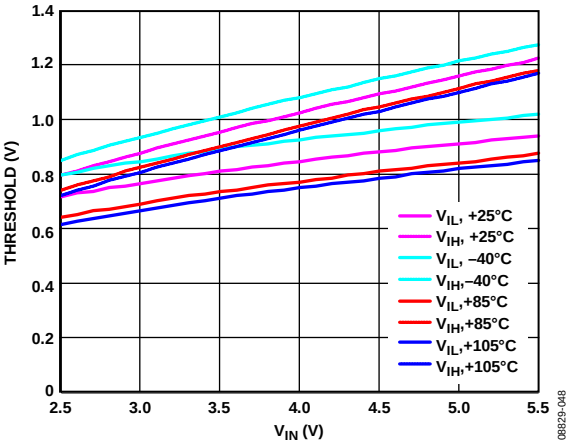


Figure 19. Typical I^2C Thresholds (V_{IH} and V_{IL})

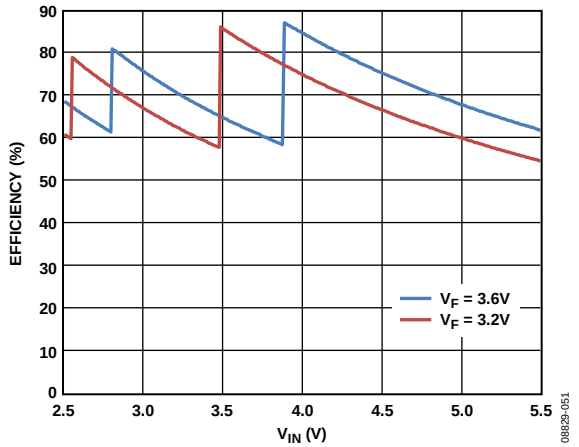


Figure 22. Typical Efficiency (Seven LEDs, 18 mA per LED)

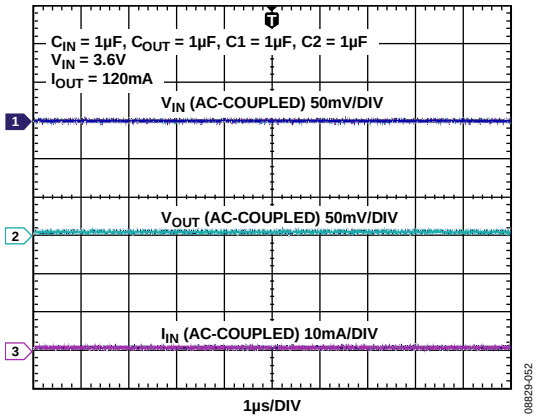


Figure 23. Typical Operating Waveforms, G = 1×

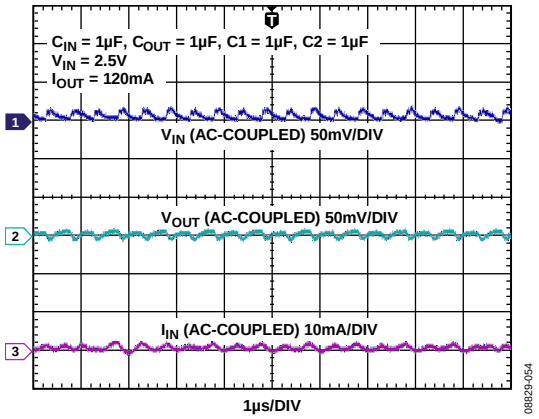


Figure 25. Typical Operating Waveforms, G = 2×

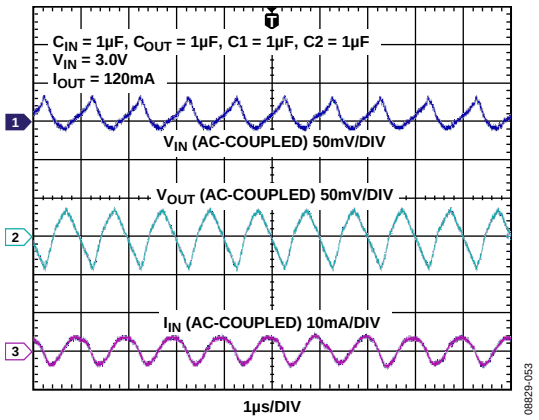


Figure 24. Typical Operating Waveforms, G = 1.5×

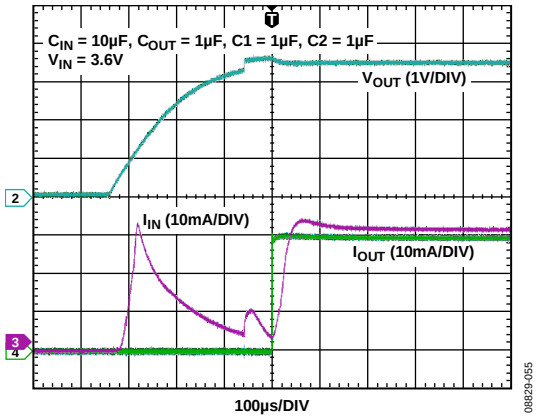


Figure 26. Typical Start-Up Waveforms

THEORY OF OPERATION

The ADP8870 combines a programmable backlight LED charge-pump driver with automatic phototransistor brightness control (LED current) and a PWM input to control the scale of the output current. This combination allows significant power savings because it automatically changes the current intensity based on the sensed ambient lighting levels and the display image content. It performs this function automatically and, therefore, removes the need for a processor to monitor the phototransistor. The light intensity thresholds are fully programmable via the I²C interface. A second phototransistor input, with dedicated comparators, improves the ambient light detection abilities for various operating conditions.

The ADP8870 allows up to seven LEDs to be independently driven up to 30 mA (typical). The seventh LED can be driven an additional 30 mA, for a maximum of up to 60 mA (typical). All LEDs can be individually programmed or combined into a group to operate backlight LEDs. A full suite of safety features, including short-circuit, overvoltage, and overtemperature protection with input-to-output isolation, allow for a robust and safe design. The integrated soft start limits inrush currents at startup, restart attempts, and gain transitions.

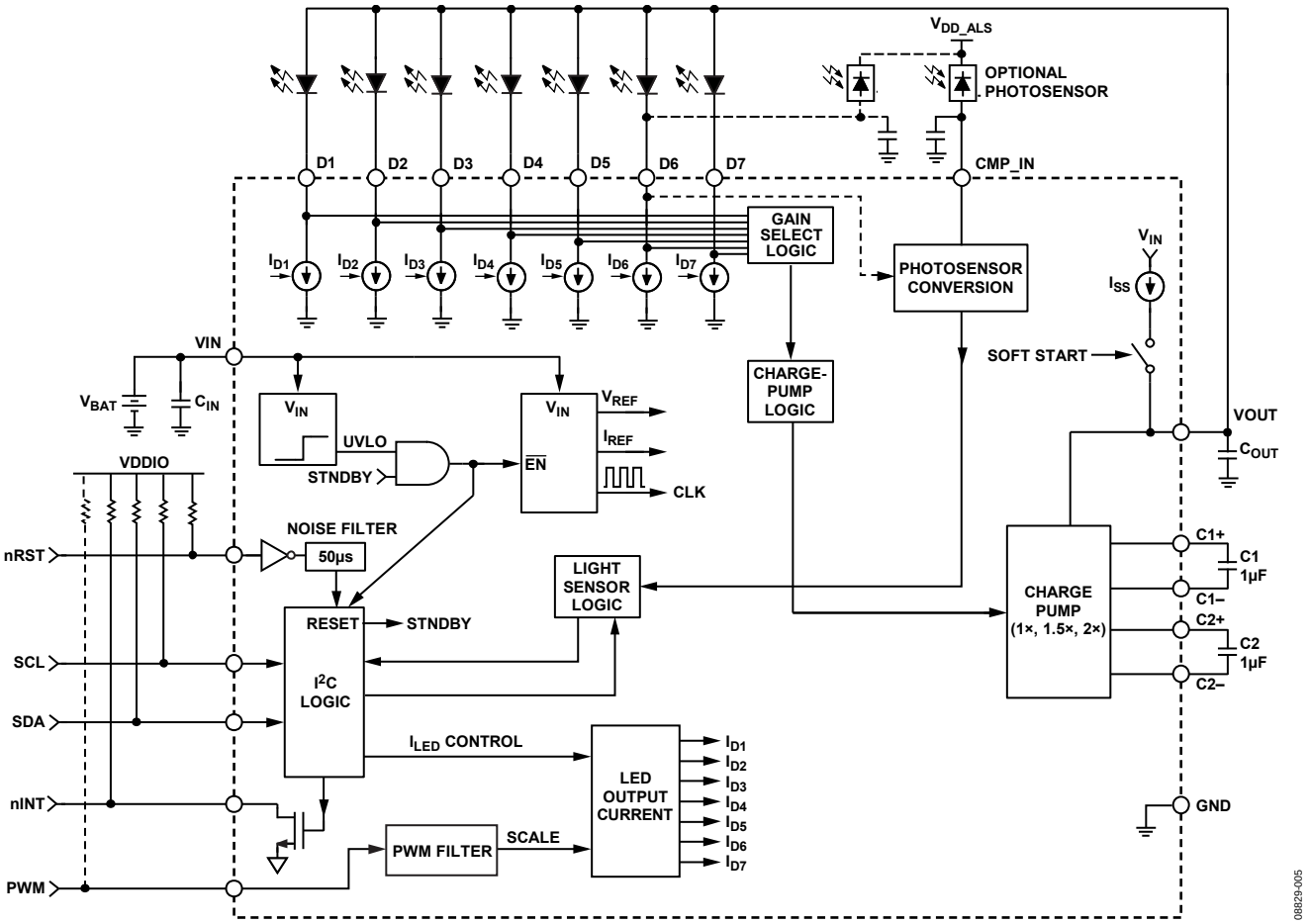


Figure 27. Detailed Block Diagram

POWER STAGE

Because typical white LEDs require up to 4 V to drive them, some form of boosting is required over the typical variation in battery voltage. The ADP8870 accomplishes this with a high efficiency charge pump capable of producing a maximum I_{OUT} of 240 mA over the entire input voltage range (2.5 V to 5.5 V). Charge pumps use the basic principle that a capacitor stores charge based on the voltage applied to it, as shown in the following equation:

$$Q = C \times V \quad (1)$$

By charging the capacitors in different configurations, the charge, and hence the gain, can be optimized to deliver the voltage required to power the LEDs. Because a fixed charging and discharging combination must be used, only certain multiples of gain are available. The ADP8870 is capable of automatically optimizing the gain (G) from 1×, 1.5×, and 2×. These gains are accomplished with two capacitors and an internal switching network.

In G = 1× mode, the switches are configured to pass VIN directly to VOUT. In this mode, several switches are connected in parallel to minimize the resistive drop from input to output. In G = 1.5× and G = 2× modes, the switches alternatively charge from the battery and discharge into the output. For G = 1.5×, the capacitors are charged from VIN in series and are discharged to VOUT in parallel. For G = 2×, the capacitors are charged from VIN in parallel and are discharged to VOUT in parallel. In certain fault modes, the switches are opened and the output is physically isolated from the input.

Automatic Gain Selection

Each LED that is driven requires a current source. The voltage on this current source must be greater than a minimum headroom voltage (225 mV typical) to maintain accurate current regulation. The gain is automatically selected based on the minimum voltage (V_{Dx}) at all of the current sources. At startup, the device is placed into G = 1× mode and the output charges to V_{IN}. If any V_{Dx} level is less than the required headroom (200 mV), then the gain is increased to the next step (G = 1.5 ×). A 100 µs delay is allowed for the output to stabilize prior to the next gain switching decision. If there remains insufficient current sink headroom, then the gain is increased again to 2×. Conversely, to optimize efficiency, it is not desirable for the output voltage to be too high. Therefore, the gain reduces when the headroom voltage is great enough. This point (labeled $V_{D(MAX)}$ in Figure 28) is internally calculated to ensure that the lower gain still results in ample headroom for all the current sinks. The entire cycle is illustrated in Figure 28.

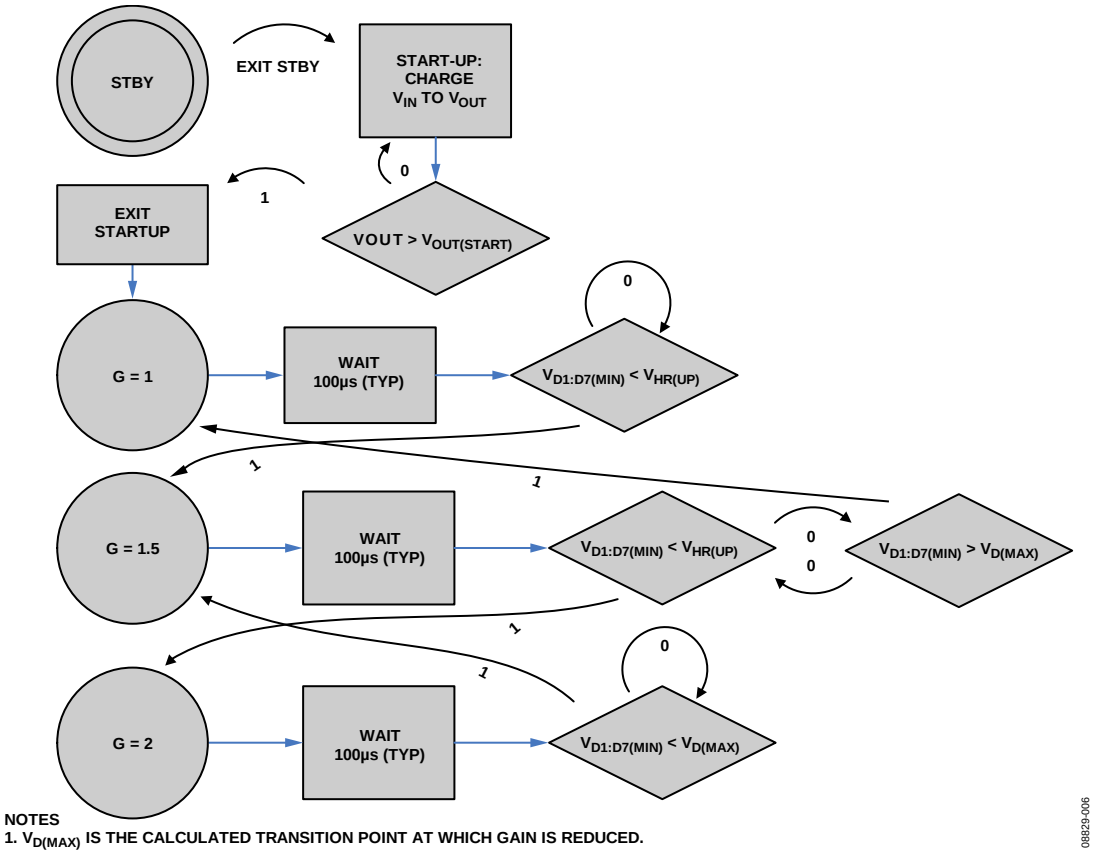


Figure 28. State Diagram for Automatic Gain Selection

Note that the gain selection criteria apply only to active current sources. If a current source has been deactivated through an I²C command (that is, if only five LEDs are used for an application), the voltages on these current sources are ignored.

Soft Start Feature

At startup (either from UVLO activation or fault/standby recovery), the output is first charged by I_{SS} (7.0 mA typical) until it reaches about 92% of V_{IN}. This soft start feature reduces the inrush current that is otherwise present when the output capacitance is initially charged to V_{IN}. When this point is reached, the controller enters 1× mode. If the output voltage is not sufficient, then the automatic gain selection determines the optimal point as described in the Automatic Gain Selection section.

OPERATING MODES

There are four different operating modes: active, standby, shutdown, and reset.

Active Mode

In active mode, all circuits are powered up and in a fully operational state. This mode is entered when nSTBY (in Register MDCR) is set to 1.

Standby Mode

Standby mode disables all circuitry except the I²C receivers. Current consumption is reduced to less than 1 μA. This mode is entered when nSTBY is set to 0 or when the nRST pin is held low for more than 100 μs (maximum). When standby is exited, a soft start sequence is performed.

Shutdown Mode

Shutdown mode disables all circuitry, including the I²C receivers. Shutdown occurs when V_{IN} is below the undervoltage thresholds. When V_{IN} rises above $V_{IN(START)}$ (2.02 V typical), all registers are reset and the part is placed into standby mode.

Reset Mode

In reset mode, all registers are set to their default values and the part is placed into standby. There are two ways to reset the part: power-on reset (POR) and the nRST pin. POR is activated anytime that the part exits shutdown mode. After a POR sequence is complete, the part automatically enters standby mode.

After startup, the part can be reset by pulling the nRST pin low. As long as the nRST pin is low, the part is held in a standby state but no I²C commands are acknowledged (all registers are kept at their default values). After releasing the nRST pin, all registers remain at their default values, and the part remains in standby; however, the part does accept I²C commands.

The nRST pin has a 50 μs (typical) noise filter to prevent inadvertent activation of the reset function. The nRST pin must be held low for this entire time to activate a reset.

The operating modes function according to the timing shown in Figure 29.

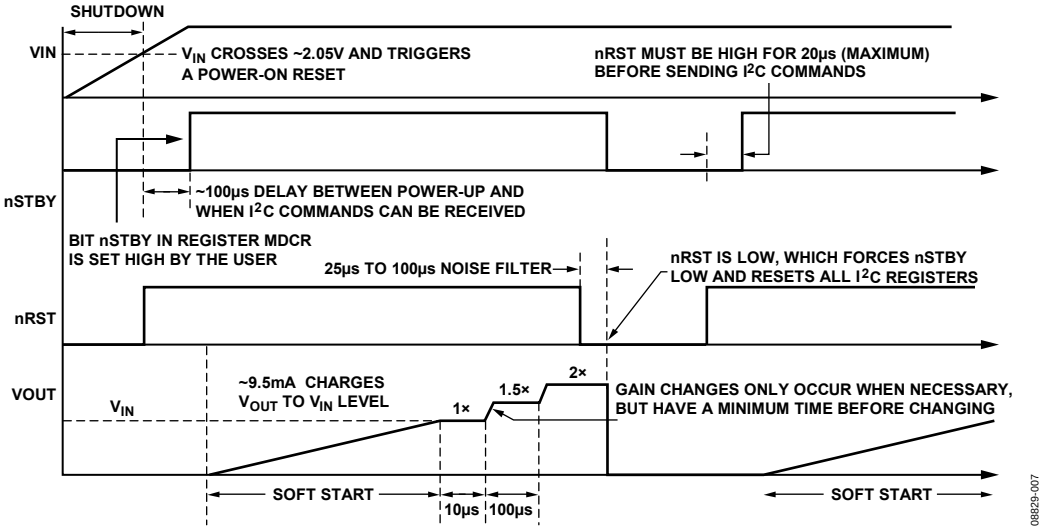


Figure 29. Typical Timing Diagram

IMAGE CONTENT CONTROL

Modern LCD display drivers often output the white intensity of the displayed image in the form of a PWM signal. When the white content of the displayed image is very small, the LCD driver generates a PWM duty cycle that is large. The ADP8870 takes advantage of this feature by incorporating a PWM input pin that scales the backlight intensity. When the PWM signal is at 100% duty cycle, the backlight current functions at its programmed value. However, when the PWM duty cycle drops, the ADP8870 automatically scales the output LED current down.

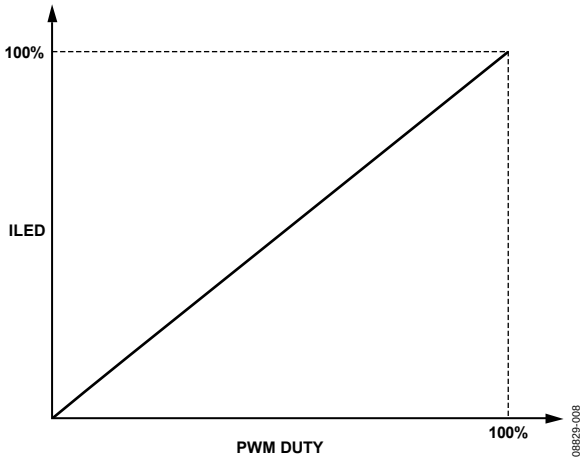


Figure 30. Output Current Response to PWM Input Duty Cycle

The LEDs that respond to the PWM input can be selected in the PWMLED register (Register 0x06). This image content works naturally with the automatic ambient light sensing and the three gains of the charge pump (see Figure 31).

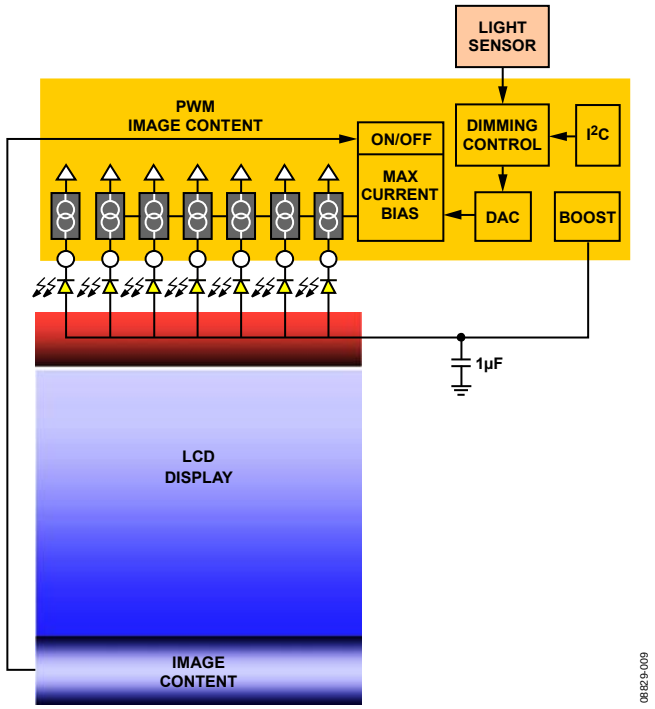


Figure 31. Functional Overview of the PWM Image Content Control, Ambient Light Sensor, and Charge Pump

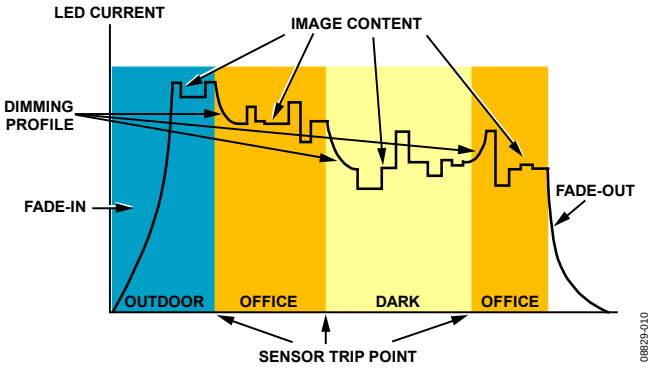


Figure 32. Example LED Output Current with the Effects of the Image Content PWM and Ambient Light Sensing

BACKLIGHT OPERATING LEVELS

Backlight brightness control can operate in five distinct levels: daylight (Level 1), bright (Level 2), office (Level 3), indoor (Level 4), and dark (Level 5). The BLV bits in Register 0x04 control the specific level in which the backlight operates. These bits can be changed manually, or if in automatic mode (that is, when CMP_AUTOEN is set high in Register 0x01), by the ambient light sensor (see the D7 Ambient Light-Sensing Control section).

By default, the backlight operates at daylight level (BLV = 000), where the maximum brightness is set using Register 0x0A (BLMX1). A daylight dim setting can also be set using Register 0x0B (BLDM1). Similarly, when operating at the bright, office, indoor, or dark level, the corresponding register is used (Register 0x0C to Register 0x13).

BACKLIGHT MAXIMUM AND DIM SETTINGS

The backlight maximum and dim current settings are determined by a 7-bit code programmed by the user into the registers previously listed in the Image Content Control section. The 7-bit resolution allows the user to set the backlight to one of 128 different levels between 0 mA and 30 mA. The ADP8870 implements a square law algorithm to achieve a nonlinear relationship between input code and backlight current. The backlight current (in milliamperes) is determined by the following equation:

$$Backlight\ Current\ (\text{mA}) = \left(Code \times \frac{\sqrt{Full-Scale\ Current}}{127} \right)^2 \quad (2)$$

where:
Code is the input code programmed by the user.
Full-Scale Current is the maximum sink current allowed per LED (typically 30 mA).

Figure 34 shows the backlight current level vs. input code.

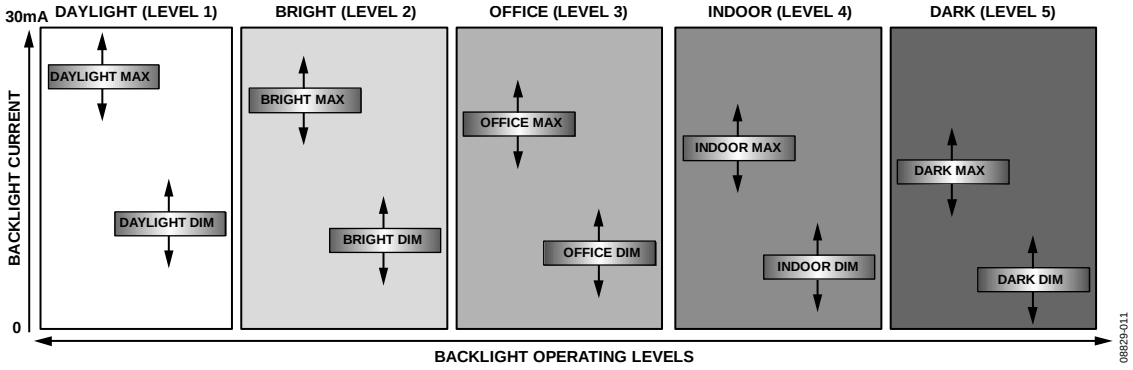


Figure 33. Backlight Operating Level

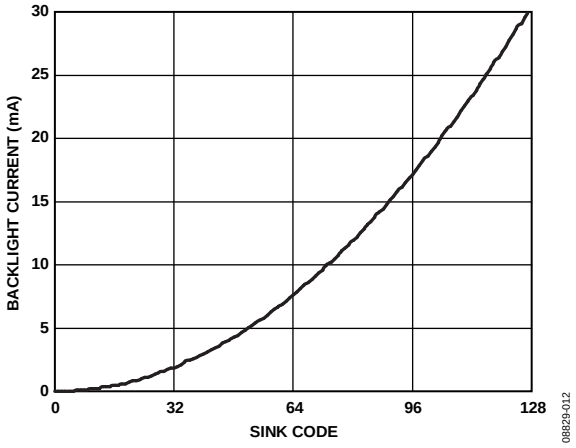


Figure 34. Backlight Current vs. Sink Code

AUTOMATED FADE-IN AND FADE-OUT

The LED drivers are easily configured for automated fade-in and fade-out. Sixteen fade-in and fade-out rates can be selected via the I²C interface. Fade-in and fade-out rates range from 0.1 sec to 5.5 sec (per full-scale current, either 30 mA or 60 mA). The BLOFF_INT bit (Register 0x02) can be used to flag the interrupt pin when an automated backlight fade-out occurs (see the Interrupts section).

Table 5. Available Fade-In and Fade-Out Times

Code	Fade Rate (sec)
0000	0.1 (disabled)
0001	0.3
0010	0.6
0011	0.9
0100	1.2
0101	1.5
0110	1.8
0111	2.1
1000	2.4
1001	2.7
1010	3.0
1011	3.5
1100	4.0
1101	4.5
1110	5.0
1111	5.5

The fade profile is based on the transfer law selected (square, Cubic 10, or Cubic 11) and the delta between the actual current and the target current. Smaller changes in current reduce the fade time. For square law fades, the fade time is given by

$$Fade\ Time = Fade\ Rate \times (Code/127) \quad (3)$$

where the *Fade Rate* is as shown in Table 5.

The Cubic 10 and Cubic 11 laws also use the square backlight currents in Equation 3; however, the time between each step is varied to produce a steeper slope at higher currents and a shallower slope at lighter currents (see Figure 35).

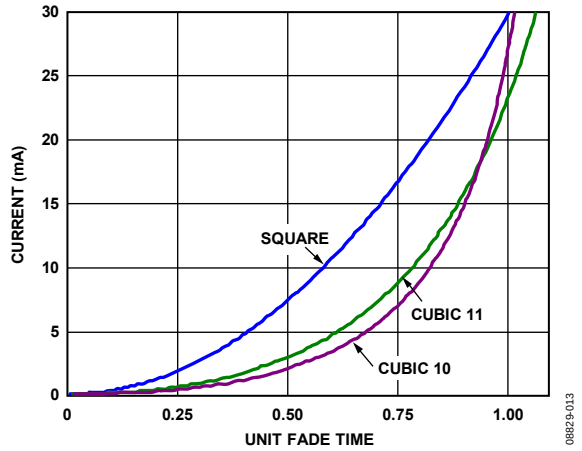


Figure 35. Comparison of the Dimming Transfers Laws

BACKLIGHT TURN ON/TURN OFF/DIM

With the device in active mode (nSTBY = 1), the backlight can be turned on using the BL_EN bit in Register 0x01. Before turning on the backlight, the user chooses which level (daylight, bright, office, indoor, or dark) in which to operate and ensures that maximum and dim settings are programmed for that level. The backlight turns on when BL_EN = 1. The backlight turns off when BL_EN = 0.

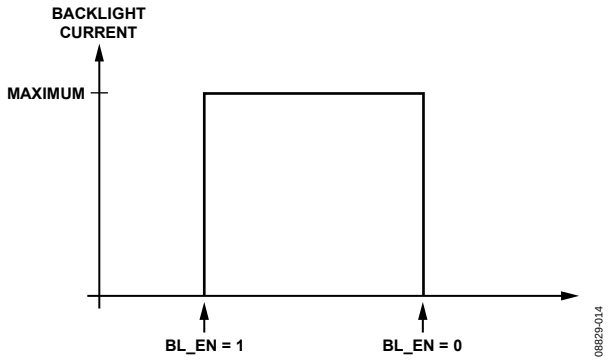


Figure 36. Backlight Turn On/Turn Off

While the backlight is on (BL_EN = 1), the user can make it change to a dim setting by programming DIM_EN = 1 in Register 0x01. If DIM_EN = 0, then the backlight reverts to its maximum setting.

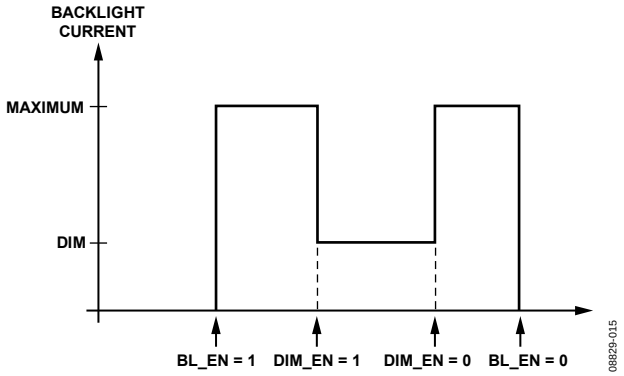


Figure 37. Backlight Turn On/Dim/Turn Off

The maximum and dim settings can be set between 0 mA and 30 mA; therefore, it is possible to program a dim setting that is greater than a maximum setting. For normal expected operation, ensure that the dim setting is programmed to be less than the maximum setting.

AUTOMATIC DIM AND TURN OFF TIMERS

The user can program the backlight to dim automatically by using the DIMT timer in Register 0x08. The dim timer has 127 settings, ranging from 1 sec to 127 sec. Program the dim timer before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the dim timer starts counting. When the dim timer expires, the internal state machine sets DIM_EN = 1, and the backlight enters its dim setting.

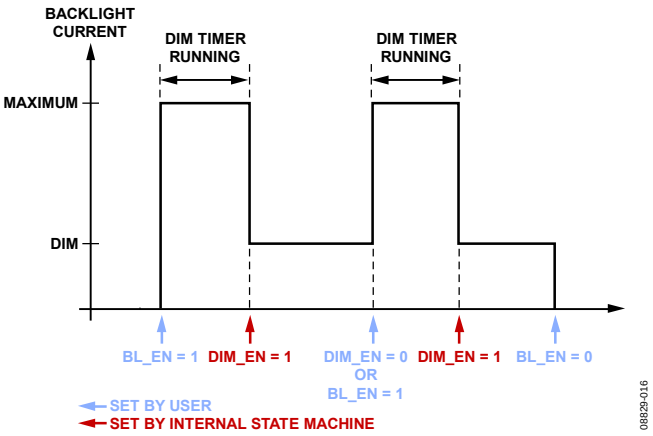


Figure 38. Dim Timer

If the user clears the DIM_EN bit (or reasserts the BL_EN bit), the backlight reverts to its maximum setting and the dim timer begins counting again. When the dim timer expires, the internal state machine again sets DIM_EN = 1, and the backlight enters its dim setting. Reasserting BL_EN at any point during the dim timer countdown causes the timer to reset and resume counting. The backlight can be turned off at any point during the dim timer countdown by clearing BL_EN.

The user can also program the backlight to turn off automatically by using the OFFT timer in Register 0x07. The off timer has 127 settings, ranging from 1 sec to 127 sec. Program the off timer before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the off timer starts counting. When the off timer expires, the internal state machine clears the BL_EN bit, and the backlight turns off.

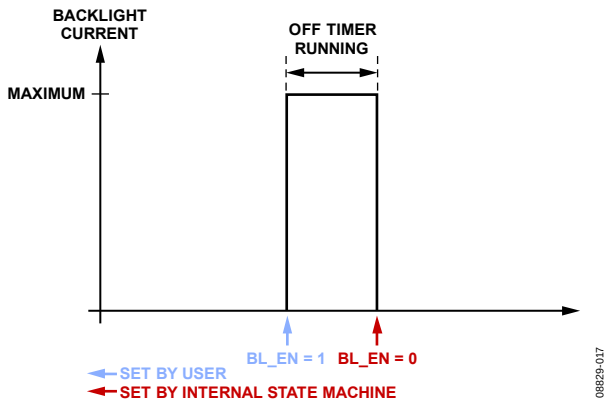


Figure 39. Off Timer

Reasserting BL_EN at any point during the off timer countdown causes the timer to reset and resume counting. The backlight can be turned off at any point during the off timer countdown by clearing BL_EN.

The dim timer and off timer can be used together for sequential maximum-to-dim-to-off functionality. With both the dim and off timers programmed, if BL_EN is asserted, the backlight turns on to its maximum setting. When the dim timer expires, the backlight changes to its dim setting. When the off timer expires, the backlight turns off.

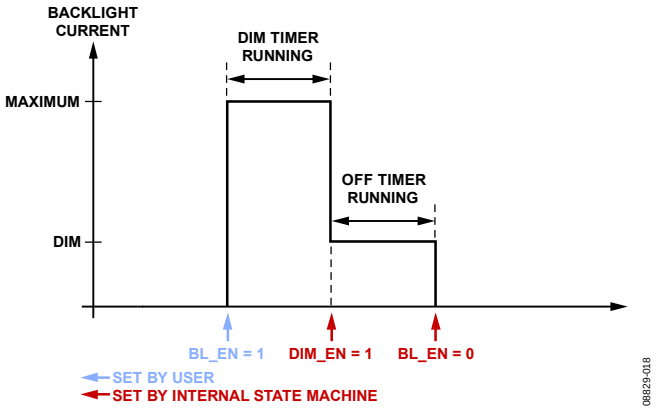


Figure 40. Dim Timer and Off Timer Used Together

FADE OVERRIDE

A fade override feature (FOVR in Register CFGR (Address 0x04)) enables the host to override the preprogrammed fade-in or fade-out settings. If FOVR is set and the backlight is enabled in the middle of a fade-out process, the backlight instantly (within approximately 100 ms) returns to its prefade brightness level. Alternatively, if the backlight is fading in, reasserting BL_EN overrides the programmed fade-in time and the backlight instantly goes to its final fade value. This is useful for situations where a key is pressed during a fade sequence. Alternatively, if FOVR is cleared and the backlight is enabled in the middle of a fade process, the backlight fades in from where it was interrupted (that is, it does not go down to 0 and then come back on).

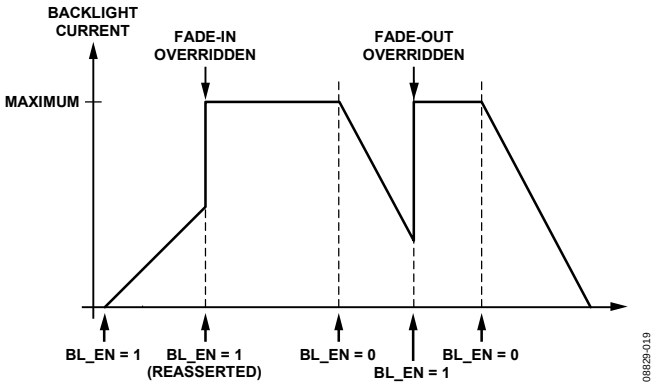


Figure 41. Fade Override Function (FOVR is High)

BACKLIGHT AMBIENT LIGHT SENSING

The ADP8870 integrates two ambient light-sensing comparators. One of the ambient light sensing comparators (CMP_IN) is always available. The second one (CMP_IN2) can be activated instead of having an LED connected to D6. Activating CMP_IN2 is accomplished through Bit CMP2_SEL in Register CFGR. Therefore, when Bit CMP2_SEL is set to 0, Pin D6 is programmed as a current sink. When Bit CMP2_SEL is set to 1, Pin D6 becomes the input for a second phototransistor.

These comparators have four programmable trip points (Level 2, Level 3, Level 4, and Level 5) that can be used to select between the five backlight operating modes (daylight, bright, office, indoor, and dark) based on the ambient lighting conditions.

The Level 5 comparator controls the dark-to-indoor mode transition. The Level 4 comparator controls the indoor-to-office transition. The Level 3 comparator controls the office-to-bright transition. The Level 2 comparator controls the bright-to-outdoor transition (see Figure 42). The currents for the different lighting modes are defined in the BLMXx and BLDMx registers (see the Backlight Operating Levels section).

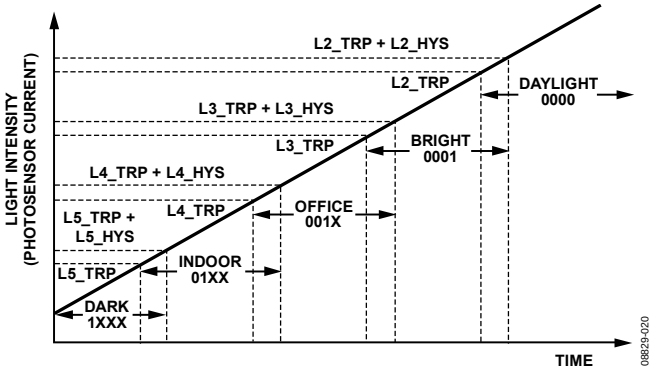


Figure 42. Light Sensor Modes are Based on the Ambient Light Level Detected

Each light sensor comparator uses an external capacitor together with an internal reference current source to form an analog-to-digital converter (ADC) that samples the output of the external photosensor. The ADC result is fed into four programmable trip comparators. The ADC has an input range of 0 µA to 1100 µA (typical).

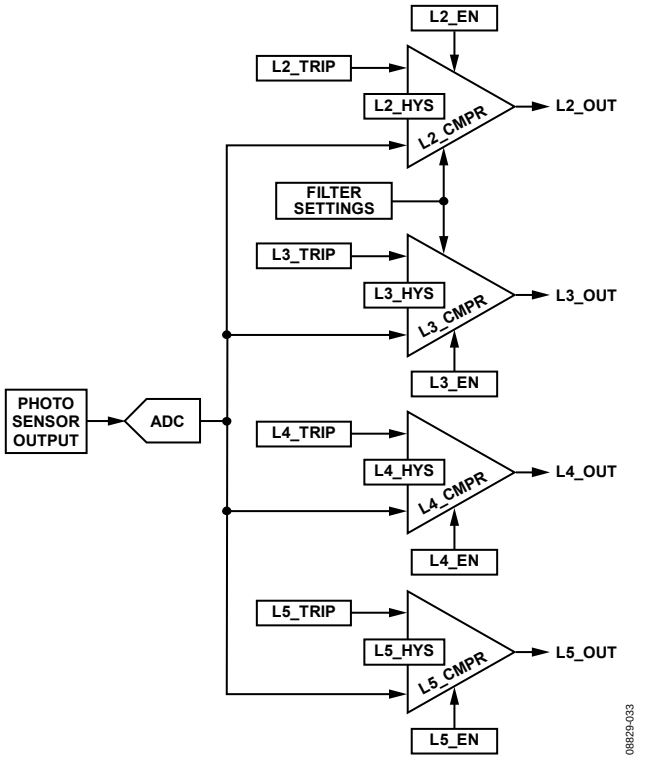


Figure 43. Ambient Light-Sensing and Trip Comparators

Each level comparator detects when the photosensor output has dropped below the programmable trip point (defined in Register 0x32, Register 0x34, Register 0x36, and Register 0x38). If this event occurs, then the corresponding level output status signal is set in Register 0x30 and Register 0x31. Each level comparator contains programmable hysteresis, meaning that the photosensor output must rise above the trip threshold plus the hysteresis value before the level output clears. Each level is enabled via a corresponding bit in the ALS1_EN (Address 0x2E) and ALS2_EN (Address 0x2F) registers.

The L2_TRP and L2_HYS values of Level 2 comparator can be set between 0 µA and 1100 µA (typical) in steps of 4.4 µA (typical).

The L3_TRP and L3_HYS values of Level 3 comparator can be set between 0 µA and 550 µA (typical) in steps of 2.2 µA (typical).

The L4_TRP and L4_HYS values of Level 4 comparator can be set between 0 µA and 275 µA (typical) in steps of 1.1 µA (typical).

The L5_TRP and L5_HYS values of Level 5 comparator can be set between 0 µA and 137 µA (typical) in steps of 0.55 µA (typical).

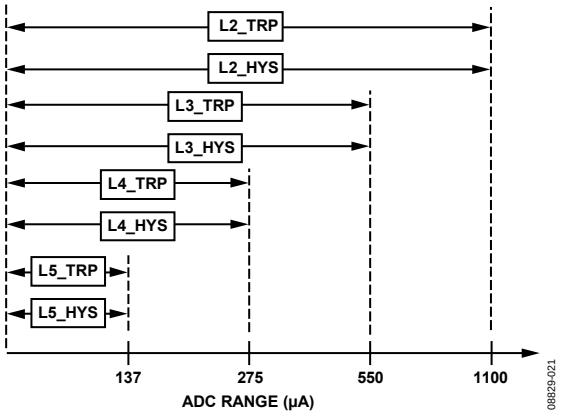


Figure 44. Comparator Ranges

It is important to note that the full-scale value of the L2_TRP and L2_HYS registers is 250 d. Therefore, if the value of L2_TRP + L2_HYS exceeds 250 d, the comparator output cannot deassert. For example, if L2_TRP is set at 204 d (80% of the full-scale value, or approximately 0.80 × 1122 µA = 898 µA), then L2_HYS must be set at less than 46 d (250 − 204 = 46). If it is not, then L2_HYS + L2_TRP exceeds 250 d and the Level 2 comparator is not allowed to go low.

When both phototransistors are enabled and programmed in automatic mode, the user application needs to determine which of the comparator outputs to use, selecting via Bit SEL_AB in Register 0x04 for automatic light sensing transitions. For example, the user's software might select the comparator of the phototransistor exposed to higher light intensity to control the transition between the programmed backlight intensity levels.

The level comparators can be enabled independent of each other or can operate simultaneously. A single conversion from each ADC takes 80 ms (typical). When set for automatic backlight adjustment (see the Automatic Backlight Adjustment section), the ADC and comparators run continuously. If the backlight is disabled, it is possible to use the light sensor comparators in a single-shot mode. A single-shot read of the photocomparators is performed by setting the FORCE_RD bit (Register 0x2D). After the single shot measurement is completed, the internal state machine clears the FORCE_RD bit.

Interrupt Flag CMP_INT (Register 0x02) is set if any of the level output status bits change state for the main photosensor input. This means that interrupts can be generated if ambient light conditions transition between any of the programmed trip points. CMP_INT can cause the nINT pin to be asserted if the CMP_IEN bit (Register 0x03) is set. The CMP_INT flag can only be cleared by writing a 1 to it or resetting the part.

The operation of CMP2_INT (Register 0x02) and CMP2_IEN (Register 0x03) is similar except that the second phototransistor (that is, CMP_IN2) is used.

D7 AMBIENT LIGHT-SENSING CONTROL

LED D7 can be programmed to operate independent from the backlight reset when under ALS control. This is useful when D7 is used to control peripheral lighting (for example, the keypad) that needs to respond differently than the backlight lighting. This feature uses the same ALS controls and thresholds as the backlight.

To engage D7 ALS control, first program the five ALS levels of D7 found in Register 0x25 to Register 0x29. Then set Bit D7ALS_EN in Register 0x01 and Bit D7SEL in Register 0x05.

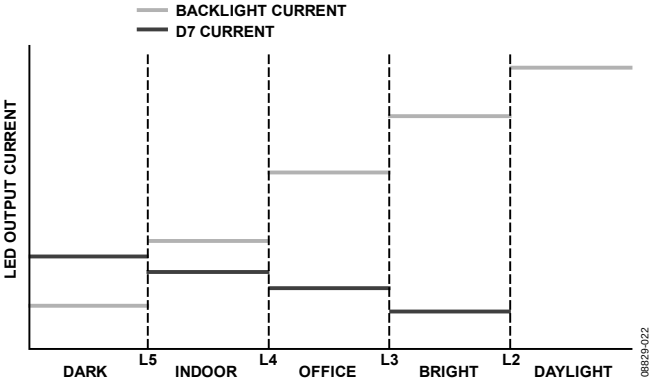


Figure 45. A Possible Example of the Separate ALS Control of D7

AUTOMATIC BACKLIGHT ADJUSTMENT

The ambient light sensor comparators can be used to automatically transition the backlight between one of its three operating levels. To enable this mode, set the CMP_AUTOEN bit in Register 0x01.

When enabled, the internal state machine takes control of the BLV bits and changes them based on the level output status bits. Table 6 shows the relationship between backlight operation and the ambient light sensor comparator outputs. The higher numbered level output status bit have greater priority over the lower numbered levels.

Filter times between 80 ms and 10 sec can be programmed for the comparators (Register 0x2D) before they change state.

Table 6. Comparator Output Truth Table[1]

L5_OUT	L4_OUT	L3_OUT	L2_OUT	ALS Level	BLV Code
1	X	X	X	Dark	100
0	1	X	X	Indoor	011
0	0	1	X	Office	010
0	0	0	1	Bright	001
0	0	0	0	Outdoor	000

[1]X is the don't care bit.

INDEPENDENT SINK CONTROL (ISC)

Each of the 7 LEDs can be configured (in Register 0x05) to operate as either part of the backlight or to operate as an independent sink current (ISC). Each ISC can be enabled independently and has its own current level. All ISCs share the same fade-in times, fade-out times, and fade law.

The ISCs have additional timers to facilitate blinking functions. A shared on timer (SCON), used in conjunction with the off timers of each ISC (SC1OFF, SC2OFF, SC3OFF, SC4OFF, SC5OFF, SC6OFF, and SC7OFF), allow the LED current sinks to be configured in various blinking modes. The on timer can be set to four settings: 0.2 sec, 0.6 sec, 0.8 sec, and 1.2 sec. The off timers also have four settings: disabled, 0.6 sec, 0.8 sec, and 1.2 sec. Blink mode is activated by setting the off timers to any setting other than disabled.

Program all fade, on, and off timers before enabling any of the LED current sinks. If ISCx is on during a blink cycle and SCx_EN is cleared, it turns off (or fades to off if fade-out is enabled). If ISCx is off during a blink cycle and SCx_EN is cleared, it stays off.

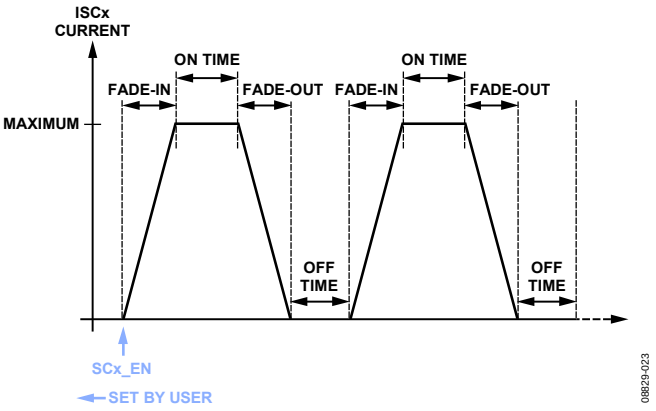


Figure 46. LEDx Blink Mode with Fading

SHORT-CIRCUIT PROTECTION (SCP) MODE

The ADP8870 can protect against short circuits on the output (V_{OUT}). Short-circuit protection (SCP) is activated at the point when V_{OUT} < 55% of V_{IN}. Note that this SCP sensing is disabled during startup and restart attempts (fault recovery). SCP sensing is reenabled 4 ms (typical) after activation. During a short-circuit fault, the device enters a low current consumption state and an interrupt flag is set. The device can be restart at any time after receiving a short-circuit fault by simply rewriting nSTBY = 1. It then repeats another complete soft start sequence. Note that the value of the output capacitance (C_{OUT}) should be small enough to allow V_{OUT} to reach approximately 55% (typical) of V_{IN} within the 4 ms (typical) time. If C_{OUT} is too large, the device inadvertently enters short-circuit protection.

OVERVOLTAGE PROTECTION (OVP)

Overvoltage protection is implemented on the output. There are two types of overvoltage events: normal (no fault) and abnormal.

Normal (No Fault) Overvoltage

The output voltage approaches $V_{OUT(REG)}$ (4.7 V typical) during normal operation. This is not caused by a fault or load change, but simply a consequence of the input voltage times the gain reaching the clamped output voltage $V_{OUT(REG)}$. To prevent this, the ADP8870 detects when the output voltage rises to $V_{OUT(REG)}$. It then increases the effective R_{OUT} of the gain stage to reduce the voltage that is delivered. This effectively regulates V_{OUT} to $V_{OUT(REG)}$; however, there is a limit to the effect that this system can have on regulating V_{OUT}. It is designed only for normal operation and is not intended to protect against faults or sudden load changes. During this mode, no interrupt is set and the operation is transparent to the LEDs and overall application. The automatic gain selection equations take into account the additional drop within R_{OUT} to maintain optimum efficiency.

Abnormal (Fault/Sudden Load Change) Overvoltage

Due to the open loop behavior of the charge pump as well as how the gain transitions are computed, a sudden load change or fault can abnormally force V_{OUT} beyond 6 V. If the event happens slowly enough, the system first tries to regulate the output to 4.7 V (typical) as in a normal overvoltage scenario. However, if this is not sufficient, or if the event happens too quickly, then the ADP8870 enters overvoltage protection mode when V_{OUT} exceeds the OVP threshold (typically 5.7 V). In this mode, the charge pump is disabled to prevent V_{OUT} from rising too high. The current sources and all other device functionality remain intact. When the output voltage falls below the OVP threshold, the charge pump resumes operation. If the fault or load step recurs, the process may repeat. An interrupt flag is set at each OVP instance.

THERMAL SHUTDOWN (TSD)/ OVERTEMPERATURE PROTECTION

If the die temperature of the ADP8870 rises above a safety limit (150°C typical), the controllers enter TSD protection mode. In this mode, most of the internal functions are shut down, the part enters standby, and the TSD_INT interrupt (Register 0x02) is set. When the die temperature decreases below ~130°C, the part is allowed to be restarted. To restart the part, simply remove it from standby. No interrupt is generated when the die temperature falls below 130°C. However, if the software clears the pending TSD_INT interrupt and the temperature remains above 130°C, another interrupt is generated.

The complete state machine for these faults (SCP, OVP, and TSD) is shown in Figure 47.

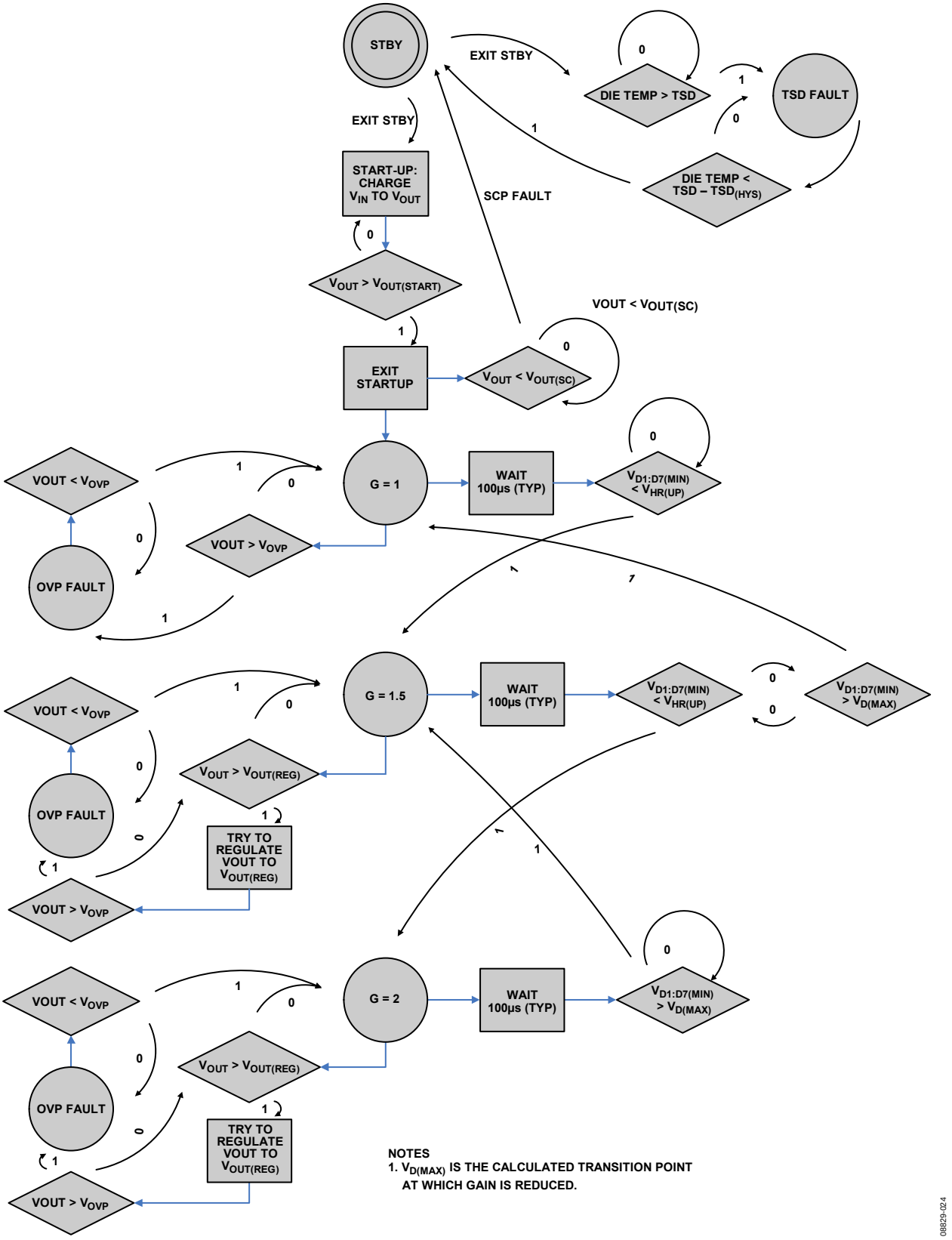


Figure 47. Fault State Machine

INTERRUPTS

There are six interrupt sources available on the ADP8870 (in Register 0x02).

- Backlight off: at the end of each automated backlight fade-out, this interrupt (BLOFF_INT) is set.
- Main light sensor comparator: CMP_INT sets every time the main light sensor comparator detects a threshold (Level 2, Level 3, Level 4, or Level 5) transition (rising or falling conditions).
- Sensor Comparator 2: CMP2_INT interrupt works the same way as CMP_INT, except that the sensing input is coming from the second light sensor. The programmable threshold is the same as the main light sensor comparator.
- Overvoltage protection: OVP_INT is generated when the output voltage exceeds 5.7 V (typical).
- Thermal shutdown circuit: an interrupt (TSD_INT) is generated when entering overtemperature protection.
- Short-circuit detection: SHORT_INT is generated when the device enters short-circuit protection mode.

The interrupt (if any) that appears on the nINT pin is determined by the bits mapped in Register INT_EN. To clear an interrupt, write a 1 to the interrupt in the INT_STAT register or reset the part.

BACKLIGHT OFF INTERRUPT

The backlight off interrupt (BLOFF_INT) is set when the backlight completes an automated fade sequence. This could be a simple fade-out command or a complete dimming profile. This feature is useful to synchronize the backlight turn off with the LCD display driver.

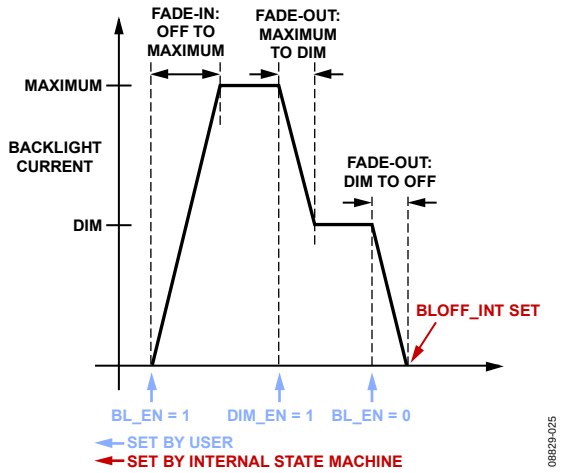


Figure 48. End of Fade-Out (EOF) Interrupt as Used for a Backlight Fade-Out (Set by User)

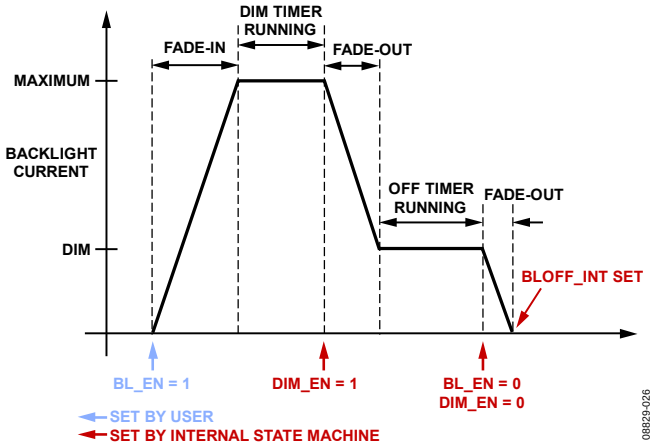


Figure 49. End of Fade-Out (EOF) Interrupt as Used for an Automated Dim Profile (Set by Internal State Machine)

APPLICATIONS INFORMATION

The ADP8870 allows the charge pump to operate efficiently with a minimum of external components, requiring only an input capacitor (C_{IN}), an output capacitor (C_{OUT}), and two charge-pump fly capacitors (C1 and C2). C_{IN} should be 1 µF or greater, and C_{OUT}, C1, and C2 should each be 1 µF. Although in some cases other values can be used, keep in mind the following:

- The value of C_{IN} must be high enough to produce a stable input voltage signal at the minimum input voltage and maximum output load.
- Values larger than 1 µF are permissible for C_{OUT}, but care must be exercised to ensure that V_{OUT} charges above 55% (typ) of V_{IN} within 4 ms (typ). See the Short-Circuit Protection (SCP) Mode section for more details.
- Values larger than 1 µF for C1 and C2 are not recommended, and smaller values may reduce the ability of the charge pump to deliver maximum current.

Furthermore, for optimal efficiency, the charge-pump fly capacitors should have low equivalent series resistance (ESR). Low ESR X5R or X7R capacitors are recommended for all four components. The use of fly capacitors sized 0402 and smaller is allowed, but the GDWN_DIS bit in Register 0x01 must be set. Minimum voltage ratings should adhere to the guidelines in Table 7.

Table 7. Capacitor Stress in Each Charge Pump Gain State

Capacitor	Gain = 1×	Gain = 1.5×	Gain = 2×
C_{IN}	V_{IN}	V_{IN}	V_{IN}
C_{OUT}	V_{IN}	V_{IN} × 1.5 (max of 5.5 V)	V_{IN} × 2.0 (max of 5.5 V)
C1	None	$V_{IN}/2$	V_{IN}
C2	None	$V_{IN}/2$	V_{IN}

If one or both ambient light sensor comparator inputs (CMP_IN and/or D6) are used, a small capacitor (0.1 µF is recommended) must be connected from the comparator input pins to ground. When a light sensor conversion reading takes place, the voltage on these pins is V_{ALS} (0.95 V typical, see Table 1). Therefore, the minimum supply voltage for the ALS sensor should be greater than $V_{ALS(MAX)}$ plus the biasing voltage required for the photosensor.

Any color of LED can be used if the V_F (forward voltage) is less than 4.1 V. However, using lower V_F LEDs reduces the input power consumption by allowing the charge pump to operate at lower gain states.

The equivalent model for a charge pump is shown in Figure 50.

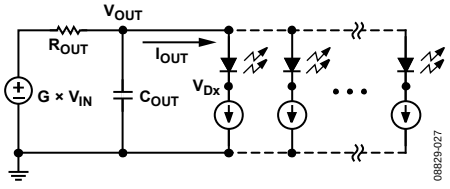


Figure 50. Charge-Pump Equivalent Circuit Model

The input voltage is multiplied by the gain (G) and delivered to the output through an effective resistance (R_{OUT}). The output current flows through R_{OUT} and produces an IR drop that yields

$$V_{OUT} = G \times V_{IN} - I_{OUT} \times R_{OUT}(G) \quad (6)$$

The R_{OUT} term is a combination of the $R_{DS(ON)}$ resistance for the switches used in the charge pump and a small resistance that accounts for the effective dynamic charge-pump resistance. The R_{OUT} level changes based on the gain, which is dependent on the configuration of the switches. Typical R_{OUT} values are given in Table 1 and Figure 15 to Figure 17. V_{OUT} is also equal to the largest V_F of the LEDs used plus the voltage drop across the regulating current source. This gives

$$V_{OUT} = V_{F(MAX)} + V_{Dx} \quad (7)$$

Combining Equation 6 and Equation 7 gives

$$V_{IN} = (V_{F(MAX)} + V_{Dx} + I_{OUT} \times R_{OUT}(G))/G \quad (8)$$

This equation is useful for calculating approximate bounds for the charge pump design.

Determining the Transition Point of the Charge Pump

Consider the following design example where:

$V_{F(MAX)}$ = 3.7 V
I_{OUT} = 140 mA (7 LEDs at 20 mA each)
$R_{OUT}(G = 1.5\times)$ = 3 Ω (obtained from Figure 12)

At the point of a gain transition, $V_{Dx} = V_{HR(UP)}$. Table 1 gives the typical value of $V_{HR(UP)}$ as 0.225 V. Therefore, the input voltage level when the gain transitions from 1.5× to 2× is

$$V_{IN} = (3.7\text{ V} + 0.225\text{ V} + 140\text{ mA} \times 3\ \Omega)/1.5 = 2.90\text{ V}$$

LAYOUT GUIDELINES

Use the following layout guidelines:

- For optimal noise immunity, place the C_{IN} and C_{OUT} capacitors as close to their respective pins as possible. These capacitors should share a short ground trace. If the LEDs are a significant distance from the VOUT pin, another capacitor on VOUT, placed closer to the LEDs, is advisable.
- For optimal efficiency, place the charge-pump fly capacitors as close to the part as possible.
- The ground pin should be connected at the ground for the input and output capacitors. If the LFCSP package is used, the exposed pad must be soldered at the board to the GND pin.
- Unused Diode Pins[D1:D7] can be connected to ground or VOUT, or can remain floating. However, the unused diode current sinks must be disabled by setting them as independent sinks in Register 0x05 and then disabling them in Register 0x1B. If they are not disabled, the charge-pump efficiency may suffer.
- If the CMP_IN phototransistor input is not used, it can be connected to ground or can remain floating.

- If the interrupt pin (nINT) is not used, connect it to ground or leave it floating. Never connect the nINT pin to a voltage supply, except through a ≥1 kΩ series resistor.
- The ADP8870 has an integrated noise filter on the nRST pin. Under normal conditions, it is not necessary to filter the reset line. However, if exposed to an unusually noisy signal, then it is beneficial to add a small RC filter or bypass capacitor on this pin. If the nRST pin is not used, it must be pulled well above the $V_{IH(MAX)}$ level (see Table 1). Do not allow the nRST pin to float.

EXAMPLE CIRCUIT

Figure 51 shows an example circuit for a generic application.

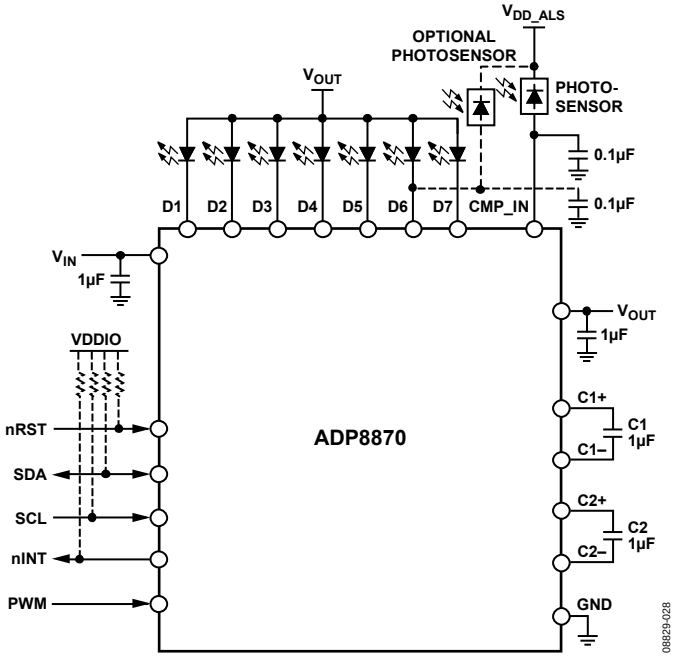


Figure 51. Generic Application Schematic

I²C PROGRAMMING AND DIGITAL CONTROL

The ADP8870 provides full software programmability to facilitate its adoption in various product architectures. The I²C address is 0101011x (x = 0 during write, x = 1 during read). Therefore, the write address is 0x56, and the read address is 0x57.

In general, all registers are set to default values on reset or in case of a UVLO event and are read/write unless otherwise specified. Unused bits are read as 0.

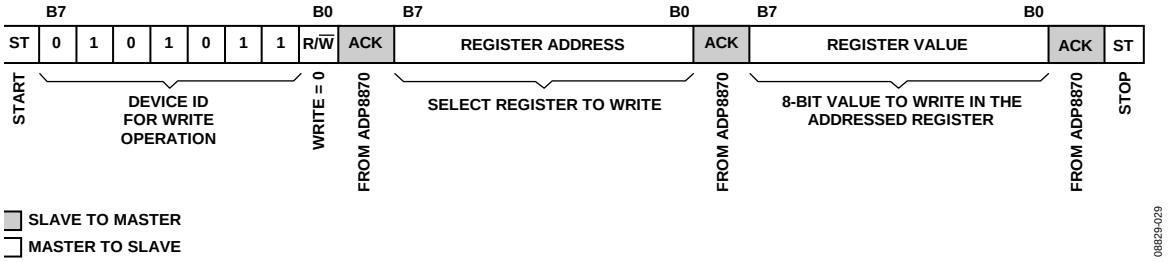


Figure 52. I²C Write Sequence

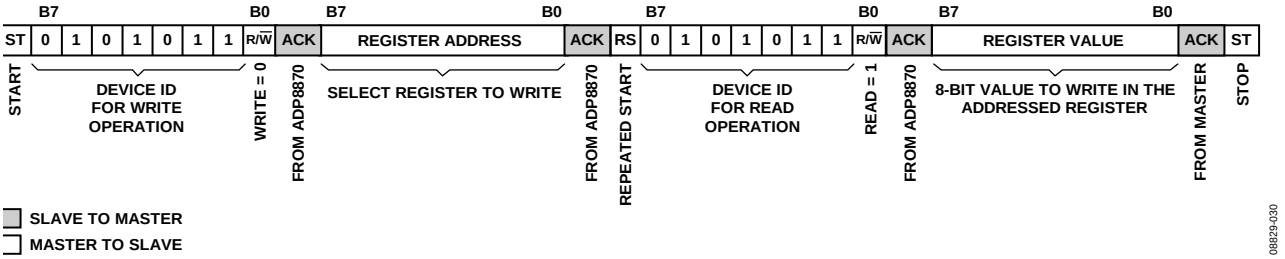


Figure 53. I²C Read Sequence

Table 8. Register Set Definitions

Address	Register Name	Description
0x00	MFDVID	Manufacturer and device ID
0x01	MDCR	Device mode and status
0x02	INT_STAT	Interrupts status
0x03	INT_EN	Interrupts enable
0x04	CFGR	Configuration register
0x05	BLSEL	Sink enable backlight or independent
0x06	PWMLED	PWM enable selection
0x07	BLOFF	Backlight off timeout
0x08	BLDIM	Backlight dim timeout
0x09	BLFR	Backlight fade-in and fade-out rates
0x0A	BLMX1	Backlight, Brightness Level 1—daylight, maximum current
0x0B	BLDM1	Backlight, Brightness Level 1—daylight, dim current
0x0C	BLMX2	Backlight, Brightness Level 2—bright, maximum current
0x0D	BLDM2	Backlight, Brightness Level 2—bright, dim current
0x0E	BLMX3	Backlight, Brightness Level 3—office, maximum current
0x0F	BLDM3	Backlight, Brightness Level 3—office, dim current
0x10	BLMX4	Backlight, Brightness Level 4—indoor, maximum current
0x11	BLDM4	Backlight, Brightness Level 4— indoor, dim current
0x12	BLMX5	Backlight, Brightness Level 5—dark, maximum current
0x13	BLDM5	Backlight, Brightness Level 5—dark, dim current
0x14 to 0x19	Reserved	Reserved
0x1A	ISCLAW	Independent sink current fade law
0x1B	ISCC	Independent sink current control
0x1C	ISCT1	Independent sink current timer for LED[7:5]
0x1D	ISCT2	Independent sink current timer for LED[4:1]

Address	Register Name	Description
0x1E	ISCF	Independent sink current fade register
0x1F	ISC1	Independent Sink Current LED1
0x20	ISC2	Independent Sink Current LED2
0x21	ISC3	Independent Sink Current LED3
0x22	ISC4	Independent Sink Current LED4
0x23	ISC5	Independent Sink Current LED5
0x24	ISC6	Independent Sink Current LED6
0x25	ISC7	Independent Sink Current LED7, Brightness Level 1—daylight
0x26	ISC7_L2	Independent Sink Current LED7, Brightness Level 2—bright
0x27	ISC7_L3	Independent Sink Current LED7, Brightness Level 3—office
0x28	ISC7_L4	Independent Sink Current LED7, Brightness Level 4—indoor
0x29	ISC7_L5	Independent Sink Current LED7, Brightness Level 5—dark
0x2A to 0x2C	Reserved	Reserved
0x2D	CMP_CTL	ALS comparator control register
0x2E	ALS1_EN	Main ALS comparator level enable
0x2F	ALS2_EN	Second ALS comparator level enable
0x30	ALS1_STAT	Main ALS comparator status register
0x31	ALS2_STAT	Second ALS comparator status register
0x32	L2_TRP	Level 2 comparator reference
0x33	L2_HYS	Level 2 hysteresis
0x34	L3_TRP	Level 3 comparator reference
0x35	L3_HYS	Level 3 hysteresis
0x36	L4_TRP	Level 4 comparator reference
0x37	L4_HYS	Level 4 hysteresis
0x38	L5_TRP	Level 5 comparator reference
0x39	L5_HYS	Level 5 hysteresis
0x3A to 0x3F	Reserved	Reserved
0x40	PH1LEVL	First phototransistor ambient light level—low byte register
0x41	PH1LEVH	First phototransistor ambient light level—high byte register
0x42	PH2LEVL	Second phototransistor ambient light level—low byte register
0x43	PH2LEVH	Second phototransistor ambient light level—high byte register

REGISTER SUMMARY

The reset value for all bits is 0, except for bits at Address 0x00 (see Table 10 for the unique reset value of Address 0x00).

Table 9. Register Map

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	MFDVID	MANUFACTURE ID				Device ID			
0x01	MDCR	D7ALS_EN	INT_CFG	nSTBY	DIM_EN	GDWN_DIS	SIS_EN	CMP_AUTOEN	BL_EN
0x02	INT_STAT	Reserved		BLOFF_INT	SHORT_INT	TSD_INT	OVP_INT	CMP2_INT	CMP_INT
0x03	INT_EN	Reserved		BLOFF_IEN	SHORT_IEN	TSD_IEN	OVP_IEN	CMP2_IEN	CMP_IEN
0x04	CFGR	SEL_AB	CMP2_SEL	BLV			BL_LAW		FOVR
0x05	BLSEL	Reserved	D7SEL	D6SEL	D5SEL	D4SEL	D3SEL	D2SEL	D1SEL
0x06	PWMLED	Reserved	D7ENPWM	D6ENPWM	D5ENPWM	D4ENPWM	D3ENPWM	D2ENPWM	D1ENPWM
0x07	BLOFF	Reserved	OFFT						
0x08	BLDIM	Reserved	DIMT						
0x09	BLFR	BL_FO				BL_FI			
0x0A	BLMX1	Reserved	BL1_MC						
0x0B	BLDM1	Reserved	BL1_DC						
0x0C	BLMX2	Reserved	BL2_MC						
0x0D	BLDM2	Reserved	BL2_DC						
0x0E	BLMX3	Reserved	BL3_MC						
0x0F	BLDM3	Reserved	BL3_DC						
0x10	BLMX4	Reserved	BL4_MC						
0x11	BLDM4	Reserved	BL4_DC						
0x12	BLMX5	Reserved	BL5_MC						
0x13	BLDM5	Reserved	BL5_DC						
0x1A	ISCLAW	Reserved						SC_LAW	
0x1B	ISCC	Reserved	SC7_EN	SC6_EN	SC5_EN	SC4_EN	SC3_EN	SC2_EN	SC1_EN
0x1C	ISCT1	SCON		SC7OFF		SC6OFF		SC5OFF	
0x1D	ISCT2	SC4OFF		SC3OFF		SC2OFF		SC1OFF	
0x1E	ISCF	SCFO				SCFI			
0x1F	ISC1	Reserved	SCD1						
0x20	ISC2	Reserved	SCD2						
0x21	ISC3	Reserved	SCD3						
0x22	ISC4	Reserved	SCD4						
0x23	ISC5	Reserved	SCD5						
0x24	ISC6	Reserved	SCD6						
0x25	ISC7	SCR	SCD7						
0x26	ISC7_L2	Reserved	SCD7_L2						
0x27	ISC7_L3	Reserved	SCD7_L3						
0x28	ISC7_L4	Reserved	SCD7_L4						
0x29	ISC7_L5	Reserved	SCD7_L5						
0x2D	CMP_CTL	FILT2			FORCE_RD2	FILT			FORCE_RD
0x2E	ALS1_EN	Reserved				L5_EN	L4_EN	L3_EN	L2_EN
0x2F	ALS2_EN	Reserved				L5_EN2	L4_EN2	L3_EN2	L2_EN2
0x30	ALS1_STAT	Reserved				CMP1_L5_OUT	CMP1_L4_OUT	CMP1_L3_OUT	CMP1_L2_OUT
0x31	ALS2_STAT	Reserved				CMP2_L5_OUT	CMP2_L4_OUT	CMP2_L3_OUT	CMP2_L2_OUT
0x32	L2_TRP	L2_TRP							
0x33	L2_HYS	L2_HYS							
0x34	L3_TRP	L3_TRP							
0x35	L3_HYS	L3_HYS							
0x36	L4_TRP	L4_TRP							
0x37	L4_HYS	L4_HYS							
0x38	L5_TRP	L5_TRP							
0x39	L5_HYS	L5_HYS							
0x40	PH1LEVL	PH1LEV_LOW							
0x41	PH1LEVH	Reserved				PH1LEV_HIGH			
0x42	PH2LEVL	PH2LEV_LOW							
0x43	PH2LEVH	Reserved				PH2LEV_HIGH			

REGISTER DETAILS

MANUFACTURER AND DEVICE ID (MFDVID)—REGISTER 0x00

Multiple device revisions are tracked by the device ID field. This is a read-only register.

Table 10. MFDVID Manufacturer and Device ID Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Manufacture ID				Device ID			
0	0	1	1	0	0	0	1

MODE CONTROL REGISTER (MDCR)—REGISTER 0x01

Table 11. MDCR Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7ALS_EN	INT_CFG	nSTBY	DIM_EN	GDWN_DIS	SIS_EN	CMP_AUTOEN	BL_EN

Table 12. MDCR Bit Descriptions

Bit Name	Bit No.	Description
D7ALS_EN	7	1 = ambient light sensing (ALS) control of independent sink (ISC) D7 is enabled. When the ADP8870 is configured as an ISC in Register 0x05, then Register 0x24 to Register 0x28 are used to set the outdoor, bright, office, indoor, and dark current levels for D7. CMPAUTO_EN (in Register 0x01) and at least one of the level enable bits (in Register 0x2D and/or Register 0x2E) must be set high for this feature to operate. 0 = ambient light sensing (ALS) control of ISC D7 is disabled (D7 responds as a standard backlight LED or ISC LED).
INT_CFG	6	Interrupt configuration. 1 = processor interrupt deasserts for 50 µs and reasserts with pending events. 0 = processor interrupt remains asserted if the host tries to clear the interrupt while there is a pending event.
nSTBY	5	1 = device is in normal mode. 0 = device is in standby, only I^2C is enabled.
DIM_EN	4	DIM_EN is set by the hardware after a DIM timeout. The user may also force the backlight into DIM mode by asserting this bit. DIM mode can only be entered if BL_EN is also enabled. 1 = backlight is operating at the DIM current level (BL_EN must also be asserted). 0 = backlight is not in DIM mode.
GDWN_DIS	3	1 = the charge pump does not switch down in gain until all LEDs are off. The charge pump switches up in gain as needed. This feature is useful if the ADP8870 charge pump is used to drive an external load. 0 = the charge pump automatically switches up and down in gain. This provides optimal efficiency, but is not suitable for driving external loads (other than those connected to the diode drivers of the ADP8870).
SIS_EN	2	Synchronous independent sinks enable. 1 = enables all LED current sinks designated as independent sinks. This bit has no effect if any of the SCx_EN bits in Register 0x1B are set. All of the sink current bits must be set to 0. 0 = disables all sinks designated as independent sinks. This bit has no effect if any of the SCx_EN bits are set in Register 0x1B. All of the sink current bits must be cleared.
CMP_AUTOEN	1	1 = backlight automatically responds to the comparator outputs. At least one of the level enable bits (Register 0x32, Register 0x34, Register 0x36, and/or Register 0x38) must be set for this to function. BLV values in Register 0x04 are overridden. 0 = backlight does not autorespond to comparator level changes. The user can manually select backlight operating levels using the BLV bits in Register 0x04.
BL_EN	0	1 = backlight is enabled, but only if the device is not in standby mode. 0 = backlight is disabled.

INTERRUPT STATUS REGISTER (INT_STAT)—REGISTER 0x02

Table 13. INT_STAT Bit Map

Bit 7	Bit 6	Bit 5	4	3	2	1	0
Reserved		BLOFF_INT	SHORT_INT	TSD_INT	OVP_INT	CMP2_INT	CMP_INT

Table 14. INT_STAT Bit Descriptions

Bit Name	Bit No.	Description[1]
Reserved	[7:6]	Reserved.
BLOFF_INT	5	Backlight off. 1 = indicates that the controller has completed a backlight fade profile. 0 = the controller has not automatically completed a backlight fade profile.
SHORT_INT	4	Short-circuit error. 1 = a short-circuit or overload condition on VOUT or current sinks was detected. 0 = no short-circuit or overload condition detected.
TSD_INT	3	Thermal shutdown. 1 = device temperature is too high and has been shut down. 0 = no overtemperature condition detected.
OVP_INT	2	Overvoltage interrupt. 1 = charge-pump output voltage has exceeded V_{OVP}. 0 = charge-pump output voltage has not exceeded V_{OVP}.
CMP2_INT	1	1 = indicates that the second sensor comparator has been triggered. 0 = the second comparator has not been triggered.
CMP_INT	0	1 = indicates that the sensor comparator has been triggered. 0 = the comparator has not been triggered.

[1] Interrupt bits are cleared by writing a 1 to the flag; writing a 0 or reading the flag has no effect.

INTERRUPT ENABLE (INT_EN)—REGISTER 0x03

Table 15. INT_EN Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		BLOFF_IEN	SHORT_IEN	TSD_IEN	OVP_IEN	CMP2_IEN	CMP_IEN

Table 16. INT_EN Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:6]	Reserved.
BLOFF_IEN	5	Automated backlight off indicator. 1 = the automated backlight off indicator is enabled. 0 = the automated backlight off indicator is disabled. When this bit is set, an interrupt is set anytime a backlight fade-out completes. This occurs after an automated fade-out or after the completion of a backlight dimming profile. This is useful to synchronize the complete turn off for the backlights with other devices in the application.
SHORT_IEN	4	Short-circuit interrupt enabled. When the SHORT_INT status bit is set after an error condition, an interrupt is raised to the host if the SHORT_IEN flag is enabled. 1 = the short-circuit interrupt is enabled. 0 = the short-circuit interrupt is disabled (SHORT_INT flag is still asserted).
TSD_IEN	3	Thermal shutdown interrupt enabled. When the TSD_INT status bit is set after an error condition, an interrupt is raised to the host if the TSD_IEN flag is enabled. 1 = the thermal shutdown interrupt is enabled. 0 = the thermal shutdown interrupt is disabled (TSD_INT flag is still asserted).
OVP_IEN	2	Overvoltage interrupt enabled. When the OVP_INT status bit is set after an error condition, an interrupt is raised to the host if the OVP_IEN flag is enabled. 1 = the overvoltage interrupt is enabled. 0 = the overvoltage interrupt is disabled (OVP_INT flag is still asserted).

Bit Name	Bit No.	Description
CMP2_IEN	1	When the CMP2_INT status bit is set after an enabled comparator trips, an interrupt is raised if the CMP2_IEN flag is enabled. 1 = the second phototransistor comparator interrupt is enabled. 0 = the second phototransistor comparator interrupt is disabled (CMP2_INT flag is still asserted).
CMP_IEN	0	When the CMP_INT status bit is set after an enabled comparator trips, an interrupt is raised if the CMP_IEN flag is enabled. 1 = the comparator interrupt is enabled. 0 = the comparator interrupt is disabled (CMP_INT flag is still asserted).

BACKLIGHT REGISTER DESCRIPTIONS

Configuration Register (CFGR)—Register 0x04

Table 17. CFGR Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SEL_AB	CMP2_SEL	BLV			BL_LAW		FOVR

Table 18. CFGR Bit Descriptions

Bit Name	Bit No.	Description
SEL_AB	7	1 = selects second phototransistor (CMP_IN2) to control the backlight. 0 = selects main phototransistor (CMP_IN) to control the backlight.
CMP2_SEL	6	1 = second phototransistor enabled, current sink on D6 disabled. 0 = current sink on D6 enabled, second phototransistor disabled.
BLV	[5:3]	Brightness level. This field indicates the brightness level at which the device is operating. The software may force the backlight to operate at one of the three brightness levels. Setting CMP_AUTOEN high (Register 0x01), automatically sets these values and overwrites any previously written values. 000 = Level 1 (daylight). 001 = Level 2 (bright). 010 = Level 3 (office). 011 = Level 4 (indoor). 100 = Level 5 (dark). 101 to 111 = disabled (backlight set to 0 mA).
BL_LAW	[2:1]	Backlight transfer law. 00 = square law DAC, linear time steps. 01 = square law DAC, linear time steps. 10 = square law DAC, nonlinear time steps (Cubic 10). 11 = square law DAC, nonlinear time steps (Cubic 11).
FOVR	0	Backlight fade override. 1 = backlight fade override enabled. 0 = backlight fade override disabled.

Backlight Selection (BLSEL)—Register 0x05

Table 19. BLSEL Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	D7SEL	D6SEL	D5SEL	D4SEL	D3SEL	D2SEL	D1SEL

Table 20. BLSEL Bit Descriptions

Bit Name	Bit No.	Description
Reserved	7	Reserved.
D7SEL	6	Diode 7 backlight selection. 1 = selects LED 7 as an independent sink. 0 = connects LED 7 sink to the backlight enable, BL_EN.
D6SEL	5	Diode 6 backlight selection. 1 = selects LED 6 as an independent sink. 0 = connects LED 6 sink to the backlight enable, BL_EN.
D5SEL	4	Diode 5 backlight selection. 1 = selects LED 5 as an independent sink. 0 = connects LED 5 sink to the backlight enable, BL_EN.
D4SEL	3	Diode 4 backlight selection. 1 = selects LED 4 as independent sink. 0 = connects LED 4 sink to the backlight enable, BL_EN.
D3SEL	2	Diode 3 backlight selection. 1 = selects LED 3 as independent sink. 0 = connects LED 3 sink to the backlight enable, BL_EN.
D2SEL	1	Diode 2 backlight selection. 1 = selects LED 2 as independent sink. 0 = connects LED 2 sink to the backlight enable, BL_EN.
D1SEL	0	Diode 1 backlight selection. 1 = selects LED 1 as independent sink. 0 = connects LED 1 sink to the backlight enable, BL_EN.

PWM Enable Selection Register (PWMLED)—Register 0x06

Table 21. PWMLED Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	D7ENPWM	D6ENPWM	D5ENPWM	D4ENPWM	D3ENPWM	D2ENPWM	D1ENPWM

Table 22. PWMLED Bit Descriptions

Bit Name	Bit No.	Description
Reserved	7	Reserved.
D7ENPWM	6	Diode 7 backlight sink PWM enable. 1 = enables the externally applied PWM signal to scale the output current of D7. 0 = D7 does not respond to the external PWM signal.
D6ENPWM	5	Diode 6 backlight sink PWM enable. 1 = enables the externally applied PWM signal to scale the output current of D6. 0 = D6 does not respond to the external PWM signal.
D5ENPWM	4	Diode 5 backlight sink PWM enable. 1 = enables the externally applied PWM signal to scale the output current of D5. 0 = D5 does not respond to the external PWM signal.
D4ENPWM	3	Diode 4 backlight sink PWM enable. 1 = enables the externally applied PWM signal to scale the output current of D4. 0 = D4 does not respond to the external PWM signal.
D3ENPWM	2	Diode 3 backlight sink PWM enable. 1 = enables the externally applied PWM signal to scale the output current of D3. 0 = D3 does not respond to the external PWM signal.

Bit Name	Bit No.	Description
D2ENPWM	1	Diode 2 backlight sink PWM enable. 1 = enables the externally applied PWM signal to scale the output current of D2. 0 = D2 does not respond to the external PWM signal.
D1ENPWM	0	Diode 1 backlight sink PWM enable. 1 = enables the externally applied PWM signal to scale the output current of D1. 0 = D1 does not respond to the external PWM signal.

Backlight Off Timeout (BLOFF)—Register 0x07

Table 23. BLOFF Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	OFFT						

Table 24. BLOFF Bit Descriptions

Bit Name	Bit No.	Description
Reserved	7	Reserved.
OFFT	[6:0]	Backlight off timeout. After the off timeout period, the backlight turns off. If the dim timeout is enabled, the off timeout starts after the dim timeout. 0000 = timeout disabled. 0000001 = 1 sec. 0000010 = 2 sec. … 1111111 = 127 sec.

Backlight Dim Timeout (BLDIM)—Register 0x08

Table 25. BLDIM Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	DIMT						

Table 26. BLDIM Bit Descriptions

Bit Name	Bit No.	Description
Reserved	7	Reserved.
DIMT	[6:0]	Backlight dim timeout. After the dim timeout period, the backlight is set to the dim current value. The dim timeout starts after the backlight reaches the maximum current. 0000 = timeout disabled. 0000001 = 1 sec. 0000010 = 2 sec. 0000011 = 3 sec. … 1111111 = 127 sec.

Backlight Fade (BLFR)—Register 0x09

Table 27. BLFR Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BL_FO				BL_FI			

Table 28. BLFR Bit Descriptions

Bit Name	Bit No.	Description
BL_FO	[7:4]	Backlight fade-out rate. If the fade-out is disabled (BL_FO = 0000), the backlight changes instantly (within 100 ms). If the fade-out rate is set, the backlight fades from its current value to the dim or the off value. The times listed for BL_FO are for a full-scale fade-out (30 mA to 0 mA). Fades between closer current values reduce the fade time. See the Automated Fade-In and Fade-Out section for more information. 0000 = 0.1 sec (fade-out disabled).[1] 0001 = 0.3 sec. 0010 = 0.6 sec. 0011 = 0.9 sec. 0100 = 1.2 sec. 0101 = 1.5 sec. 0110 = 1.8 sec. 0111 = 2.1 sec. 1000 = 2.4 sec. 1001 = 2.7 sec. 1010 = 3.0 sec. 1011 = 3.5 sec. 1100 = 4.0 sec. 1101 = 4.5 sec. 1110 = 5.0 sec. 1111 = 5.5 sec.
BL_FI	[3:0]	Backlight fade-in rate. If the fade-in is disabled (BL_FI = 0000), the backlight changes instantly (within 100 ms). If the fade-in rate is set, the backlight fades from its current value to its maximum value when the backlight is turned on. The times listed for BL_FI are for a full-scale fade-in (0 mA to 30 mA). Fades between closer current values reduce the fade time. See the Automated Fade-In and Fade-Out section for more information. 0000 = 0.1 sec (fade-in disabled). 0001 = 0.3 sec. 0010 = 0.6 sec. 0011 = 0.9 sec. … 1111 = 5.5 sec.

[1] Even with fade-in and fade-out disabled, the backlight does not instantaneously fade, but instead fades rapidly in about 100 ms.

Backlight Level 1 (Daylight) Maximum Current Register (BLMX1)—Register 0x0A

Table 29. BLMX1 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL1_MC						

Table 30. BLMX1 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL1_MC	[6:0]	Backlight maximum Level 1 (daylight) current. The backlight maximum current can be set according to the square law function (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Table 31. Diode Output Currents Per DAC Code

DAC Code	Current (mA)[1]	DAC Code	Current (mA)[1]
0x00	0.000	0x22	2.150
0x01	0.002	0x23	2.279
0x02	0.007	0x24	2.411
0x03	0.017	0x25	2.546
0x04	0.030	0x26	2.686
0x05	0.047	0x27	2.829
0x06	0.067	0x28	2.976
0x07	0.091	0x29	3.127
0x08	0.119	0x2A	3.281
0x09	0.151	0x2B	3.439
0x0A	0.186	0x2C	3.601
0x0B	0.225	0x2D	3.767
0x0C	0.268	0x2E	3.936
0x0D	0.314	0x2F	4.109
0x0E	0.365	0x30	4.285
0x0F	0.419	0x31	4.466
0x10	0.476	0x32	4.650
0x11	0.538	0x33	4.838
0x12	0.603	0x34	5.029
0x13	0.671	0x35	5.225
0x14	0.744	0x36	5.424
0x15	0.820	0x37	5.627
0x16	0.900	0x38	5.833
0x17	0.984	0x39	6.043
0x18	1.071	0x3A	6.257
0x19	1.163	0x3B	6.475
0x1A	1.257	0x3C	6.696
0x1B	1.356	0x3D	6.921
0x1C	1.458	0x3E	7.150
0x1D	1.564	0x3F	7.382
0x1E	1.674	0x40	7.619
0x1F	1.787	0x41	7.859
0x20	1.905	0x42	8.102
0x21	2.026	0x43	8.350

DAC Code	Current (mA)[1]
0x44	8.601
0x45	8.855
0x46	9.114
0x47	9.376
0x48	9.642
0x49	9.912
0x4A	10.185
0x4B	10.463
0x4C	10.743
0x4D	11.028
0x4E	11.316
0x4F	11.608
0x50	11.904
0x51	12.203
0x52	12.507
0x53	12.814
0x54	13.124
0x55	13.439
0x56	13.757
0x57	14.078
0x58	14.404
0x59	14.733
0x5A	15.066
0x5B	15.403
0x5C	15.743
0x5D	16.087
0x5E	16.435
0x5F	16.787
0x60	17.142
0x61	17.501
0x62	17.863
0x63	18.230
0x64	18.600
0x65	18.974
0x66	19.351
0x67	19.733
0x68	20.118
0x69	20.507
0x6A	20.899
0x6B	21.295
0x6C	21.695
0x6D	22.099
0x6E	22.506
0x6F	22.917
0x70	23.332
0x71	23.750
0x72	24.173
0x73	24.599
0x74	25.028
0x75	25.462
0x76	25.899
0x77	26.340
0x78	26.784
0x79	27.232
0x7A	27.684
0x7B	28.140
0x7C	28.599
0x7D	29.063
0x7E	29.529
0x7F	30.000

[1] Cubic 10 and Cubic 11 laws use the same current settings but vary the time step per DAC code.

Backlight Level 1 (Daylight) Dim Current Register (BLDM1)—Register 0x0B

Table 32. BLDM1 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL1_DC						

Table 33. BLDM1 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL1_DC	[6:0]	Backlight Level 1 (daylight) dim current. The backlight is set to the dim current value after a dim timeout or when the DIM_EN flag is set by the user (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 2 (Bright) Maximum Current Register (BLMX2)—Register 0x0C

Table 34. BLMX2 Backlight Maximum Level 2 Current Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL2_MC						

Table 35. BLMX2 Backlight Maximum Level 2 Current Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL2_MC	[6:0]	Backlight Level 2 (bright) maximum current (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 2 (Bright) Dim Current Register (BLDM2)—Register 0x0D

Table 36. BLDM2 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL2_DC						

Table 37. BLDM2 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL2_DC	[6:0]	Backlight Level 2 (bright) dim current. The backlight is set to the dim current value after a dim timeout or when the DIM_EN flag is set by the user (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 3 (Office) Maximum Current Register (BLMX3)—Register 0x0E

Table 38. BLMX3 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL3_MC						

Table 39. BLMX3 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL3_MC	[6:0]	Backlight Level 3 (office) maximum current (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 3 (Office) Dim Current Register (BLDM3)—Register 0x0F

Table 40. BLDM3 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL3_DC						

Table 41. BLDM3 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL3_DC	[6:0]	Backlight Level 3 (office) dim current. The backlight is set to the dim current value after a dim timeout or when the DIM_EN flag is set by the user (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 4 (Indoor) Maximum Current Register (BLMX4)—Register 0x10

Table 42. BLMX4 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL4_MC						

Table 43. BLMX4 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL4_MC	[6:0]	Backlight Level 4 (indoor) maximum current (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 4 (Indoor) Dim Current Register (BLDM4)—Register 0x11

Table 44. BLDM4 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL4_DC						

Table 45. BLDM4 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL4_DC	[6:0]	Backlight Level 4 (indoor) dim current. The backlight is set to the dim current value after a dim timeout or when the DIM_EN flag is set by the user (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 5 (Dark) Maximum Current Register (BLMX5)—Register 0x12

Table 46. BLMX5 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL5_MC						

Table 47. BLMX5 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL5_MC	[6:0]	Backlight Level 5 (dark) maximum current (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Backlight Level 5 (Dark) Dim Current Register (BLDM5)—Register 0x13

Table 48. BLDM5 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BL5_DC						

Table 49. BLDM5 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
BL5_DC	[6:0]	Backlight Level 5 (dark) dim current. The backlight is set to the dim current value after a dim timeout or when the DIM_EN flag is set by the user (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

INDEPENDENT SINK REGISTER DESCRIPTIONS

Independent Sink Current Fade Law Register (ISCLAW)—Register 0x1A

Table 50. ISCLAW Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						SC_LAW	

Table 51. ISCLAW Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:2]	Reserved.
SC_LAW	[1:0]	SC fade transfer law. 00 = square law DAC, linear time steps. 01 = square law DAC, linear time steps. 10 = square law DAC, nonlinear time steps (Cubic 10). 11 = square law DAC, nonlinear time steps (Cubic 11).

Independent Sink Current Control (ISCC)—Register 0x1B

Table 52. ISCC Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SC7_EN	SC6_EN	SC5_EN	SC4_EN	SC3_EN	SC2_EN	SC1_EN

Table 53. ISCC Bit Descriptions

Bit Name	Bit No.	Description
Reserved	7	Reserved.
SC7_EN	6	This enable acts on the LED 7. 1 = Independent Sink Current LED7 is turned on. 0 = Independent Sink Current LED7 is turned off.
SC6_EN	5	This enable acts on the LED 6. 1 = Independent Sink Current LED6 is turned on. 0 = Independent Sink Current LED6 is turned off.
SC5_EN	4	This enable acts on the LED 5. 1 = Independent Sink Current LED5 is turned on. 0 = Independent Sink Current LED5 is turned off.
SC4_EN	3	This enable acts on the LED 4. 1 = Independent Sink Current LED4 is turned on. 0 = Independent Sink Current LED4 is turned off.
SC3_EN	2	This enable acts on the LED 3. 1 = Independent Sink Current LED3 is turned on. 0 = Independent Sink Current LED3 is turned off.
SC2_EN	1	This enable acts on the LED 2. 1 = Independent Sink Current LED2 is turned on. 0 = Independent Sink Current LED2 is turned off.
SC1_EN	0	This enable acts on the LED 1. 1 = Independent Sink Current LED1 is turned on. 0 = Independent Sink Current LED1 is turned off.

Independent Sink Current Time (ISCT1)—Register 0x1C

Table 54. ISCT1 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON		SC7OFF		SC6OFF		SC5OFF	

Table 55. ISCT1 Bit Descriptions

Bit Name	Bit No.	Description[1, 2]
SCON	[7:6]	Sink current on time. If the sink current off time is not disabled, then when the independent current sink is enabled (Register 0x1B), it remains on for the on time selected (per the following times) and then turns off. 00 = 0.2 sec. 01 = 0.6 sec. 10 = 0.8sec. 11 = 1.2 sec.
SC7OFF	[5:4]	Independent Sink Current LED7 off time. When the sink current off time is disabled, the sink current remains on while enabled. If the sink current off time is set to any other value, then the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting. 00 = off time disabled. 01 = 0.6 sec. 10 = 1.2 sec. 11 = 1.8 sec.
SC6OFF	[3:2]	Independent Sink Current LED6 off time. When the sink current off time is disabled, the sink current remains on while enabled. If the sink current off time is set to any other value, then the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting. 00 = off time disabled. 01 = 0.6 sec. 10 = 1.2 sec. 11 = 1.8 sec.
SC5OFF	[1:0]	Independent Sink Current LED5 off time. When the sink current off time is disabled, the sink current remains on while enabled. If the sink current off time is set to any other value, then the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting. 00 = off time disabled. 01 = 0.6 sec. 10 = 1.2 sec. 11 = 1.8 sec.

[1] An independent sink remains on continuously when SCx_EN = 1 and SCx_OFF = 00 (disabled).
[2] To enable multiple independent sinks, set the appropriate SCx_EN bits. To create equivalent blinking and fading sequences, enable all independent sinks in one write cycle to cause a preprogrammed sequence to start simultaneously.

Independent Sink Current Time (ISCT2)—Register 0x1D

Table 56. ISCT2 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SC4OFF		SC3OFF		SC2OFF		SC1OFF	

Table 57. ISCT2 Bit Descriptions

Designation	Bit	Description[1, 2]
SC4OFF	[7:6]	Independent Sink Current LED4 off time. When the sink current off time is disabled, the sink current remains on while enabled. If the sink current off time is set to any other value, then the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting. 00 = off time disabled. 01 = 0. 6 sec. 10 = 1.2 sec. 11 = 1.8 sec.
SC3OFF	[5:4]	Independent Sink Current LED3 off time. When the sink current off time is disabled, the sink current remains on while enabled. If the sink current off time is set to any other value, then the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting. 00 = off time disabled. 01 = 0. 6 sec. 10 = 1.2 sec. 11 = 1.8 sec.
SC2OFF	[3:2]	Independent Sink Current LED2 off time. When the sink current off time is disabled, the sink current remains on while enabled. If the sink current off time is set to any other value, then the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting. 00 = off time disabled. 01 = 0. 6 sec. 10 = 1.2 sec. 11 = 1.8 sec.
SC1OFF	[1:0]	Independent Sink Current LED1 off time. When the sink current off time is disabled, the sink current remains on while enabled. If the sink current off time is set to any other value, then the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting. 00 = off time disabled. 01 = 0. 6 sec. 10 = 1.2 sec. 11 = 1.8 sec.

[1] An independent sink remains on continuously when SCx_EN = 1 and SCx_OFF = 00 (disabled).
[2] To enable multiple independent sinks, set the appropriate SCx_EN bits. To create equivalent blinking and fading sequences, enable all independent sinks in one write cycle. This causes a preprogrammed sequence to start simultaneously.

Independent Sink Current Fade (ISCF)—Register 0x1E

Table 58. ISCF Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCFO				SCFI			

Table 59. ISCF Bit Descriptions

Bit Name	Bit No.	Description
SCFO	[7:4]	Sink current fade-out time. The maximum fade time is from full-scale to 0 mA. Therefore, a fade is shorter between maximum and dim or between dim and off. Binary code fade-out times are as follows: 0000 = disabled. 0001 = 0.30 sec. 0010 = 0.60 sec. 0011 = 0.90 sec. 0100 = 1.2 sec. 0101 = 1.5 sec. 0110 = 1.8 sec. 0111 = 2.1 sec. 1000 = 2.4 sec. 1001 = 2.7 sec. 1010 = 3.0 sec. 1011 = 3.5 sec. 1100 = 4.0 sec. 1101 = 4.5 sec. 1110 = 5.0 sec. 1111 = 5.5 sec.
SCFI	3:0	Sink current fade-in time. The maximum fade time is from 0 mA to full scale. Binary code fade-out times are as follows: 0000 = disabled. 0001 = 0.30 sec. 0010 = 0.60 sec. 0011 = 0.90 sec. 0100 = 1.2 sec. 0101 = 1.5 sec. 0110 = 1.8 sec. 0111 = 2.1 sec. 1000 = 2.4 sec. 1001 = 2.7 sec. 1010 = 3.0 sec. 1011 = 3.5 sec. 1100 = 4.0 sec. 1101 = 4.5 sec. 1110 = 5.0 sec. 1111 = 5.5 sec.

Sink Current Register LED1 (ISC1)—Register 0x1F

Table 60. ISC1 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD1						

Table 61. ISC1 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved	
SCD1	[6:0]	Sink current. Use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Sink Current Register LED2 (ISC2)—Register 0x20

Table 62. ISC2 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD2						

Table 63. ISC2 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
SCD2	[6:0]	Sink current. Use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Sink Current Register LED3 (ISC3)—Register 0x21

Table 64. ISC3 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD3						

Table 65. ISC3 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
SCD3	[6:0]	Sink current. Use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Sink Current Register LED4 (ISC4)—Register 0x22

Table 66. ISC4 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD4						

Table 67. ISC4 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
SCD4	[6:0]	Sink current. Use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Sink Current Register LED5 (ISC5)—Register 0x23

Table 68. ISC5 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD5						

Table 69. ISC5 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
SCD5	[6:0]	Sink current. Use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Sink Current Register LED6 (ISC6)—Register 0x24

Table 70. ISC6 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD6						

Table 71. ISC6 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved	
SCD6	[6:0]	Sink current. Use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000

Sink Current Register LED7 Brightness Level 1 (ISC7)—Register 0x25

Table 72. ISC7 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCR	SCD7						

Table 73. ISC7 Bit Descriptions

Bit Name	Bit No.	Description	
SCR	7	1 = Sink Current 1.	
		0 = Sink Current 0.	
SCD7	[6:0]	For Sink Current 0, use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000
		For Sink Current 1, use the following DAC code schedule (see Table 74 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.004
		0000010	0.014
		0000011	0.034
		…	…
		1111111	60.000

Output Currents for LED7 with SCR = 1

Table 74. Diode Output Currents for LED7 (SCR High)

DAC Code	Diode Current (mA)	DAC Code	Diode Current (mA)
0x00	0.000	0x17	1.968
0x01	0.004	0x18	2.142
0x02	0.014	0x19	2.326
0x03	0.034	0x1A	2.514
0x04	0.06	0x1B	2.712
0x05	0.094	0x1C	2.916
0x06	0.134	0x1D	3.128
0x07	0.182	0x1E	3.348
0x08	0.238	0x1F	3.574
0x09	0.302	0x20	3.81
0x0A	0.372	0x21	4.052
0x0B	0.45	0x22	4.3
0x0C	0.536	0x23	4.558
0x0D	0.628	0x24	4.822
0x0E	0.73	0x25	5.092
0x0F	0.838	0x26	5.372
0x10	0.952	0x27	5.658
0x11	1.076	0x28	5.952
0x12	1.206	0x29	6.254
0x13	1.342	0x2A	6.562
0x14	1.488	0x2B	6.878
0x15	1.64	0x2C	7.202
0x16	1.8	0x2D	7.534

DAC Code	Diode Current (mA)
0x2E	7.872
0x2F	8.218
0x30	8.57
0x31	8.932
0x32	9.3
0x33	9.676
0x34	10.058
0x35	10.45
0x36	10.848
0x37	11.254
0x38	11.666
0x39	12.086
0x3A	12.514
0x3B	12.95
0x3C	13.392
0x3D	13.842
0x3E	14.3
0x3F	14.764
0x40	15.238
0x41	15.718
0x42	16.204
0x43	16.7
0x44	17.202
0x45	17.71
0x46	18.228
0x47	18.752
0x48	19.284
0x49	19.824
0x4A	20.37
0x4B	20.926
0x4C	21.486
0x4D	22.056
0x4E	22.632
0x4F	23.216
0x50	23.808
0x51	24.406
0x52	25.014
0x53	25.628
0x54	26.248
0x55	26.878

DAC Code	Diode Current (mA)
0x56	27.514
0x57	28.156
0x58	28.808
0x59	29.466
0x5A	30.132
0x5B	30.806
0x5C	31.486
0x5D	32.174
0x5E	32.87
0x5F	33.574
0x60	34.284
0x61	35.002
0x62	35.726
0x63	36.46
0x64	37.2
0x65	37.948
0x66	38.702
0x67	39.466
0x68	40.236
0x69	41.014
0x6A	41.798
0x6B	42.59
0x6C	43.39
0x6D	44.198
0x6E	45.012
0x6F	45.834
0x70	46.664
0x71	47.5
0x72	48.346
0x73	49.198
0x74	50.056
0x75	50.924
0x76	51.798
0x77	52.68
0x78	53.568
0x79	54.464
0x7A	55.368
0x7B	56.28
0x7C	57.198
0x7D	58.126
0x7E	59.058
0x7F	60.000

Sink Current Register LED7 Brightness Level 2 (ISC7_L2)—Register 0x26

Table 75. ISC7_L2 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD7_L2						

Table 76. ISC7_L2 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
SCD7_L2	[6:0]	For SCR = 0 (Register ISC7), use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000
		For SCR = 1 (Register ISC7), use the following DAC code schedule (see Table 74 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.004
		0000010	0.014
		0000011	0.034
		…	…
		1111111	60.000

Sink Current Register LED7 Brightness Level 3 (ISC7_L3)—Register 0x27

Table 77. ISC7_L3 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD7_L3						

Table 78. ISC7_L3 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
SCD7_L3	[6:0]	For SCR = 0 (Register ISC7), use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000
		For SCR = 1 (Register ISC7), use the following DAC code schedule (see Table 74 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.004
		0000010	0.014
		0000011	0.034
		…	…
		1111111	60.000

Sink Current Register LED7 Brightness Level 4 (ISC7_L4)—Register 0x28

Table 79. ISC7_L4 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD7_L4						

Table 80. ISC7_L4 Bit Descriptions

Bit Name	Bit No.	Description	
N/A	7	Reserved.	
SCD7_L4	6:0	For SCR = 0 (Register ISC7), use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30.000
		For SCR = 1 (Register ISC7), use the following DAC code schedule (see Table 74 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.00
		0000001	0.004
		0000010	0.014
		0000011	0.034
		…	…
		1111111	60.000

Sink Current Register LED7 Brightness Level 5 (ISC7_L5)—Register 0x29

Table 81. ISC7_L5 Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SCD7_L5						

Table 82. ISC7_L5 Bit Descriptions

Bit Name	Bit No.	Description	
Reserved	7	Reserved.	
SCD7_L5	[6:0]	For SCR = 0 (Register ISC7), use the following DAC code schedule (see Table 31 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.002
		0000010	0.007
		0000011	0.017
		…	…
		1111111	30
		For SCR = 1 (Register ISC7), use the following DAC code schedule (see Table 74 for a complete list of values).	
		DAC Code	**Current (mA)**
		0000000	0.000
		0000001	0.004
		0000010	0.014
		0000011	0.034
		…	…
		1111111	60.000

COMPARATOR REGISTER DESCRIPTIONS

Register 0x2D to Register 0x39 control the comparators, and Register 0x40 to Register 0x43 provide the raw data obtained from the comparators.

ALS Comparator Control (CMP_CTL)—Register 0x2D

Table 83. CMP_CTL Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FILT2			FORCE_RD2	FILT			FORCE_RD

Table 84. CMP_CTL Bit Descriptions

Bit Name	Bit No.	Description
FILT2	[7:5]	Filter setting for the second light sensor. 000 = 80 ms. 001 = 160 ms. 010 = 320 ms. 011 = 640 ms. 100 = 1280 ms. 101 = 2560 ms. 110 = 5120 ms. 111 = 10,240 ms.
FORCE_RD2	4	Forces a read of the second light sensor while the backlight is off. This bit is reset by the chip after the conversion is complete and is ignored if the backlight is enabled.
FILT	[3:1]	Filter setting for the main light sensor. 000 = 80 ms. 001 = 160 ms. 010 = 320 ms. 011 = 640 ms. 100 = 1280 ms. 101 = 2560 ms. 110 = 5120 ms. 111 = 10,240 ms.
FORCE_RD	0	Forces a read of the main light sensor while the backlight is off. This bit is reset by the chip after the conversion is complete and is ignored if the backlight is enabled.

Main ALS Comparator Level Enable (ALS1_EN)—Register 0x2E

Table 85. ALS1_EN Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				L5_EN	L4_EN	L3_EN	L2_EN

Table 86. ALS1_EN Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:4]	Reserved.
L5_EN	3	1 = the Level 5 comparator is enabled for the CMP_IN comparator. 0 = the Level 5 comparator is disabled for the CMP_IN comparator.
L4_EN	2	1 = the Level 4 comparator is enabled for the CMP_IN comparator. 0 = the Level 4 comparator is disabled for the CMP_IN comparator.
L3_EN	1	1 = the Level 3 comparator is enabled for the CMP_IN comparator. 0 = the Level 3 comparator is disabled for the CMP_IN comparator.
L2_EN	0	1 = the Level 2 comparator is enabled for the CMP_IN comparator. 0 = the Level 2 comparator is disabled for the CMP_IN comparator.

Secondary ALS Comparator Level Enable (ALS2_EN)—Register 0x2F

Table 87. ALS2_EN Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				L5_EN2	L4_EN2	L3_EN2	L2_EN2

Table 88. ALS2_EN Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:4]	Reserved.
L5_EN2	3	1 = the Level 5 comparator and auto level changing is enabled for the CMP2 comparator. 0 = the Level 5 comparator is disabled for the CMP2 comparator.
L4_EN2	2	1 = the Level 4 comparator and auto level changing is enabled for the CMP2 comparator. 0 = the Level 4 comparator is disabled for the CMP2 comparator.
L3_EN2	1	1 = the Level 3 comparator and auto level changing is enabled for the CMP2 comparator. 0 = the Level 3 comparator is disabled for the CMP2 comparator.
L2_EN2	0	1 = the Level 2 comparator and auto level changing is enabled for the CMP2 comparator. 0 = the Level 2 comparator is disabled for the CMP2 comparator.

Main ALS Comparator Status (ALS1_STAT)—Register 0x30

Table 89. ALS1_STAT Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				CMP1_L5_OUT	CMP1_L4_OUT	CMP1_L3_OUT	CMP1_L2_OUT

Table 90. ALS1_STAT Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:4]	Reserved.
CMP1_L5_OUT	3	This bit is the output of the Level 5 comparator for the main light sensor.
CMP1_L4_OUT	2	This bit is the output of the Level 4 comparator for the main light sensor.
CMP1_L3_OUT	1	This bit is the output of the Level 3 comparator for the main light sensor.
CMP1_L2_OUT	0	This bit is the output of the Level 2 comparator for the main light sensor.

Second ALS Comparator Status (ALS2_STAT)—Register 0x31

Table 91. ALS2_STAT Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				CMP2_L5_OUT	CMP2_L4_OUT	CMP2_L3_OUT	CMP2_L2_OUT

Table 92. ALS2_STAT Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:4]	Reserved.
CMP2_L5_OUT	3	This bit is the output of the Level 5 comparator for the second light sensor.
CMP2_L4_OUT	2	This bit is the output of the Level 4 comparator for the second light sensor.
CMP2_L3_OUT	1	This bit is the output of the Level 3 comparator for the second light sensor.
CMP2_L2_OUT	0	This bit is the output of the Level 2 comparator for the second light sensor.

Comparator Level 2 Threshold (L2_TRP)—Register 0x32

Table 93. L2_TRP Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L2_TRP							

Table 94. L2_TRP Bit Descriptions

Bit Name	Bit No.	Description
L2_TRP	[7:0]	Comparator Level 2 threshold. If the comparator input is below L2_TRP, then the comparator trips and the backlight enters Level 2 (bright) mode. The code settings for photosensor current are as follows: 00000000 = 0 µA. 00000001 = 4.3 µA. 00000010 = 8.6 µA. 00000011 = 12.9 µA. … 11111010 = 1080 µA. … 11111111 = 1106 µA. Although codes above 1111010 (250 d) are possible, they should not be used. Furthermore, the maximum value of L2_TRP + L2_HYS must not exceed 1111010 (250 d).

Comparator Level 2 Hysteresis (L2_HYS)—Register 0x33

Table 95. L2_HYS Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L2_HYS							

Table 96. L2_HYS Bit Descriptions

Bit Name	Bit No.	Description
L2_HYS	[7:0]	Comparator Level 2 hysteresis. If the comparator input is above L2_TRP + L2_HYS, the comparator trips and the backlight enters Level 1 (daylight) mode. The code settings for photosensor current hysteresis are as follows: 0000000 = 0 µA. 00000001 = 4.3 µA. 00000010 = 8.6 µA. 00000011 = 12.9 µA. … 11111010 = 1080 µA. … 11111111 = 1106 µA. Although codes above 1111010 (250 d) are possible, they should not be used. Furthermore, the maximum value of L2_TRP + L2_HYS must not exceed 1111010 (250 d).

Comparator Level 3 Threshold (L3_TRP)—Register 0x34

Table 97. L3_TRP Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L3_TRP							

Table 98. L3_TRP Bit Descriptions

Bit Name	Bit No.	Description
L3_TRP	[7:0]	Comparator Level 3 threshold. If the comparator input is below L3_TRP, then the comparator trips and the backlight enters Level 3 (office) mode. The code settings for photosensor current are as follows: 00000000 = 0 µA. 00000001 = 2.16 µA. 00000010 = 4.32 µA. 00000011 = 8.64 µA. … 11111111 = 550.8 µA.

Comparator Level 3 Hysteresis (L3_HYS)—Register 0x35

Table 99. L3_HYS Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L3_HYS							

Table 100. L3_HYS Bit Descriptions

Bit Name	Bit No.	Description
L3_HYS	[7:0]	Comparator Level 3 hysteresis. If the comparator input is above L3_TRP + L3_HYS, the comparator trips and the backlight enters Level 2 (bright) mode. The code settings for photosensor current hysteresis are as follows: 00000000 = 0 µA. 00000001 = 2.16 µA. 00000010 = 4.32 µA. 00000011 = 8.64 µA. … 11111111 = 550.8 µA.

Comparator Level 4 Threshold (L4_TRP)—Register 0x36

Table 101. L4_TRP Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L4_TRP							

Table 102. L4_TRP Bit Descriptions

Bit Name	Bit No.	Description
L4_TRP	[7:0]	Comparator Level 4 threshold. If the comparator input is below L4_TRP, then the comparator trips and the backlight enters Level 4 (indoor) mode. The code settings for photosensor current are as follows: 00000000 = 0 µA. 00000001 = 1.08 µA. 00000010 = 2.16 µA. 00000011 = 4.32 µA. … 11111111 = 275.4 µA.

Comparator Level 4 Hysteresis (L4_HYS)—Register 0x37

Table 103. L4_HYS Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L4_HYS							

Table 104. L4_HYS Bit Descriptions

Bit Name	Bit No.	Description
L4_HYS	[7:0]	Comparator Level 4 hysteresis. If the comparator input is above L4_TRP + L4_HYS, the comparator trips and the backlight enters Level 3 (office) mode. The code settings for photosensor current hysteresis are as follows: 00000000 = 0 µA. 00000001 = 1.08 µA. 00000010 = 2.16 µA. 00000011 = 4.32 µA. … 11111111 = 275.4 µA.

Comparator Level 5 Threshold (L5_TRP)—Register 0x38

Table 105. L5_TRP Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L5_TRP							

Table 106. L5_TRP Bit Descriptions

Bit Name	Bit No.	Description
L5_TRP	[7:0]	Comparator Level 5 threshold. If the comparator input is below L5_TRP, then the comparator trips and the backlight enters Level 5 (dark) mode. The code settings for photosensor current are as follows: 0000000 = 0 µA. 0000001 = 0.54 µA. 0000010 = 1.08 µA. 0000011 = 1.62 µA. … 1111111 = 137.7 µA.

Comparator Level 5 Hysteresis (L5_HYS)—Register 0x39

Table 107. L5_HYS Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L5_HYS							

Table 108. L5_HYS Bit Descriptions

Bit Name	Bit No.	Description
L5_HYS	[7:0]	Comparator Level 5 hysteresis. If the comparator input is above L5_TRP + L5_HYS, the comparator trips and the backlight enters Level 4 (indoor) mode. The code settings for photosensor current hysteresis are as follows: 0000000 = 0 µA. 0000001 = 0.54 µA. 0000010 = 1.08 µA. 0000011 = 1.62 µA. … 1111111 = 137.7 µA.

First Phototransistor Register: Low Byte (PH1LEVL)—Register 0x40

Table 109. PH1LEVL Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH1LEV_LOW							

Table 110. PH1LEVL Bit Descriptions

Bit Name	Bit No.	Description
PH1LEV_LOW	[7:0]	13-bit conversion value for the first light sensor—low byte (Bit 7 to Bit 0). The value is updated every 80 ms when the light sensor is enabled. This is a read-only register.

First Phototransistor Register: High Byte (PH1LEVH)—Register 0x41

Table 111. PH1LEVH Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			PH1LEV_HIGH				

Table 112. PH1LEVH Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:5]	Reserved
PH1LEV_HIGH	[4:0]	13-bit conversion value for the first light sensor—high byte (Bit 12 to Bit 8). The value is updated every 80 ms when the light sensor is enabled. This is a read-only register. The full 13-bit conversion value is equal (in hex) to raw photosensor conversion (RPC) = PH1LEV_HIGH × 0x100 + PH1LEV_LOW. This 13-bit number has a maximum value of 0x1F40 (decimal = 8000). To convert from the RPC (decimal) value into the photosensor current, use the following equation: I_{ALS} (measured) = RPC (decimal)/8000 × I_{ALS}, where I_{ALS} is given in Table 1.

Second Phototransistor Register: Low Byte (PH2LEVL)—Register 0x42

Table 113. PH2LEVL Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH2LEV_LOW							

Table 114. PH2LEVL Bit Descriptions

Bit Name	Bit No.	Description
PH2LEV_LOW	[7:0]	13-bit conversion value for the second light sensor—low byte (Bit 7 to Bit 0). The value is updated every 80 ms when the light sensor is enabled. This is a read-only register.

Second Phototransistor Register: High Byte (PH2LEVH)—Register 0x43

Table 115. PH2LEVH Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			PH2LEV_HIGH				

Table 116. PH2LEVH Bit Descriptions

Bit Name	Bit No.	Description
Reserved	[7:5]	Reserved
PH2LEV_HIGH	[4:0]	13-bit conversion value for the second light sensor—high byte (Bit 12 to Bit 8). The value is updated every 80 ms when the light sensor is enabled. This is a read-only register. The full 13-bit conversion value is equal (in hex) to raw photosensor conversion (RPC) = PH2LEV_HIGH × 0x100 + PH2LEV_LOW. This 13-bit number has a maximum value of 0x1F40 (decimal = 8000). To convert from the RPC (decimal) value into the photosensor current, use the following equation: I_{ALS}(measured) = RPC(decimal)/8000 × I_{ALS}, where I_{ALS} is given in Table 1.

OUTLINE DIMENSIONS

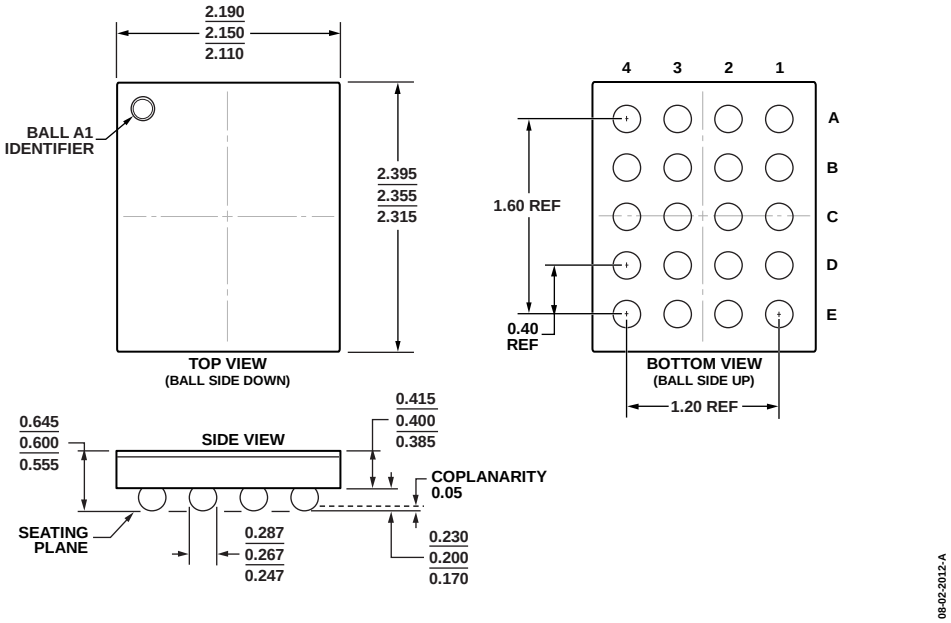


Figure 54. 20-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-20-7)
Dimensions shown in millimeters

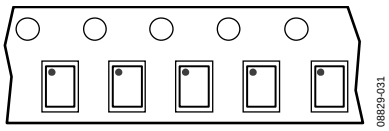
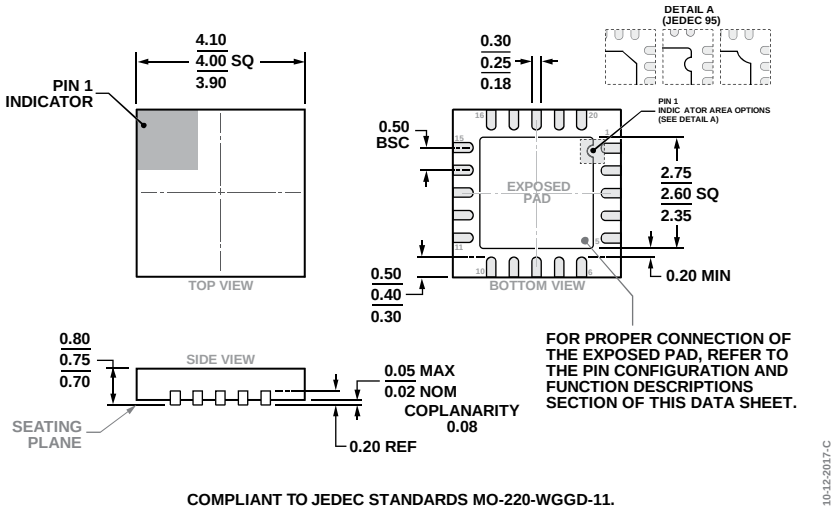


Figure 55. Tape and Reel Orientation for WLCSP Units



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 56. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

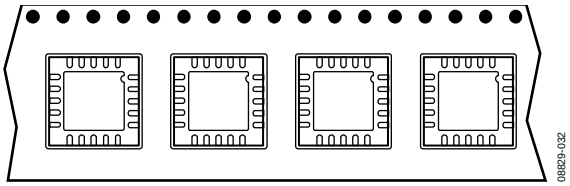


Figure 57. Tape and Reel Orientation for LFCSP Units

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP8870ACBZ-R7	−40°C to +105°C	20-Ball WLCSP, 7″ Tape and Reel	CB-20-7
ADP8870ACPZ-R7	−40°C to +105°C	20-Lead LFCSP, 7″ Tape and Reel	CP-20-8
ADP8870DBCB-EVALZ		ADP8870 Daughter Card and LED Board	

[1] Z = RoHS Compliant Part.

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