Document Number: MC33784
Rev 3.0, 11/2009

RoHS

DSI 2.02 Sensor Interface

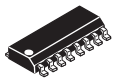
The 33784 is a slave, Distributed System Interface Bus (DBUS), version 2.02 compatible device, optimized as a sensor interface. The device contains circuits to power sensors such as accelerometers, and to digitize the analog level from the sensor. The device is controlled by commands over the bus, and returns measured data and other information over the bus.

Features

- DSI version 2.02 compatible
- 2-channel, 10-bit analog-to-digital converter (ADC)
- 3 pins configurable as logic inputs or outputs
- Provides regulated +5.0v output for sensor power from bus
- On-board clock (no external elements required)
- Includes bus switches on bus and bus return
- Pb-free packaging designated by suffix code EF

33784

SENSOR INTERFACE



EF SUFFIX (PB-FREE)
98ASB42566B
16-LEAD SOICN

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ33784EF/R2	-40°C to 125°C	16 SOICN

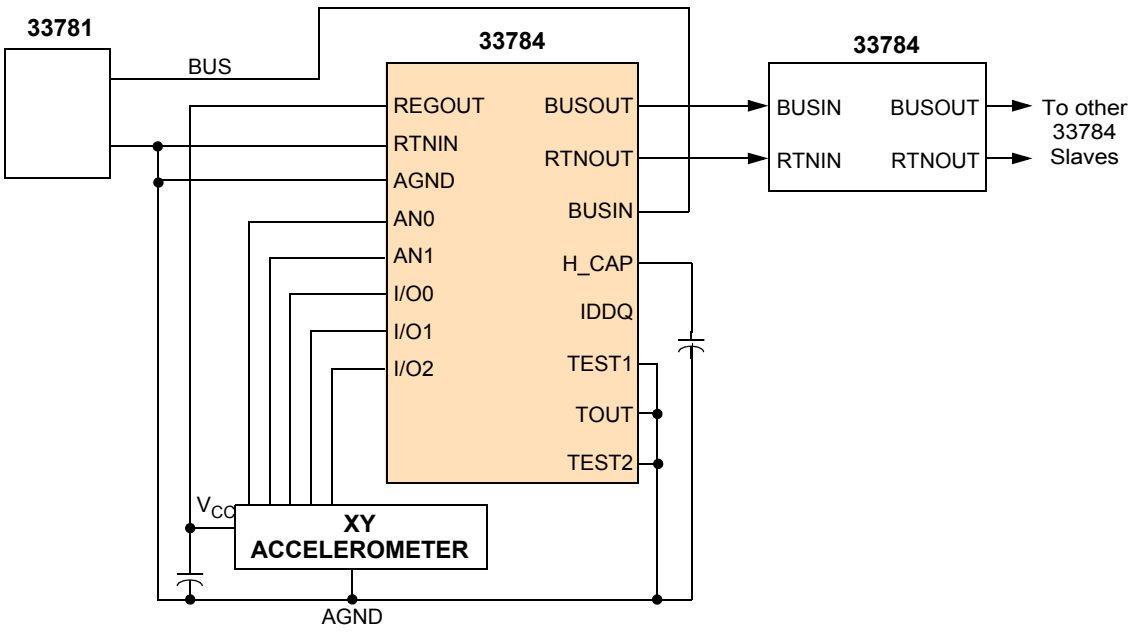


Figure 1. 33784 Simplified Application Diagram (Daisy Chain Shown)

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

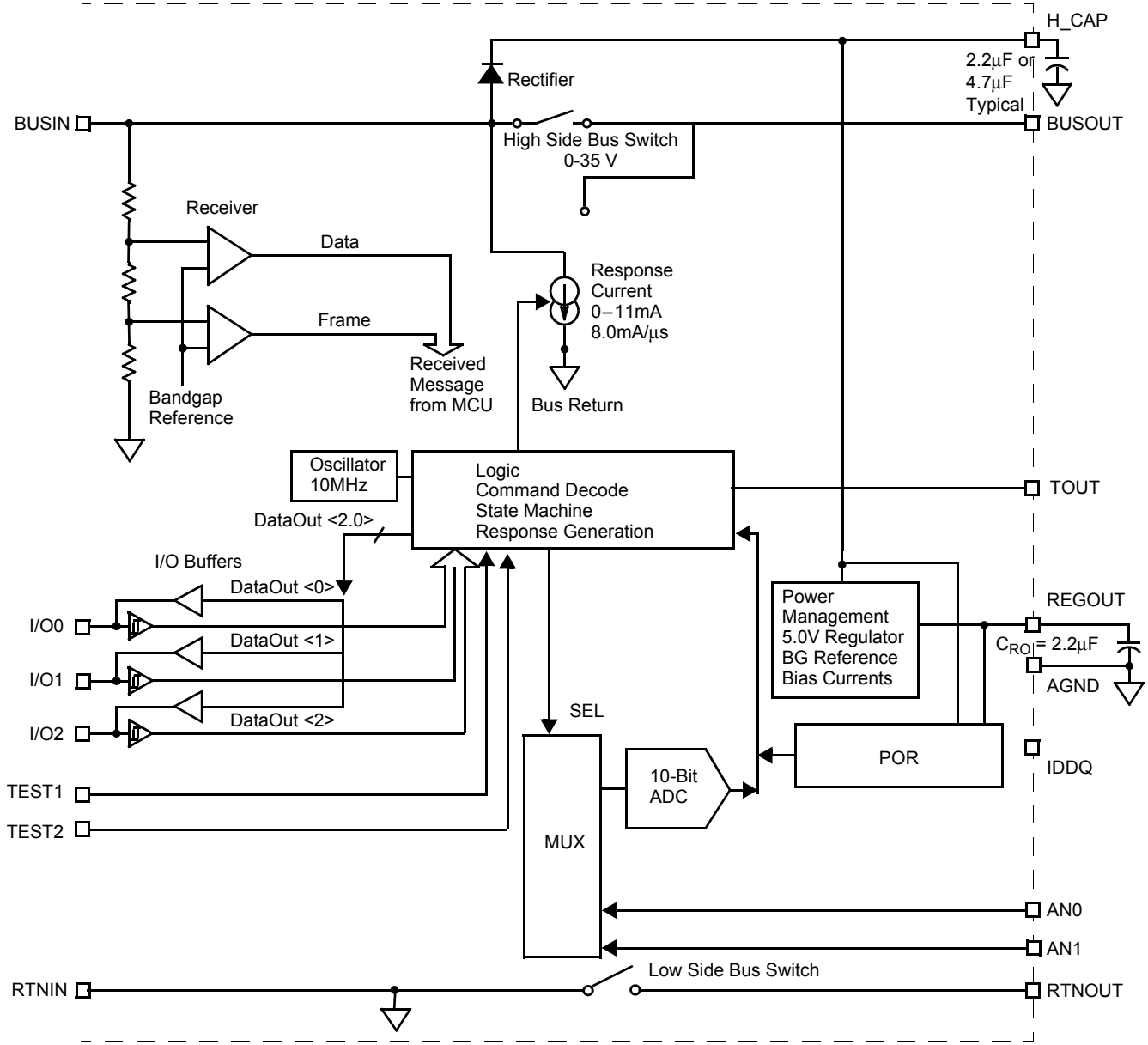


Figure 2. 33784 Simplified Internal Block Diagram

PIN CONNECTIONS

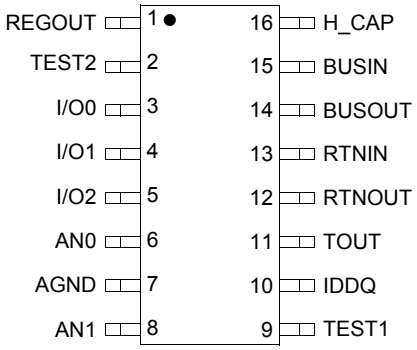


Figure 3. 33784 Pin Connections

Table 1. 33784 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	REGOUT	Output	Regulator Output	Pin provides a regulated 5.0V output. The power is derived from the bus.
2	TEST2	Test	Test2	This pin must be grounded in the application.
3 4 5	I/O0 I/O1 I/O2	Input/Output	Logic I/O	Pins can be used to provide a logic level output or a logic input.
6, 8	AN0,AN1	Input	Analog Input	Inputs to the ADC.
7	AGND	Ground Reference	Analog Ground	Pin is the low reference level and power return for the analog-to-digital converter (ADC). It is internally connected to RTNIN.
9	TEST1	Test	Test1	This pin must be grounded in the application.
10	IDDQ	Test	IDDQ	Input pin for measuring device quiescent current. Must be left open in the application.
11	TOUT	Test	Test Output	This pin must be grounded in the application.
12	RTNOUT	Power	Bus Return	Switched RTNIN pin, attaches to the next RTNIN pin in the daisy chain.
13	RTNIN	Power	Bus Return	Pin attaches to the low side of the differential bus, and provides the common return for power and signalling. It is internally connected to AGND.
14	BUSOUT	Output	DBUS Output	Switched BUSIN Pin, attaches to the next BUSIN pin in the daisy chain.
15	BUSIN	Input	DBUS Input	Pin attaches to the high side of the differential bus and responds to initialization commands.
16	H_CAP	Output	Holding Capacitor	A capacitor attached to this pin is charged by the bus during bus idle and supplies current to run the device and for external devices via the REGOUT pin during non-idle periods.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to Analog Ground (AGND) unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
I/O0, I/O1, I/O2, AN0, AN1, TEST1, TEST2, TOUT Voltage	V_{IO}	-0.3 to V_{REGOUT} + 0.3	V
I/On, ANn, TESTn, TOUT Pin Current	I_{IO}	5.0	mA
BUSOUT Voltage, BUS SW = open	V_{IN}	-14 to 40	V
BUSIN Voltage, BUS SW = open	V_{IN}	-0.3 to 40	V
RTNOUT Voltage, BUS SW = open	V_{IN}	-14 to 25	V
H_CAP Voltage	V_{IN}	-0.3 to 40	V
BUSIN, BUSOUT, and H_CAP Current (Continuous)	I_{IN}	400	mA
BUSIN, RTNIN, reverse current (max 5 ms)	I_{REVLK}	400	mA
RTNIN, RTNOUT Current	I_{BUSRTN}	400	mA
IDDQ Voltage	V_{IDDQ}	2.75	V
V_{REG} Range	V_{RO}	0.3 - 7.0	V
ESD Voltage[1]	V_{ESD}		V
Human Body Model (HBM)		±2000	
Machine Model (MM)		±200	
Charge Device Model (CDM)			
Corner pins		±750	
All other pins		±500	
THERMAL RATINGS			
Storage Temperature	T_S	-55 to 150	°C
Operating Ambient Temperature	T_A	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS			
Resistance, Junction-to-Ambient (Single Layer (1s) PCB Board)	$R_{\theta JA}$	125	°C/W
Resistance, Junction-to-Board (Multi-Layer (2s2P) PCB Board)	$R_{\theta JB}$	62	°C/W
Peak Package Reflow Temperature During Reflow[2],[3]	T_{PPRT}	Note 3	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (HBM) (CZAP= 100pF, RZAP=1500Ω), ESD2 testing is performed in accordance with the Machine Model (MM) (C_{ZAP}=200pF, R_{ZAP}=0Ω); and Charge Body Model (CBM)
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions -0.3V ≤ V_{BUSIN} ≤ 30V, 6.0V ≤ V_{H_CAP} ≤ 30V, -40°C ≤ T_A ≤ 125°C, RTNIN=AGND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Quiescent Current Drain V_{H_CAP} = 25V, I/O = Input	I_Q	 –	 –	 4.0	mA
BUSIN to H_CAP Rectifier Voltage Drop I_{HCAP} = 15mA I_{HCAP} = 100mA	V_{RECT}	 – –	 0.75 0.9	 1.00 1.4	V
H_CAP Diode Efficiency[4] I_{HCAP} = 400mA, BUSIN = 25V		 99	 –	 –	%
BUSIN Bias Current V_{BUSIN} = 8.0V, V_{H_CAP} = 9.0V V_{BUSIN} = 4.5V, V_{H_CAP} = 9.0V when device is not signalling	I_{BIAS}	 -100 -100	 –	 100 100	µA
Rectifier Leakage Current V_{BUSIN} = 0V, V_{H_CAP} = 25V	I_{RLKG}	-20	–	20	µA
REGOUT 5.8V ≤ V_{H_CAP} ≤ 25V, 0 ≤ I_{RO} ≤ 14mA	V_{RO}	4.9	5.0	5.1	V
REGOUT Line Regulation I_{RO} = 14mA, 6.0V ≤ V_{H_CAP} ≤ 25V I_{RO} is the total internal and external load current	VR_{LINE}	–	–	20	mV
REGOUT Load Regulation 0 ≤ I_{RO} ≤ 14mA, 6.0V ≤ V_{H_CAP} ≤ 25V,	VR_{LD}	–	–	15	mV
REGOUT Transient Line Regulation[5] I_{RO} = 14mA, 0 V ≤ V_{BUSIN} ≤ 30 V, 8V/us @ BUSIN, or, 5V/us @ HCAP C_{RO} = 2.2 uF, C_{RO} ESR = 0.063-2.2Ω @ 20kHz, 0.004-0.072Ω @ 200kHz		–	–	(25)	mV
REGOUT Transient Load Regulation[5] 0 ≤ I_{RO} ≤ 14mA, 6.0V ≤ V_{H_CAP} ≤ 25V, 2mA/us @ I_{RO}, C_{RO} = 2.2uF, C_{RO} ESR = 0.063-2.2Ω @ 20kHz, 0.004-0.072Ω @ 200kHz		–	–	(50)	mV
REGOUT Current Limit, V_{REGOUT} = 0V	I_{LMT}	25	35	45	mA
Hi-side Bus Switch Resistance 0 ≤ V_{BUSIN} ≤ 30V, I_{SWH} = 160mA (Bus Switch Active)	R_{SWH}	 –	 3.0	 6.0	Ω
Low-side Bus Switch Resistance I_{SWL} = 160mA (Bus Switch Active)	R_{SWL}	 –	 3.0	 6.0	Ω

Notes

4. E_{FF} = 400mA/I_{BUSIN} - I_Q
5. Assured by design.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions -0.3V ≤ V_{BUSIN} ≤ 30V, 6.0V ≤ V_{H_CAP} ≤ 30V, -40°C ≤ T_A ≤ 125°C, RTNIN=AGND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Switch Resistance Matching = | R_{SWH} - R_{SWL} |, T_A = 25°C = | R_{SWH} - R_{SWL} |, T_A = 125°C	R_{DSW}	– –	–	0.3 0.6	Ω
I/O0, I/O1, I/O2, and TEST Pull-down Current V_{IN} = 1.0V	I_{PD}	5.0	–	20	µA
I/O0, I/O1, I/O2, and TEST Leakage Current I/On, TEST = 0V	I_{LK}	-10	–	10	µA
AN0, AN1 Pull-down Current (Enabled mode) V_{IN} = 1.0V(6)	I_{PDANn}	5.0	–	20	µA
AN0, AN1 Leakage Current (Disabled mode)(6)	I_{ANnLKG}	-1.0	–	1.0	µA
BUSIN Logic Thresholds Signal Frame	 V_{THS} V_{THF}	 2.8 5.5	 3.0 6.0	 3.2 6.5	V
BUSIN Hysteresis Signal Frame	 V_{HYSS} V_{HYSF}	 60 100	 – –	 120 300	mV
BUSIN Response Current V_{BUSIN} = 4.0V V_{BUSIN} = 1.175V	I_{RSP}	 9.9 7.0	 11 –	 12.1 –	mA
BUSIN, BUSOUT Leakage Current High Side Bus Switch Open BUSIN = 25V, BUSOUT = 0V BUSIN= 0V, BUSOUT = 16V	$I_{BUSINLK}$	-20	–	20	µA
RTNIN, RTNOUT Leakage Current Low Side Bus Switch Open RTNIN = 14V, RTNOUT = 0V RTNIN = 0V, RTNOUT = 16V	$I_{BUSRTNLK}$	 -20 -125	 – –	 20 125	µA
RTNIN to BUSOUT Leakage Current High Side Bus Switch Open RTNIN = 14, BUSOUT 0V	$I_{CROSSLK}$	-20	–	20	µA
ADC Resolution	ADC_{RES}	10	10	10	bit
ANn Input Capacitance(7)	C_{ADC}	–	–	20	pF
Input Source Impedance(7)	Z_{IN}	–	–	5.0	kΩ
ADC Code Conversion Error (INL) Source Resistance < 1.0kΩ	ADC_{INL}	-3.5	–	+3.5	LSB
Full Scale Error	ADC_{FS}	-3.5	–	+3.5	LSB

6. In the default, AN0 pull-down current is disabled and AN1 pull-down current is enabled. AN1 pull-down current is disabled during AN1 A2D conversion. At the same time, AN0 pull-down current is enabled.
7. Assured by design.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions -0.3V ≤ V_{BUSIN} ≤ 30V, 6.0V ≤ V_{H_CAP} ≤ 30V, -40°C ≤ T_A ≤ 125°C, RTNIN=AGND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Absolute Error[8] 0.5V ≤ Input Voltage ≤ 4.5V	ADC_{ABS}	-4.0	–	+4.0	LSB
ADC Code Conversion Error (DNL) Source Resistance < 1.0 kΩ	ADC_{DNL}	–	–	2.0	LSB
I/O Input Levels Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	 70%*V_{REG} –	 – –	 – 30%*V_{REG}	V
I/O Input Hysteresis[8]	V_{HYS}	300			mV
I/O Logic Output Levels Output Low (I_L = 1.0mA) Output High (I_L = -500µA)	 V_{OL} V_{OH}	 0 V_{REGOUT} - 0.8	 – –	 0.8 V_{REGOUT}	V
POR Detect Thresholds Voltage at HCAP Voltage at REGOUT	 $V_{PORHCAP}$ V_{PORREG}	 6.0 4.25	 6.39 4.5	 6.77 4.75	V

Notes
8. Assured by design.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions -0.3V ≤ V_{BUSIN} or V_{BUSOUT} ≤ 30V, 6.0V ≤ V_{H_CAP} ≤ 30V, -40°C ≤ T_A ≤ 125°C, AGND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Oscillator Frequency	f_{OSC}	9.0	10.0	11.0	MHz
Internal Oscillator Duty Cycle	DC_{OSC}	45	50	55	%
Initialization to Bus Switches Close	t_{BS}	–	–	50	µs
Communication Data Rate	D_{RATE}	100	–	200	kbps
Loss of Signal Reset Time[9] Maximum Time for BUSIN to Be Below Frame Threshold	t_{TO}	2.0	–	4.0	ms
ADC Code Conversion Time[10]	t_{ADC}	–	–	20	µs
BUSIN Response Current Slew Rate					mA/µs
1.0mA to 9.0mA Transition Rise	t_{ITR_R}	–	–	8.0	
9.0mA to 1.0mA Transition Fall	t_{ITR_F}	–	–	8.0	
BUSIN Timing to Response Current					µs
BUSIN Negative Voltage Transition = 3.0V to I_{RSP} = 7.0mA Rise	t_{RSP_R}				
T_A = -40°C		–	–	2.5	
T_A = +25°C		–	–	2.5	
T_A =+125°C		–	–	3.0	
BUSIN Negative Voltage Transition = 3.0V to I_{RSP} = 5.0mA Fall	t_{RSP_F}	–	–	2.5	
Bus Signal Duty Cycle[9]					%
Logic [0] (~ 1/3 ± 20%)	DC_L	25	33	40	
Logic [1] (~ 2/3 ± 20%)	DC_H	54	67	80	
I/O Transition Time (C_{Load} = 50pF)[9]	t_{TRIO}	–	–	100	ns
I/O Delay from Input State Change to Status Register Valid[9]	$t_{INDLYIO}$	–	–	300	ns
I/O Delay from DBUS Command to I/O Output State Change	$t_{OUTDLYIO}$	–	11.5	15	µs
Delay from I/O1 Rising Edge to ADC Value = 3F8[9]	t_{ADCDIS}	–	–	300	ns
HCAP t_{POR} Mask					µs
ON (rising edge)	$t_{PORMASKHCAP(ON)}$	2.0	5.0	9.0	
OFF (falling edge)	$t_{PORMASKHCAP(OFF)}$	1.0	3.5	8.0	
REGOUT t_{POR} Mask					µs
ON (rising edge)	$t_{PORMASKREGOUT(ON)}$	2.0	5.0	9.0	
OFF (falling edge)	$t_{PORMASKREGOUT(OFF)}$	1.0	3.5	8.0	

Notes
9. Assured by design.
10. Assured by design. Conversion is started and completed during idle time.

TIMING DIAGRAMS

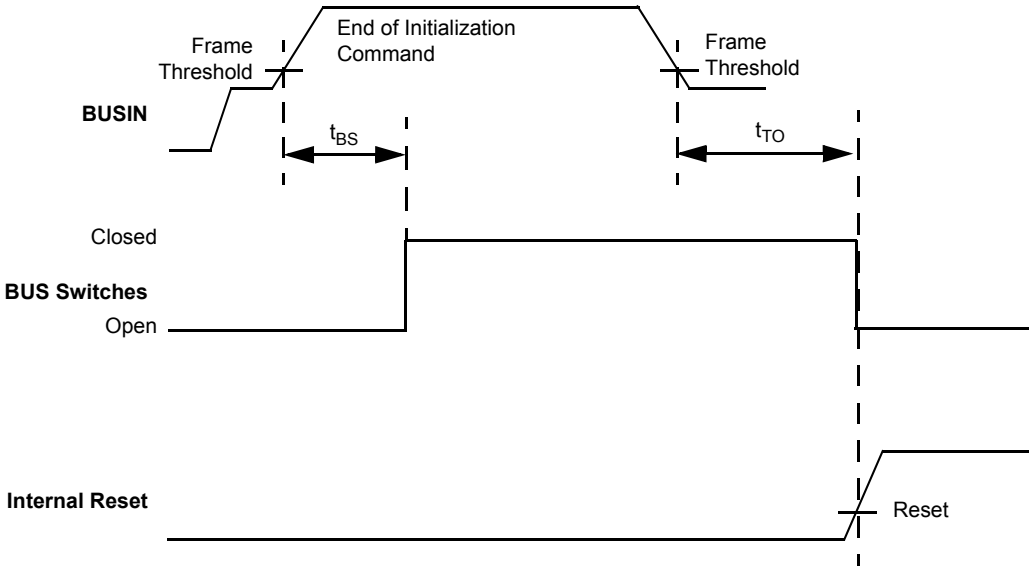


Figure 4. Bus Switch and Reset Timing

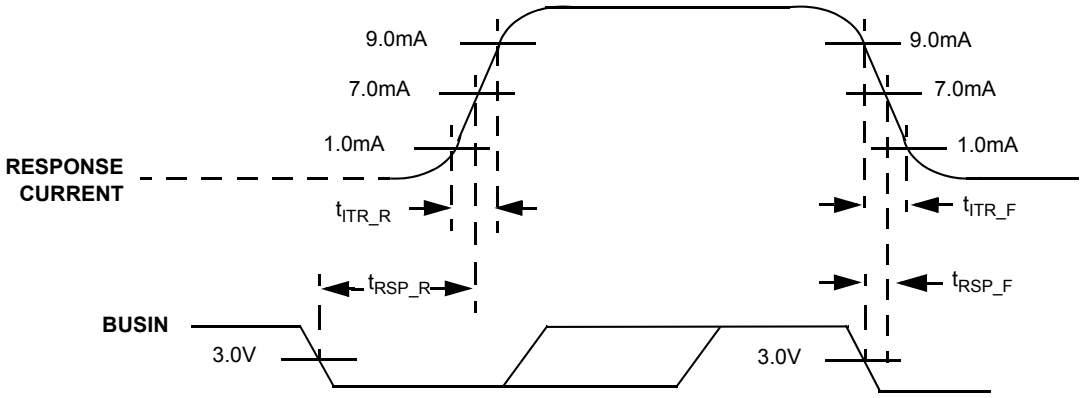


Figure 5. Response Current Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33784 is designed to be used with a sensor at a location remote from a centralized MCU. This device provides power, measurement, and communications between the remote sensor and the centralized MCU over a DSI 2.02 compliant bus. Sensors such as accelerometers can be powered from the regulated output of the device, and the resulting analog value from the sensor can be converted from an analog level to a digital value for transmission over the bus, in response to a query from the MCU. There are two analog inputs to a 10-bit analog-to-digital converter (ADC). Three I/O lines can be configured by the central MCU over the bus as digital inputs or digital outputs.

Power is passed from BUSIN through on-chip rectifiers to an external storage capacitor. The capacitor stores energy during the highest voltage excursions of the BUSIN pin (idle) and supplies energy to power the device during low excursions of BUSIN.

An under-voltage circuit provides a reset signal during low-voltage conditions and during power-up/power-down.

Data from the Central Control Unit (CCU) is applied to the BUSIN pin as voltage levels that are sensed by level detection circuitry. A serial decoder detects these transitions and decodes the incoming data. Responses are passed through a serial encoder and are transmitted via a switched current source that is slew-rate controlled.

FUNCTIONAL PIN DESCRIPTION

ANALOG GROUND (AGND)

This pin is the low reference level and power return for the analog-to-digital converter (ADC). It is internally connected to RTNIN

TEST OUTPUT (TOUT)

This output is low for normal operation and will go high when the device is placed into a test mode. See Test Mode on page 14.

IDDQ (IDDQ)

This input is used for measuring the quiescent current of the device during IC manufacturing test. This pin should be open in the application.

ANALOG INPUT (AN0, AN1)

Inputs to the analog-to-digital converter.

LOGIC I/O (I/O0, I/O1, I/O2)

These pins provide a logic level outputs or inputs.

TEST MODE ENABLE (TEST)

A high input places this device into special test mode. See Test Mode on page 14.

HOLDING CAPACITOR (H_CAP)

A capacitor attached to this pin is charged by the bus during bus idle and supplies current to run the device and for external devices via the REGOUT pin during non-idle periods.

DBUS INPUT (BUSIN)

This pin attaches to the high side of the differential bus and responds to initialization commands.

BUS RETURN IN (RTNIN)

This pin connects to the low side of the differential bus and provides the common return for power and signalling. It is internally connected to AGND.

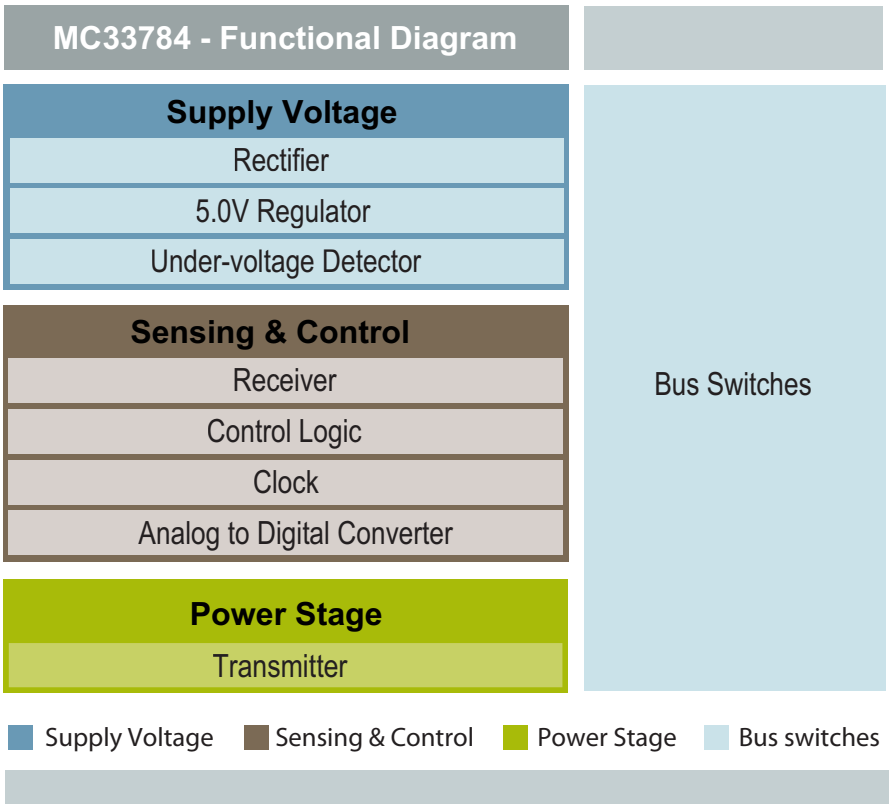
DBUS OUTPUT (BUSOUT)

This pin is the switched BUSIN signal and is connected to the BUSIN pin of the next device in the daisy chain.

BUS RETURN OUT (RTNOUT)

This pin is the switched RTNIN signal and is connected to the RTNIN pin of the next device in the daisy chain.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



Functional Internal Block Diagram

SUPPLY VOLTAGE

RECTIFIER

There is an on-chip rectifier, which allows power and communications to be delivered to the 33784 over the bus. The rectifier lies between BUSIN and H_CAP. During the idle state of the bus, the rectifier allows the bus to charge an external storage capacitor attached to H_CAP. During signaling, the rectifier isolates H_CAP from the bus to prevent the bus from draining the external capacitor while signaling. The capacitor then supplies power to the 33784 during signaling. The signaling time and the size of the external capacitor must be selected so that the voltage on HCAP does not drop below 6.77V during signaling.

5.0V REGULATOR

An on-chip 5V regulator supplies internal power for the 33784 and also supplies power to external devices, such as accelerometers via the REGOUT pin. A bypass capacitor is required on the REGOUT pin to keep the regulator stable. All current supplied by the regulator is derived from the external capacitor attached to H_CAP.

UNDER-VOLTAGE DETECTOR

The under-voltage detector issues a power-ON reset (POR) signal during power-up and power-down of the 33784. It also monitors the voltage on HCAP and REGOUT and issues a reset when either of these pins fall below their respective POR thresholds. The reset signal is filtered to prevent glitches on HCAP or REGOUT from causing an erroneous reset. Any time the 33784 is reset, the device will need to be re-initialized before it will respond to further commands.

LOGIC AND CONTROL

RECEIVER

The receiver detects the voltage on BUSIN and senses when the bus is idle and when it is signaling. Communication on the bus always begins when the voltage on BUSIN drops below the frame threshold. This change from idle mode to signal mode is sensed by the receiver and is interpreted as the start of an incoming word.

The first bit in the word begins when the bus voltage drops below the Signal threshold. This starts a counter in a serial decoder, which essentially measures the amount of time that the bus voltage is below the signal threshold. When the bus

voltage rises above the signal threshold, the counter measures the time the bus is above the signal threshold. When the bus voltage falls below the signal threshold again, the first bit is finished and the next bit begins. The process is repeated for each bit in the command.

The decoder interprets the bit as a logic [0] if the bus spent more time below the signal threshold than above it. Conversely, the decoder interprets the bit as a logic [1] if the bus spent more time above the signal threshold than below it. The advantage to this method of communication is that it will accept data over a wide range of data rates and it is not dependent on an accurate clock. A logic [0] is typically indicated by spending 2/3 of the total bit time low, and a logic [1] is typically indicated by spending 2/3 of the total bit time high.

The command ends when the bus voltage rises above the frame threshold and returns to the idle state.

Each threshold comparator has hysteresis to help to filter noise on the bus during the transitions. There is also a filter, which issues a reset if the bus remains below the frame threshold for longer than the timeout limit. This allows the 33784 to reset itself if the connection to the Master IC is lost, or if power is removed from the system, or if a short-to-analog ground condition exists on one of the bus pins and the bus switch is closed.

CONTROL LOGIC

The control logic performs the digital operations carried out by this device. Its principle functions include:

- Decoding input instructions
- Controlling the general purpose I/O in response to BUSIN commands
- Controlling A/D conversions
- Forming response words
- Capturing and storing addresses
- Controlling the bus switch (BS)
- Resetting the device on power-up
- Reading the general purpose I/O logic values and responding to requests for these values
- Generating a cycle redundancy check (CRC) for the received data and transmitted data in conformance with the DBUS standard

Additionally, the control logic performs error checking on the received data. If errors are found, no action is taken and no response is made. Errors include:

- CRC received doesn't match CRC of received data
- Number of received bits doesn't match required bit count

See Figure 6 for the Control Logic Block Diagram

CLOCK

An internal 10 MHz oscillator provides the clock for all logic and timing functions in the IC. The signaling system and all internal operations are such that no external precision timing device is needed in the normal operation of the 33784.

An LFSR-based PRBS is clocked by the oscillator and generates a random bitstream that dithers the oscillator via a switch. Dither on the clock creates a spread spectrum for noise improvement.

ANALOG-TO-DIGITAL CONVERTER

The ADC has 10-bit resolution. It uses REGOUT as a full-scale reference voltage and AGND for a zero-level reference. The ADC uses the on-chip oscillator for sequencing.

The analog voltage on AN0 or AN1 is converted to a digital value in response to the Request AN0 or Request AN1 commands on the bus. Only the Request ANn commands will trigger a new conversion. The requested bits will be transmitted during the next command sent on the bus.

To prevent inaccurate reporting near analog ground and the supply rail, the ADC will only report digital values between hex 0020 and 03E3. Any analog voltage that would result in a digital value below 0020 will be reported as 0020. Likewise, any voltage that would result in a value above 03E3 will be reported as 03E3. The only time the ADC will report a value outside the range of hex 0020:03E3 is when an error occurs during the analog conversion inside the IC. In this case, the error code 03F8 will be reported. This is summarized in Table 5, page 14.

The ADC is also designed to report an error depending on the state of I/O1. If I/O1 is configured as an input and is set high when the conversion takes place, then the ADC will always report the error code 03F8. If I/O1 is low when the conversion takes place, then the ADC will report the converted digital value as described above. If I/O1 is configured as an output, then the state of I/O1 is irrelevant and the ADC will always report the converted digital value, as described above.

POWER STAGE

TRANSMITTER

At the same moment the receiver detects incoming commands by sensing the voltage on the bus, the transmitter replies by changing the current flowing in the bus. Each time the bus voltage falls below the signal threshold to start a new incoming bit, the transmitter switches a fixed current source on or off. A logic [1] is indicated if the current source is switched on during the bit time. A logic [0] is indicated if the current source is switched off during the bit time.

The current source is always switched off while the bus is idle.

As the response current is switched on and off, the transitions are slew-rate limited to reduce EMI. Without the slew control, the fast transitions could generate higher frequency harmonics, that could interfere with receivers tuned to frequencies well above the data rate of this device.

BUS SWITCHES

A high side bus switch lies between BUSIN and BUSOUT and a low side bus switch lies between RTNIN and RTNOUT. These switches can be opened or closed via commands on the bus. The bus switch facilitates the daisy chain operation of the 33784. When the switch is open, BUSIN is isolated from BUSOUT, RTNIN is isolated from RTNOUT, and any communication that is seen on one pin will not be transmitted to the other. In this way, the CCU can initialize the first 33784 or any other slave device in the daisy chain and program an address into it.

Once the first device in the daisy chain is initialized, the bus switches can be closed, effectively shorting BUSIN to BUSOUT, and RTNIN to RTNOUT. Now all communication that is seen on one pin will be passed to the other. The Master IC can send a command through the initialized device to the next un-initialized device in the daisy chain. The process is repeated until every device in the daisy chain has been initialized with a unique address.

Once a device' bus switches are closed they remain closed except for the following conditions:

- reception of a CLEAR command

- bus lines remain below the frame threshold for longer than the bus timeout period in which case the device will reset and the bus switches will open.

- HCAP or V_{REG} decay below the POR threshold for a time exceeding the POR Mask time in which case the device will reset and the bus switches will open.

Once the bus switches open they can only be closed again with an initialization command.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

INPUT/OUTPUT PINS

There are three I/O pins on the 33784 that can serve as either logic inputs or logic outputs. At power-up or after a Clear Command, the pins default to inputs. They can be individually configured as outputs as needed via the I/O Control Command on the bus.

Table 5. 10-Bit ADC Value Mapping

Hex	Description
03FF	Prohibited
. . .	. . .
03F9	Prohibited
03F8	Error Code
03F7	Prohibited
. . .	. . .
03E4	Prohibited
03E3	G Range
. . .	. . .
0020	G Range
001F	Prohibited
. . .	. . .
0000	Prohibited

Table 6. 8-Bit ADC Value Mapping

Hex	Description
FF	Prohibited
FE	Error Code
FD	Prohibited
. . .	. . .

Table 6. 8-Bit ADC Value Mapping

Hex	Description
FA	Prohibited
F9	Prohibited
F8	G Range
. . .	. . .
08	G Range
07	Prohibited
. . .	. . .
02	Prohibited
01	Prohibited
00	Prohibited

ADDRESSING

The 33784 may be connected in a daisy chain to other DBUS devices. If this device is connected in a daisy chain, then it will receive its 4-bit address during initialization on the bus.

TEST MODE

The 33784 can be configured in a special test mode for evaluation purposes. The test mode can only be entered if all of the following conditions are true:

- The TEST1 pin is at a logic high level
- The correct test mode command is sent to the device on the bus
- One of the internal test mode registers is accessed

Accessing the test mode registers and writing different values to them can change the behavior of many of the pins on the device, including the TOUT pin, which is only active in test mode. The test mode can be intermixed with other bus commands to evaluate the behavior of internal circuit blocks.

To prevent accidental activation of the test mode, the TEST1 pin should be tied externally to AGND. The TOUT pin should be grounded when not in TEST mode.

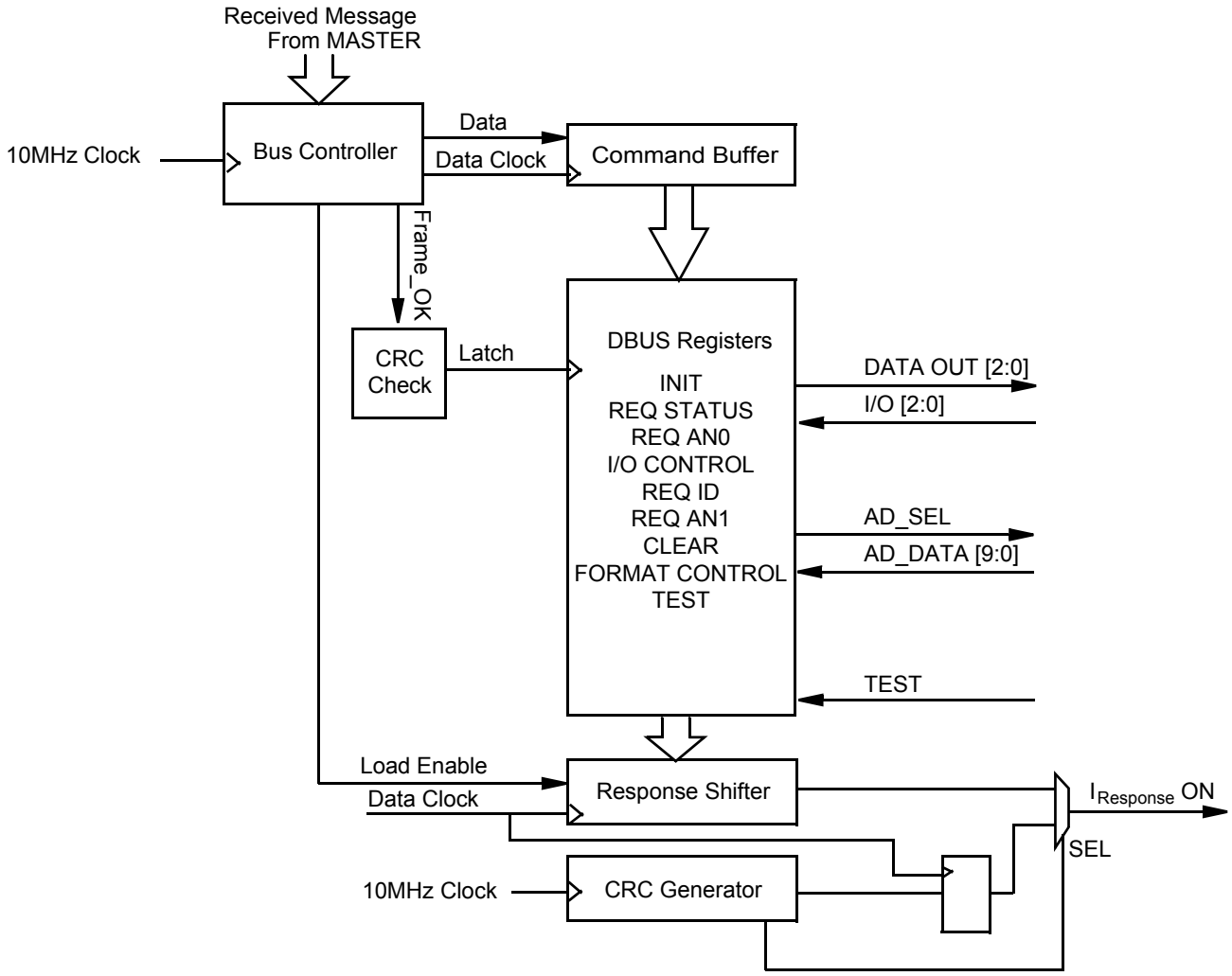


Figure 6. DBUS Slave Logic Block Diagram

COMMUNICATION FORMAT

DBUS messages are composed of individual words separated by a frame delay. Transfers are full duplex. Command messages from the master occur at the same time as responses from the slaves. Slave responses to commands occur during the next command message. This allows slaves time to decode the command, retrieve the information, and prepare to send it to the master. A bus traffic example is shown in Figure 7.

The example shows three commands separated by the minimum frame delay followed by a command after a longer delay.

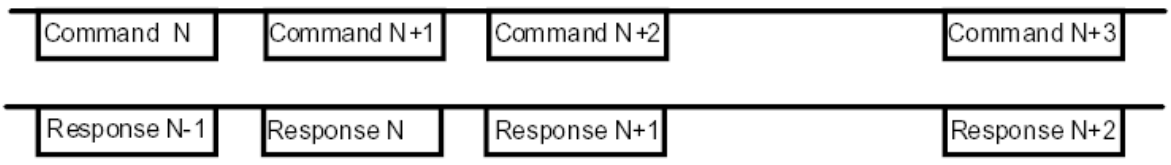


Figure 7. Bus Traffic Example

In case there is a bus error (due to induced noise or a bus fault), both the master and slave devices will likely read bad data. The slave reacts to bad data by not sending a response during the next frame, and clears the any pending response. The master will detect a CRC error (if enabled) once it receives the corrupted data sent by the slave, and once again when the slave fails to respond. This is illustrated in Figure 8.

When this error occurs, the system software needs to acknowledge this condition and resend a command of the same size so that it can receive the proper response.

Failure to take corrective action will result in unintended errors as shown in Figure 8. In this case, the master will miss Responses N and N+1.

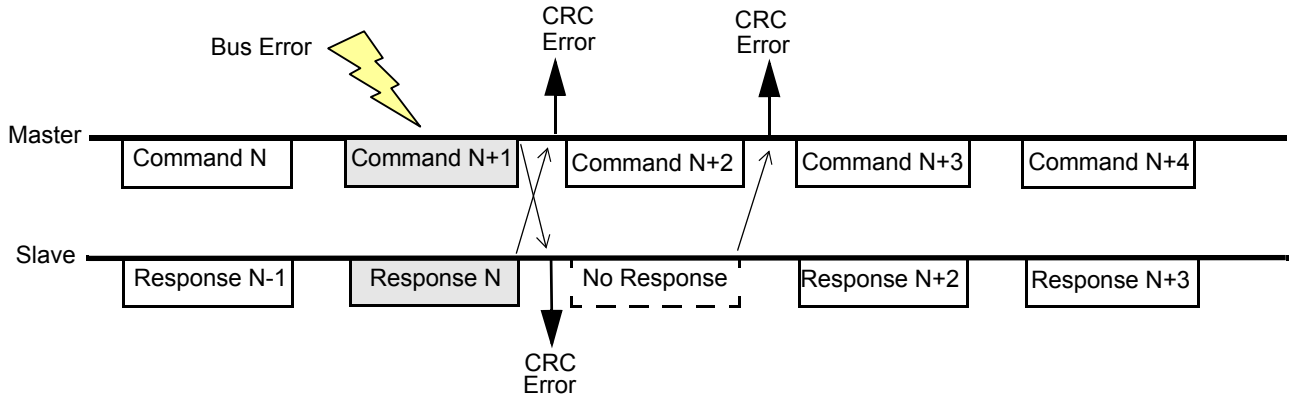


Figure 8. Bus Traffic With Receive Error and Recovery

STANDARD DBUS COMMAND STRUCTURE

Two word sizes are available for standard DBUS commands. These are termed “long word” and “short word”. A standard long word always consists of 8 data bits, 4 address bits, 4 command bits, and 4 cyclic redundancy check (CRC) bits. The data bits are always sent first, starting with the MSB, and are followed by the address bits, then the command bits, and ending with the CRC bits. Refer to Table 7, page 17.

A standard short word consists of 4 address bits, 4 command bits, and 4 CRC bits. The address bits are always sent first, starting with the MSB, followed by the command bits, and ending with the CRC bits. This is also shown in Table 7.

Some commands can be sent in either standard long word or standard short word format as desired. If these commands are sent in long word format, the data bits are “don’t-care” for the 33784, but should all be set to 0 to maintain future compatibility.

When a standard long word or short word is sent on the bus, the 33784 will calculate a CRC as each bit is received. The CRC is calculated using the polynomial X^4+1 and seed 1010. The polynomial and seed cannot be changed when communicating in standard mode. At the conclusion of the transmission, the 33784 will compare the calculated CRC with the CRC included within the message. If the two match, the message is considered valid and the 33784 will act on the message accordingly. If the calculated CRC does not match the CRC included within the message, the 33784 will ignore the transmission and the message will be discarded.

ENHANCED DBUS COMMAND STRUCTURE

In addition to standard DBUS commands, the 33784 can accept enhanced DBUS commands. Like standard commands, there are two word sizes available for enhanced commands. These, like the standard long word, are termed “enhanced long word” and “enhanced short word”. An enhanced long word always consists of 8 data bits, 4 address bits, 4 command bits, and 4 CRC bits. The data bits are always sent first, starting with the MSB, and are followed by the address bits, then the command bits, and ending with the CRC bits. Refer to Table 7.

However, an enhanced long word differs from a standard long word in that the CRC polynomial and seed are not fixed and can be programmed into the IC via the bus. The method of programming the polynomial and seed is discussed in Format Control Command and Response, page 23.

Likewise, enhanced short words will also use the polynomial and seed that have been programmed into the IC. Enhanced short words consist of 0 or 2 data bits, 4 address bits, 4 command bits, and 4 CRC bits. The data bits (if any) are sent first, followed by the address bits, followed by the command bits, and ending with the CRC bits. This is shown in Table 7. The optional data bits are only place holders and are used so that longer responses can be transmitted. If the optional data bits are used, they are “don’t-care” for the 33784, but should both be set to 0 to maintain future compatibility.

Some commands can be sent in either enhanced long word or enhanced short word format as desired. If these commands are sent in enhanced long word format, the data bits are “don’t-care” for the 33784, but should all be set to 0 to maintain future compatibility.

When an enhanced long word or short word is sent on the bus, the 33784 will calculate a CRC as each bit is received. The CRC is calculated using the polynomial and seed that have been programmed into the IC via the bus. At the conclusion of the transmission, the 33784 will compare the calculated CRC with the CRC included within the message. If the two match, the message is considered valid and the 33784 will act on the message accordingly. If the calculated CRC does not match the CRC included within the message, the 33784 will ignore the transmission and the message will be discarded.

Table 7. Standard and Enhanced DBUS Command Structure

Word Type	Symbol	First				Data				Address				Command				CRC			Last
Standard Long Word	LW	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0
Enhanced Long Word	ELW	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0
Standard Short Word	SW									A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0
8-Bit Enhanced Short Word	8-Bit ESW									A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0
10-Bit Enhanced Short Word	10-Bit ESW							D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0

Table 8. Standard and Enhanced DBUS Response Structure

Word Type	Symbol	First							Response									CRC			Last
Standard Long Word	LW	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0
Enhanced Long Word	ELW	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0
Standard Short Word	SW									D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0
8-Bit Enhanced Short Word	8-Bit ESW									D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0
10-Bit Enhanced Short Word	10-Bit ESW							D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0

STANDARD DBUS RESPONSE STRUCTURE

There are two standard response lengths to correspond with the two standard command word lengths. A standard long response always consists of 16 data bits and 4 CRC bits. A standard short response always consists of 8 data bits and 4 CRC bits. Refer to Table 8.

In both cases, the data bits are sent first, starting with the MSB, and are followed by the CRC bits. The CRC bits are calculated from the data bits using the standard polynomial X^4+1 and seed 1010. The polynomial and seed cannot be changed when responding in standard mode.

Normally, standard long responses will be sent for standard long commands, and standard short responses will be sent for standard short commands. However, if a long command is followed by a short command, then the response to the long command will occur during the short command and will be truncated. In this case, the response to the long command is considered invalid.

Similarly, if a short command is followed by a long command, then the response to the short command will occur during the long command and will contain extra bits. In this case the response to the short command is considered invalid.

ENHANCED DBUS RESPONSE STRUCTURE

There are two enhanced response lengths to correspond with the two enhanced command word lengths. Like the standard long word, an enhanced long response always consists of 16 data bits and 4 CRC bits. The data bits are sent first, starting with the MSB, and are followed by the CRC bits. The CRC bits are calculated from the data bits using the polynomial and seed that was programmed into the IC via the bus.

An enhanced short response consists of either 8 or 10 data bits and 4 CRC bits. The enhanced short response will have 8 data bits if the enhanced short command did not use the optional 2 bits, and it will have 10 data bits if the enhanced short command did use the optional 2 bits.

In certain cases, the optional 2 bits might be used in the command, but due to the nature of the command, the response only contains 8 bits of data. In this circumstance, the response will be right-padded with zeros so that 10 data bits are sent, followed by the CRC.

In other cases, the optional 2 bits might not be used in the command, but due to the nature of the command, the response contains 10 bits of data. In this circumstance, the 2 least significant bits of the response data will be dropped and only the 8 most significant data bits are sent, followed by the CRC. This is illustrated in logic Commands and Registers, page 18.

Normally enhanced long responses will be sent for enhanced long commands, and enhanced short responses will be sent for enhanced short commands of the same length. If an enhanced long word is sent after an enhanced short word, or an enhanced short word is sent after an enhanced long word, or two enhanced short words of different lengths are sent in succession, then the first response will have a different length than the second command, and therefore the first response will be invalid.

LOGIC COMMANDS AND REGISTERS

INTRODUCTION

The following sections describe in detail each of the commands that can be sent to the 33784. All of these commands can be sent in long-word format (standard or enhanced). Some of the commands can be sent in short-word format (standard or enhanced), but not all. Refer to the table in each section for the available formats for each command. The responses for each command can also be found in the tables. The 4-bit CRC, which is appended to every command and every response, has been omitted.

Many commands have “don't-care” bits, which can be set to 0 or 1 without affecting the command. Although the 33784 will respond the same in either case, it is recommended that all “don't-care” bits be set to 0 to maintain future compatibility.

INITIALIZATION COMMAND AND RESPONSE (BUSIN INPUT ONLY)

Following power-up or after a POR has occurred, the Initialization Command must be sent to the 33784 before it will respond to other commands. The command format is found in Figure 9.

The Initialization Command may be used to initialize a daisy chain device. The Initialization Command is sent to address zero. The command will be received by the next daisy chain device with its bus switch open. Reception of this command will assign the device address and close the bus switch if the BSH and BSL bits are logic [1]

Once a device has received an Initialization Command, it will ignore further initialization commands unless it has received a clear command or undergone a power-ON reset.

The response is sent during the next message following a valid Initialization Command to the addressed device. The response is shown in Figure 9. Because this is a long-word only command, there is no short word response. The BSH and BSL bits returned are the same as the bits sent in the command. The Request Status command can be used to find the logic commanded state of the bus switches.

Data								Address				Command				Word Type
–	BSH	BSL	OD	PA3	PA2	PA1	PA0	A3	A2	A1	A0	0	0	0	0	LW
								Not Valid								SW & ESW (8-bit)
								Not Valid								ESW (10-bit)

Response																Word Type
A3	A2	A1	A0	0	0	0	0	0	BSH	BSL	0	PA3	PA2	PA1	PA0	LW
								No Response								SW & ESW (8-bit)
								No Response								ESW (10-bit)

Legend

A[3:0] = Address bits. The slave address.

An address value of 0000 is ignored by all devices (no initialization, no bus switch closure, and no response)

BSH = High Side Bus Switch Position (1 = closed).

BSL = Low Side Bus Switch Position (1 = closed).

“–” = Don’t care bit. Can be 0 or 1.

PA[3:0] = Bus address to set the device to.

An address value of 0000 is ignored by all devices (no initialization, no bus switch closure, and no response)

OD = Oscillator dither:

0 = no dither (default)

1 = dither

Figure 9. Initialization Command Response Format

REQUEST STATUS COMMAND AND RESPONSE

This command causes the addressed device to return the status of the BSH and BSL bits and the logic levels of the I/O. The command format is found in Figure 10.

The 33784 will only act on this command if the address bits in the command match the address that the device was initialized with. If the addresses do not match, the device will do nothing and no response will be generated.

The response is sent during the next message following a valid Request Status command to the addressed device. Because this is a long-word only command, there is no short-word response.

The I/O bits reflect the logic states of the I/O pins. These states are latched into an internal register after the Request Status command is received (approximately TBD µs after the bus rises above the frame threshold), and are held until the response is transmitted. Any activity that occurs on the I/O pins after the states are latched will be ignored.

Data								Address				Command				Word Type
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	0	0	1	LW & ELW
								Not Valid								SW & ESW (8-bit)
								Not Valid								ESW (10-bit)

Response																Word Type
A3	A2	A1	A0	0	0	0	0	0	BSH	BSL	0	0	IO2	IO1	IO0	LW & ELW
								No Response								SW & ESW (8-bit)
								No Response								ESW (10-bit)

Legend

A[3:0] = Address bits. The address of the selected device. An address value of 0000 is ignored by all devices.

BSH = High Side Bus switch position (1 = closed).

BSL = Low Side Bus switch position (1 = closed).

"–" = Don't care bit. Can be 0 or 1.

IO[2:0] = Values at logic I/Os.

Figure 10. Request Status Command and Response Format

REQUEST AN0 COMMAND AND RESPONSE

This command causes the analog voltage on the AN0 pin to be measured and converted by the on-chip 10-bit ADC. The approximate timing for the conversion following this command is shown in Figure 11. The response to this command depends on the format in which the command was sent. The sensor data is sent in the format shown in Table 10.

The 33784 will only act on this command if the address bits in the command match the address that the device was initialized with. If the addresses do not match, the device will do nothing and no response will be generated.

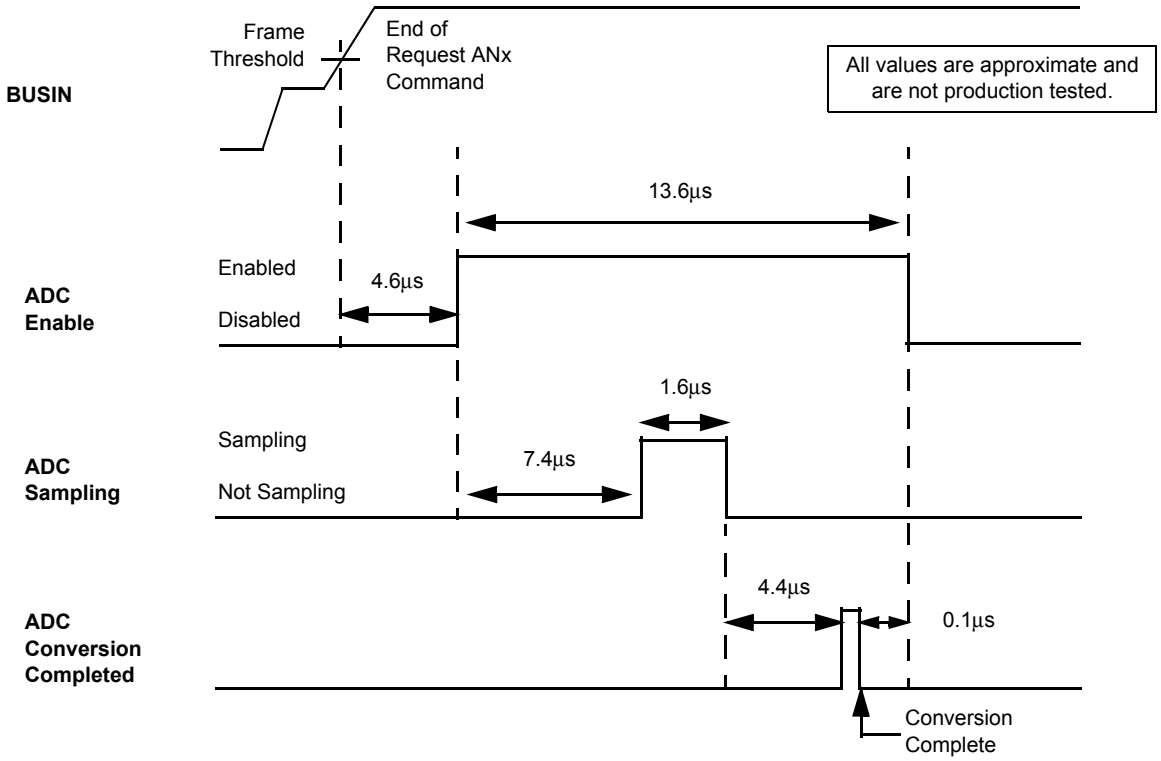


Figure 11. Approximate ADC Conversion Timing

Data								Address				Command				Word Type
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	0	1	0	LW & ELW
								A3	A2	A1	A0	0	0	1	0	SW & ESW (8-bit)
						–	–	A3	A2	A1	A0	0	0	1	0	ESW (10-bit)

Response																Word Type
A3	A2	A1	A0	0	0	0	0	B9	B8	B7	B6	B5	B4	B3	B2	LW & ELW
								B9	B8	B7	B6	B5	B4	B3	B2	SW & ESW (8-bit)
						B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	ESW (10-bit)

Legend

A[3:0] = Address bits. The address of the selected device. An address value of 0000 is ignored by all devices.

B[9:0] = Measured value.

"–" = Don't care bit. Can be 0 or 1.

Figure 12. Request AN0 Command and Response Format

REQUEST AN1 COMMAND AND RESPONSE

This command causes the analog voltage on the AN1 pin to be measured and converted by the on-chip 10-bit ADC. The approximate timing for the conversion following this command is shown in Figure 11, page 20. The response to this command depends on the format in which the command was sent. The sensor data is sent in the format shown in Figure 12.

The 33784 will only act on this command if the address bits in the command match the address that the device was initialized with. If the addresses do not match, the device will do nothing and no response will be generated.

Data								Address				Command				Word Type
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	0	1	LW & ELW
								A3	A2	A1	A0	0	1	0	1	SW & ESW (8-bit)
						–	–	A3	A2	A1	A0	0	1	0	1	ESW (10-bit)

Response																Word Type
A3	A2	A1	A0	0	0	0	0	B9	B8	B7	B6	B5	B4	B3	B2	LW & ELW
								B9	B8	B7	B6	B5	B4	B3	B2	SW & ESW (8-bit)
						B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	ESW (10-bit)

Legend

A[3:0] = Address bits. The address of the selected device. B[9:0] = Measured value.

An address value of 0000 is ignored by all devices.

"–" = Don't care bit. Can be 0 or 1.

Figure 13. Request AN1 Command and Response Format

I/O CONTROL COMMAND AND RESPONSE

This command can be used to configure the direction of the I/O pins, and force their states if configured as outputs. Refer to Figure 14 for the command and response format.

The response is sent during the next message following a valid I/O Control command to the addressed device. Because this is a long-word only command, there is no short word response.

The direction (DR) bits are used to specify the direction (input or output) of each pin independently. If the DR bit for a specific I/O pin is set to 1, then that I/O pin will be an output and the state of the level (Lx) bit will determine whether the pin is driven high or low. If the DR bit for a specific I/O pin is set to 0, then that pin will be an input and the Lx bit in the command will have no affect on the state of the pin.

In the response to the I/O Control Command, the DR bits will show the direction that the pins were programmed. The Lx bits will have the values that were set in the command. These values may not reflect the actual states of the pins. To obtain the accurate states of the pins, the Request Status Command should be used.

The 33784 will only act on the I/O Control Command if the address bits in the command match with the address that the device was initialized. If the addresses do not match, the device will do nothing and no response will be generated.

Address '0000' is a global command. All slaves in the signal path will configure their I/O pins according to the state of the data bits. No response results from the I/O control global command.

Data								Address				Command				Word Type
–	L2	L1	L0	–	DR2	DR1	DR0	A3	A2	A1	A0	0	0	1	1	LW & ELW
								Not Valid								SW & ESW (8-bit)
								Not Valid								ESW (10-bit)

Response																Word Type
A3	A2	A1	A0	0	0	0	0	0	L2	L1	L0	0	DR2	DR1	DR0	LW & ELW
								No Response								SW & ESW (8-bit)
								No Response								ESW (10-bit)

Legend

A[3:0] = Address bits.

DR[2:0] = I/O direction bits. 1 = Output. All bits are set to 0 by reset/clear.

"–" = Don't care bit. Can be 0 or 1.

L[2:0] = Level to output on I/O if configured as outputs.

Figure 14. I/O Control Command and Response Format

REQUEST ID COMMAND AND RESPONSE

This command will cause the device ID information to be read from internal storage and returned to the master. The command format is found in Figure 15.

The response is sent during the next message following a valid Request ID command to the addressed device.

Because this is a long-word only command, there is no short word response.

The 33784 will only act on this command if the address bits in the command match with the address that the device was initialized. If the addresses do not match, the device will do nothing and no response will be generated.

Data								Address				Command				Word Type
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	0	0	LW & ELW
								Not Valid								SW & ESW (8-bit)
								Not Valid								ESW (10-bit)

Response																Word Type
A3	A2	A1	A0	0	0	0	0	V3	V2	V1	V0	0	0	0	FPAR	LW & ELW
								No Response								SW & ESW (8-bit)
								No Response								ESW (10-bit)

Legend

A[3:0] = Address bits. The address of the selected device. An address value of 0000 is ignored by all devices.

"–" = Don't care bit. Can be 0 or 1.

V[3:0] = Device version number. The silicon version number of the device. V0 always = 0, indicating MC33784

FPAR = Some parameters in the device are trimmed by fuses. Since these parameters can be impacted by the state of the fuses a fuse parity is calculated and stored during device manufacturing. When the device is powered up the current fuse parity is checked against the stored parity. If they do not match this bit is set.

Figure 15. Request ID Command and Response Format

CLEAR COMMAND AND RESPONSE

This command will open the bus switch and reset all registers to the reset state. The command format is found in Figure 16. No response is generated for the clear command.

The 33784 will only act on this command if the address bits in the command match the address that the device was initialized with, or if the address bits are 0000.

Data								Address				Command				Word Type
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	1	1	LW & ELW
								A3	A2	A1	A0	0	1	1	1	SW & ESW (8-bit)
						–	–	A3	A2	A1	A0	0	1	1	1	ESW (10-bit)

Response	Word Type
No Response	LW & ELW
No Response	SW & ESW (8-bit)
No Response	ESW (10-bit)

Legend

A[3:0] = Address bits. The address of the selected device.
An address value of 0000 clears all devices.

"–" = Don't care bit. Can be 0 or 1.

Figure 16. Clear Command Format and Response Format

FORMAT CONTROL COMMAND AND RESPONSE

This command allows the short-word length, the CRC polynomial, and the CRC seed to be changed. It is also the command needed to switch the device from the "standard" mode to the "enhanced" mode.

The response is sent during the next message following a valid Format Control command to the addressed device. Because this is a long-word only command, there is no short word response.

On power-up or following a "Clear" command, the device uses the standard DSI short-word length (8 data bits) and standard CRC polynomial ($x^4 + 1$) and seed (1010).

The registers associated with Format Control default to values that correspond to Standard DBUS operation upon power-up, or at the issuance of a "Clear" command.

Changes made to the Format Control Register do not become active until the 4 bits of the format selection register are set during a single write command. It will not switch back to Standard DBUS settings unless all 4 bits of the format selection register are cleared by a single write.

Any attempts to change the format will be ignored while in the enhanced mode.

The Format Control command is a long-word Command and contains 8 bits of data which are used to determine read or write, the specific format control register, and the data to be written/read. The format for this command is defined in Figure 17.

If the R/W bit is set, the value in the Data Bits will be written to the format control register pointed to by the 3-bit format register address. If the R/W bit is clear, the bits in the register pointed to by the format register address will not be changed, but the values in it will be returned in the following response from the device. No data can be written to the reserved registers.

The response to this command will be the data that was written/read by the command. Attempts to write to the reserved registers will return zeros in the data bits of the response.

The 33784 will only act on the Format Control Command if the address bits in the command match the address that the device was initialized with. If the addresses do not match, the device will do nothing and no response will be generated. The only exception is the global address of 0000. If the address bits in the command are 0000, the 33784 will perform all normal functions associated with the command, but no response will be generated.

Data								Address				Command				Word Type
R/W	ADD R2	ADD R1	ADD R0	Data 3	Data 2	Data 1	Data 0	A3	A2	A1	A0	1	0	1	0	LW & ELW
								Not Valid								SW & ESW (8-bit)
								Not Valid								ESW (10-bit)

Response																Word Type
A3	A2	A1	A0	0	0	0	0	R/W	ADD R2	ADD R1	ADD R0	DAT A3	DAT A2	DAT A1	DAT A0	LW & ELW
								No Response								SW & ESW (8-bit)
								No Response								ESW (10-bit)

Legend

A[3:0] = Address bits. The address of the selected device.

R/W = Controls if this is a read or write. Write = 1.

ADDR[2:0] = Pointer to Format control register which is to be accessed.

DATA[3:0] = Data to read from or write to in the pointed to Format Control Register.

Figure 17. Format Control Command and Response Format

FORMAT CONTROL REGISTERS

The enhanced DSI Register locations are shown in Figure 9. The ADDR bits in the Format Control Command select the Format Control Register to which data is written or from which data is read. The data is 4 bits.

Table 9. Format Control Registers

Format Control Register Address	Description
0	CRC Polynomial
1	Reserved
2	Seed
3	Reserved
4	Reserved
5	Short-Word Data Length
6	Reserved
7	Format Selection

CRC POLYNOMIAL

The CRC Taps control the feedback for the CRC Polynomial. The MSB represents the X3 bit. The LSB represents X0 or the value 1 if set or 0 if not set. The standard DSI CRC of X^4+1 would be obtained by loading 0001 into the Format register 0. The X^4 pin is always considered on, so nothing has to be done for it. On a reset or clear, the standard DSI CRC taps are loaded into these registers.

SEED

The Seed is the starting value loaded into the CRC checking registers before each transaction starts. The default DSI seed of 1010 would be selected by loading 1010 into control register 2. On reset or clear, the standard DSI seed is loaded into this register.

SHORT-WORD DATA LENGTH

The Short-Word Data Length controls the number of bits of data in a short word. This can be set to 8 or 10. On a reset or clear, the value in this register defaults to 8. If a number other than 8 or 10 is written to the register, it is ignored and the contents of the register are not changed. The standard DSI short-word data length would be set by loading 1000 into this register.

FORMAT SELECTION

The Format selection determines whether the standard DSI values will be used or the values in the Format register. The switch to the values in the format registers occurs when 1111 is successfully written to control register 7 in a single command. If the register is currently cleared, and one of the data bits is not received as a logic [1], the data in the register will remain all zeroes and the device will not use the Format register settings. A switch back to standard DBUS occurs when a ‘0000’ is successfully written to control register 7. If the registers bits are all set, and one of the bits is received as a logic [1], the value of the bits in the register will remain 1111 and the switch back to Standard DSI values will not occur. This is done to reduce the possibility of switching operation modes due to a corrupted command. When using the Format Register settings, any command to change them, other than this register back to 0000, will be ignored.

COMMAND SUMMARY

Refer to Table 10 for a summary of the commands available in the 33784. The responses to these commands are summarized in Table 11, page 26, and Table 12, page 27. The four-bit CRC, which appended to the end of every command and every response, has been committed.

Table 10. Command Summary

Command Names		Data (LW & ELW only)								Address				Command			
Hex	**Description**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**A3**	**A2**	**A1**	**A0**	**C3**	**C2**	**C1**	**C0**
0	Initialization	–	BSH	BSL	OD	PA3	PA2	PA1	PA0	A3	A2	A1	A0	0	0	0	0
1	Request Status	–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	0	0	1
2	Request AN0	–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	0	1	0
3	I/O Control	–	L2	L1	L0	–	DR2	DR1	DR0	A3	A2	A1	A0	0	0	1	1
4	Request ID Information	–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	0	0
5	Request AN1	–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	0	1
6	Reserved	–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	1	0
7	Clear	–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	1	1
8	Reserved	–	–	–	–	–	–	–	–	A3	A2	A1	A0	1	0	0	0
9	Reserved	–	–	–	–	–	–	–	–	A3	A2	A1	A0	1	0	0	1
A	Format Control	R/W	ADDR2	ADDR1	ADDR0	DATA3	DATA2	DATA1	DATA0	A3	A2	A1	A0	1	0	1	0
B	Reserved																
C	Reserved																
D	Reserved																
E	Reserved for test																
F	Reserved	–	-	–	–	-	-	-	-	-	-	-	-	-	-	-	-

Legend

BSH = Controls closing of the High Side Bus Switch (1 = close).

BSL = Controls closing of the Low Side Bus Switch (1 = close).

DR[2:0] = Direction of I/O. 1 = Output.

L[2:0] = Level to output on I/O if configured as outputs.

"–" = Don't care bit. Can be 0 or 1.

PA[3:0] = Bus Address to set the device to.

R/W = Controls if this is a read or write. Write = 1.

ADDR[2:0] = Pointer to Format Control Register that is to be accessed.

DATA[3:0] = Data to read from or write to in the pointed to Format Control Register.

OD = Oscillator dither:

0 = no dither (default)

1 = dither

Table 11. Long Word Response Summary

	Command Name	LW & ELW															
Hex	**Description**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Initialization	A3	A2	A1	A0	0	0	0	0	0	BSH	BSL	0	PA3	PA2	PA1	PA0
1	Request Status	A3	A2	A1	A0	0	0	0	0	0	BSH	BSL	0	0	IO2	IO1	IO0
2	Request AN0	A3	A2	A1	A0	0	0	0	0	B9	B8	B7	B6	B5	B4	B3	B2
3	I/O Control	A3	A2	A1	A0	0	0	0	0	0	L2	L1	L0	0	DR2	DR1	DR0
4	Request ID Information	A3	A2	A1	A0	0	0	0	0	V3	V2	V1	V0	0	0	0	FPAR
5	Request AN1	A3	A2	A1	A0	0	0	0	0	B9	B8	B7	B6	B5	B4	B3	B2
6	Reserved	No Response															
7	Clear	No Response															
8	Reserved	No Response															
9	Reserved	No Response															
A	Format Control	A3	A2	A1	A0	0	0	0	0	R/W	ADDR2	ADDR1	ADDR0	DATA3	DATA2	DATA1	DATA0
B	Reserved	No Response															
C	Reserved	No Response															
D	Reserved	No Response															
E	Reserved for test	No Response															
F	Reserved	No Response															

Legend

A[3:0] = Address bits. The slave address.

B[9:0] = Data bits.

BSH = Status of the High Side Bus Switch (1 = close).

BSL = Status of the Low Side Bus Switch (1 = close).

DR[2:0] = I/O direction bits (1 = Output).

IO[2:0] = Logic level of I/O.

L[2:0] = Level to output on I/O if configured as outputs.

PA[3:0] = Bus address to set the device to.

V[2:0] = Version number.

R/W = Shows if last command was a read Or Write. Write = 1.

ADDR[2:0] = Pointer to Format Control Register that was accessed.

DATA[3:0] = Data in the pointed-to Format Control Register.

Table 12. Enhanced Short-Word Response Summary

Command Names		10-Bit ESW									
Hex	**Description**	**8-Bit ESW**									
0	Initialization	No Response									
1	Request Status	No Response									
2	Request AN0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
3	I/O Control	No Response									
4	Request ID Information	No Response									
5	Request AN1	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
6	Reserved	No Response									
7	Clear	No Response									
8	Reserved	No Response									
9	Reserved	No Response									
A	Format Control	No Response									
B	Reserved	No Response									
C	Reserved	No Response									
D	Reserved	No Response									
E	Reserved for test	No Response									
F	Reserved	No Response									

Legend No SW or ESW response except for commands 2 and 5

B[9:0] = Data bits.

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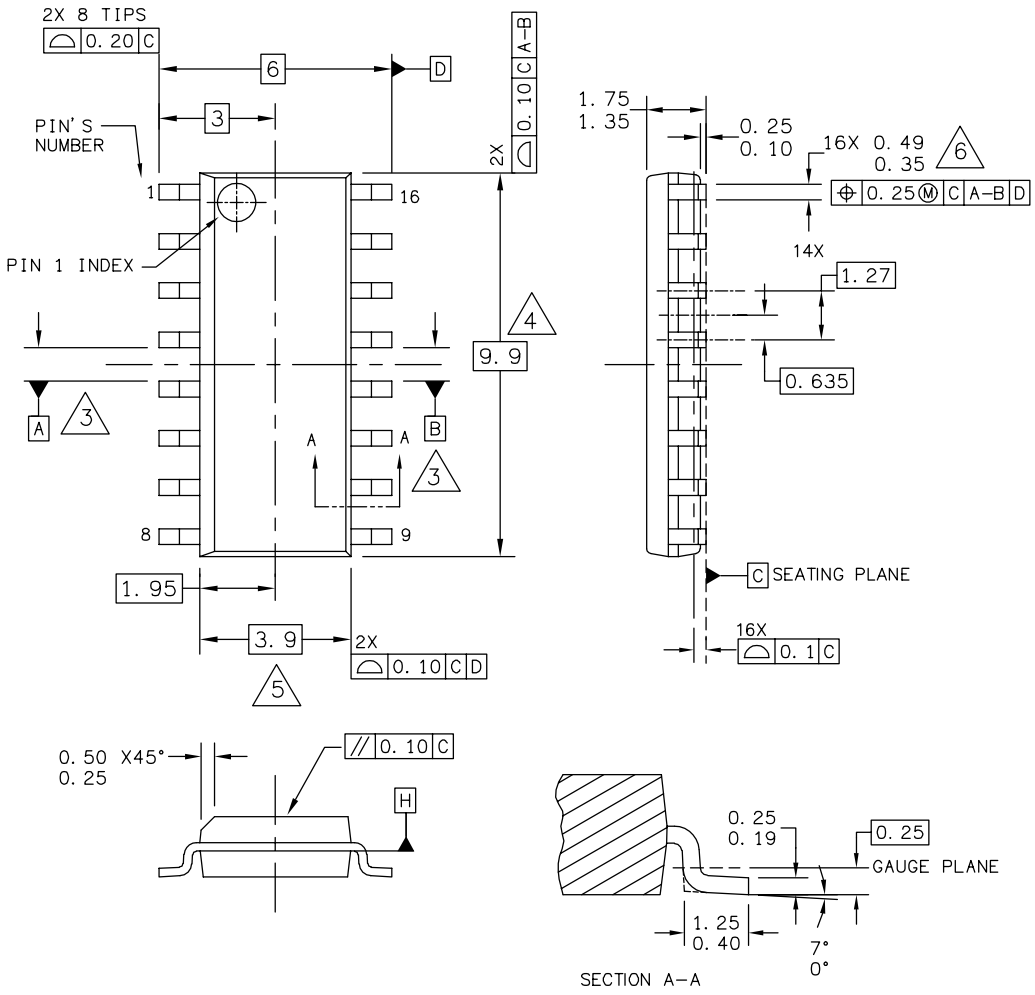

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REVISION	DATE	DESCRIPTION OF CHANGES
1.0	3/2008	• Initial Release
2.0	7/2008	• Added RoHS logo to page 1, provided t_{RSP_R} temperature parameters, page 8
3.0	11/2009	• Changed Part Number from PCZ33784EF/R2 to MCZ33784EF/R2 on page 1.

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