



# TEA1708T

## GreenChip X capacitor discharge IC

Rev. 1 — 25 September 2013

Product data sheet

## 1. General description

The TEA1708 is an automatic discharge IC for X capacitors with a low power consumption (typically 1 mW at 230 V (AC)).

A 500 V clamping circuit is integrated, protecting the IC during mains surges. In a typical application with only two 200 k $\Omega$  resistors, the maximum differential mode mains surge voltage allowed exceeds 6 kV. A metal oxide varistor is not required to protect the IC.

The X capacitor discharge current is internally limited to 2.3 mA. The discharge delay timer is set externally using a low voltage capacitor.

The very low power consumption in combination with a large discharge current enables the use of a large value X capacitor to reduce EMI while retaining the low standby power.

## 2. Features and benefits

- 1 mW power consumption at 230 V (AC)
- Integrated 500 V clamp; no metal oxide varistor required to protect the IC
- Self supplied, no external bias required
- Discharge current internally limited
- Adjustable discharge delay
- Very high differential surge: 6 kV with two 200 k $\Omega$  resistors
- Easier application design, resolving EMI issues while retaining the efficiency level

## 3. Applications

- All AC connected power supplies with X capacitors > 100 nF requiring a low load standby power.

## 4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1708T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1



5. Block diagram

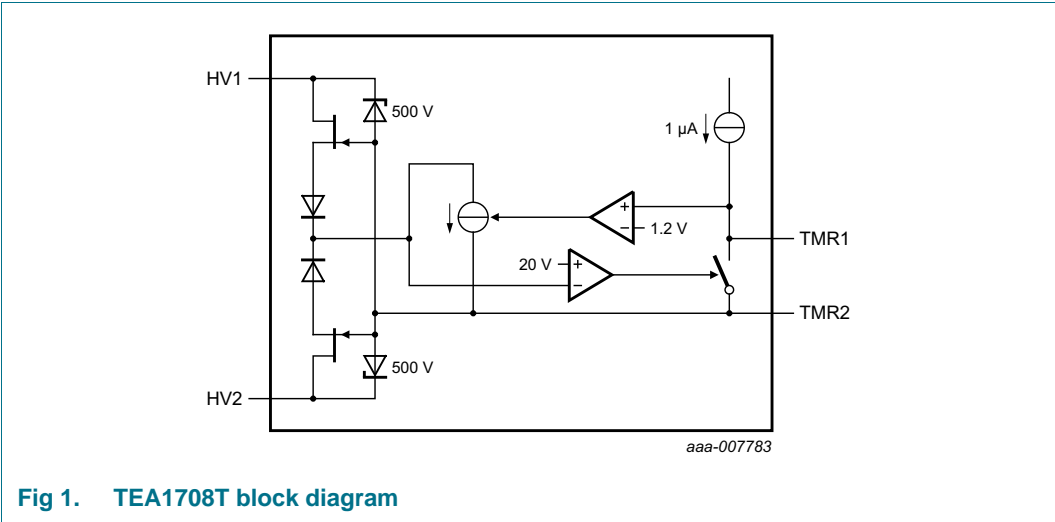


Fig 1. TEA1708T block diagram

6. Pinning information

6.1 Pinning

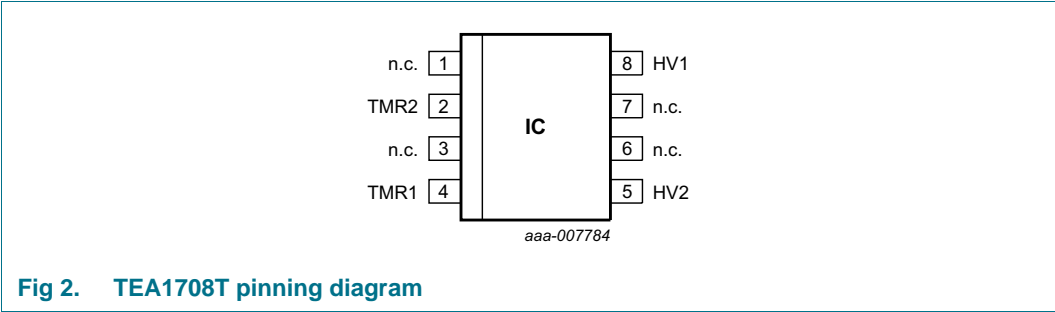


Fig 2. TEA1708T pinning diagram

6.2 Pin description

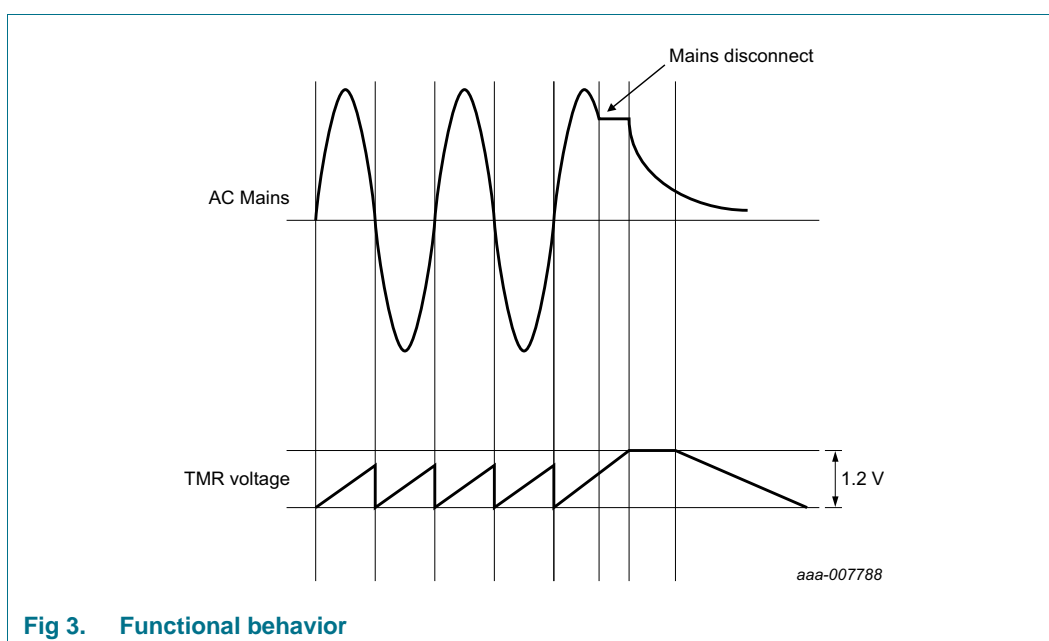
Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
TMR2	2	timer pin 2
n.c.	3	not connected
TMR1	4	timer pin 1
HV2	5	high-voltage mains connection 2
n.c.	6	not connected
n.c.	7	not connected
HV1	8	high-voltage mains connection 1

## 7. Functional description

The TEA1708 incorporates a timer and a zero-crossing mains voltage detector. If a positive or negative voltage above the threshold zero-crossing mains voltage (20 V) is applied between the high-voltage pins, the timer charges the external capacitor on the TMR1 and TMR2 pins. If the voltage between the TMR1 and TMR2 pins reaches 1.2 V, a discharge current is activated. If the voltage applied between the high-voltage pins, is below the threshold zero-crossing mains voltage, the external capacitor is discharged and the discharging stops. The discharge current is internally limited.

When an AC mains voltage is applied, the timer capacitor is charged between the mains zero crossings and discharged during the mains zero crossings. When the AC mains is disconnected and a high voltage remains on the X capacitor, the timer charges the external capacitor above its discharge activation threshold voltage point (1.2 V), switching on the internally limited discharge current of the external X capacitor.



**Fig 3. Functional behavior**

To protect the IC during mains surges, a high voltage clamping circuit is integrated. The clamping circuit is activated for > 500 V positive and negative voltages. The high-voltage pins HV1 and HV2 are fully symmetrical.

## 8. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Voltages</b>					
$V_{\text{TMR1-TMR2}}$	voltage between pin TMR1 and pin TMR2	$0 \mu\text{A} > I_{\text{dch(tmr)}} < 10 \mu\text{A}$	-0.4	+3.5	V
$V_{\text{HV1-HV2}}$	voltage between pin HV1 and pin HV2	normal operation, so no mains surge	-410	+410	V
<b>Currents</b>					
$I_{\text{HV}}$	current on pin HV	on both HV pins; $t < 2 \text{ ms}$ , during mains surge	-15	+15	mA
<b>General</b>					
$P_{\text{tot}}$	total power dissipation	$T_{\text{amb}} < 75 \text{ }^{\circ}\text{C}$	-	0.5	W
$T_{\text{stg}}$	storage temperature		-55	+150	$^{\circ}\text{C}$
$T_{\text{j}}$	junction temperature		-40	+150	$^{\circ}\text{C}$
<b>ESD</b>					
$V_{\text{ESD}}$	electrostatic discharge voltage	class 1			
		human body model; pins HV1 and HV2	[1] -	1000	V
		human body model; all other pins	-	4000	V
		charged device model; all pins	[2] -	750	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75  $\mu\text{H}$  coil and a 10  $\Omega$  resistor.

## 9. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{\text{th(j-a)}}$	thermal resistance from junction to ambient	in free air; JEDEC test board	160	K/W
$R_{\text{th(j-c)}}$	thermal resistance from junction to case	in free air; JEDEC test board	72	K/W

## 10. Characteristics

**Table 5. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>High voltage (pins HV1 and HV2)</b>						
$I_{HV}$	current on pin HV	on both HV pins; $V_{HV1} > 50\text{ V}$ ; $V_{HV2} > 50\text{ V}$				
		$V_{TMR} < 1.2\text{ V}$	2.5	3.5	4.5	$\mu\text{A}$
		current limited; $V_{TMR} > 1.2\text{ V}$	1.8	2.3	2.8	mA
$V_{clamp}$	clamp voltage		475	500	525	V
$V_{th(ch)}$	charge threshold voltage	threshold zero-crossing mains voltage	19	21	23	V
<b>Timer (pins TMR1 and TMR2)</b>						
$V_{th(act)dch}$	discharge activation threshold voltage	to discharge the X capacitor	1.1	1.2	1.3	V
$I_{dch(tmr)}$	timer discharge current		-1.20	-0.95	-0.70	$\mu\text{A}$

## 11. Application information

The TEA1708 is typically connected across the X capacitor. A metal oxide varistor is not required to protect the IC because the device incorporates a high-voltage clamping circuit. The IC is sufficiently protected for differential mode surge voltages up to 4 kV with only two 200 k $\Omega$  resistors (see [Figure 4](#)).

The discharge delay time is set externally using a low-voltage capacitor connected between the TMR1 and TMR2 pins. Select a value between 10 nF and 22 nF for a mains frequency of 50 Hz or 60 Hz. The minimum value is 10 nF which gives the smallest delay time. Do not use values < 10 nF. They can lead to unwanted discharge of the X capacitor.

The delay time ( $t_d$ ) for discharge can be calculated with [Equation 1](#):

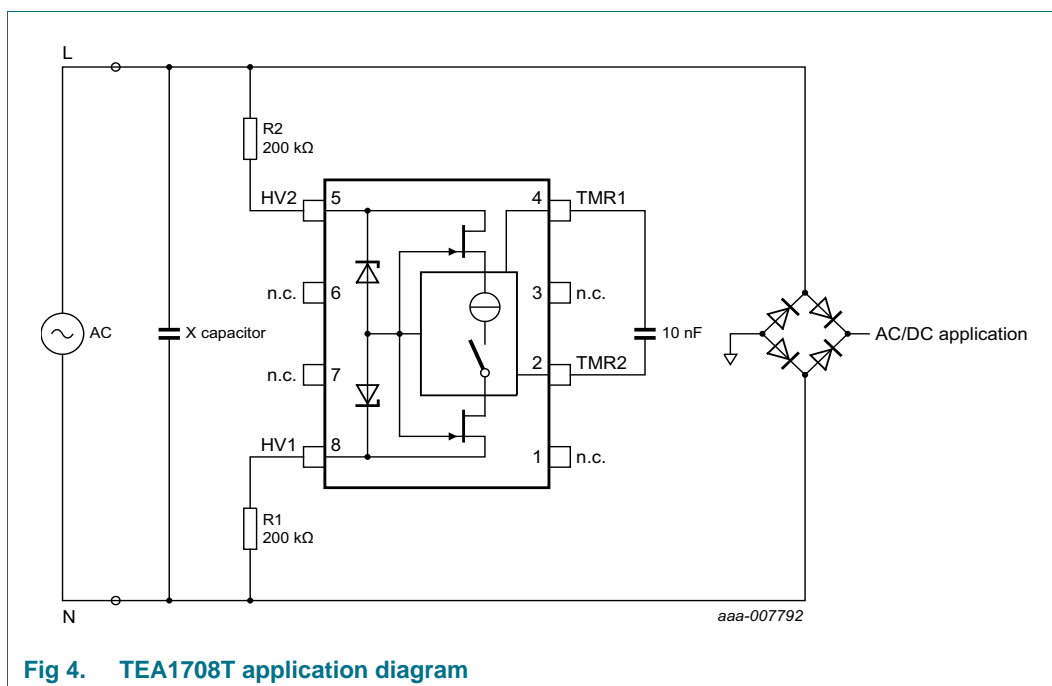
$$t_d = C_{tmr} \times \frac{V_{th(act)dch}}{I_{dch(tmr)}} \quad (1)$$

If the low-voltage capacitor value is 22 nF the delay time is:  $22\text{ nF} \times \frac{1.2\text{ V}}{I\text{ }\mu\text{A}} = 26\text{ ms}$ .

The discharge current is activated when the voltage across the device exceeds the threshold zero-crossing mains voltage. The current is limited to  $\approx 2.3\text{ mA}$ . When the current < the current limit,  $I_{HV}$  is calculated with [Equation 2](#):

$$I_{HV1} = I_{HV2} \approx \frac{V_{xcap(t)} - (V_{th(ch)} + 4\text{ V})}{(R1 + R2)} \quad (2)$$

When the X capacitor value is 330 nF and  $R1 = R2 = 200\text{ k}\Omega$ , the capacitor is discharged to a voltage < 60 V at a mains of 230 V (AC) in 300 ms.



**Fig 4. TEA1708T application diagram**

Use  $R1 = R2 = 200\text{ k}\Omega$  for X-capacitor values  $< 1.8\text{ }\mu\text{F}$  to ensure that the capacitor is discharged to a voltage  $< 60\text{ V}$  within 2 seconds. Lowering  $R1 + R2$ , for faster discharge or when a higher value for the X capacitor is required is possible but it decreases the surge protection level.

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1

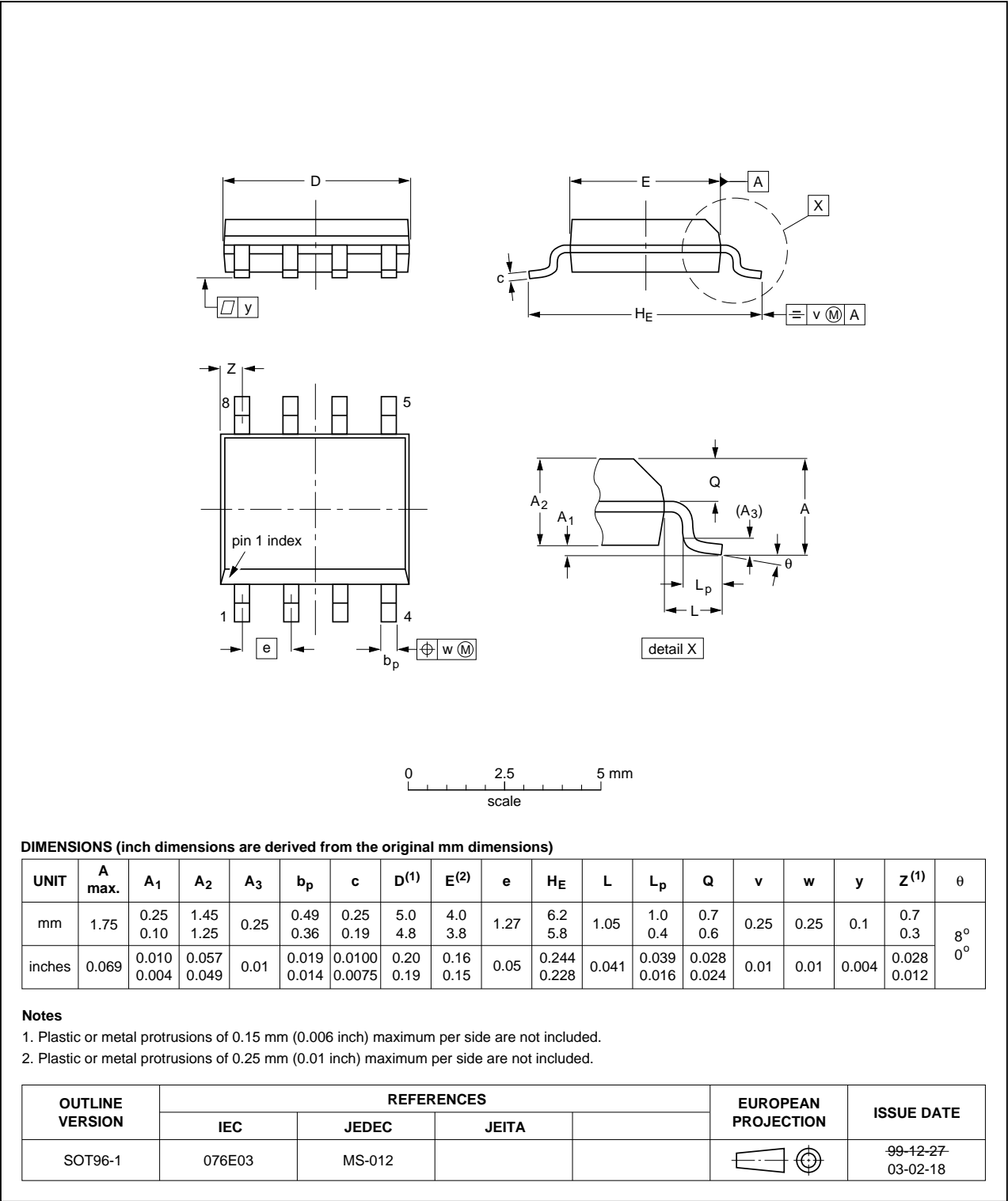


Fig 5. Package outline SOT96-1 (SO8)

## 13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1708T v.1	20130925	product data sheet	-	-



## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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