Light Management Unit with 2 LDOs and SemPulse® Interface

POWER MANAGEMENT

Features

- Input supply voltage range — 2.9V to 5.5V
- Four programmable current sinks with 29 steps from 0mA to 25mA
- Very high efficiency charge pump driver system with three modes — 1x, 1.5x and 2x
- Two programmable 200mA low-noise LDO regulators
- Charge pump frequency — 250kHz
- SemPulse single wire interface
- Backlight current accuracy — ±1.5% typical
- Backlight current matching — ±0.5% typical
- Fade-in/fade-out feature for main backlight
- Automatic sleep mode (LEDs off) — I_Q = 100µA
- Shutdown current — 0.1µA (typical)
- Ultra-thin package — 2.3 x 2.3 x 0.6 (mm)
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Cellular phones, smart phones, and PDAs
- LCD modules
- Portable media players
- Digital cameras and GPS units
- Display backlighting and LED indicators

Description

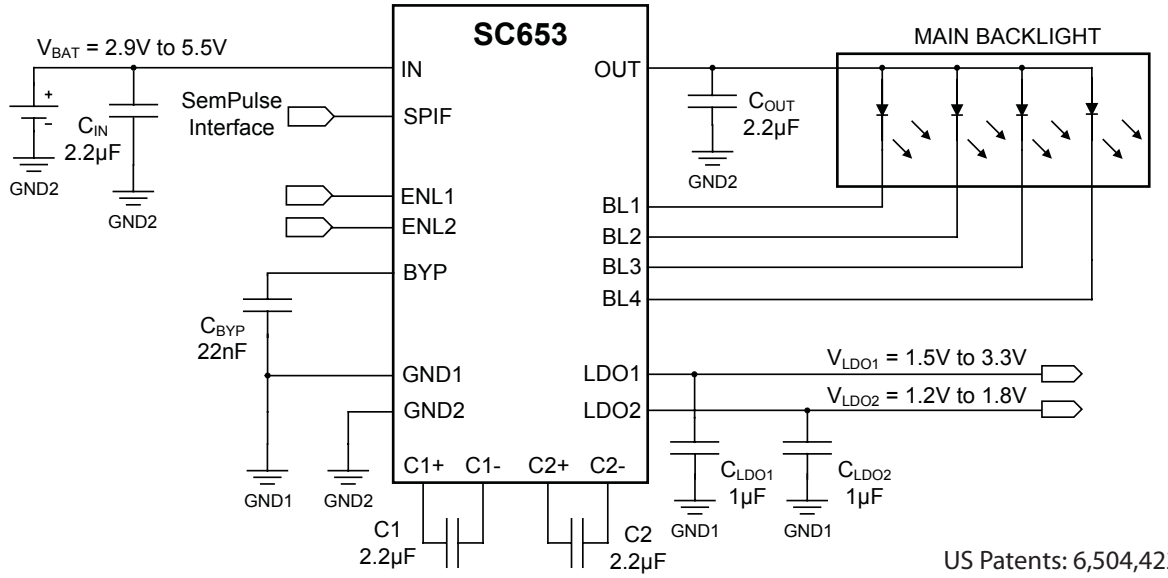
The SC653 is a highly integrated light management unit that provides two low-noise LDOs, a multi-mode high efficiency charge pump, and four programmable LED drivers. Performance is optimized for use in single-cell Li-ion battery applications.

The load and supply conditions determine whether the charge pump operates in 1x, 1.5x, or 2x mode. A programmable fading feature can be enabled to gradually adjust the backlight current, simplifying control software. The low-dropout, low-noise linear regulators can be used for powering a camera module or other peripheral circuits.

The SC653 uses the proprietary SemPulse® single wire interface. This interface controls all functions of the device, including backlight currents and LDO voltage outputs. The single wire interface minimizes microcontroller and interface pin counts.

The SC653 enters sleep mode when all the LED drivers are disabled. In this mode, the quiescent current is reduced while the device continues to monitor the SemPulse interface. The two LDOs can be enabled when the device is in sleep mode.

Typical Application Circuit



US Patents: 6,504,422; 6,794,926

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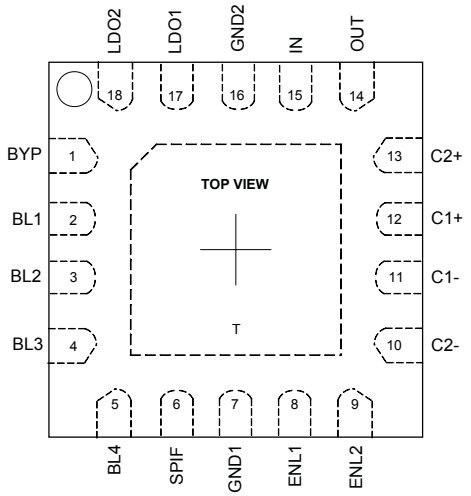
Pin Configuration



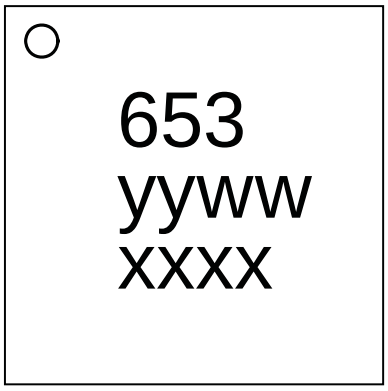
MLPQ-UT-18; 2.3x2.3, 18 LEAD
θ_{JA} = 45°C/W

Ordering Information

Device	Package
SC653ULTRT[1][2]	MLPQ-UT-18 2.3×2.3
SC653EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen-free.

Marking Information



yyww = date code
xxxx = Semtech Lot Number

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Absolute Maximum Ratings

IN, OUT (V) ..... -0.3 to +6.0
C1+, C2+ (V) ..... -0.3 to (V_{OUT} + 0.3)
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
OUT — Short Circuit Duration ..... Continuous
LDO1, LDO2 — Short Circuit Duration ..... Continuous
ESD Protection Level[1] (kV) 3

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... -40 ≤ T_A ≤ +85
Input Voltage (V) ..... 2.9 ≤ V_{IN} ≤ 5.5
Output Voltage (V) ..... 2.5 ≤ V_{OUT} ≤ 5.25
Voltage Difference between any two LEDs (V). . ΔV_F < 1.0[2]

Thermal Information

Thermal Resistance, Junction to Ambient[3] (°C/W) 45
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) $\Delta V_{F(max)}$ = 1.0V when V_{IN} = 2.9V, higher V_{IN} supports higher $\Delta V_{F(max)}$
(3) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, T_A = +25°C for Typ, -40°C to +85°C for Min and Max, $T_{J(MAX)}$ = 125°C, V_{IN} = 3.7V, C_{IN} = C_1 = C_2 = 2.2µF, C_{OUT} = 2.2µF (ESR = 0.03Ω), ΔV_F ≤ 1.0V[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Specifications						
Shutdown Current	$I_{Q(OFF)}$	Shutdown		0.1	2	µA
Total Quiescent Current	I_Q	Sleep (LDOs off), SPIF = V_{IN}[2]		100		µA
		Sleep (LDOs on), SPIF = V_{IN}[2], I_{LDOn} = 0mA		220		
		Charge pump in 1x mode, I_{OUT} = 20mA, I_{BLn} = 5mA		3.8		mA
		Charge pump in 1.5x mode, I_{OUT} = 20mA, I_{BLn} = 5mA		4.6		
		Charge pump in 2x mode, I_{OUT} = 20mA, I_{BLn} = 5mA		4.6		
Charge Pump Electrical Specifications						
Maximum Total Output Current	$I_{OUT(MAX)}$	V_{IN} > 3.2V, sum of all active LED currents, $V_{OUT(MAX)}$ = 4.2V	100			mA
Backlight Current Setting	I_{BL}	Nominal setting for BL1 thru BL4	0.5		25	mA
Backlight Current Accuracy	I_{BL_ACC}	I_{BLn} = 12mA[3], T_A = 25°C	-8	±1.5	+8	%
Backlight Current Matching	I_{BL-BL}	I_{BLn} = 12mA[4]	-3.5	±0.5	+3.5	%

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Charge Pump Electrical Specifications (continued)						
1x Mode to 1.5x Mode Falling Transition Voltage	$V_{TRANS1x}$	I_{OUT} = 40mA, I_{BLn} = 10mA, V_{OUT} = 3.2V		3.27		V
1.5x Mode to 1x Mode Hysteresis	V_{HYST1x}	I_{OUT} = 40mA, I_{BLn} = 10mA, V_{OUT} = 3.2V		250		mV
1.5x Mode to 2x Mode Falling Transition Voltage	$V_{TRANS1.5x}$	I_{OUT} = 40mA, I_{BLn} = 10mA, V_{OUT} = 4.0V(5)		2.92		V
2x Mode to 1.5x Mode Hysteresis	$V_{HYST1.5x}$	I_{OUT} = 40mA, I_{BLn} = 10mA, V_{OUT} = 4.0V(5)		300		mV
Current Sink Off-State Leakage Current	I_{BLn}	$V_{IN} = V_{BLn}$ = 4.2V		0.1	1	µA
Pump Frequency	f_{PUMP}	V_{IN} = 3.2V		250		kHz
LDO Electrical Specifications						
LDO1 Voltage Setting	V_{LDO1}	Range of nominal settings in 100mV increments	1.5		3.3	V
LDO2 Voltage Setting	V_{LDO2}	Range of nominal settings in 100mV increments	1.2		1.8	V
LDO1, LDO2 Output Voltage Accuracy	ΔV_{LDO}	I_{LDOn} = 1mA, T_A = 25°C, 2.9V ≤ V_{IN} ≤ 4.2V	-3		+3	%
		I_{LDOn} = 1mA to 100mA, 2.9V ≤ V_{IN} ≤ 4.2V	-3.5	±3	+3.5	%
Line Regulation	ΔV_{LINE}	I_{LDO1} = 1mA, V_{OUT} = 2.8V		2.1	7.2	mV
		I_{LDO2} = 1mA, V_{OUT} = 1.8V		1.3	4.8	
Load Regulation	ΔV_{LOAD}	V_{LDO1} = 3.3V, I_{LDO1} = 1mA to 100 mA			25	mV
		V_{LDO2} = 1.8V, I_{LDO2} = 1mA to 100 mA			20	
Dropout Voltage(6)	V_D	I_{LDO1} = 150mA		150	200	mV
Power Supply Rejection Ratio	$PSRR_{LDO1}$	1.5V < V_{LDO1} < 3.0V, f < 1kHz, C_{BYP} = 22nF, I_{LDO1} = 50mA with 0.5V_{P-P} supply ripple		55		dB
	$PSRR_{LDO2}$	1.2V < V_{LDO2}, f < 1kHz, C_{BYP} = 22nF, I_{LDO2} = 50mA, with 0.5V_{P-P} supply ripple		60		
Output Voltage Noise	e_{n-LDO1}	LDO1, 10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDOn} = 1µF, I_{LDO1} = 50 mA, 1.5V < V_{LDO1} < 3.0V		100		μV_{RMS}
	e_{n-LDO2}	LDO2, 10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDO} = 1µF, I_{LDO2} = 50 mA		50		
Minimum Output Capacitor	$C_{LDO(MIN)}$			1		µF

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital I/O Electrical Specifications (SPIF, ENL1, ENL2)						
Input High Threshold[7]	V_{IH}	V_{IN} = 5.5V	1.6			V
Input Low Threshold[7]	V_{IL}	V_{IN} = 3.0V			0.4	V
Input High Current	I_{IH}	V_{IN} = 5.5V	-1		+1	µA
Input Low Current	I_{IL}	V_{IN} = 5.5V	-1		+1	µA
SemPulse Electrical Specifications (SPIF)						
SemPulse Start-up Time[8]	t_{SU}		1			ms
Bit Pulse Duration[7]	t_{HI}		0.75		250	µs
Duration Between Bits[7]	t_{LO}		0.75		250	µs
Hold Time - Address[7]	t_{HOLDA}	SPIF is held high	500		5000	µs
Hold Time - Data[7]	t_{HOLDD}	SPIF is held high	500			µs
Bus Reset Time[7]	t_{BR}	SPIF is held high	10			ms
Shutdown Time[9]	t_{SD}	SPIF is pulled low	10			ms
Fault Protection						
Output Short Circuit Current Limit	$I_{OUT(SC)}$	OUT pin shorted to GND		250		mA
LDO Current Limit	I_{LIM}	V_{LDOn} enabled	200			mA
Over-Temperature	T_{OTP}	Rising threshold		165		°C
	T_{HYS}	Hysteresis		30		°C
Charge Pump Over-Voltage Protection	V_{OVP}	OUT pin open circuit, $V_{OUT} = V_{OVP}$ rising threshold	5.3	5.7	6.0	V
Under Voltage Lockout	$V_{UVLO-OFF}$	Increasing V_{IN}		2.7		V
	$V_{UVLO-HYS}$	Hysteresis		800		mV

Notes:

(1) ΔV_F is the voltage difference between any two LEDs.

(2) SPIF is high for more than 10ms

(3) Subscript n = 1 and 2 for the LDOs, and n = 1, 2, 3, and 4 for the backlights.

(4) Current matching equals $\pm [I_{BL(MAX)} - I_{BL(MIN)}] / [I_{BL(MAX)} + I_{BL(MIN)}]$.

(5) Test voltage is V_{OUT} = 4.0V — a relatively extreme LED voltage — to force a transition during test. Typically V_{OUT} = 3.2V for white LEDs.

(6) Dropout is defined as (V_{IN} - V_{LDO1}) when V_{LDO1} drops 100mV from nominal. Dropout does not apply to LDO2 since it has a maximum output voltage of 1.8V.

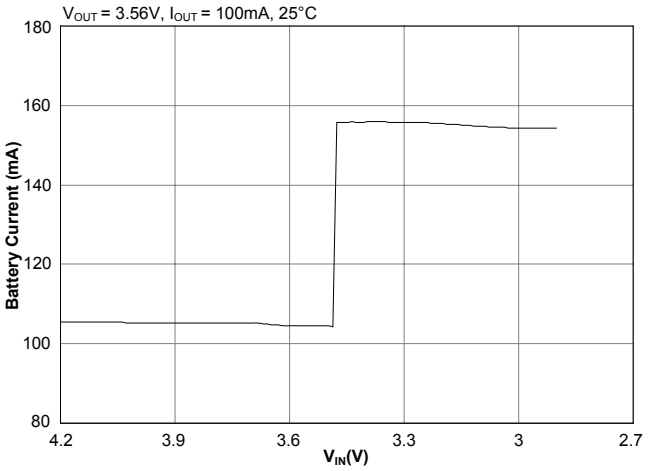
(7) The source driver used to provide the SemPulse output must meet these limits.

(8) The SemPulse start-up time is the minimum time that the SPIF pin must be held high to enable the part before starting communication.

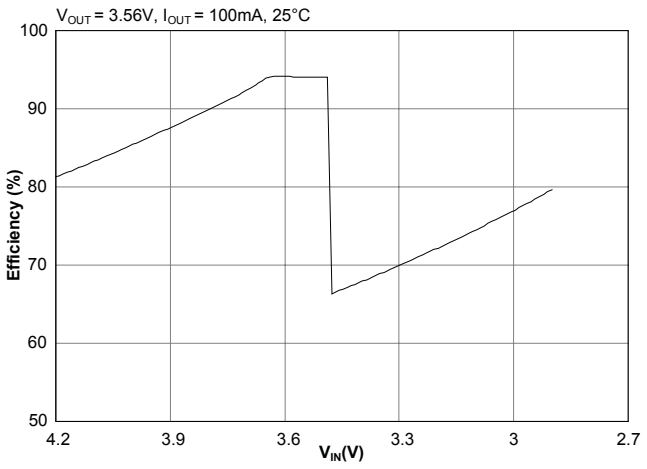
(9) The SemPulse shutdown time is the minimum time that the SPIF pin must be pulled low to shut the part down.

Typical Characteristics

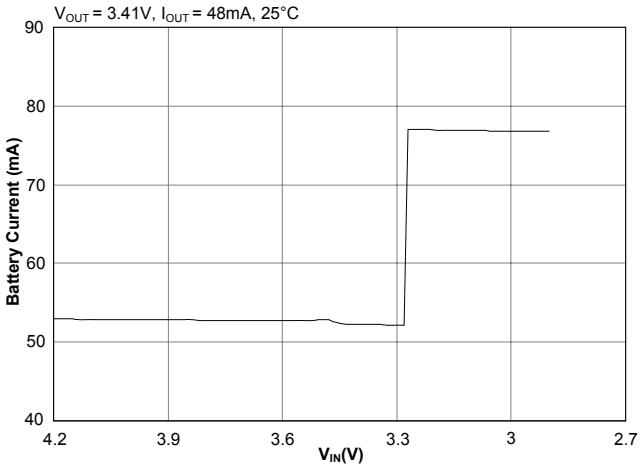
Battery Current (4 LEDs) — 25mA Each



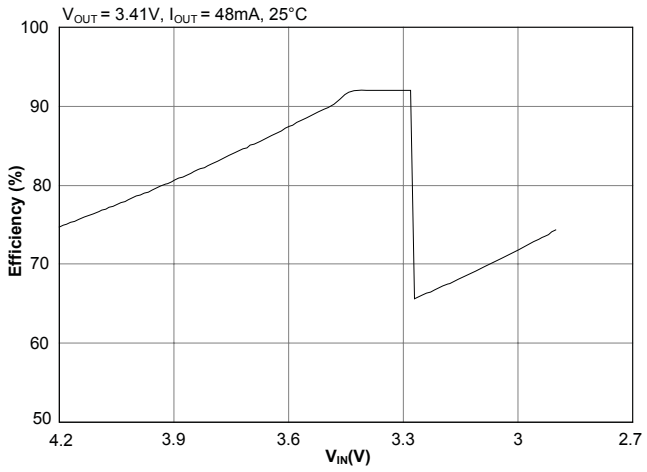
Backlight Efficiency (4 LEDs) — 25mA Each



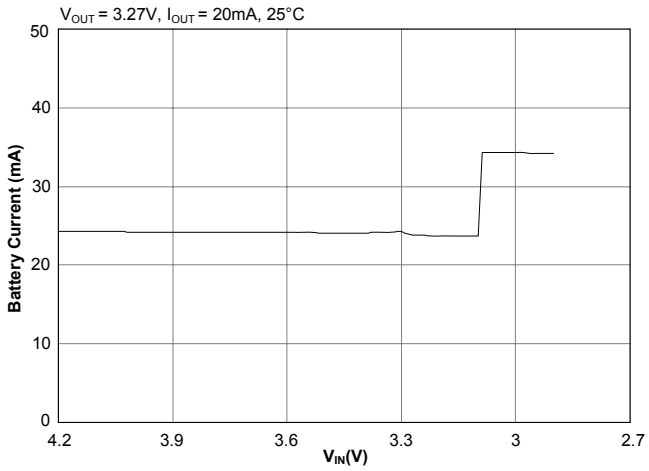
Battery Current (4 LEDs) — 12mA Each



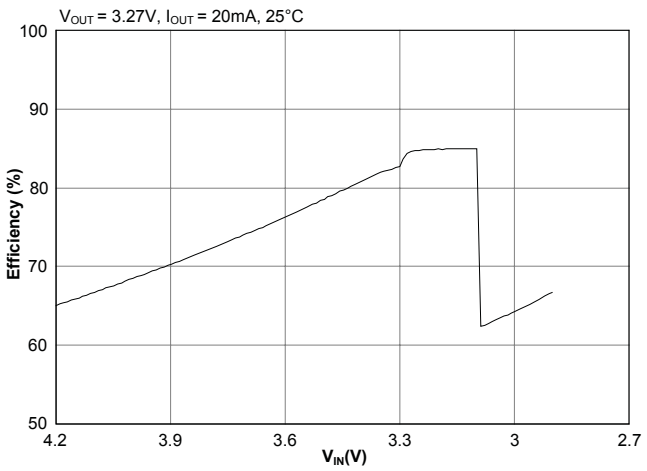
Backlight Efficiency (4 LEDs) — 12mA Each



Battery Current (4 LEDs) — 5.0mA Each

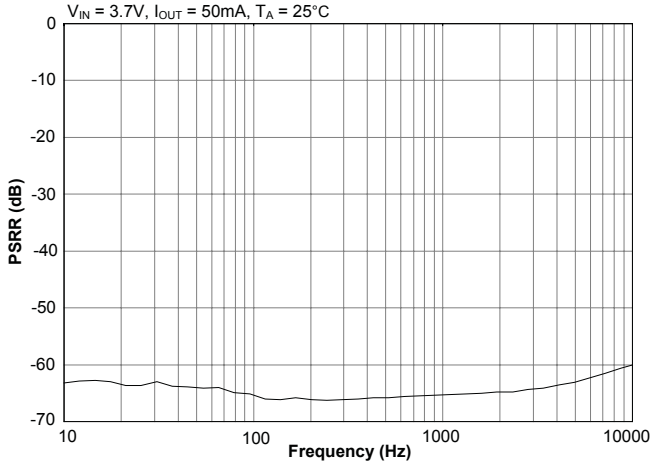


Backlight Efficiency (4 LEDs) — 5.0mA Each

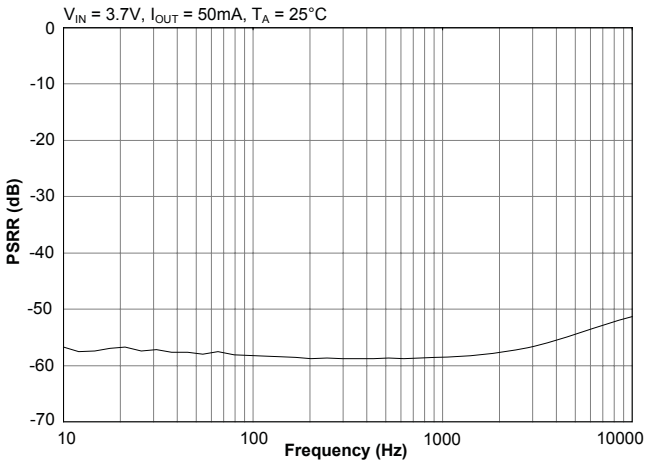


Typical Characteristics (continued)

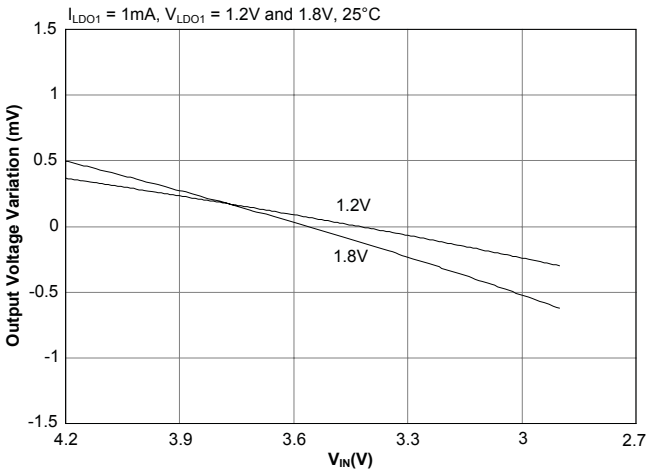
PSRR vs. Frequency — 1.8V



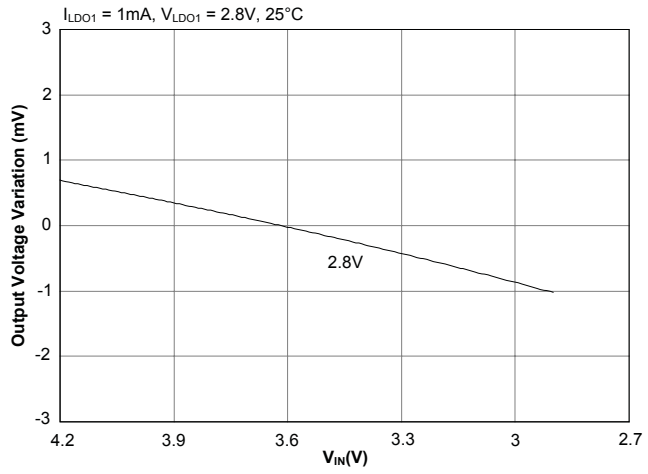
PSRR vs. Frequency — 2.8V



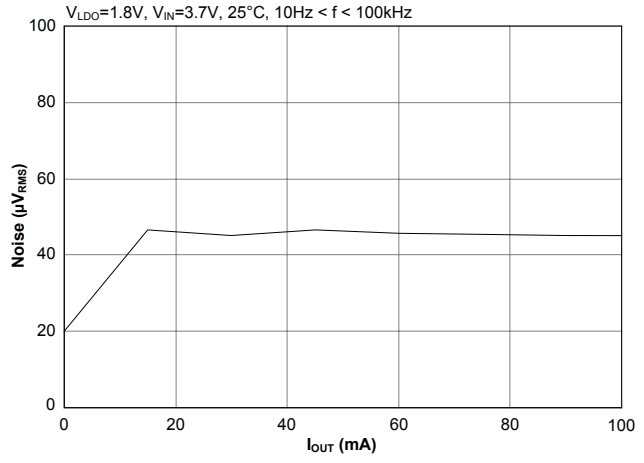
Line Regulation (LDO2)



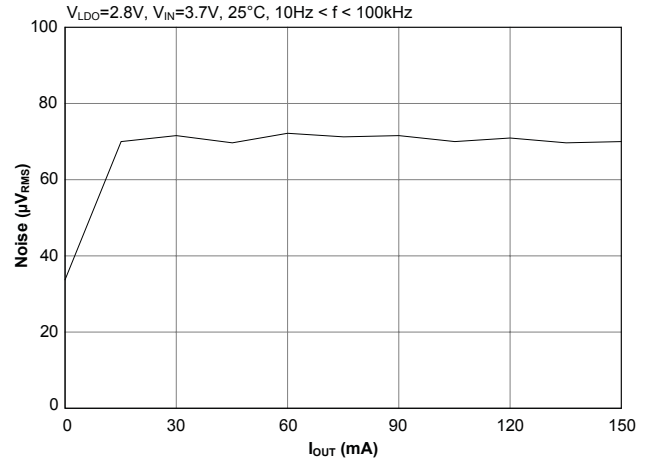
Line Regulation (LDO1)



LDO Noise vs. Load Current — 1.8V

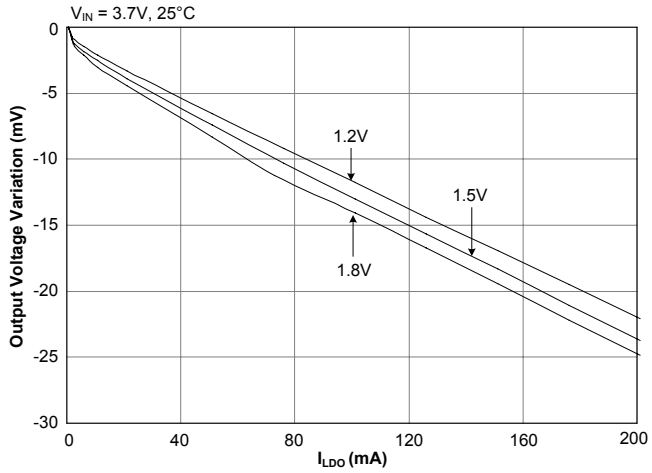


LDO Noise vs. Load Current — 2.8V

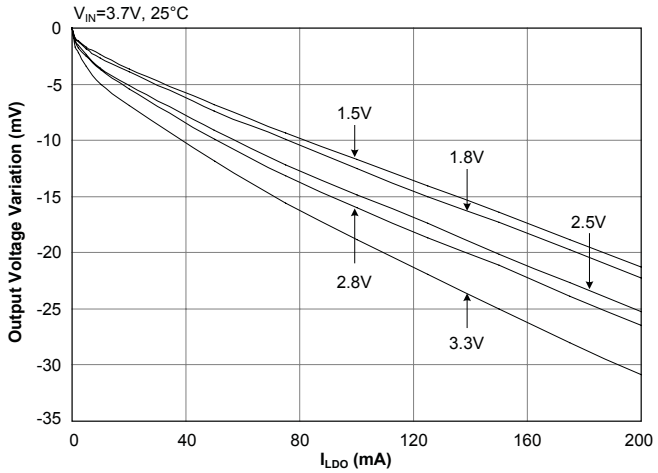


Typical Characteristics (continued)

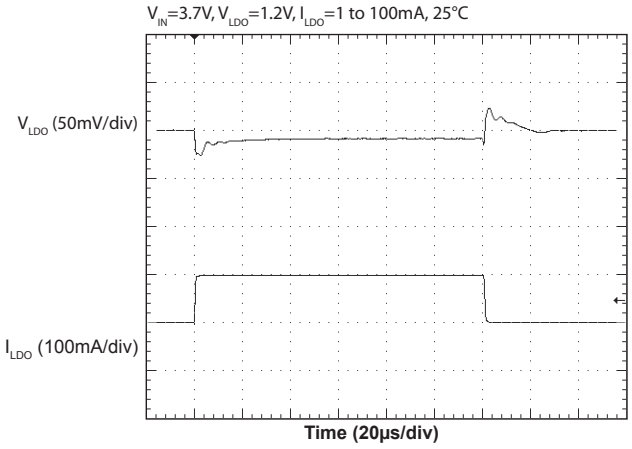
Load Regulation (LDO2)



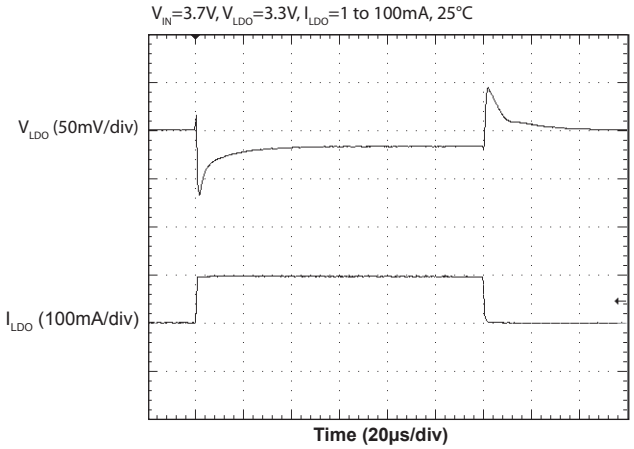
Load Regulation (LDO1)



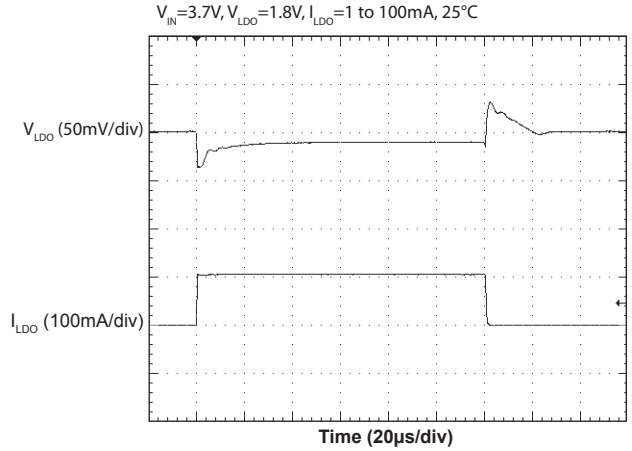
LDO Load Transient Response (1.2V)



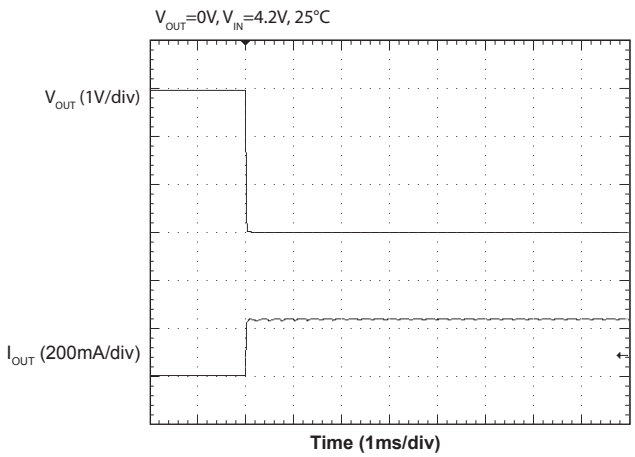
LDO Load Transient Response (3.3V)



LDO Load Transient Response (1.8V)

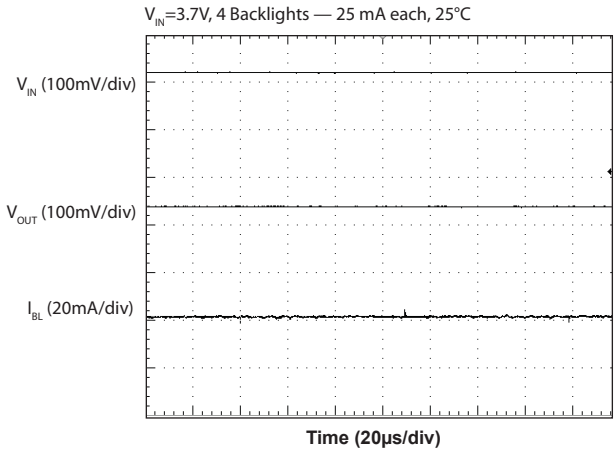


Output Short Circuit Current Limit

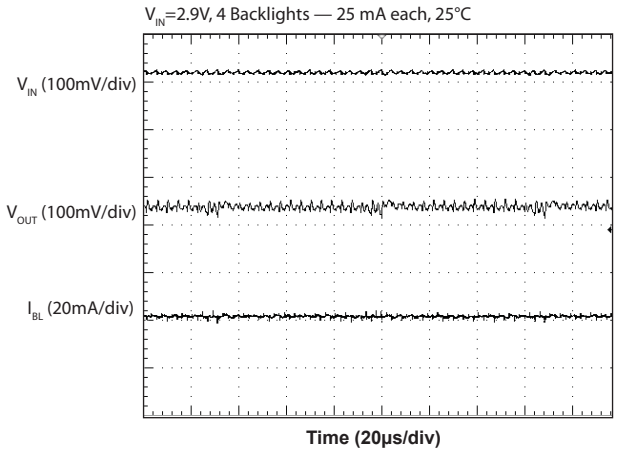


Typical Characteristics (continued)

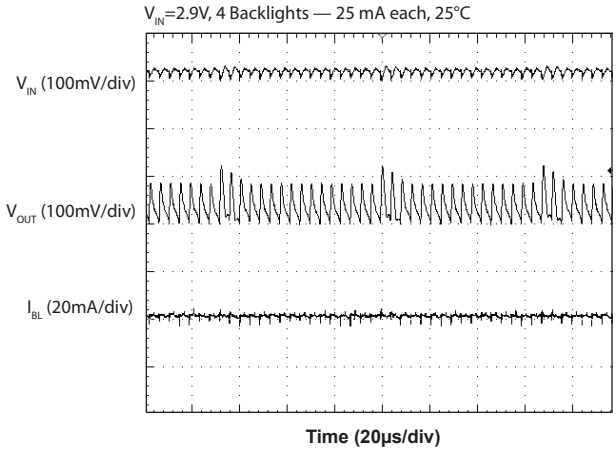
Ripple — 1X Mode



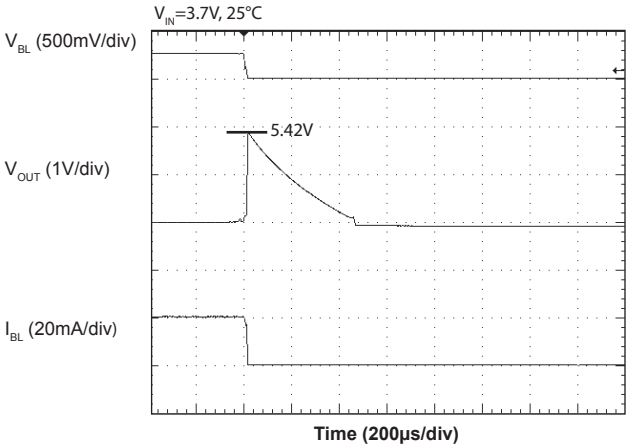
Ripple — 1.5X Mode



Ripple — 2X Mode



Output Open Circuit Protection



Pin Descriptions

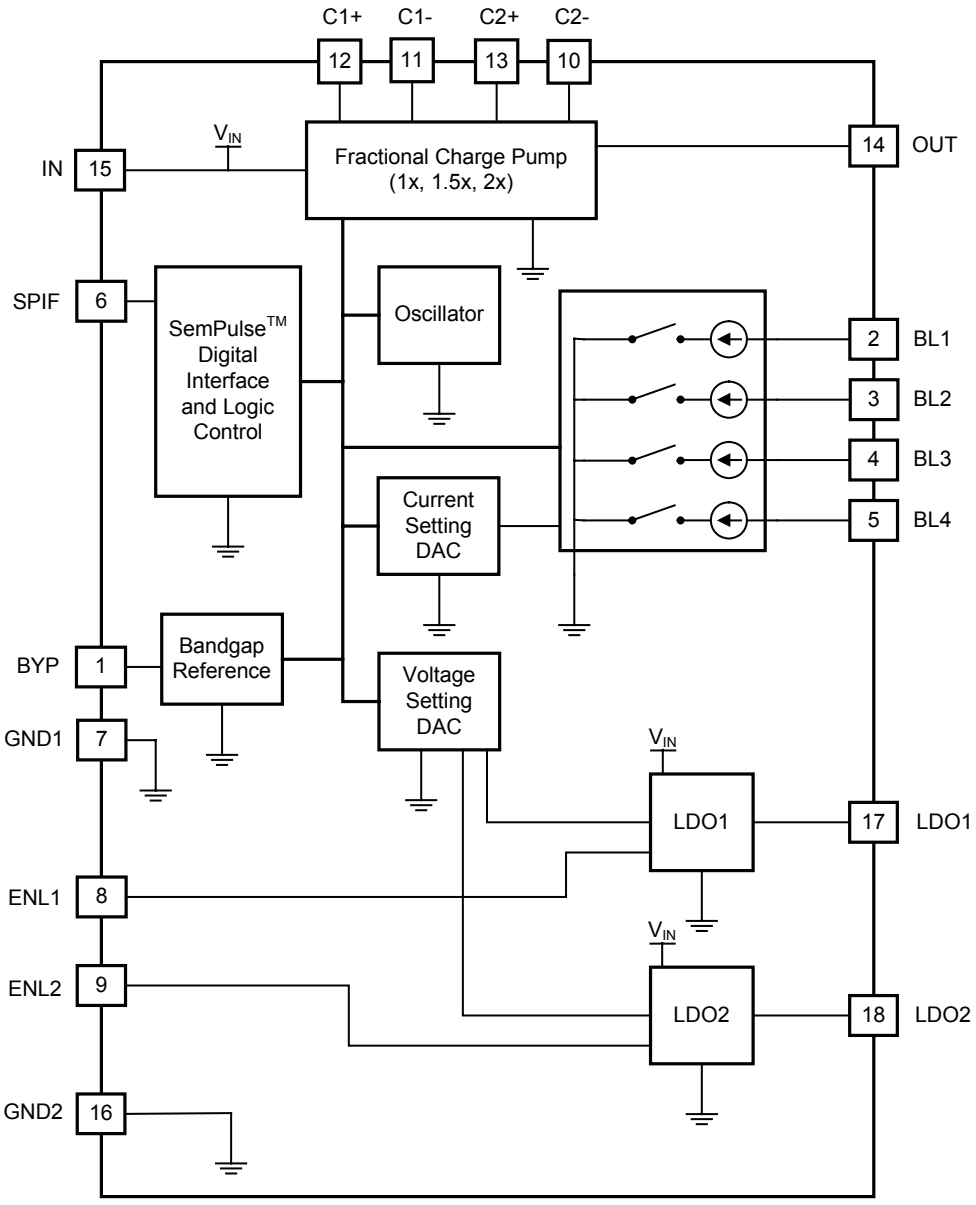
Pin #	Pin Name	Pin Function
1	BYP	Bypass pin for voltage reference — ground C_{BYP} to GND1 on ground island.
2	BL1	Current sink output for main backlight LED 1 — leave this pin open if unused
3	BL2	Current sink output for main backlight LED 2 — leave this pin open if unused
4	BL3	Current sink output for main backlight LED 3 — leave this pin open if unused
5	BL4	Current sink output for main backlight LED 4 — leave this pin open if unused
6	SPIF	SemPulse single wire interface pin — used to enable/disable the device and to configure all registers (refer to Register Map and SemPulse Interface sections)
7	GND1	Ground pin — Ground C_{BYP}, C_{LDO1}, C_{LDO2} to GND1 on ground island.
8	ENL1 (1)	LDO1 enable input — active high
9	ENL2 (2)	LDO2 enable input — active high
10	C2-	Negative connection to bucket capacitor 2
11	C1-	Negative connection to bucket capacitor 1
12	C1+	Positive connection to bucket capacitor 1
13	C2+	Positive connection to bucket capacitor 2
14	OUT	Charge pump output — all LED anode pins should be connected to this pin
15	IN	Battery voltage input
16	GND2	Ground Pin — connect to ground plane
17	LDO1	Output of LDO1 — ground C_{LDO1} to GND1 on ground island.
18	LDO2	Output of LDO2 — ground C_{LDO2} to GND1 on ground island.
T	THERMAL PAD	Thermal pad for heatsinking purposes — connect to ground plane using multiple vias. This pad is internally connected to ground and to pins 7 and 16.

NOTES:

(1) ENL1 must be high for the SPIF interface to control LDO1. When low, ENL1 disables LDO1.

(2) ENL2 must be high for the SPIF interface to control LDO2. When low, ENL2 disables LDO2.

Block Diagram



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Applications Information

General Description

This design is optimized for handheld applications supplied from a single Li-Ion cell and includes the following key features:

- A high efficiency fractional charge pump that supplies power to all LEDs
- Four matched current sinks that control LED backlighting current, with 0mA to 25mA per LED
- Two adjustable LDOs with outputs ranging from 1.5V to 3.3V for LDO1 and 1.2V to 1.8V for LDO2, adjustable in 100mV increments

High Current Fractional Charge Pump

The backlight outputs are supported by a high efficiency, high current fractional charge pump output at the OUT pin. The charge pump multiplies the input voltage by 1, 1.5, or 2 times. The charge pump switches at a fixed frequency of 250kHz in 1.5x and 2x modes and is disabled in 1x mode to save power and improve efficiency.

The mode selection circuit automatically selects the mode as 1x, 1.5x, or 2x based on circuit conditions such as LED voltage, input voltage, and load current. The 1x mode is the most efficient of the three modes, followed by 1.5x and 2x modes. Circuit conditions such as low input voltage, high output current, or high LED voltage place a higher demand on the charge pump output. A higher numerical mode (1.5x or 2x) may be needed momentarily to maintain regulation at the OUT pin during intervals of high demand. The charge pump responds to momentary high demands, setting the charge pump to the optimum mode to deliver the output voltage and load current while optimizing efficiency. Hysteresis is provided to prevent mode toggling.

The charge pump requires two bucket capacitors for proper operation. One capacitor must be connected between the C1+ and C1- pins and the other must be connected between the C2+ and C2- pins as shown in the typical application circuit diagram. These capacitors should be equal in value, with a nominal capacitance of 1.0µF to support the charge pump current requirements. Note that small package capacitors can decrease in value by up to 50% under DC loading, so it is strongly recommended that 2.2uF capacitors be selected when using 0402 size ceramic capacitors. The device also requires a 2.2µF capacitor on the IN pin and a 2.2µF capacitor on the OUT pin to minimize noise and support the output drive requirements. Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

LED Backlight Current Sinks

The backlight current is set via the SemPulse interface. The current is regulated to one of 29 values between 0mA and 25mA. The step size varies depending upon the current setting. The step sizes are 0.5mA for current settings between 0mA and 5mA. The step size increases to 1mA for settings between 5mA and 21mA. Steps are 2mA between 21mA and 25mA. The variation in step size allows finer adjustment for dimming functions in the low current setting range and coarse adjustment at higher current settings where small current changes are not visibly noticeable in LED brightness. A zero setting is also included to allow the current sink to be disabled by writing to either the enable bit or the current setting register for maximum flexibility.

All backlight current sinks have matched currents, even when there is variation in the forward voltages (ΔV_F) of the LEDs. A ΔV_F of 1.2V is supported when the input voltage is at 3.0V. Higher ΔV_F LED mis-match is supported when V_{IN} is higher than 3.0V. All current sink outputs are compared and the lowest output is used for setting the voltage regulation at the OUT pin. This is done to ensure that sufficient bias exists for all LEDs.

The backlight LEDs default to the off state upon power-up. For backlight applications using less than four LEDs, any unused output must be left open and the unused LED driver must remain disabled. When writing to the Backlight Enable register, a zero (0) must be written to the corresponding bit of any unused output.

Applications Information (continued)

Backlight Quiescent Current

The quiescent current required to operate all four backlights is reduced by 1.5mA when backlight current is set to 4.0mA or less. This feature results in higher efficiency under light-load conditions. Further reduction in quiescent current will result from using fewer than four LEDs.

Fade-In and Fade-Out

The SC653 contains bits that control the fade state of the main bank. When enabled, the fade function causes the backlight settings to step from their current state to the next programmed state as soon as the new state is stored in its register. For example, if the backlight is set at 25mA and the next setting is the off state, the backlight will step from 25mA down to 0mA using all 29 settings at the fade rate specified by the bits in register 04h. The same is true when turning on or increasing the backlight current — the backlight current will step from the present level to the new level at the step rate defined in register 04h. This process applies for both the main and the sub displays.

The fade rate may be changed dynamically when a fade operation is active by writing new values to the fade register. When a new backlight level is written during an ongoing fade operation, the fade will be redirected to the new value from the present state. An ongoing fade operation may be cancelled by disabling fade which will result in the backlight current changing immediately to the final value. If fade is disabled, the current level will change immediately without the fade delay. The state diagram in Figure 1 describes all possible conditions for a fade operation. More details can be found in the Register Map Section.

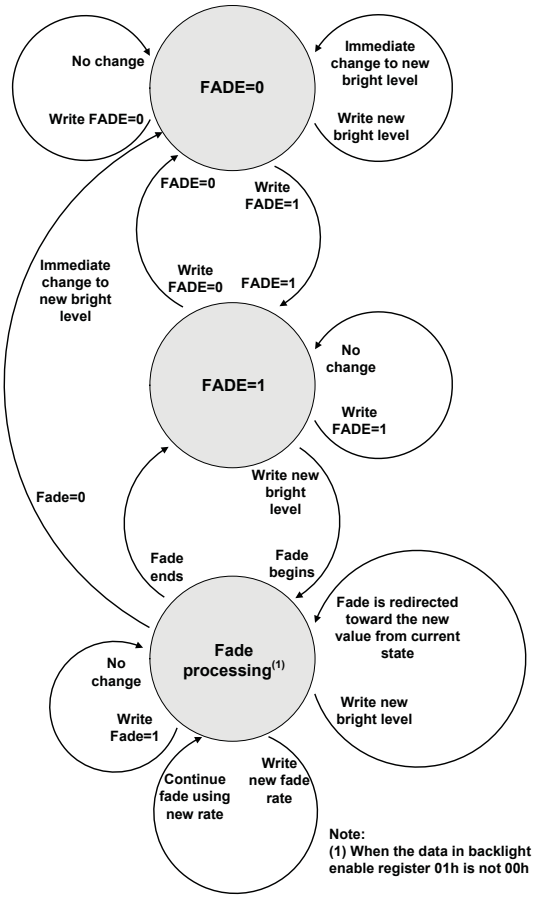


Figure 1 — Fade State Diagram

Programmable LDO Outputs

Two low dropout (LDO) regulators are provided for camera module I/O and core power. Each LDO output voltage setting has ±3.5% accuracy over the operating temperature range. Output current greater than the specification is possible at somewhat reduced accuracy.

Input pins ENL1 and ENL2 may be used to directly enable and disable the LDOs without communication via the SPIF interface. When power is first applied to the SC653, the register defaults reset the LDOs to the off state, so SPIF must be used one time to set the voltages before ENL1 and ENL2 can be used to enable the LDOs.

Applications Information (continued)

To control LDOs exclusively by software, ENL1 and ENL2 may be permanently terminated to the battery voltage. ENL1 must be high for the SPIF interface to control LDO1. When low, ENL1 disables LDO1. ENL2 is used exactly the same way to enable and disable LDO2.

A 1µF, low ESR capacitor should be used as a bypass capacitor on each LDO output to reduce noise and ensure stability. In addition, it is recommended that a nominal minimum 22nF capacitor be connected between the BYP pin and the GND1 pin to minimize noise and achieve optimum power supply rejection. A larger capacitor can be used for this function, but at the expense of increasing turn-on time. Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

Shutdown Mode

The device is disabled when the SPIF pin is held low for the shutdown time specified in the electrical characteristics section. All registers are reset to default condition at shutdown. Typical current consumption in this mode is 0.1µA.

Sleep Mode

When all LEDs are disabled, sleep mode is activated. This is a reduced current mode that helps minimize overall current consumption by disabling the clock and the charge pump while continuing to monitor the serial interface for commands. The two LDOs can be enabled when the device is in sleep mode.

Protection Features

The SC653 provides several protection features to safeguard the device from catastrophic failures. These features include:

- Output Open Circuit Protection
- Over-Temperature Protection
- Charge Pump Output Current Limit
- LDO Current Limit
- LED Float Detection

Output Open Circuit Protection

Over-Voltage Protection (OVP) is provided at the OUT pin to prevent the charge pump from producing an excessively high output voltage. In the event of an open circuit at OUT, the charge pump runs in open loop and the voltage rises up to the OVP limit. OVP operation is hysteretic, meaning the charge pump will momentarily turn off until V_{OUT} is sufficiently reduced. The maximum OVP threshold is 6.0V, allowing the use of a ceramic output capacitor rated at 6.3V.

Over-Temperature Protection

The Over-Temperature (OT) protection circuit prevents the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 165°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown. Hysteresis of 30°C is provided to ensure that the device cools sufficiently before re-enabling.

Charge Pump Output Current Limit

The device limits the charge pump current at the OUT pin. When OUT is shorted to ground, the output current will typically equal 250mA. The output current is also limited to 250mA when over-loaded resistively.

LDO Current Limit

The device limits the output currents of LDO1 and LDO2 to help prevent the device from overheating and to protect the loads. The minimum limit is 200mA, so load current greater than the rated current and up to 200mA can be used with degraded accuracy and larger dropout without tripping the current limit.

LED Float Detection

Float detect is a fault detection feature of the LED current sink outputs. If an output is programmed to be enabled and an open circuit fault occurs at any current sink output, that output will be disabled to prevent a sustained output OVP condition from occurring due to the resulting open loop. Float detect ensures device protection but does not ensure optimum performance. Unused LED outputs must be disabled to prevent an open circuit fault from occurring.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 2 illustrates a proper two-layer PCB layout for the SC653 and supporting components. Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. The following guidelines are recommended when developing a PCB layout:

- Place all bucket, bypass, and decoupling capacitors — C1, C2, CIN, COUT, CLDO1, CLDO2, and CBYP as close to the device as possible.
- All charge pump current passes through IN, OUT, and the bucket capacitor connection pins. Ensure that all connections to these pins make use of wide traces so that the resistive drop on each connection is minimized.
- The thermal pad should be connected to the ground plane using multiple vias to ensure proper thermal connection for optimal heat transfer.
- The following capacitors — CLDO1, CLDO2, and CBYP should be grounded together through an isolated copper island. Using no vias, connect the island only, to pin 7 as shown in Figure 2.
- Figure 3 shows only the vias that should be connected to the ground plane with multiple vias.
- Make all ground connections to a solid ground plane as shown in Figure 4.
- All LDO output traces should be made as wide as possible to minimize resistive losses.

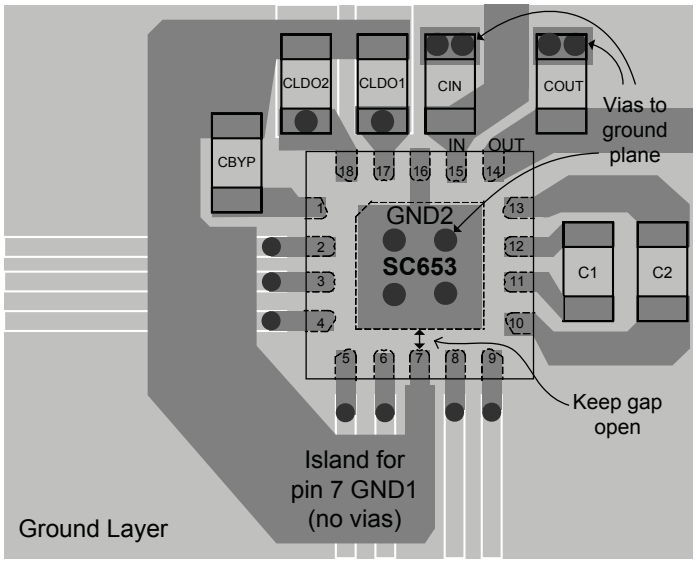


Figure 2 — Recommended PCB Layout

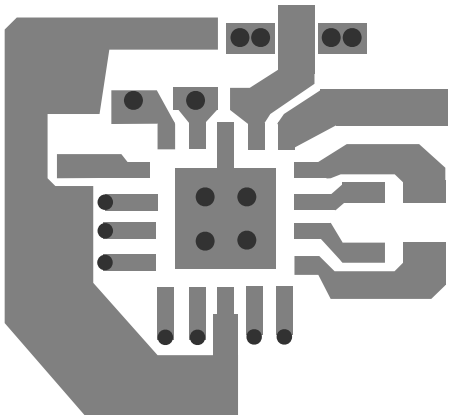


Figure 3 — Layer 1

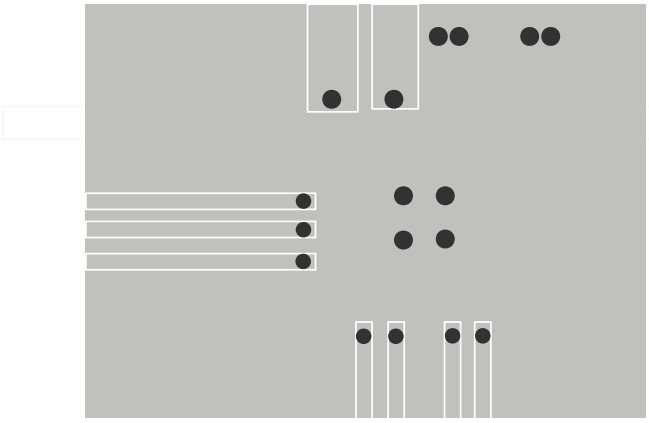


Figure 4 — Layer 2

SemPulse® Interface

Introduction

SemPulse is a write-only single wire interface. It provides access to up to 32 registers that control device functionality. Two sets of pulse trains are transmitted via the SPIF pin. The first pulse set is used to set the desired address. After the bus is held high for the address hold period, the next pulse set is used to write the data value. After the data pulses are transmitted, the bus is held high again for the data hold period to signify the data write is complete. At this point the device latches the data into the address that was selected by the first set of pulses. See the SemPulse Timing Diagrams for descriptions of all timing parameters.

Chip Enable/Disable

The device is enabled when the SemPulse interface pin (SPIF) is pulled high for greater than t_{SU}. If the SPIF pin is pulled low again for more than t_{SD}, the device will be disabled.

Address Writes

The first set of pulses can range between 0 and 31 (or 1 to 32 rising edges) to set the desired address. After the pulses are transmitted, the SPIF pin must be held high for t_{HOLDA} to notify the slave device that the address write is finished. If the pulse count is between 0 and 31 and the line is held high for t_{HOLDA}, the address is latched as the destination for the data word. If the SPIF pin is not held high for t_{HOLDA}, the slave device will continue to count pulses. If the total exceeds 31 pulses, the write will be ignored and the bus will reset after the next valid hold time is detected. Note that if t_{HOLDA} exceeds its maximum specification, the bus will reset. This means that the communication is ignored and the bus resumes monitoring the pin, expecting the next pulse set to be an address.

Data Writes

After the bus has been held high for the minimum address hold period, the next set of pulses are used to write the data value. The total number of pulses can range from 0 to 63 (or 1 to 64 rising edges) since there are a total of 6 register bits per register. Just like with the address write, the data write is only accepted if the bus is held high for t_{HOLDD} when the pulse train is completed. If the proper hold time is not received, the interface will keep counting pulses until the hold time is detected. If the total exceeds 63 pulses, the write will be ignored and the bus will reset after the next valid hold time is detected. After the bus has been held high for t_{HOLDD}, the bus will expect the next pulse set to be an address write. Note that this is the same effect as the bus reset that occurs when t_{HOLDA} exceeds its maximum specification. For this reason, there is no maximum limit on t_{HOLDD} — the bus simply waits for the next valid address to be transmitted.

Multiple Writes

It is important to note that this single-wire interface requires the address to be paired with its corresponding data. If it is desired to write multiple times to the same address, the address must always be re-transmitted prior to the corresponding data. If it is only transmitted one time and followed by multiple data transmissions, every other block of data will be treated like a new address. The result will be invalid data writes to incorrect addresses. Note that multiple writes only need to be separated by the minimum t_{HOLDD} for the slave to interpret them correctly. As long as t_{HOLDA} between the address pulse set and the data pulse set is less than its maximum specification but greater than its minimum, multiple pairs of address and data pulse counts can be made with no detrimental effects.

Standby Mode

Once data transfer is completed, the SPIF line must be returned to the high state for at least 10ms to return to the standby mode. In this mode, the SPIF line remains idle while monitoring for the next command. This mode allows the device to minimize current consumption between commands. Once the device has returned to standby mode, the bus is automatically reset to expect the address pulses as the next data block. This safeguard is intended to reset the bus to a known state (waiting for the beginning of a write sequence) if the delay exceeds the reset threshold.

SemPulse® Interface (continued)

The SemPulse single wire interface is used to enable or disable the device and configure all registers (see Figure 2). The timing parameters refer to the digital I/O electrical specifications.

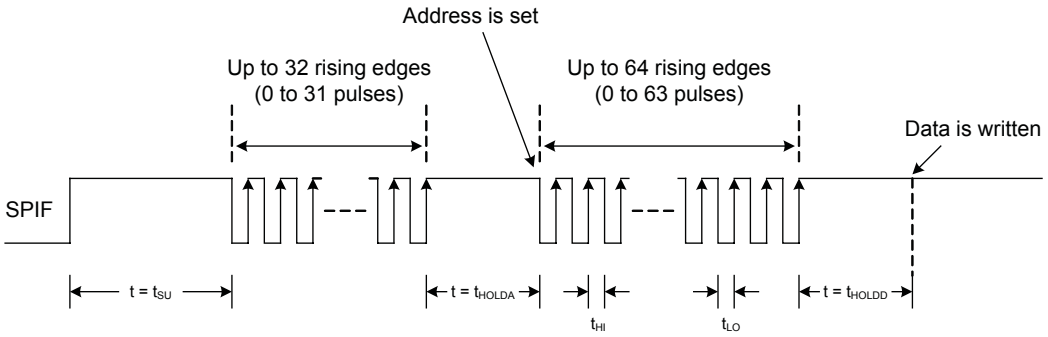


Figure 2 — Uniform Timing Diagram for SemPulse Communication

Timing Example 1

In this example (see Figure 3), the slave chip receives a sequence of pulses to set the address and data, and the pulses experience interrupts that cause the pulse width to be non-uniform. Note that as long as the maximum high and low times are satisfied and the hold times are within specification, the data transfer is completed regardless of the number of interrupts that delay the transmission.

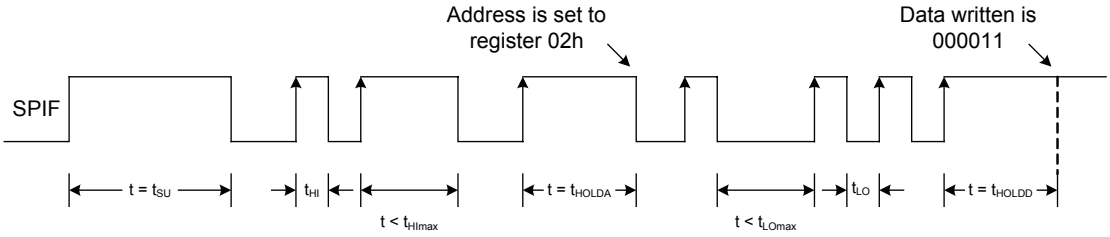


Figure 3 — SemPulse Data Write with Non-Uniform Pulse Widths

Timing Example 2

In this example (see Figure 4), the slave chip receives two sets of pulses to set the address and data, but an interrupt occurs during a pulse that causes it to exceed the minimum address hold time. The write is meant to be the value 03h in register 05h, but instead it is interpreted as the value 02h written to register 02h. The extended pulse that is delayed by the interrupt triggers a false address detection, causing the next pulse set to be interpreted as the data set. To avoid any problems with timing, make sure that all pulse widths comply with their timing requirements as outlined in this datasheet.

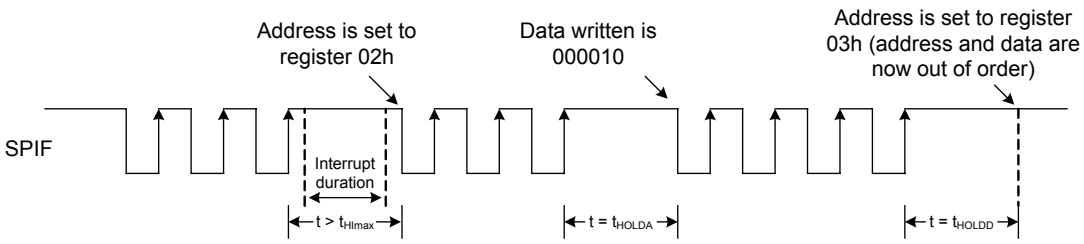


Figure 4 — Faulty SemPulse Data Write Due to Extended Interrupt Duration

Register Map[1]

Address	D5	D4	D3	D2	D1	D0	Reset Value	Description
00h	0[2]	BL_4	BL_3	BL_2	BL_1	BL_0	00h	Backlight Current
01h	0[2]	0[2]	BLEN_4	BLEN_3	BLEN_2	BLEN_1	00h	Backlight Enable
02h	0[2]	0[2]	LDO1_3	LDO1_2	LDO1_1	LDO1_0	00h	LDO1
03h	0[2]	0[2]	0[2]	LDO2_2	LDO2_1	LDO2_0	00h	LDO2
04h	0[2]	0[2]	0[2]	FADE_1	FADE_0	FADE_EN	00h	Fade

Notes:
(1) All registers are write-only.
(2) 0 = always write a 0 to these bits

Definition of Registers and Bits

BL Current Control Register (00h)

This register is used to set the currents for the backlight current sinks. These current sinks need to be enabled in the Backlight Enable Control register to be active.

BL[D4:D0]

These bits are used to set the current for the backlight current sinks. All enabled backlight current sinks will sink the same current, as shown in Table 1.

Table 1 — Backlight Current Settings

BL_4	BL_3	BL_2	BL_1	BL_0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	See note 1
0	0	0	1	0	See note 1
0	0	0	1	1	See note 1
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

(1) Reserved for future use

Register and Bit Definitions (continued)

Backlight Enable Control Register (01h)

This register is used to enable the backlight current sinks.

BLEN[D4:D1]

These bits are used to enable current sinks (active high, default low).

BLEN_4 — Enable bit for backlight BL4
BLEN_3 — Enable bit for backlight BL3
BLEN_2 — Enable bit for backlight BL2
BLEN_1 — Enable bit for backlight BL1

When enabled, the current sinks will carry the current set by the backlight current control bits BL[4:0], as shown in Table 1.

LDO1 Control Register (02h)

This register is used to enable LDO1 and set the output voltage V_{LDO1}.

LDO1[D3:D0]

These bits set the output voltage, V_{LDO1}, as shown in Table 2.

Table 2 — LDO1 Control Bits

LDO1_3	LDO1_2	LDO1_1	LDO1_0	V_{LDO1}
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1	0	1	0	2.4V
1	0	1	1	2.2V
1	1	0	0	1.8V
1	1	0	1	1.7V
1	1	1	0	1.6V
1	1	1	1	1.5V

LDO2 Control Register (03h)

This register is used to enable the LDO2 and to set the output voltage V_{LDO2}.

LDO2[D2:D0]

These bits are used to set the output voltage, V_{LDO2}, as shown in Table 3.

Table 3 — LDO2 Control Bits

LDO2_2	LDO2_1	LDO2_0	V_{LDO2}
0	0	0	OFF
0	0	1	1.8V
0	1	0	1.7V
0	1	1	1.6V
1	0	0	1.5V
1	0	1	1.4V
1	1	0	1.3V
1	1	1	1.2V

Fade Control Register (04h)

This register is used to enable the backlight fade and to set the rise and fall rate at which fading proceeds.

FADE[D2:D1]

These bits are used to set the rise/fall rate between two backlight currents as shown in Table 4.

Table 4 — Fade Control Bits

FADE_1	FADE_0	Fade Feature Rise/Fall Rate (ms/step)
0	0	32
0	1	24
1	0	16
1	1	8

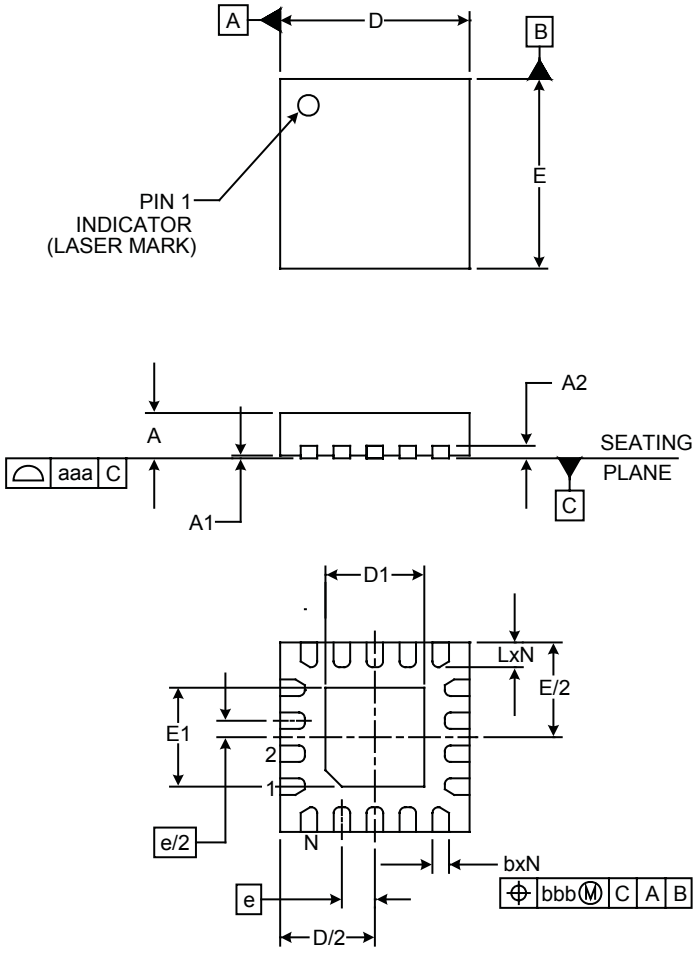
The number of steps in changing the backlight current will be equal to the change in binary count of bits BL[4:0].

Register and Bit Definitions (continued)

FADE_EN [D0]

This bit is used to enable or disable the fade feature. When the fade function is enabled and a new backlight current is set, the backlight current will change from its current value to a new value set by bits BL[4:0] at a rate of 8ms to 32ms per step. A new backlight level cannot be written during an ongoing fade operation, but an ongoing fade operation may be cancelled by resetting the fade bit. Clearing the fade bit during an ongoing fade operation changes the backlight current immediately to the value of BL[4:0]. The number of counts to complete a fade operation equals the difference between the old and new backlight values to increment or decrement the BL[4:0] bits. If the fade bit is cleared, the current level will change immediately without the fade delay. The rate of fade may be changed dynamically, even while a fade operation is active, by writing new values to the FADE_1 and FADE_0 bits. The total fade time is determined by the number of steps between old and new backlight values, multiplied by the rate of fade in ms/step. The longest elapsed time for a full scale fade-out of the backlight is nominally 938ms when the default interval of 32ms is used.

Outline Drawing — MLPQ-UT-18 2.3x2.3

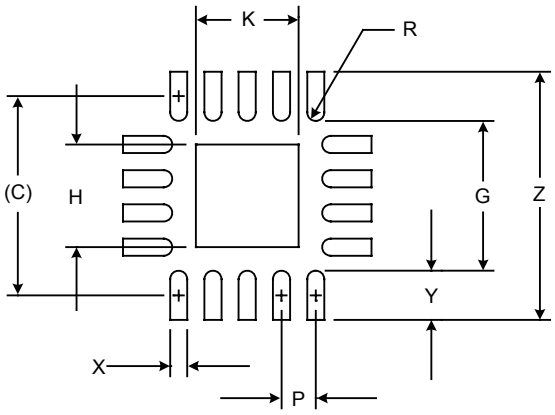


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	-	0.60
A1	0.00	-	0.05
A2		(0.152)	
b	0.15	0.20	0.25
D	2.20	2.30	2.40
D1	1.15	1.20	1.25
E	2.20	2.30	2.40
E1	1.15	1.20	1.25
e		0.40 BSC	
L	0.25	0.30	0.35
N		18	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-UT-18 2.3x2.3



DIMENSIONS	
DIM	MILLIMETERS
C	(2.33)
G	1.76
H	1.20
K	1.20
P	0.40
R	0.10
X	0.20
Y	0.57
Z	2.90

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

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