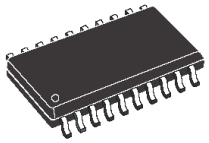
L6374

Industrial quad line driver

Features

- Four independent line drivers with 100 mA up to 35 V outputs
- Input signals between - 7 V and + 35 V, with pre-setting threshold
- Push-pull outputs with three state control and true zero current between Vs and ground
- Current limiting on each output effective in the full "ground to Vs" output voltage range
- Output voltage clamp to Vs and to ground
- Overtemperature and undervoltage protections
- Diagnostic for overtemperature, undervoltage and overcurrent
- Pre-setting delay for overcurrent diagnostic
- High speed operation: up to 300 kHz with 35 V swing



SO-20

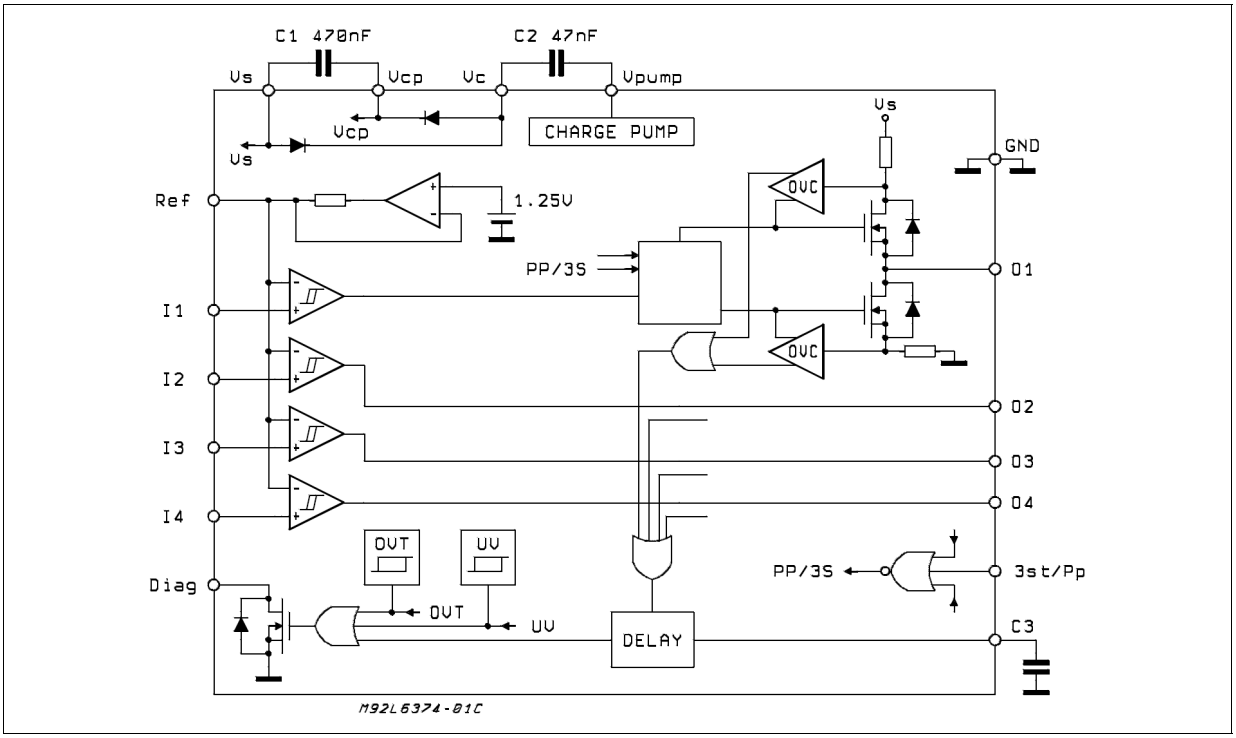
Description

The L6374 is especially designed to be used as a line driver in industrial control systems based on the 24 V signal levels (IEC 61131, 24VDC).

Table 1. Device summary

Order codes	Package	Packaging
L6374FP	SO-20	Tube
L6374FPT	SO-20	Tape and reel

Figure 1. Block diagram



Contents

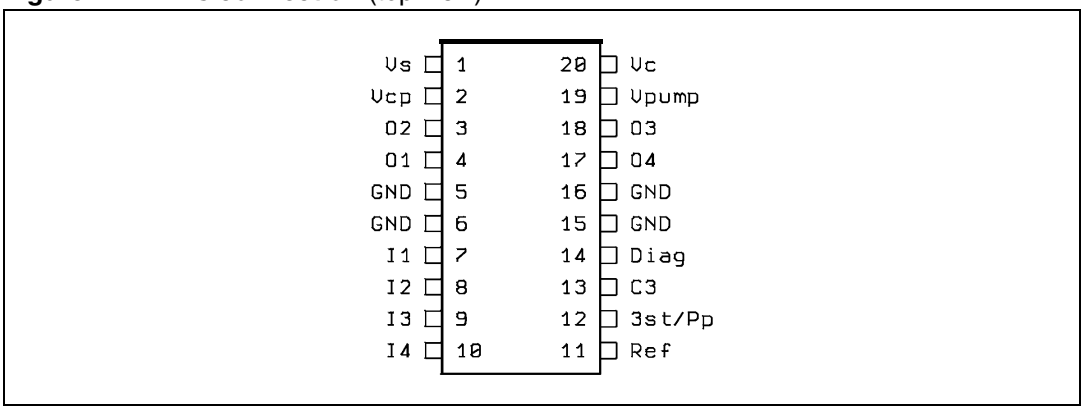
1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_S	1	Supply voltage ($t_W \leq 10$ ms)	50	V
		Supply voltage (DC)	40	V
V_{ilog}	12, 13	Logic input voltage (DC)	-0.3 to 7	V
I_{ilog}		Logic input forced current, per pin	±1	mA
I_i	7, 8, 9, 10	Channel input current (forced)	±2	mA
V_i		Channel input voltage	- 7 to 35	V
I_{out}	3, 4, 17, 18	Output current (forced, apart from inductive load)	±100	mA
		Output current (forced, apart from inductive load) same $t_W \leq 10$ ms	±1	A
V_{out}		Output Voltage (forced, not resulting from an inductive kick)	-0.3 to V_S +0.3	V
I_{set}	11	Setting pin forced current	±1	mA
V_{set}		Setting pin forced voltage	-0.3 to 5	V
V_{diag}	14	External voltage	-0.3 to 35	V
I_{diag}		Externally forced current	-10 to 10	mA
V_{C3}	13	Voltage on the delay capacitor, externally forced	-0.3 to 4.5	V
T_{op}		Ambient temperature, operating range	-25 to 85	°C
T_J		Junction temperature, operating range (see overtemperature protection)	-25 to 125	°C
T_{stg}		Storage temperature	-55 to 150	°C

2 Pin connections

Figure 2. Pins connection (top view)



3 Electrical characteristics

Table 3. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
DC operation (V_S = 24 V; T_J = -25 to 125 °C; unless otherwise specified)							
V_S	1	Supply voltage		10.8		35	V
V_{sh}		UV upperthreshold		9		10.8	V
H_{ys1}		UV hysteresis		250	450	650	mV
I_{qsc}		Quiescent current	Outputs open		3	5	mA
V_{ref}	11	Input comparators reference voltage	Reference pin floating	1.05	1.25	1.35	V
I_{ref}		Sink/source current on reference pin	V_{ref} = 0 V	-30	-20	-10	µA
			V_{ref} = 5 V	10	20	30	µA
V_{th}	7, 8, 9, 10	Comparator threshold with external bias	V_S = 9 to 12 V	-0.2		2.0	V
			V_S = 12 to 35 V	-0.2		5.0	V
V_{il}		Input low level	V_{REF} externally biased	-7		V_{REF} -0.2	V
			Pin V_{REF} floating	-7		0.8	V
V_{ih}		Input high level	V_{REF} externally biased	V_{REF} +0.2		35	V
			Pin V_{REF} floating	2		35	V
V_i		Input voltage (operative range)		-7		35	V
I_{bias}		Input bias current	$0 < V_i < V_S$	-1		1	µA
			V_i = -7 V	-1	-0.5	-0.1	mA
Hys_2		Input comparators hysteresis	See analog inputs sections	100	200	350	mV
T_h		OVT upper threshold			170		°C
H_T		OVT hysteresis			20		°C
I_{sc}	3, 4, 17, 18	Current limit	V_i = -7 to V_S; V_{out} = 0 to V_S;	110	200	300	mA
V_{on}		Internal voltage drop @ rated current	I_{out} = ±100mA; sourced @ high output, sunk @ low output T_J = 125 °C		400	600	mV
			Same, T_J = 25 °C		250	400	mV
I_{lkg}		Output 3-state leakage current	V_{out} = 0 to V_S	-25		25	µA
V_{in}	12	Push-pull mode request		-0.2		0.8	V
		3-state mode request		2		5.5	V
I_{in}		Input current	V_i = 0 V		10	25	µA
I_{dlkg}	14	Diagnostic output leakage	Diagnostic OFF; V_{diag} = 24 V			5	µA
V_{diag}		Diagnostic output voltage drop	I_{diag} = 5 mA		200	500	mV

Table 3. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
AC operation (V_S = 10.8 to 35 V; T_J = -25 to 125 °C; I_{out} = 100 mA; unless otherwise specified; see switching waveforms diagrams)							
t_{dr}	7 to 4 8 to 3 9 to18 10 to 17	Delay time on rising edge	R_l to ground		1000	1500	ns
			R_l to V_S		500	1000	ns
t_{df}		Delay time on falling edge	R_l to ground		500	1000	ns
			R_l to V_S		1000	1500	ns
t_r	3, 4, 17,18	Rise time	R_l to ground		120	250	ns
			R_l to V_S		120	250	ns
t_f		Fall time	R_l to ground		150	300	ns
			R_l to V_S		150	300	ns

4 Thermal characteristics

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJP}	Thermal resistance, junction to pin	17	°C/W
R_{thJA1}	Thermal resistance, junction to ambient (see thermal characteristics)	65	°C/W
R_{thJA2}	Thermal resistance, junction to ambient (see thermal characteristics)	80	°C/W

4.1 R_{thJP}

The reference point is the knee on the four central pins, where the pins are upwardly bent and the soldering joint with the PCB footprint can be made.

4.2 R_{thJA1}

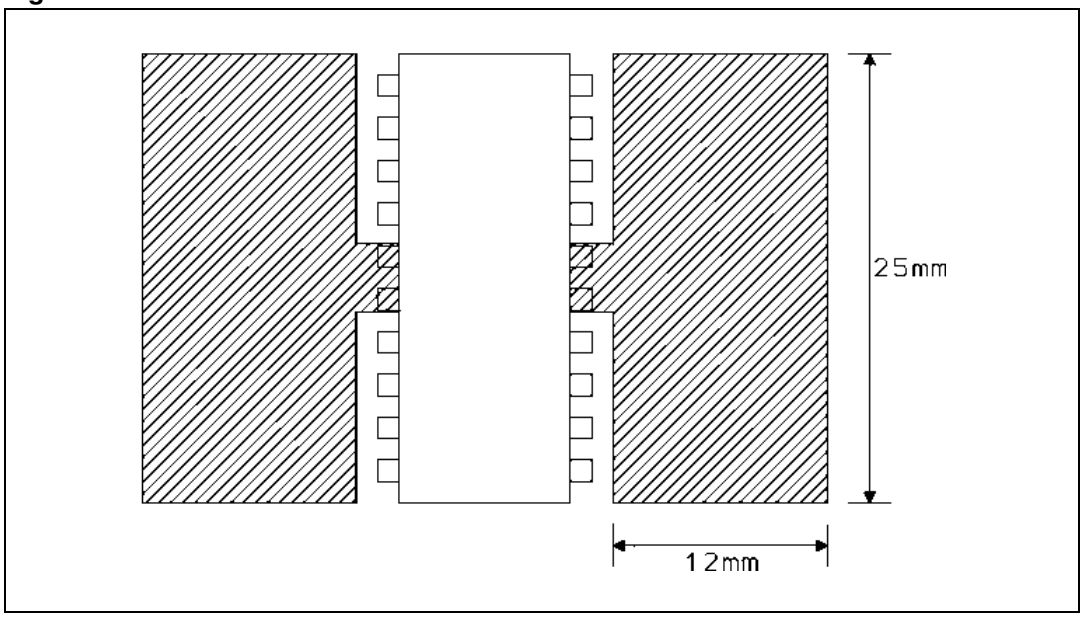
If a dissipating surface, thick at least 35 µm, and with a surface similar or bigger than the one shown, is created making use of the printed circuit. Such heatsinking surface is considered on the bottom side of an horizontal PCB (worst case).

4.3 R_{thJA2}

If the power dissipating pins (the four central ones), as well as the others, have a minimum thermal connection with the external world (very thin strips only) so that the dissipation takes place through still air and through the PCB itself.

It is the same situation of point above, without any heatsinking surface created on purpose on the board.

Figure 3. Printed heatsink



5 Overtemperature protection (OVT)

If the chip temperature exceeds T_h (measured in a central position in the chip) the chip deactivates itself.

The following actions are taken:

- all the output stages are forced in the "three state" condition, i.e. are disconnected from the output pins; only the clamping diodes at the outputs remain active;
- the signal Diag is activated (active low).

Normal operation is resumed as soon as (typically after some seconds) the chip temperature monitored goes back below T_h -H_T.

The different upper and lower thresholds with hysteretic behavior, assure that no intermittent conditions can be generated.

6 Undervoltage protection (UV)

The supply voltage is expected to range from 11 V to 35 V, even if its reference value is considered to be 24 V.

In this range the L6374 operates correctly. Below 10.8 V the overall system has to be considered not reliable.

Consequently the supply voltage is monitored continuously and a signal, called UV, is internally generated and used.

The signal is "on" as long as the supply voltage does not reach the upper internal threshold of the V_s comparator (called V_{sh}). The UV signal disappears above V_{sh}.

Once the UV signal has been removed, the supply voltage must decrease below the lower threshold (i.e. below V_{sh} -H_{ys1}) before it is turned on again.

The hysteresis H_{ys1} is provided to prevent intermittent operation of the device at low supply voltages that may have a superimposed ripple around the average value.

The UV signal inhibits the outputs, putting them in three-state, but has no effect on the creation of the reference voltages for the internal comparators, nor on the continuous operation of the charge-pump circuits.

7 Diagnostic logic

The situations that are monitored and signalled with the Diag output pin are:

- current limit (OVC) in action; there are 8 individual current limiting circuits, two per each output, i.e. one per every output transistor; they limit the current that can be either sourced or sunk from each output, to a typical value of 150 mA, equal for all of them;
- undervoltage protection (UV);
- overtemperature protection (OVP); The diagnostic signal is transmitted via an open drain output (for ease of wired-or connection of several such signals) and a low level represents the presence of at least one of the monitored conditions, mentioned above.

8 Programmable delay

The current limiting circuits can be requested to perform even in absence of a real fault condition, for a short period, if the load is of capacitive nature or if it is a filament lamp (that exhibits a very low resistance during the initial heating phase). To avoid the forwarding of misleading, short diagnostic pulses in coincidence with the intervention of the current limiting circuits when operating on capacitive loads, a delay of about 5 µs is inserted on the signal path, between the "OR" of the current limit signals and its use as external diagnostic. It takes about 1µs to charge (or discharge) by 24 V a capacitor of 5 nF with a current of 120 mA . To implement longer delays (from the intervention of one of the current limiting circuits to the activation of the diagnostic) an external capacitor can be connected between pin C3 and ground (pin C3 is otherwise left open).

The delay shall then be determined by the ratio of about 10 pF/µs, using the value of the capacitance connected to the pin.

9 Analog inputs (I1,I2,I3,I4)

The input stage of each channel is a high im-pedence comparator with built-in hysteresis (200 mV) for high noise immunity. Each comparator has one input connected to all the others and tied to a common pin Ref (Pin 11). If this pin is left floating an internal precise band gap voltage reference (1.25 V) is applied, otherwise these inputs can be externally programmed by connecting an external voltage source (from 0 to 5 V) and the current on this pin is internally limited to ±20 mA. The other input pin of each comparator can swing from -7 to 35 V.

For this reason it has been implemented the structure shown in *Figure 4 on page 10* and the device can also be used as line receiver.

When the input voltage is negative, the current is internally limited by a 15 kΩ resistor as shown in *Figure 4 on page 10*. High and low input thresholds can be obtained by adding and subtracting half of the hysteresis to the voltage of pin Ref (see *Figure 5 on page 10*).

10 State / push-pull input

The input 3st/Pp is instead intended for a digital incoming signal. It has an internal threshold set at 1.26 V; an internal bias circuit (10 mA typical) simulates a high level (three-state) if the pin is disconnected.

Figure 4. Equivalent input circuit

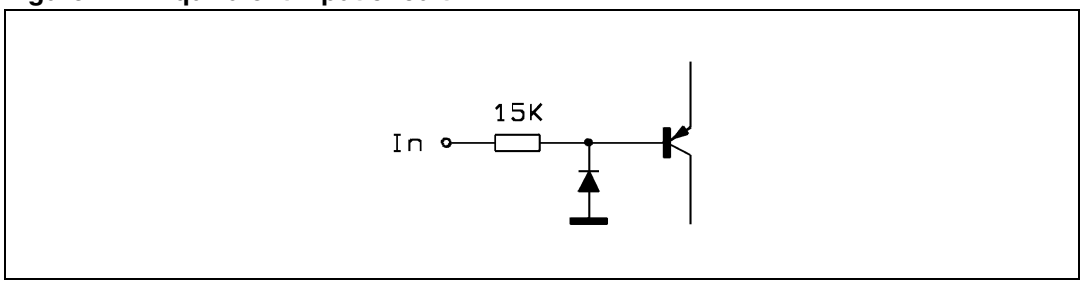
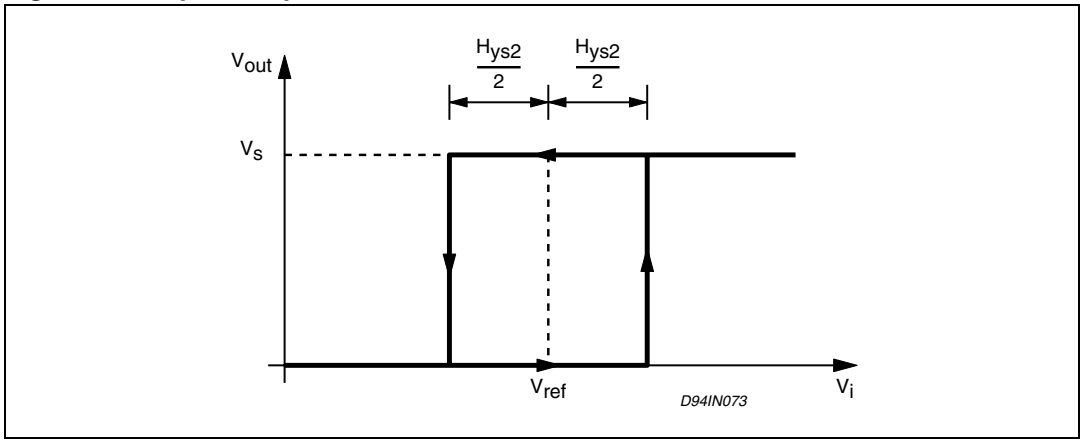


Figure 5. Input comparator threshold



11 The switching of the output stage

The cross conduction of the two transistors of an output stage of the L6374 would be significantly noisy, because the transistors here can carry peak currents in excess of 100 mA, and even more in the few nanoseconds before the current limiting circuits are really effective.

Consequently the device has been designed so as to avoid such cross conduction. At every switching transition, first of all the transistor in conduction is turned OFF. Then, after a safe interval of around 200 ns, the other transistor is turned on.

When analyzing the switching cycle, and the associated switching times, it is useful to identify some subsequent phases:

- delay from the input pin to the output reaction;
- OFF transition in the output stage;
- dead time
- on transition in the output stage.

Figure 6. V_S = 35 V, 350 Ω connected to V_S/2.

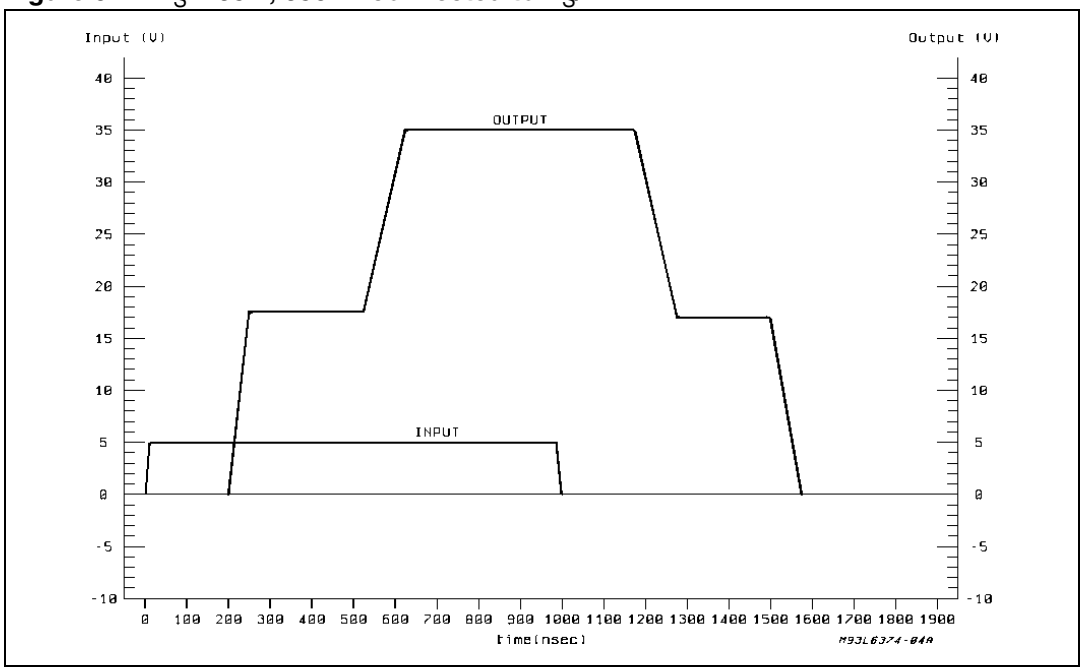


Figure 6 helps understand such sequence. In fact, with a purely resistive load connected to V_s/2 no parasitic elements interfere significantly. The waveform can be significantly less easy to in terpret if the load has not the perfect symmetry of that case, as showed below. For instance, it is enough to connect the resistive load to ground, or to V_s – as *Figure 7* and *Figure 8* – show to hide some of the switching phases described.

If the load is connected to ground, the waveform stays stuck to ground as long as the output stage is in high impedance; viceversa when the load is connected to Vs the waveform will linger close to the supply voltage as long as possible.

If an output load made of an inductor and a resistor in series is used, the inductive kick at the beginning of every output transition generates the equivalent effect of an "anticipated"

switching when the inductor can discharge; while the switching looks "delayed" if the output transition tends to initiate a charging phase (see *Figure 9*). With a load almost free from parasitic elements, the waveforms resemble the ones of the purely resistive cases.

With a real, more composite load, the effect of the inductive kick in comparison to the resistive load, would be more apparent.

With a capacitor and a resistor in parallel as a load, another type of waveform can be seen (reported in *Figure 10*).

As long as the output stage stays in the transient high impedance state, the output voltage will follow the classic exponential law of an RC relaxation.

As soon as the other transistor is switched on and takes charge, the waveform is quickly forcibly brought to its steady state value.

From the above it is possible to see how the switching times, inherently very fast, of the output stages, may be difficult to identify in a waveform if the output load is not accurately taken into consideration.

Figure 11 show typical switching waveform for inputs and outputs.

Figure 7. V_S = 35 V, 350 Ω connected to ground

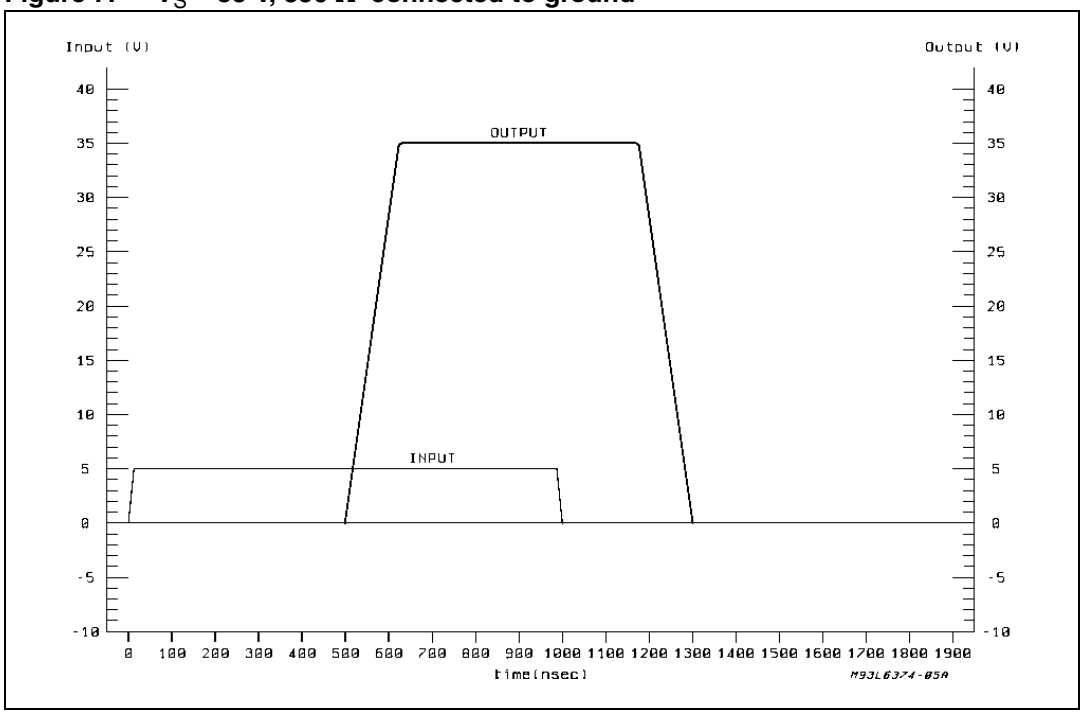


Figure 8. V_S = 35 V, 350 Ω connected to V_S

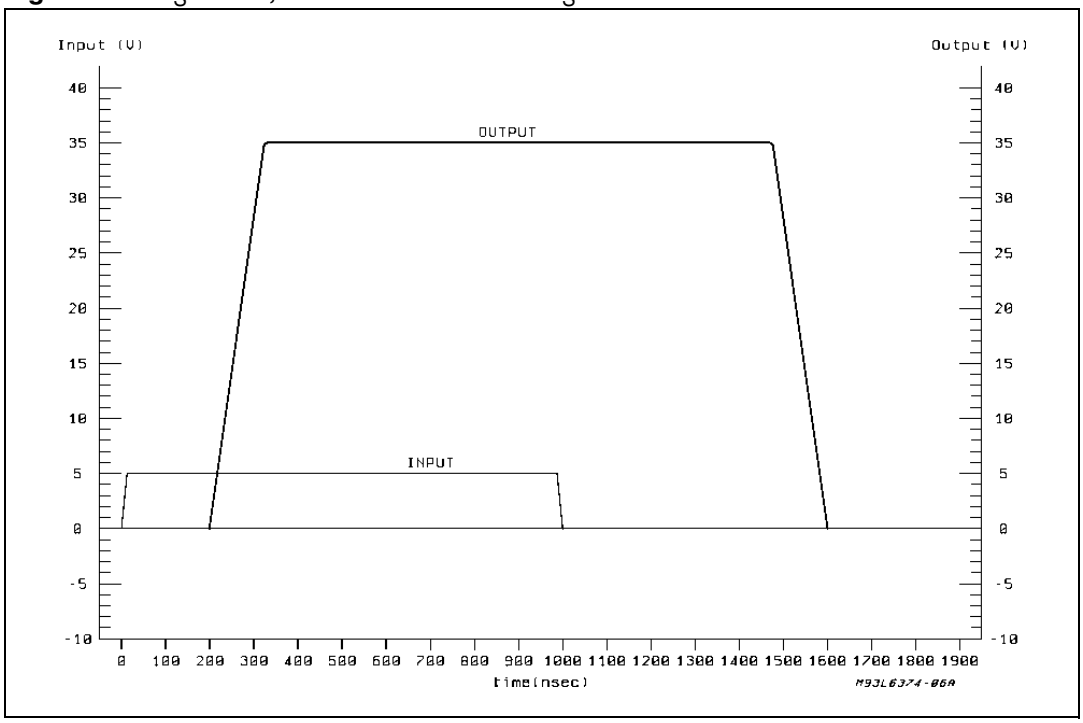


Figure 9. V_S = 35 V, 350 Ω and 1 mH connected to ground.

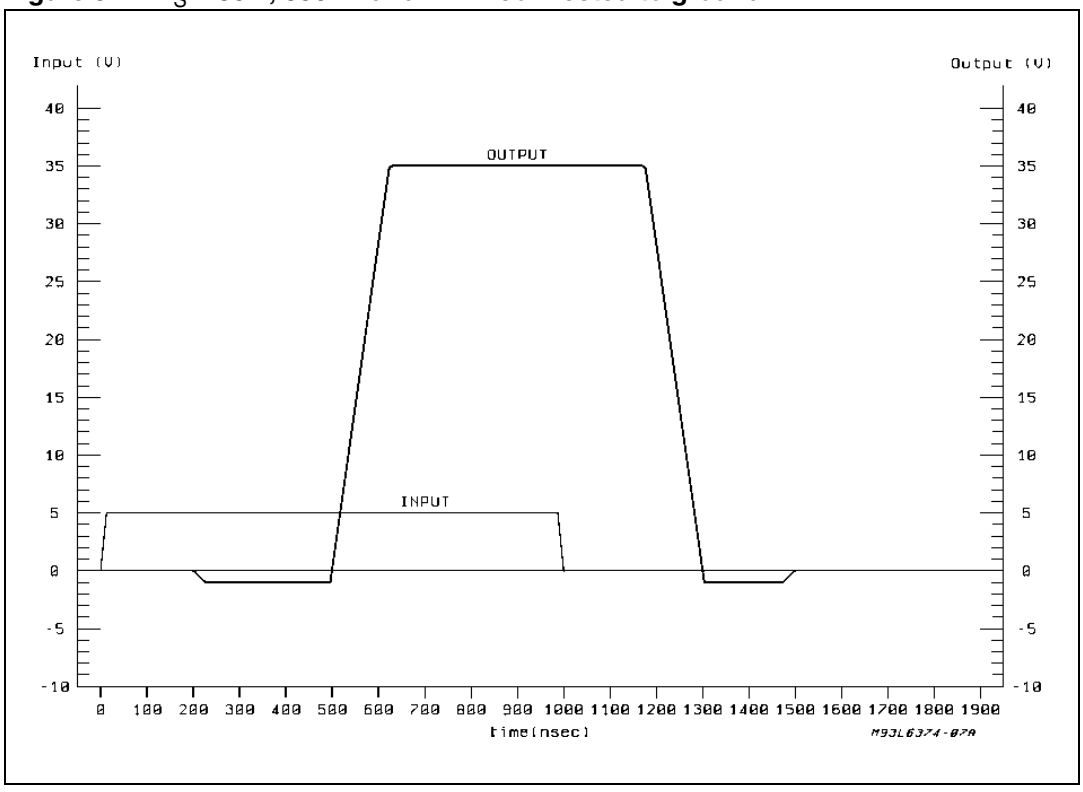


Figure 10. V_S = 35 V, 350 Ω || 1 nF connected to ground.

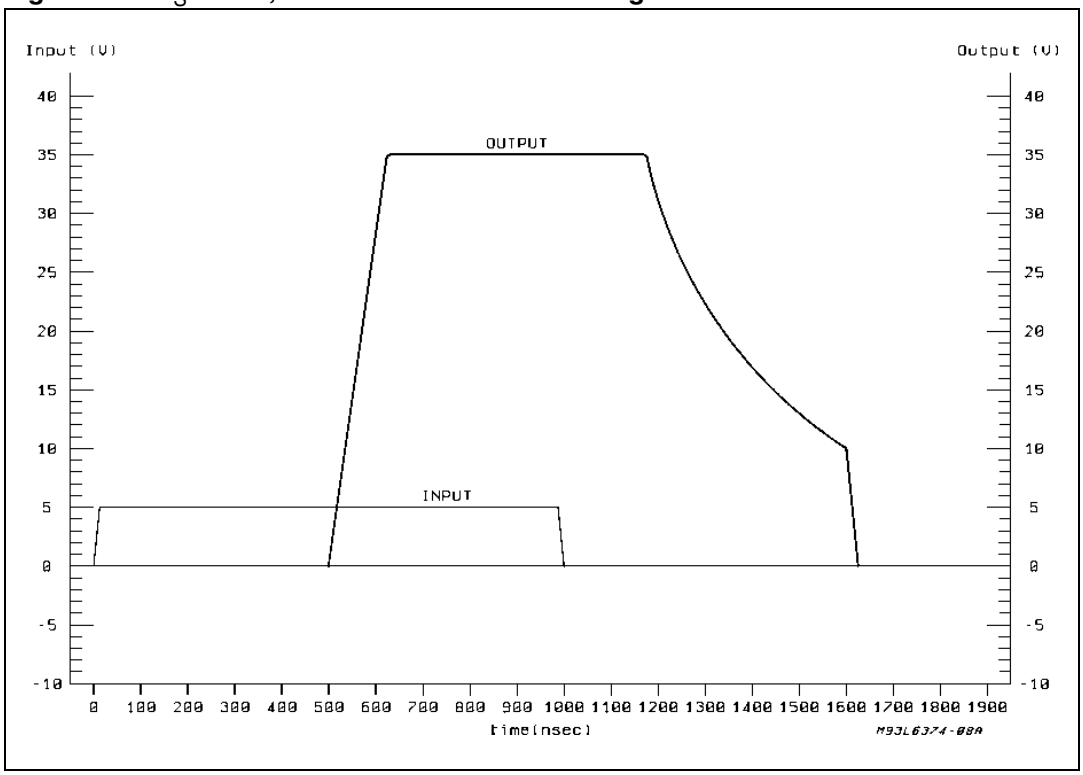
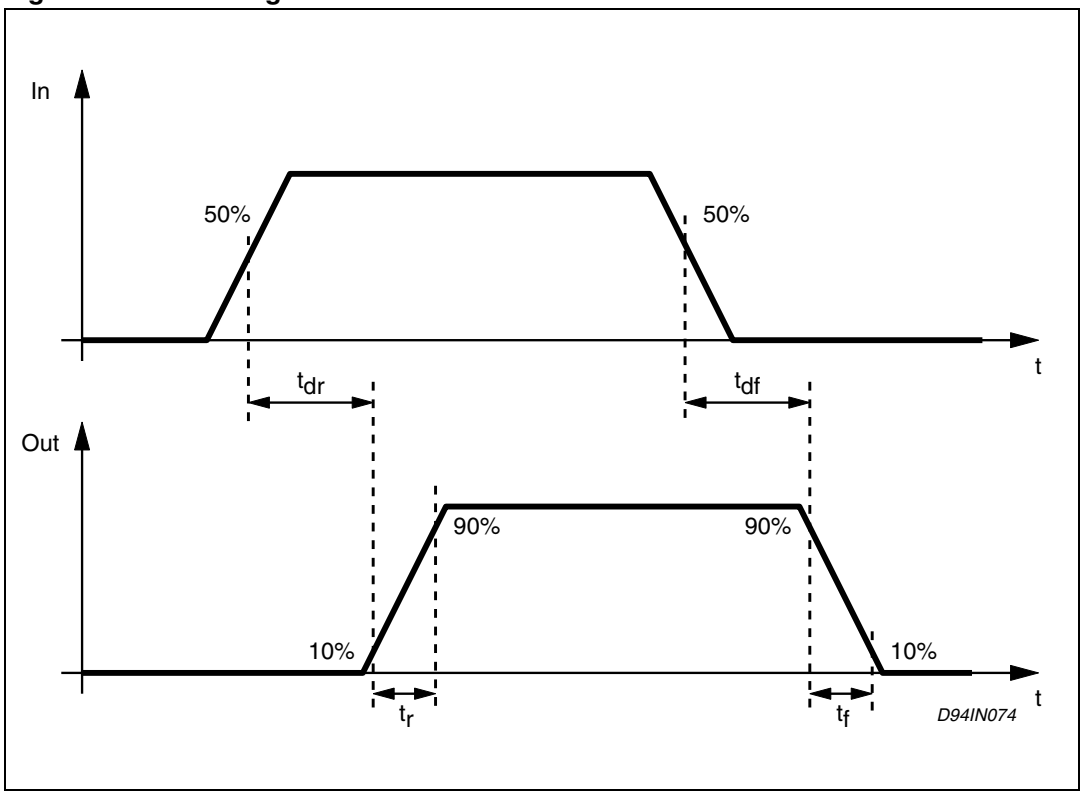


Figure 11. Switching waveforms.



12 Application note

It is recommended not to leave the Ref pin (pin 11) floating: if not used with an external voltage reference, it is better to connect an external capacitor (of at least 10 nF) between this pin and ground.

This capacitor filters the voltage reference against voltage spikes that can be generated by the commutation of the output stages.

This is very common using capacitive loads: in fact, the initial transient of such loads behaves like a short circuit, so the current flowing through the outputs presents very high spikes.

Moreover, if the device is used as a line receiver. (i.e. the input signals can go below ground) it is required not to leave the Ref pin (pin 11) floating: in this case, the pin can be connected to ground or to a fixed external voltage reference.

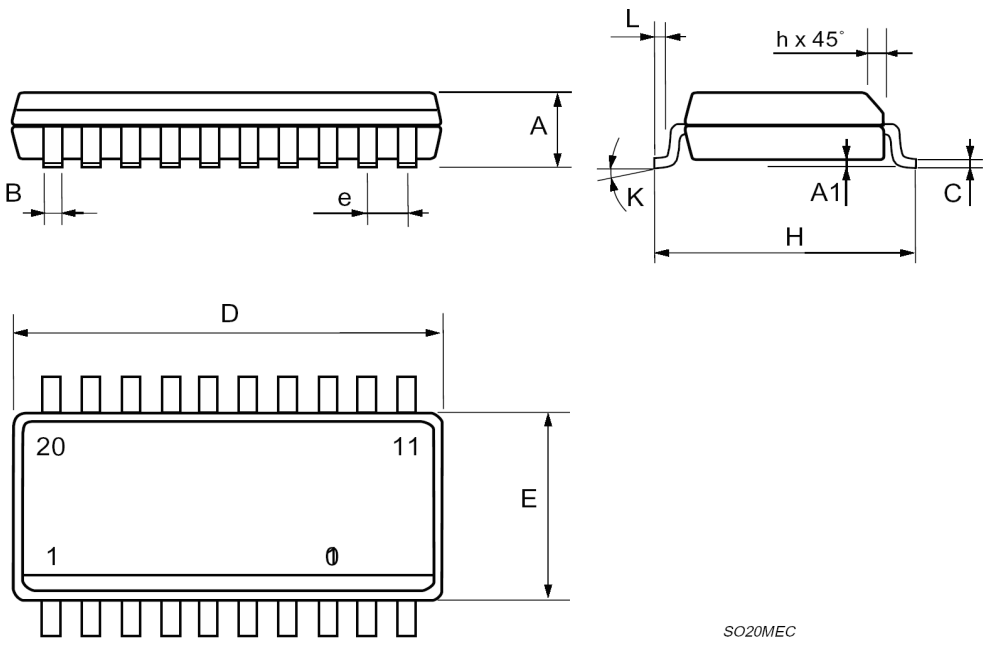
13 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 5. SO-20 mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

Figure 12. Package dimensions



14 Revision history

Table 6. Document revision history

Date	Revision	Changes
August 2003	1	First Issue
June 2004	2	Technical migration from ST-PRESS to EDOCS.
03-Mar-2008	3	Modified: Removed obsolete package DIP-20

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