

## H-Bridge Drivers for DC Brush Motors

# Dual H-Bridge Driver

**BD6735FV**

### General Description

The BD6735FV provides a dual H-bridge motor driver which features wide range of motor power supply voltage from 2.0V to 8.0V and low power consumption to switch low ON-Resistance DMOS transistors. This small surface mounting package is most suitable for mobile system, home appliance and various applications.

### Features

- Low ON-Resistance Power DMOS Output
- Charge Pump for the High-Side DMOS Gates
- Drive Mode Switch Function
- Under Voltage Locked Out Protection & Thermal Shut Down Circuit

### Applications

- Mobile system
- Home appliance
- Amusement system, etc

### Key Specifications

- Power Supply Voltage Range: 2.0V to 8.0V
- Motor Power Supply Voltage Range: 2.0V to 8.0V
- Circuit Current: 2.0mA(Typ)
- Stand-By Current: 1μA (Max)
- Control Input Voltage Range: 0V to V<sub>CC</sub>V
- Logic Input Frequency: 100kHz(Max)
- Minimum Logic Input Pulse Width: 0.5μs(Min)
- H-Bridge Output Current (DC): -1.0A to +1.0A
- Output ON-Resistance (Total): 1.0Ω(Typ)
- Operating Temperature Range: -30°C to +75°C

### Package

SSOP-B20

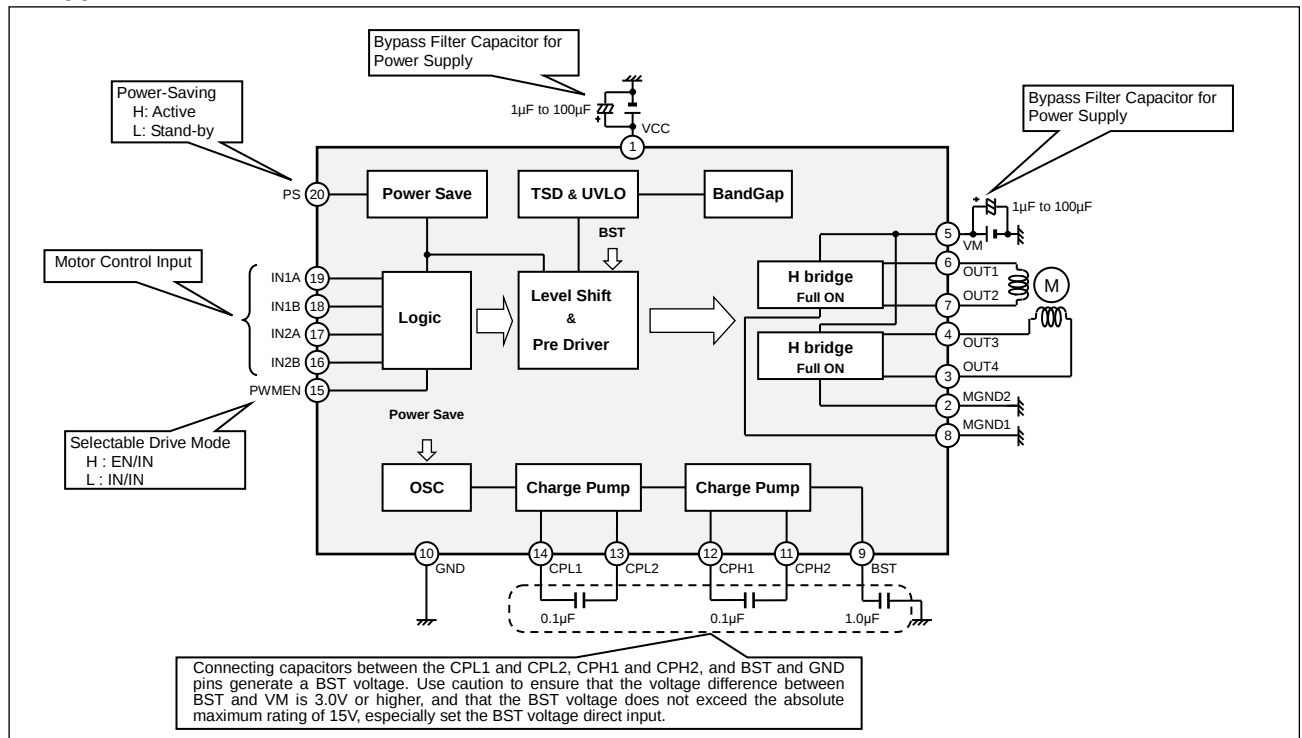
**W(Typ) x D(Typ) x H(Max)**

6.50mm x 6.40mm x 1.45mm



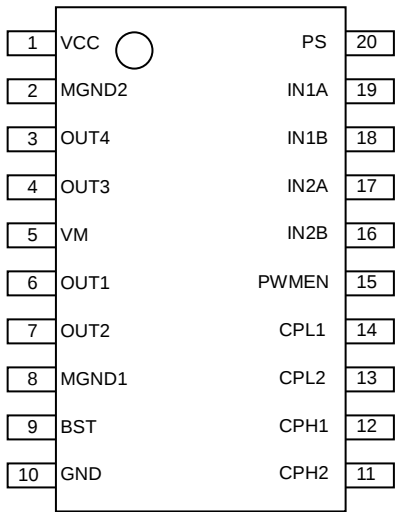
SSOP-B20

### Typical Application Circuit



Pin Configuration

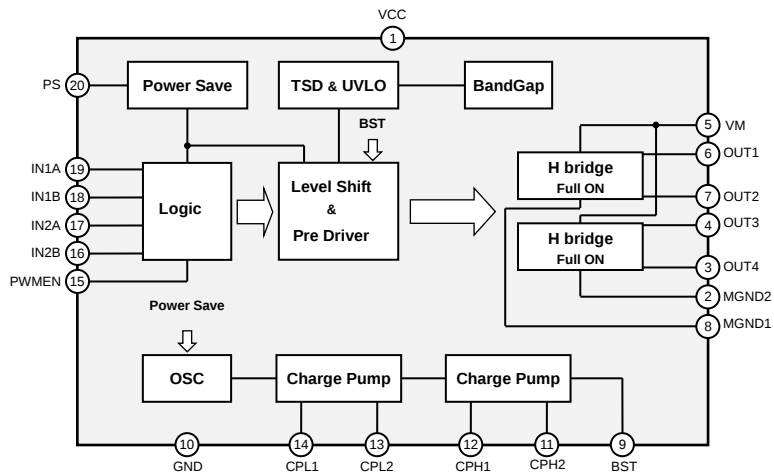
(TOP VIEW)



Pin Description

| Pin No. | Pin Name | Function                          | Pin No. | Pin Name | Function                                      |
|---------|----------|-----------------------------------|---------|----------|-----------------------------------------------|
| 1       | VCC      | Power supply                      | 11      | CPH2     | 2 <sup>nd</sup> Bucket stage with capacitor 2 |
| 2       | MGND2    | Motor ground 2                    | 12      | CPH1     | 2 <sup>nd</sup> Bucket stage with capacitor 1 |
| 3       | OUT4     | H-bridge output 4                 | 13      | CPL2     | 1 <sup>st</sup> Bucket stage with capacitor 2 |
| 4       | OUT3     | H-bridge output 3                 | 14      | CPL1     | 1 <sup>st</sup> Bucket stage with capacitor 1 |
| 5       | VM       | Motor power supply                | 15      | PWMEN    | Drive mode logic input                        |
| 6       | OUT1     | H-bridge output 1                 | 16      | IN2B     | Control logic input 2B                        |
| 7       | OUT2     | H-bridge output 2                 | 17      | IN2A     | Control logic input 2A                        |
| 8       | MGND1    | Motor ground 1                    | 18      | IN1B     | Control logic input 1B                        |
| 9       | BST      | Charge pump output with capacitor | 19      | IN1A     | Control logic input 1A                        |
| 10      | GND      | Ground                            | 20      | PS       | Power-saving function                         |

Block Diagram



## Description of Blocks

1. Power-Saving Function  
A power-saving function is included, which allows the system to save power when not driving the motor. The voltage level on this pin should be set high so as to keep the operation mode. (See the Electrical Characteristics; p.4/12)
2. Motor Control Input
  - (a) IN1A, IN1B, IN2A and IN2B Pins  
Logic level controls the output logic of H-Bridge.  
(See the Electrical Characteristics; p.4/12, and I/O Truth Table; p.6/12)
  - (b) PWMEN Pin  
Logic level sets the IN/IN or EN/IN drive mode.  
(See the Electrical Characteristics; p.4/12, and I/O Truth Table; p.6/12)
3. H-Bridge  
Each H-bridge can be controlled independently. It is therefore possible to drive the H-bridges simultaneously, as long as the package thermal tolerances are not exceeded. Because the output transistors consist of power DMOS that can be controlled the charge pump output  $V_{BST}$ , the total ON-Resistance of high and low-side transistor is dependent on BST voltage  $V_{BST}$ .
4. Charge Pump  
The BD6735FV includes charge pump circuit which is used to generate a supply above  $V_M$  to drive the high-side DMOS gates. Three external capacitors should be connected between CPL1 and CPL2, CPH1 and CPH2, BST and GND pin. The voltage difference between BST and VM must be 3.0V or higher where the BST voltage  $V_{BST}$  must not exceed the absolute maximum rating of 15.0V in order to ensure better performance.

## Absolute Maximum Ratings

| Parameter                          | Symbol     | Rating                           | Unit |
|------------------------------------|------------|----------------------------------|------|
| Power Supply Voltage               | $V_{CC}$   | -0.5 to +10.0                    | V    |
| Motor Power Supply Voltage         | $V_M$      | -0.5 to +10.0                    | V    |
| Charge Pump Step-up Supply Voltage | $V_{BST}$  | -0.5 to +15.0                    | V    |
| Control Input Voltage              | $V_{IN}$   | -0.5 to $+V_{CC}+0.5$            | V    |
| Power Dissipation                  | $P_d$      | 0.81 <sup>(Note 1)</sup>         | W    |
| H-bridge Output Current (DC)       | $I_{OUT}$  | -1.0 to +1.0 <sup>(Note 2)</sup> | A    |
| Storage Temperature Range          | $T_{stg}$  | -55 to +150                      | °C   |
| Junction Temperature               | $T_{jmax}$ | 150                              | °C   |

(Note 1) Reduced by 6.48mW/°C over 25°C, when mounted on a glass epoxy board (70mm x 70mm x 1.6mm).

(Note 2) Must not exceed  $P_d$ , ASO, or  $T_{jmax}$  of 150°C

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions

| Parameter                       | Symbol    | Min | Typ | Max      | Unit |
|---------------------------------|-----------|-----|-----|----------|------|
| Power Supply Voltage            | $V_{CC}$  | 2.0 | -   | 8.0      | V    |
| Motor Power Supply Voltage      | $V_M$     | 2.0 | -   | 8.0      | V    |
| Control Input Voltage           | $V_{IN}$  | 0   | -   | $V_{CC}$ | V    |
| Logic Input Frequency           | $F_{IN}$  | 0   | -   | 100      | kHz  |
| Minimum Logic Input Pulse Width | $T_{IN}$  | 0.5 | -   | -        | μs   |
| Operating Temperature Range     | $T_{opr}$ | -30 | -   | +75      | °C   |

**Electrical Characteristics (Unless otherwise specified  $V_{CC}=5.0V$ ,  $V_M=5.0V$ ,  $T_a=25^{\circ}C$ )**

| Parameter                                        | Symbol     | Min  | Typ | Max      | Unit     | Conditions                                  |
|--------------------------------------------------|------------|------|-----|----------|----------|---------------------------------------------|
| All Circuits                                     |            |      |     |          |          |                                             |
| Stand-by Current                                 | $I_{CCST}$ | -    | 0   | 1        | $\mu A$  | $V_{PS}=0V$                                 |
| Circuit Current                                  | $I_{CC}$   | 0.5  | 2.0 | 4.0      | mA       | $V_{PS}=5V$ , $f_{IN}=100kHz$               |
| PS Input (PS)                                    |            |      |     |          |          |                                             |
| High-Level Input Voltage                         | $V_{PSH}$  | 2.0  | -   | $V_{CC}$ | V        |                                             |
| Low-Level Input Voltage                          | $V_{PSL}$  | -0.3 | -   | +0.5     | V        |                                             |
| High-Level Input Current                         | $I_{PSH}$  | 25   | 50  | 100      | $\mu A$  | $V_{PS}=5V$                                 |
| Low-Level Input Current                          | $I_{PSL}$  | -1   | 0   | +1       | $\mu A$  | $V_{PS}=0V$                                 |
| Control Input (IN=IN1A, IN1B, IN2A, IN2B, PWMEN) |            |      |     |          |          |                                             |
| High-Level Input Voltage                         | $V_{INH}$  | 2.0  | -   | $V_{CC}$ | V        |                                             |
| Low-Level Input Voltage                          | $V_{INL}$  | -0.3 | -   | +0.7     | V        |                                             |
| High-Level Input Current                         | $I_{INH}$  | 25   | 50  | 100      | $\mu A$  | $V_{IN}=5V$                                 |
| Low-Level Input Current                          | $I_{INL}$  | -1   | 0   | +1       | $\mu A$  | $V_{IN}=0V$                                 |
| UVLO                                             |            |      |     |          |          |                                             |
| UVLO Voltage                                     | $V_{UVLO}$ | 1.5  | -   | 1.9      | V        |                                             |
| Full ON Type H-Bridge Driver                     |            |      |     |          |          |                                             |
| Output On-Resistance                             | $R_{ON}$   | -    | 1.0 | 1.35     | $\Omega$ | $I_{OUT}=\pm 700mA$ , High & Low-side total |

Typical Performance Curves (Reference data)

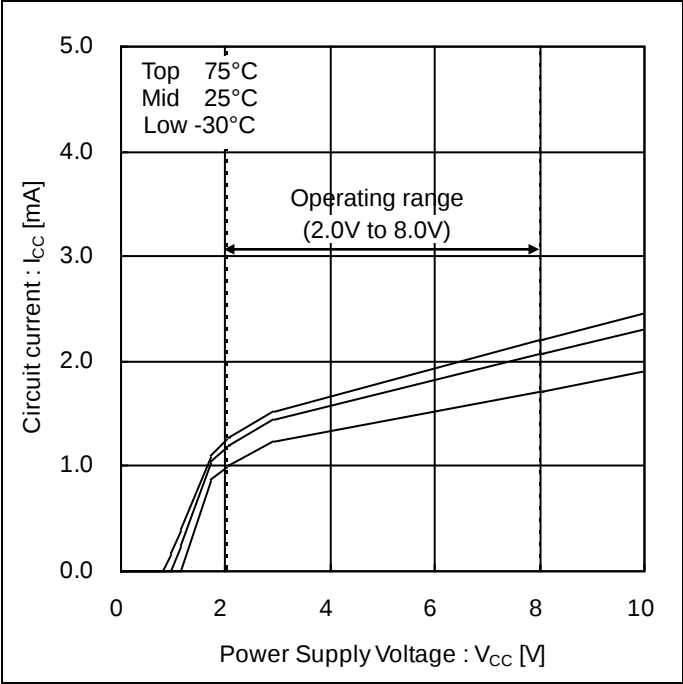


Figure 1.  
Circuit Current vs Power Supply Voltage  
(Operation Mode)

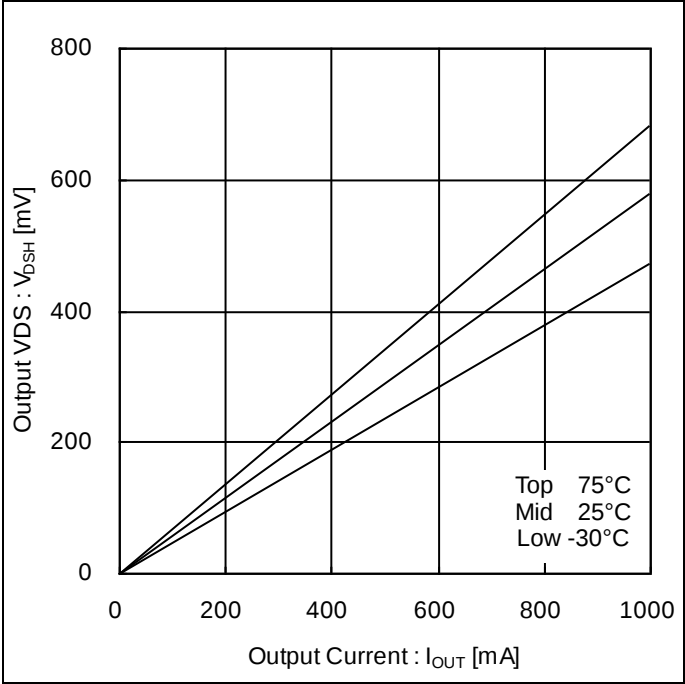


Figure 2.  
Output VDS vs Power Output Current  
(Output On-Resistance on high-side,  $V_M=5V$ ,  $V_{CC}=5V$ )

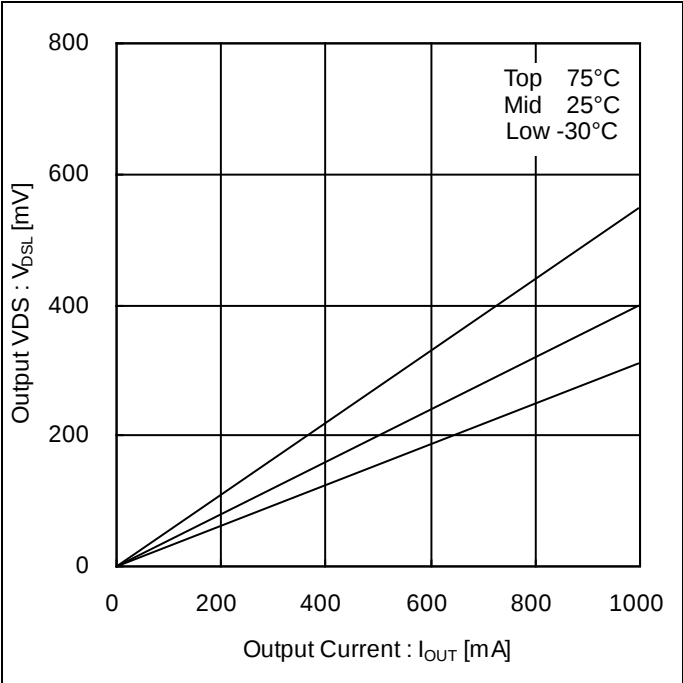


Figure 3.  
Output VDS vs Power Output Current  
(Output On-Resistance on low-side,  $V_M=5V$ ,  $V_{CC}=5V$ )

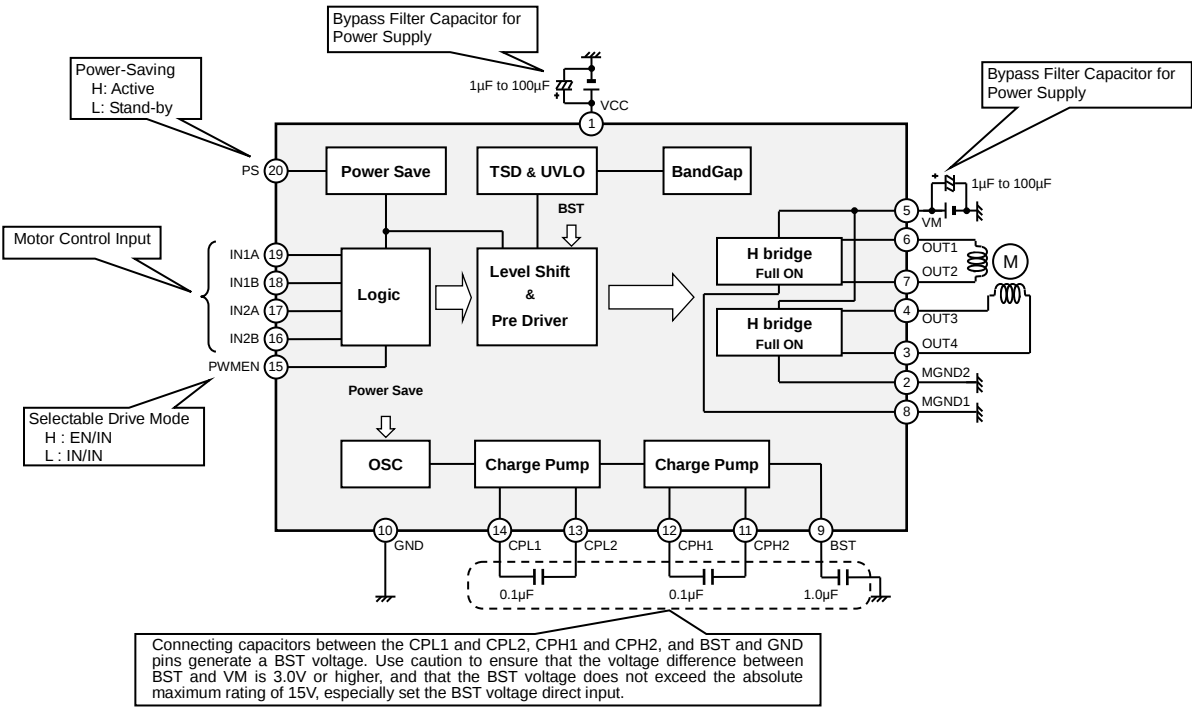
Timing Chart

Table 1. I/O Truth Table

| Input Mode | INPUT                  |     |         |         | OUTPUT |        |                                 |
|------------|------------------------|-----|---------|---------|--------|--------|---------------------------------|
|            | PS <sup>(Note 3)</sup> | PWM | IN1A/2A | IN1B/2B | OUT1/3 | OUT2/4 | Output Mode <sup>(Note 4)</sup> |
| EN/IN      | H                      | H   | L       | X       | L      | L      | Short Brake                     |
|            |                        |     | H       | L       | H      | L      | CW                              |
|            |                        |     | H       | H       | L      | H      | CCW                             |
| IN/IN      |                        | L   | L       | L       | Z      | Z      | Open                            |
|            |                        |     | H       | L       | H      | L      | CW                              |
|            |                        |     | L       | H       | L      | H      | CCW                             |
|            |                        |     | H       | H       | L      | L      | Short Brake                     |
| -          | L                      | X   | X       | X       | Z      | Z      | Open                            |

L: Low, H: High, X: Don't care, Z: Hi impedance  
(Note 3)PS=High: Operation Mode, PS=Low: Stand-by Mode  
(Note 4)CW: Current flows from OUT1 to OUT2 and OUT3 to OUT4, CCW: Current flows from OUT2 to OUT1 and OUT4 to OUT3

Application Example



Selection of Components Externally Connected

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

Power Dissipation

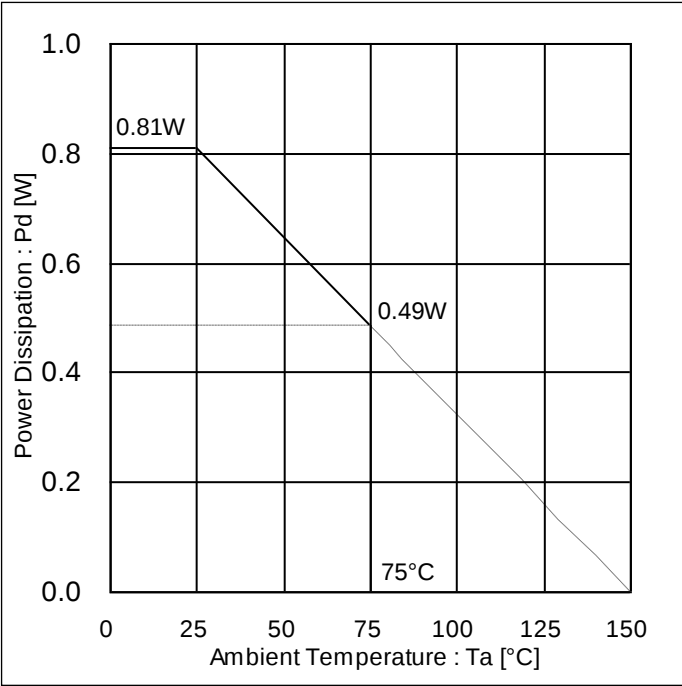


Figure 4.  
Power Dissipation vs Ambient Temperature

I/O Equivalent Circuits

| PS         | IN1A, IN1B, IN2A, IN2B, PWMEN | VM, MGND1, MGND2, OUT1 to OUT4 |
|------------|-------------------------------|--------------------------------|
|            |                               |                                |
| CPH1, CPL1 | BST, CPH2, CPL2               |                                |
|            |                               |                                |

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal(GND) and large-current ground(MGND) traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

**12. Regarding the Input Pin of the IC**

This monolithic IC contains P<sup>+</sup> isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

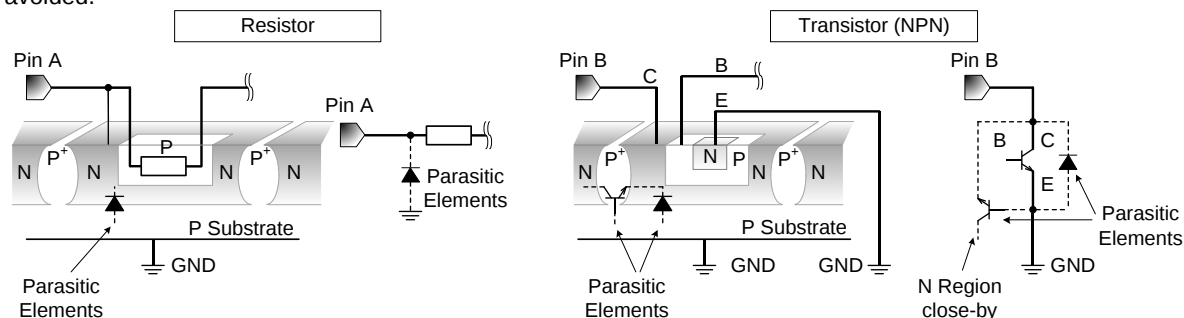


Figure 5.

Example of monolithic IC structure

**13. Ceramic Capacitor**

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**14. Area of Safe Operation (ASO)**

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

**15. Thermal Shutdown Circuit(TSD)**

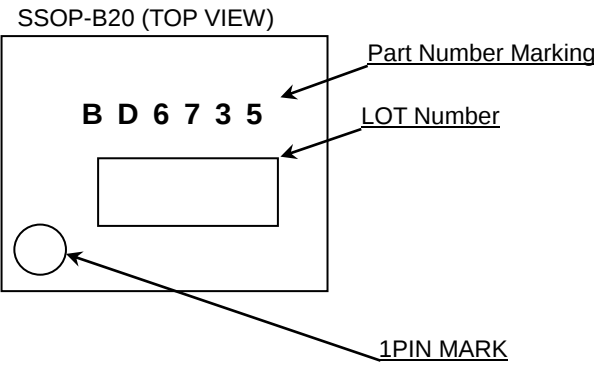
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

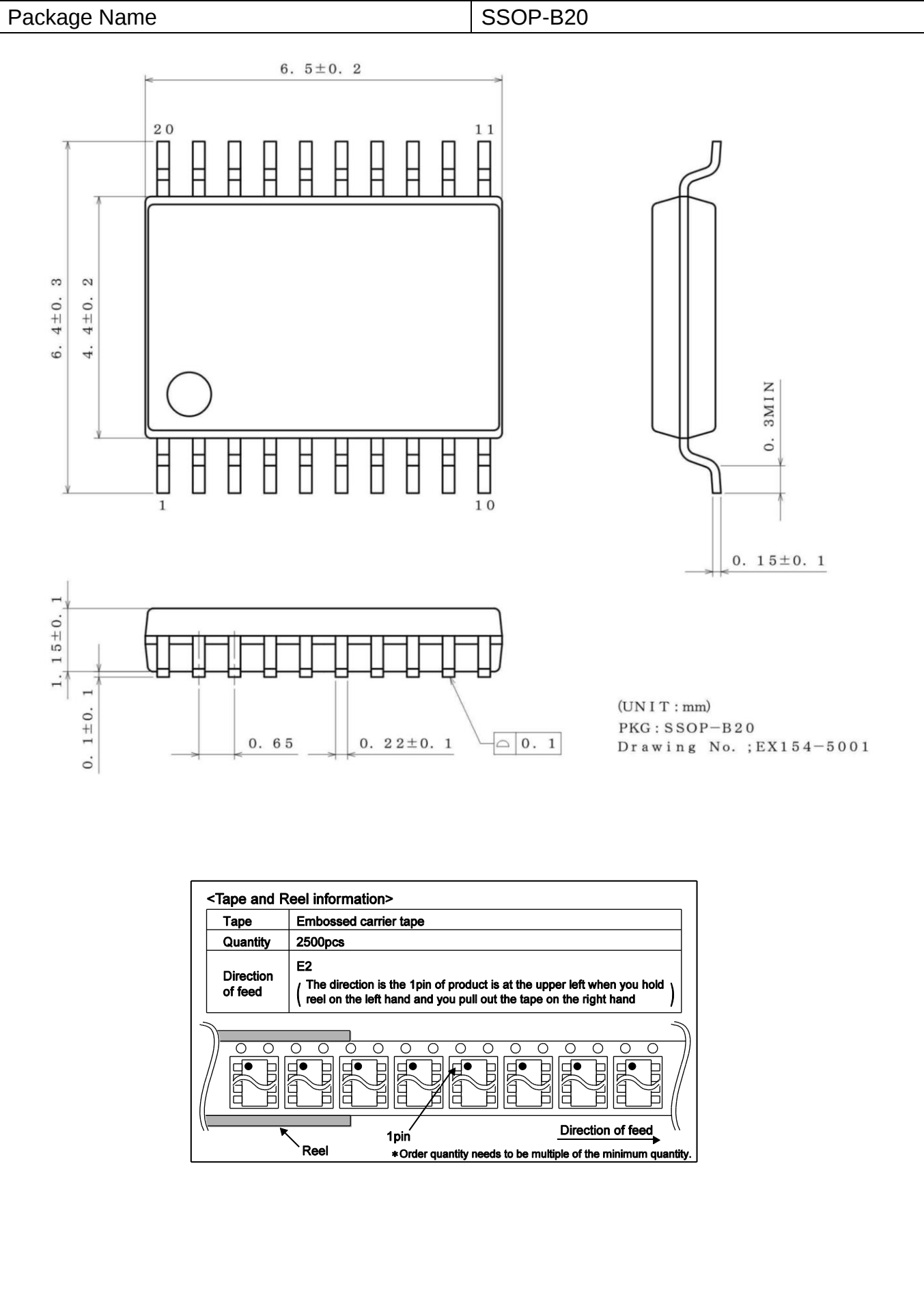
|                 |  |  |  |  |  |  |                          |                                                                   |  |
|-----------------|--|--|--|--|--|--|--------------------------|-------------------------------------------------------------------|--|
| B D 6 7 3 5 F V |  |  |  |  |  |  | -                        | E 2                                                               |  |
| Part Number     |  |  |  |  |  |  | Package<br>FV : SSOP-B20 | Packaging and forming specification<br>E2: Embossed tape and reel |  |

Marking Diagram



| Part Number Marking | Package  | Orderable Part Number |
|---------------------|----------|-----------------------|
| BD6735              | SSOP-B20 | BD6735FV-E2           |

Physical Dimension, Tape and Reel Information



**Revision History**

| Date        | Revision | Changes     |
|-------------|----------|-------------|
| 09.Dec.2015 | 001      | New Release |

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  - Use of the Products in places subject to dew condensation
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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- Confirm that operation temperature is within the specified range described in the product specification.
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## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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  - [b] the temperature or humidity exceeds those recommended by ROHM
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  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
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Связь**

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Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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