74LVC74A

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 06 — 4 June 2007 Product data sheet

1. General description

The 74LVC74A is a dual edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{SD}$) and ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features

- 5 V tolerant inputs for interlacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM JESD22-A114D exceeds 2000 V
  - CDM JESD22-C101C exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to 125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC74AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC74ADB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC74APW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC74ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

NXP founded by Philips

4. Functional diagram

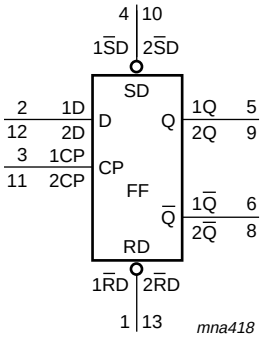

Fig 1. Logic symbol

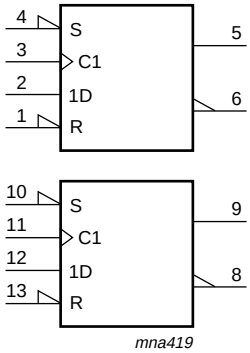

Fig 2. IEC logic symbol

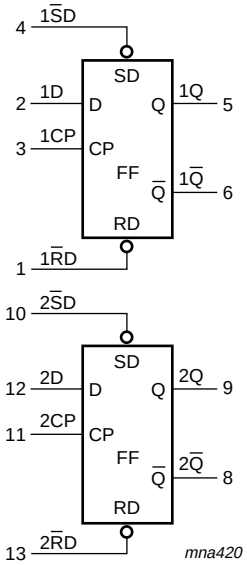

Fig 3. Functional diagram

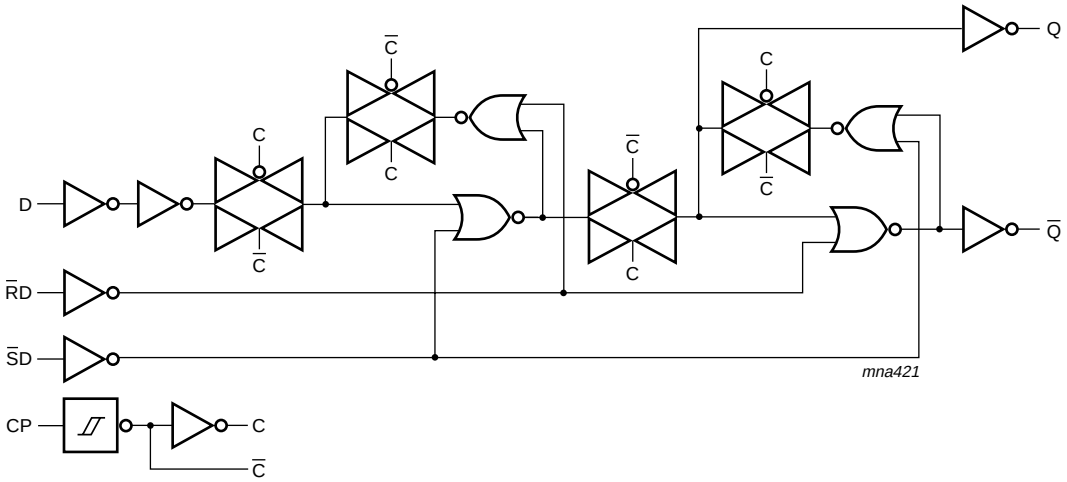

Fig 4. Logic diagram for one flip-flop

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5. Pinning information

5.1 Pinning

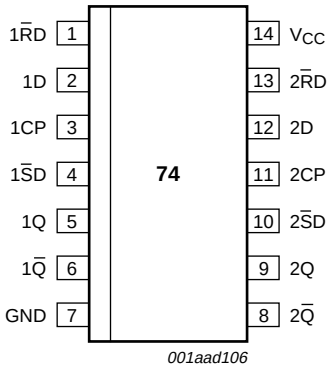
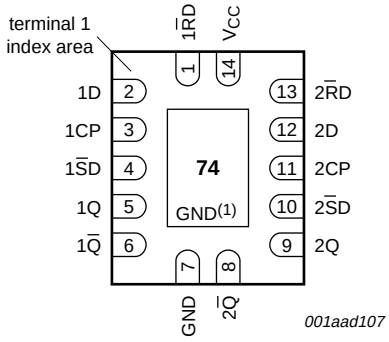


Fig 5. Pin configuration for SO14 and (T)SSOP14



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 6. Pin configuration for DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1R̄D	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)
1S̄D	4	asynchronous set-direct input (active LOW)
1Q	5	true output
1Q̄	6	complement output
GND	7	ground (0 V)
2Q̄	8	complement output
2Q	9	true output
2S̄D	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
2R̄D	13	asynchronous reset-direct input (active LOW)
V_{CC}	14	supply voltage

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6. Functional description

Table 3. Function table[1]

Input				Output	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care

Table 4. Function table[1]

Input				Output	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition
X = don't care

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage		[2]	–0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

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8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_o	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V_{CC}	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0	-	0	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.2		-	V_{CC} – 0.3	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

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10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Figure 7	[2]						
		V_{CC} = 1.2 V		-	15	-	-	-	ns
		V_{CC} = 2.7 V		1.0	2.7	6.0	1.0	7.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.5	5.2	1.0	6.5	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; see Figure 8							
		V_{CC} = 1.2 V		-	15	-	-	-	ns
		V_{CC} = 2.7 V		1.0	3.2	6.4	1.0	8.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.5	5.4	1.0	7.0	ns
		n$\overline{RD}$ to nQ, n$\overline{Q}$; see Figure 8							
		V_{CC} = 1.2 V		-	15	-	-	-	ns
		V_{CC} = 2.7 V		1.0	3.2	6.4	1.0	8.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.5	5.4	1.0	7.0	ns
t_W	pulse width	clock HIGH or LOW; see Figure 7							
		V_{CC} = 2.7 V		3.3	-	-	4.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.3	1.3	-	4.5	-	ns
		set or reset LOW; see Figure 8							
		V_{CC} = 2.7 V		3.3	-	-	4.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.3	1.7	-	4.5	-	ns
t_{rec}	recovery time	set or reset; see Figure 8							
		V_{CC} = 2.7 V		1.5	-	-	1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		+1.0	–3.0	-	1.0	-	ns
t_{su}	set-up time	nD to nCP; see Figure 7							
		V_{CC} = 2.7 V		2.2	-	-	2.2	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.0	0.8	-	2.0	-	ns
t_h	hold time	nD to nCP; see Figure 7							
		V_{CC} = 2.7 V		1.0	-	-	1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		+1.0	–0.2	-	1.0	-	ns
f_{max}	maximum frequency	nCP; see Figure 7							
		V_{CC} = 2.7 V		83	-	-	66	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	250		120	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC}	[4]						
		V_{CC} = 3.3 V		-	15	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C. For V_{CC} = 3.0 V to 3.6 V range, typical values are measured at 3.3 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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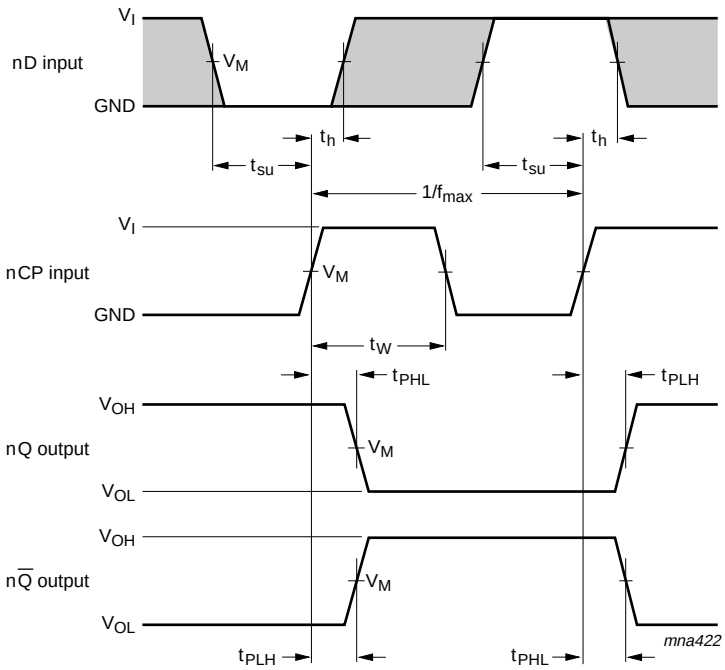
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. AC waveforms



The shaded areas indicate when the input is permitted to change for predictable output performance.

V_M = 1.5 V at $V_{CC} \geq 2.7$ V;

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock input (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, and the maximum frequency

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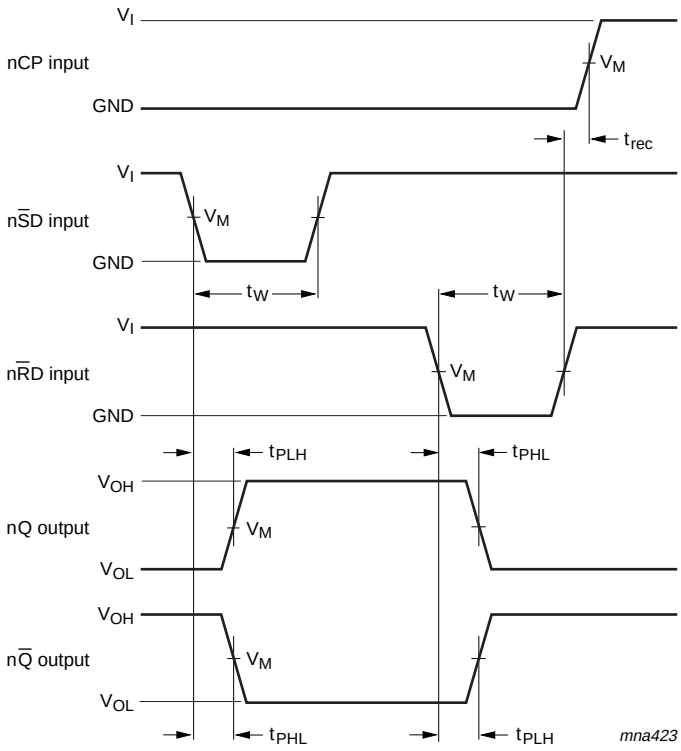

V_M = 1.5 V at $V_{CC} \geq 2.7$ V;

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The set ($n\overline{SD}$) and reset ($n\overline{RD}$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths, and the $n\overline{RD}$ to nCP recovery time

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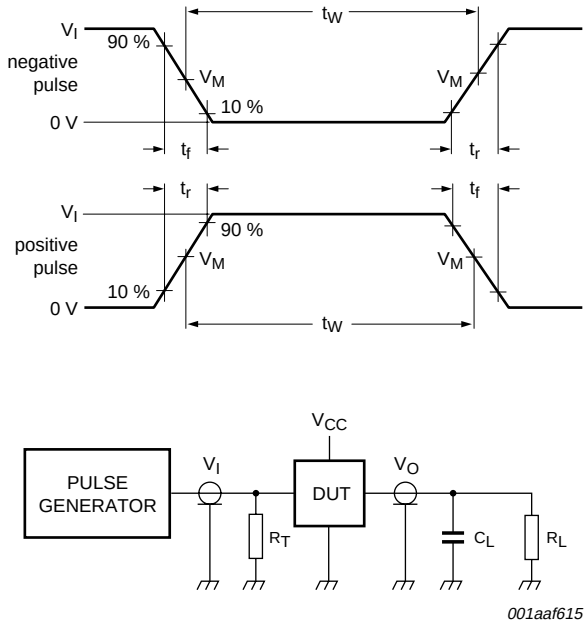

Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 9. Load circuitry for switching times

Table 9. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

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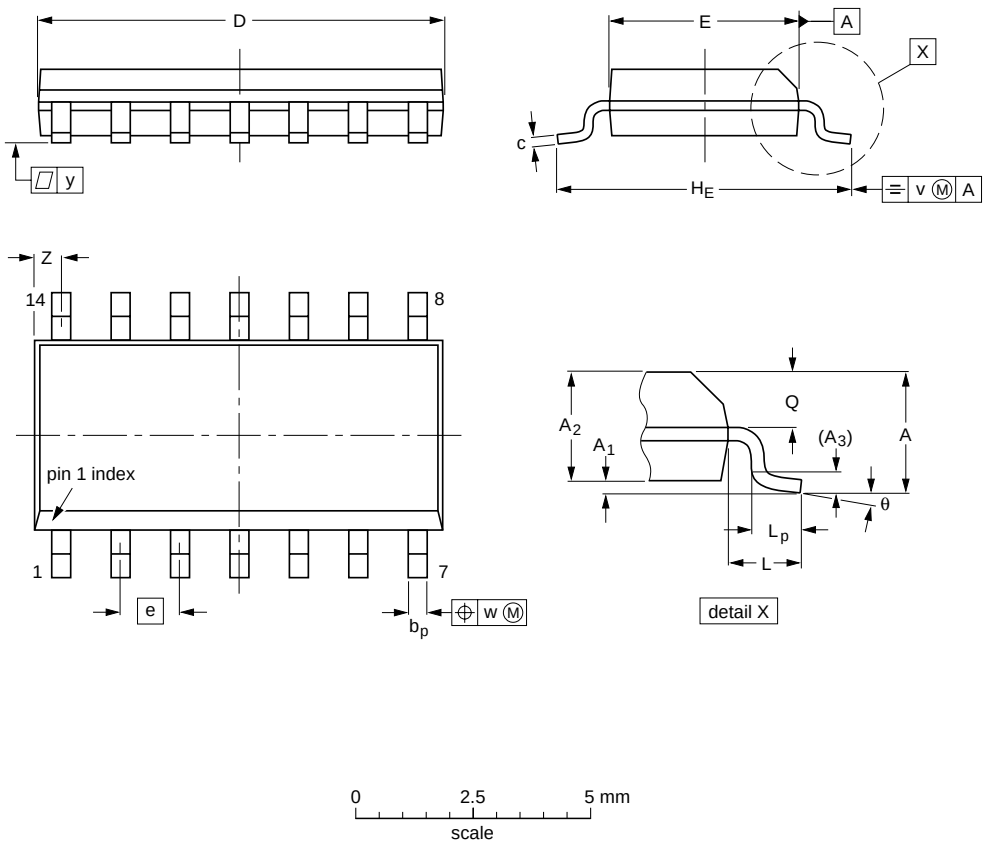
12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

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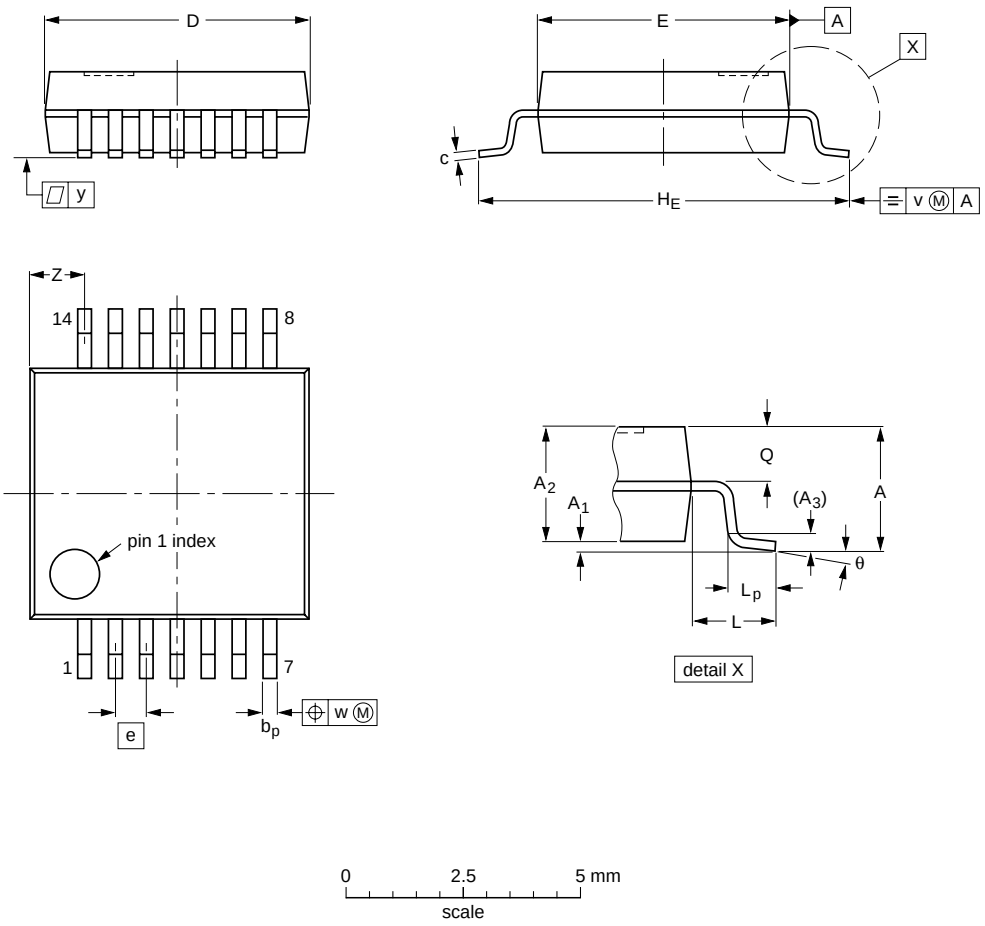
SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT337-1 (SSOP14)

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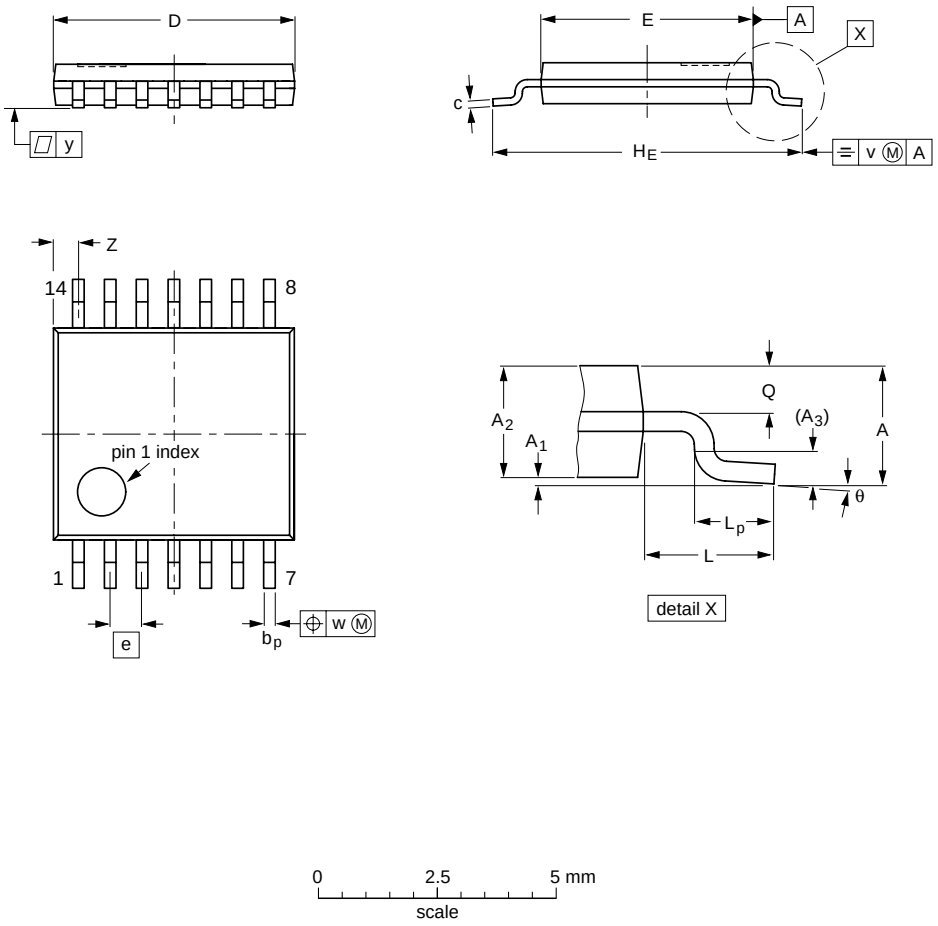
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

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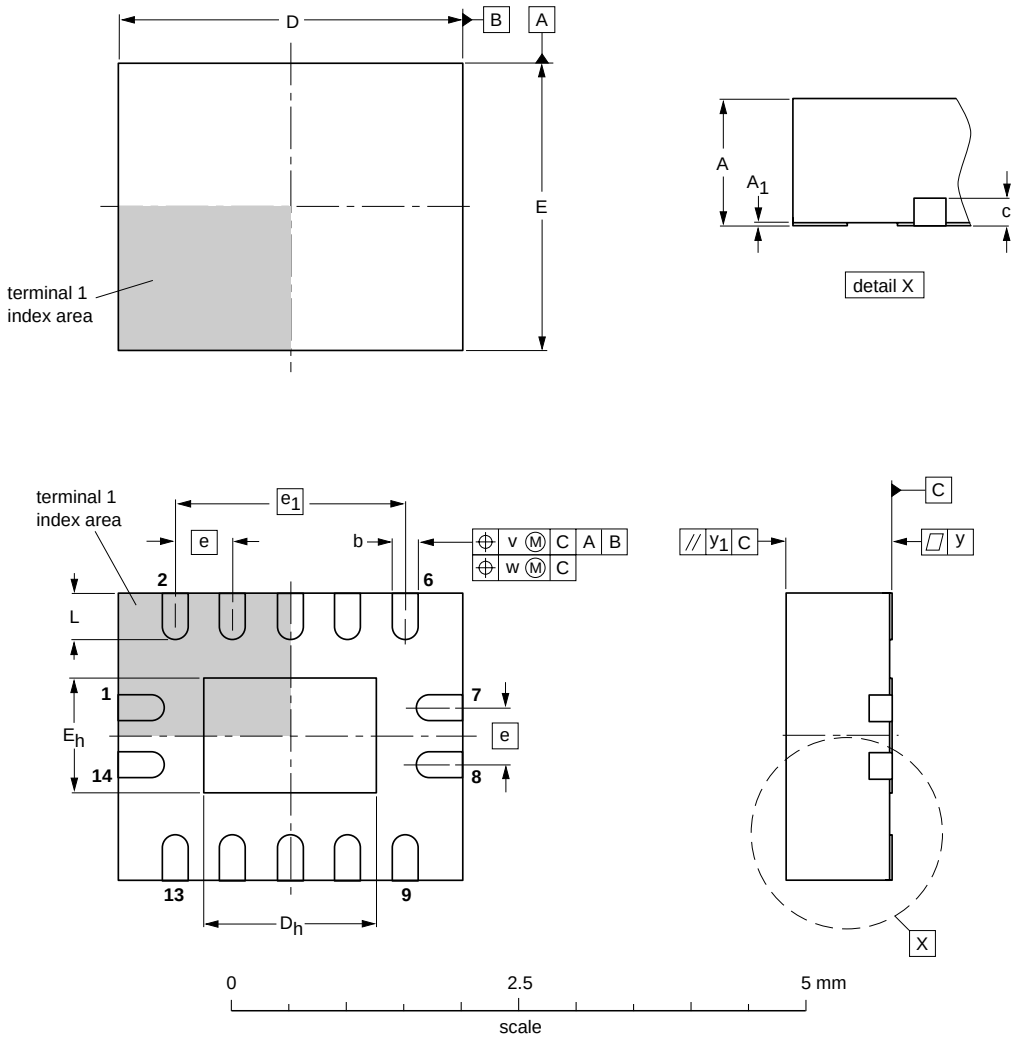
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT762-1 (DHVQFN14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC74A_6	20070604	Product data sheet	-	74LVC74A_5
Modifications:	• Change of hold time in Table 8 “Dynamic characteristics”. Minimum values changed to 1.0 ns.			
74LVC74A_5	20070525	Product data sheet	-	74LVC74A_4
74LVC74A_4	20030526	Product specification	-	74LVC74A_3
74LVC74A_3	20020618	Product specification	-	74LVC74A_2
74LVC74A_2	19980617	Product specification	-	74LVC74A_1
74LVC74A_1	19980617	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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