

74LVC74A

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 06 — 4 June 2007

Product data sheet

1. General description

The 74LVC74A is a dual edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set (\overline{SD}) and (\overline{RD}) inputs, and complementary Q and \overline{Q} outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features

- 5 V tolerant inputs for interlacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
 - ◆ HBM JESD22-A114D exceeds 2000 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC74AD	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC74ADB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC74APW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC74ABQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

4. Functional diagram

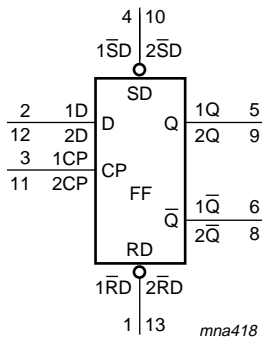


Fig 1. Logic symbol

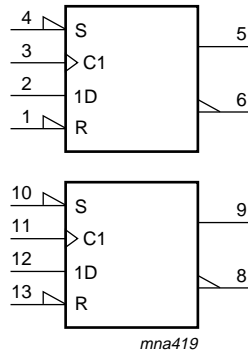


Fig 2. IEC logic symbol

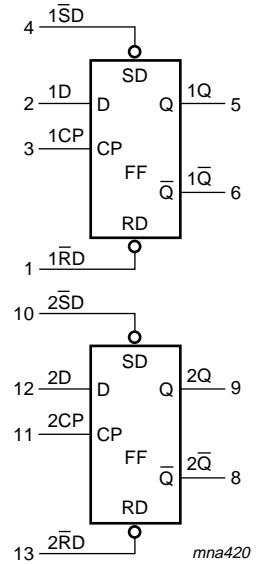


Fig 3. Functional diagram

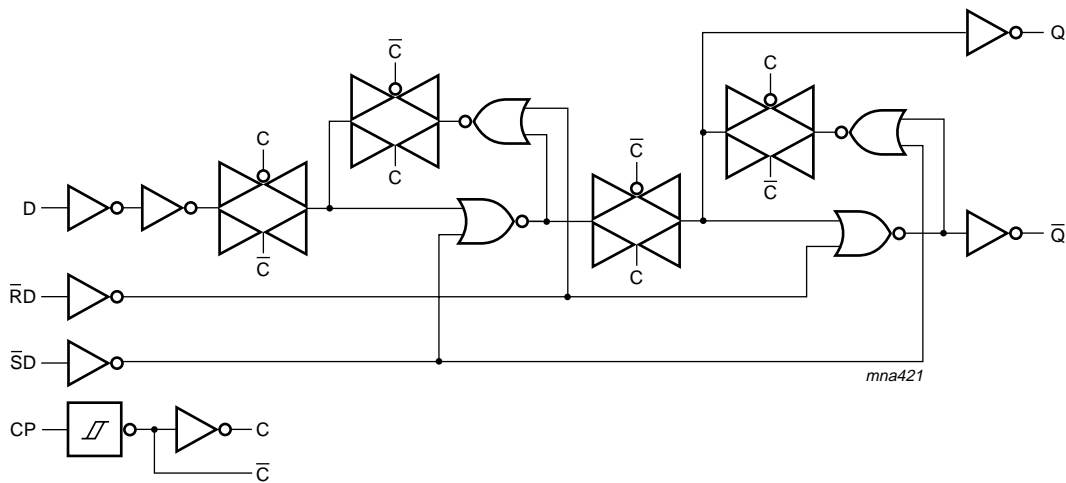
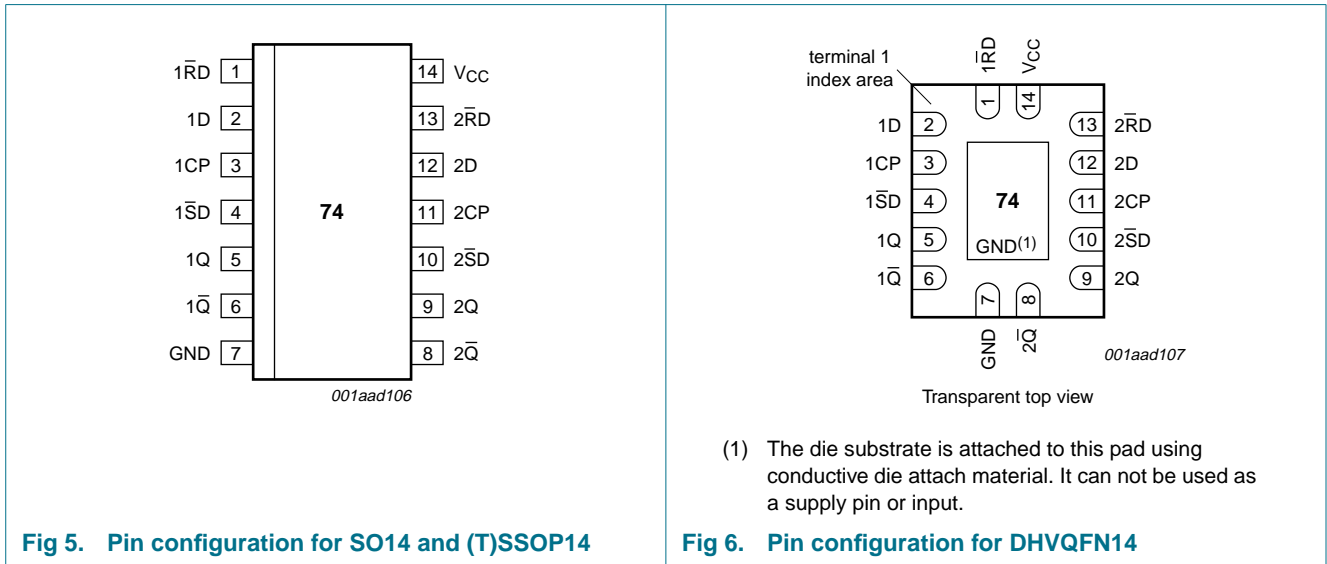


Fig 4. Logic diagram for one flip-flop

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1 $\bar{R}D$	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)
1 $\bar{S}D$	4	asynchronous set-direct input (active LOW)
1Q	5	true output
1 \bar{Q}	6	complement output
GND	7	ground (0 V)
2 \bar{Q}	8	complement output
2Q	9	true output
2 $\bar{S}D$	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
2 $\bar{R}D$	13	asynchronous reset-direct input (active LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input				Output	
nSD	nRD	nCP	nD	nQ	nQ̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

- [1] H = HIGH voltage level
 L = LOW voltage level
 X = don't care

Table 4. Function table^[1]

Input				Output	
nSD	nRD	nCP	nD	nQ _{n+1}	nQ̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

- [1] H = HIGH voltage level
 L = LOW voltage level
 ↑ = LOW-to-HIGH transition
 Q_{n+1} = state after the next LOW-to-HIGH CP transition
 X = don't care

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage		[2] -0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3] -	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
 [2] The output voltage ratings may be exceeded if the output current ratings are observed.
 [3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	V _{CC}	-	-	V _{CC}	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0	-	0	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -100 μA; V _{CC} = 2.7 V to 3.6 V						
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 2.7 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nCP to nQ, nQ̄; see Figure 7 ^[2]						
		V _{CC} = 1.2 V	-	15	-	-	-	ns
		V _{CC} = 2.7 V	1.0	2.7	6.0	1.0	7.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	5.2	1.0	6.5	ns
		nSD to nQ, nQ̄; see Figure 8						
		V _{CC} = 1.2 V	-	15	-	-	-	ns
		V _{CC} = 2.7 V	1.0	3.2	6.4	1.0	8.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	5.4	1.0	7.0	ns
		nRD to nQ, nQ̄; see Figure 8						
		V _{CC} = 1.2 V	-	15	-	-	-	ns
		V _{CC} = 2.7 V	1.0	3.2	6.4	1.0	8.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	5.4	1.0	7.0	ns
t _w	pulse width	clock HIGH or LOW; see Figure 7						
		V _{CC} = 2.7 V	3.3	-	-	4.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.3	1.3	-	4.5	-	ns
		set or reset LOW; see Figure 8						
		V _{CC} = 2.7 V	3.3	-	-	4.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.3	1.7	-	4.5	-	ns
t _{rec}	recovery time	set or reset; see Figure 8						
		V _{CC} = 2.7 V	1.5	-	-	1.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	+1.0	-3.0	-	1.0	-	ns
t _{su}	set-up time	nD to nCP; see Figure 7						
		V _{CC} = 2.7 V	2.2	-	-	2.2	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	0.8	-	2.0	-	ns
t _h	hold time	nD to nCP; see Figure 7						
		V _{CC} = 2.7 V	1.0	-	-	1.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	+1.0	-0.2	-	1.0	-	ns
f _{max}	maximum frequency	nCP; see Figure 7						
		V _{CC} = 2.7 V	83	-	-	66	-	MHz
		V _{CC} = 3.0 V to 3.6 V	150	250	-	120	-	MHz
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V ^[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per flip-flop; V _I = GND to V _{CC} ^[4]						
		V _{CC} = 3.3 V	-	15	-	-	-	pF

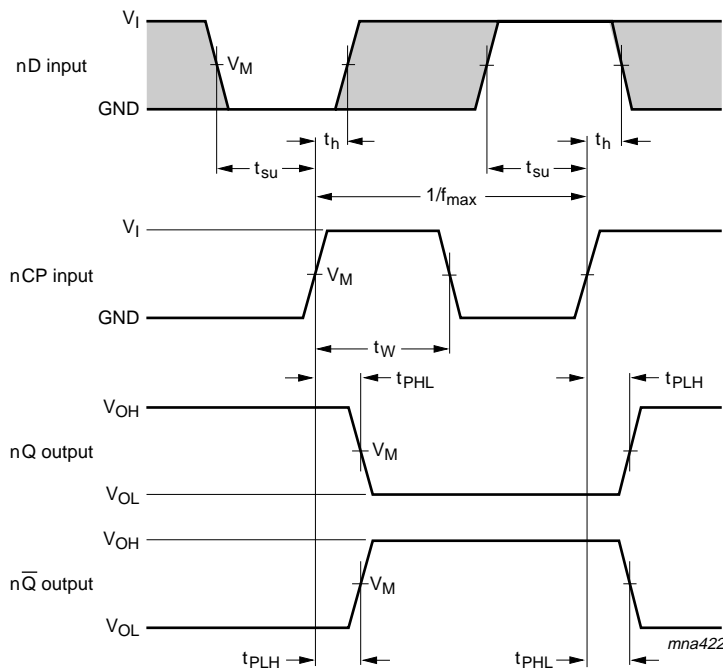
[1] Typical values are measured at T_{amb} = 25 °C. For V_{CC} = 3.0 V to 3.6 V range, typical values are measured at 3.3 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
- $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
- f_i = input frequency in MHz; f_o = output frequency in MHz
 - C_L = output load capacitance in pF
 - V_{CC} = supply voltage in Volts
 - N = number of inputs switching
 - $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. AC waveforms



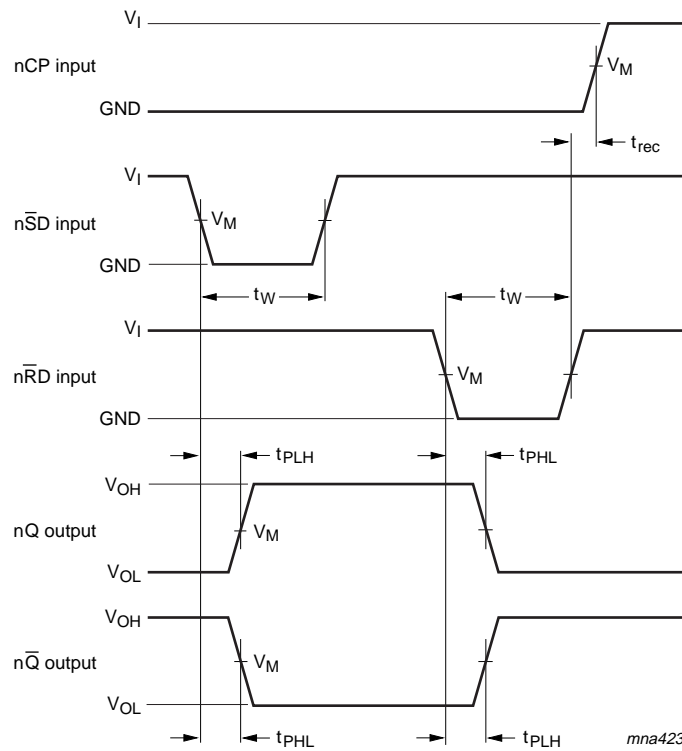
The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_M = 1.5 V$ at $V_{CC} \geq 2.7 V$;

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 V$;

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock input (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, and the maximum frequency

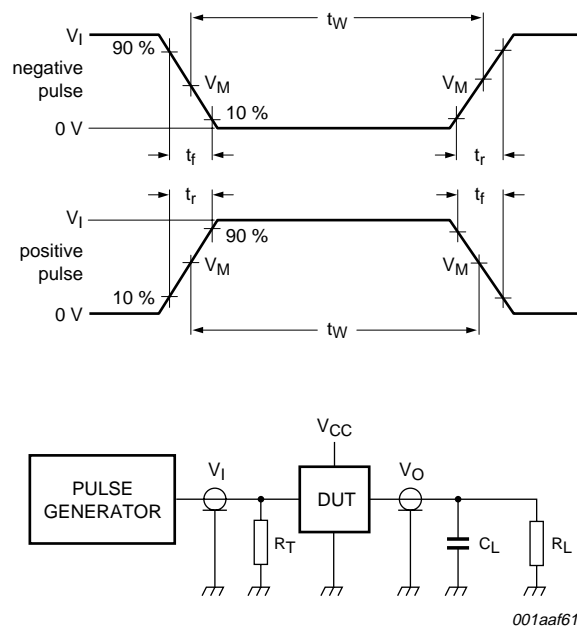


$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$;

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The set ($n\bar{S}D$) and reset ($n\bar{R}D$) input to output (nQ , $n\bar{Q}$) propagation delays, the set and reset pulse widths, and the $n\bar{R}D$ to nCP recovery time



001aaf615

Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 9. Load circuitry for switching times

Table 9. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

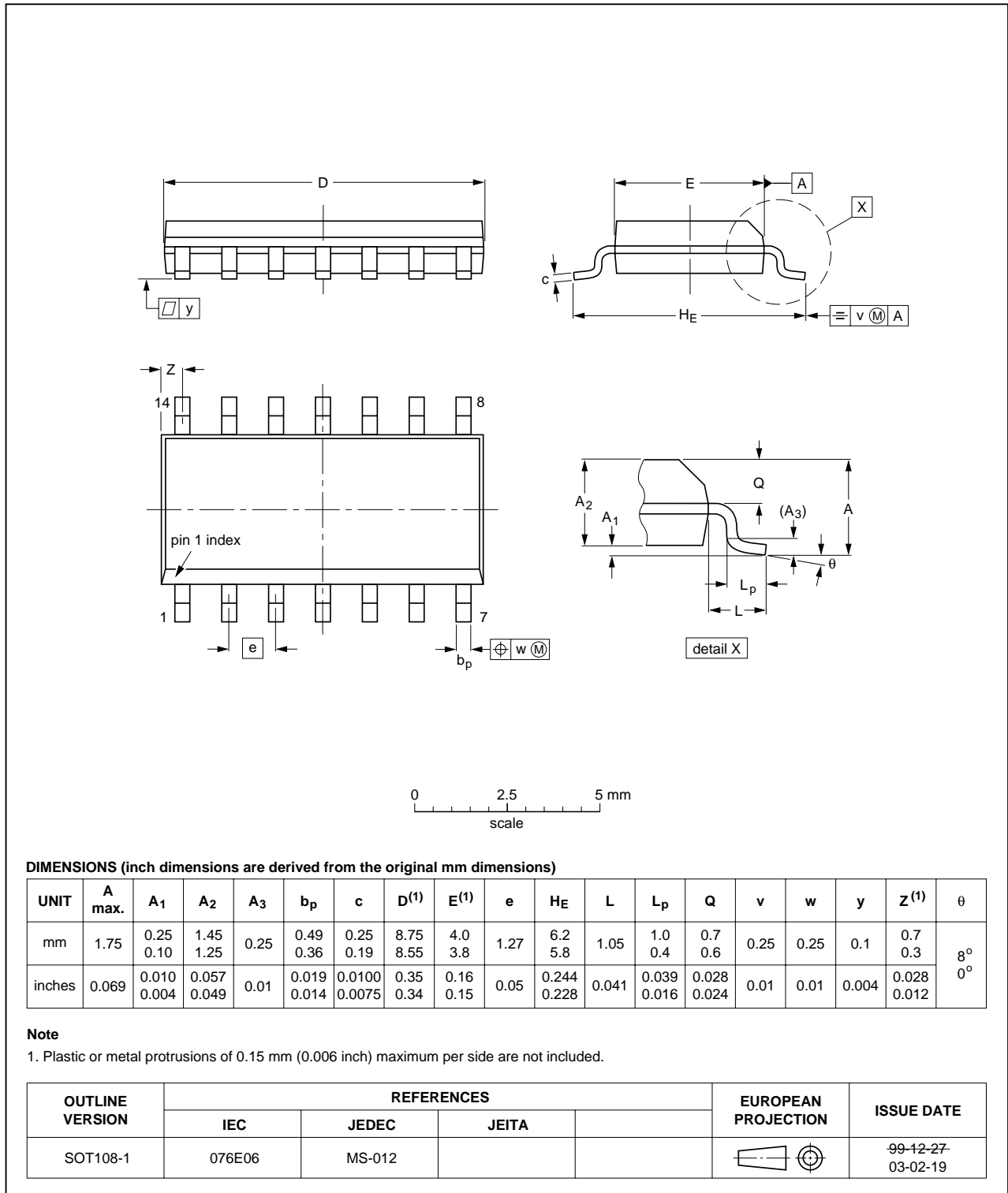


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

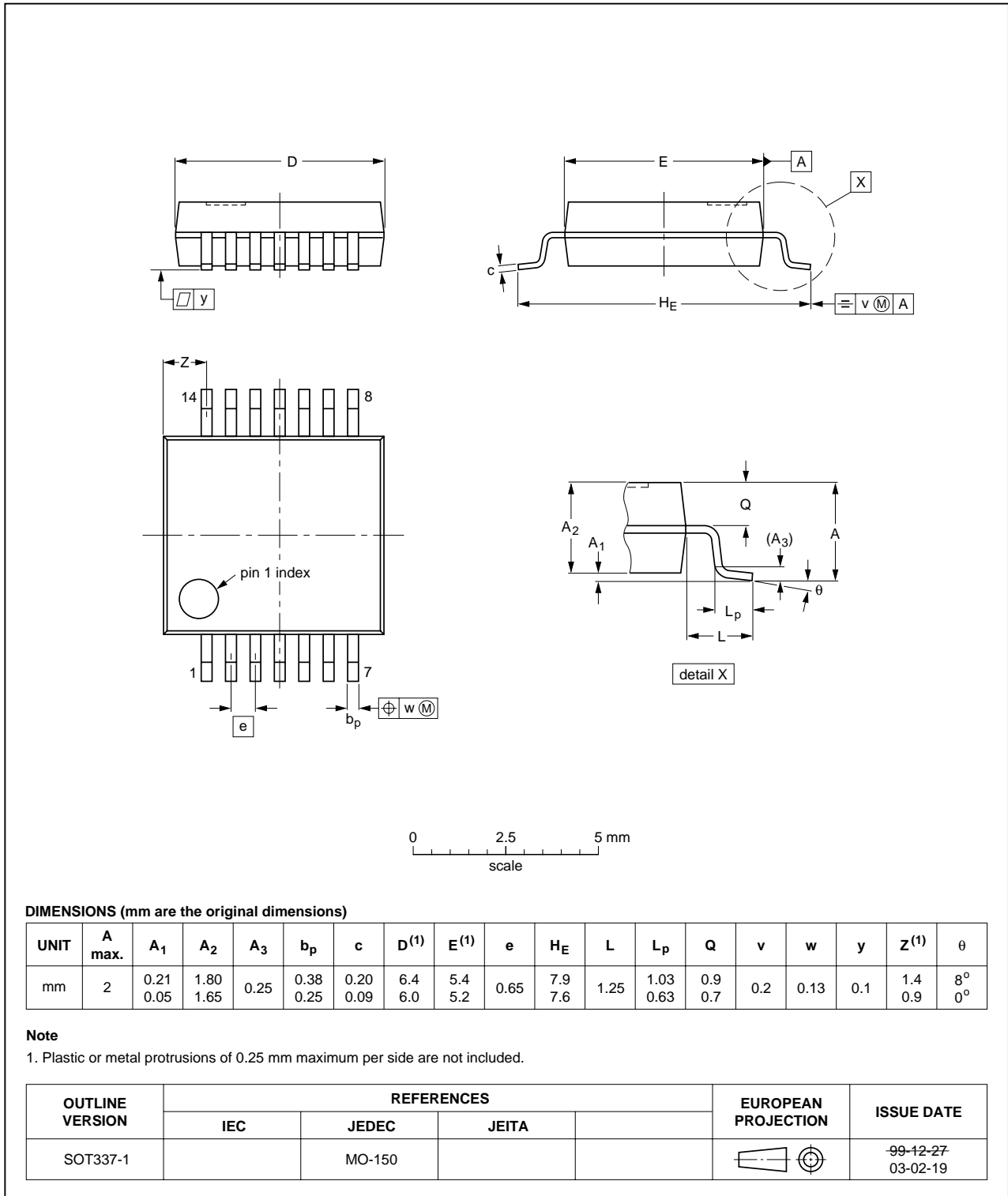


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

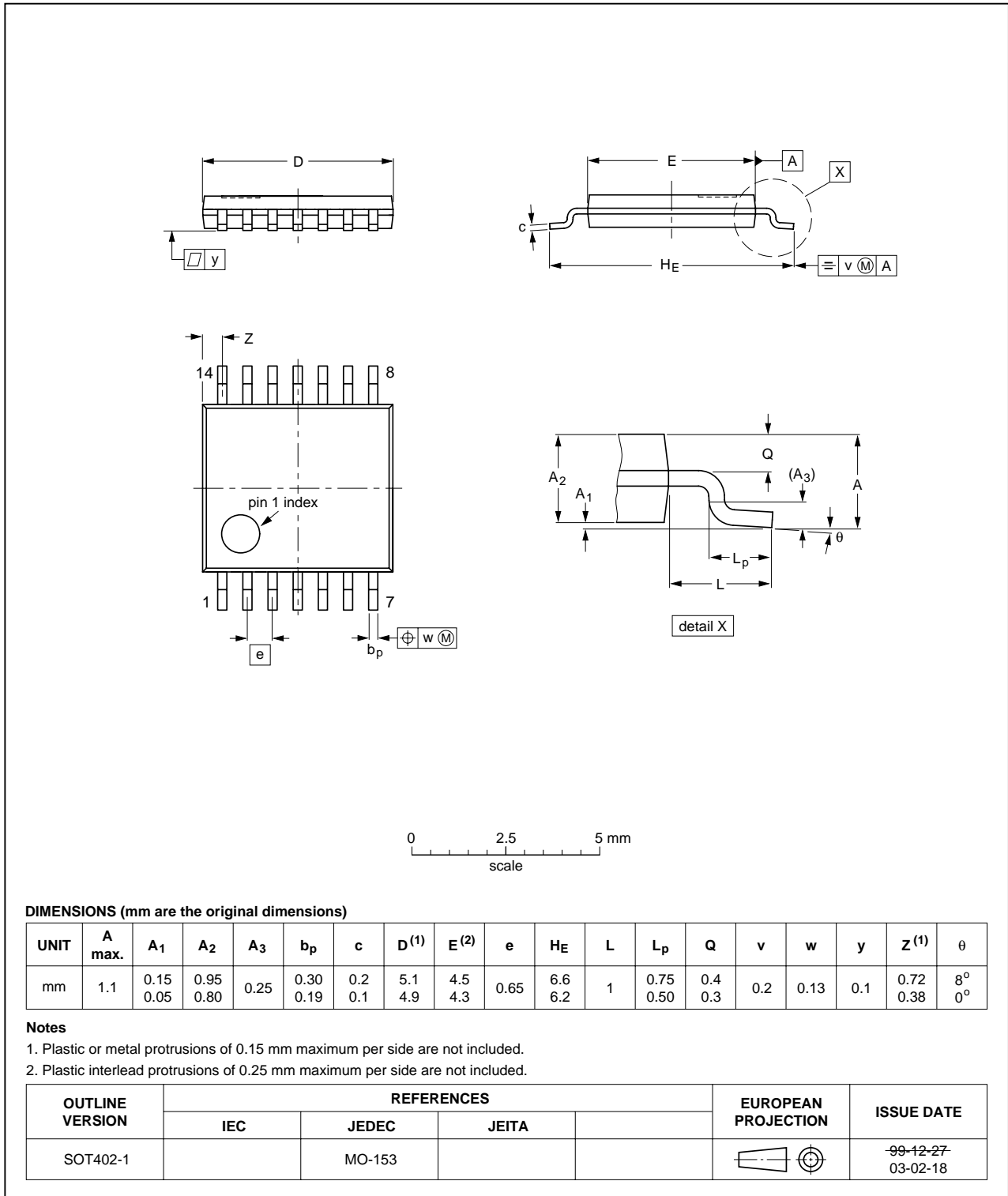


Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

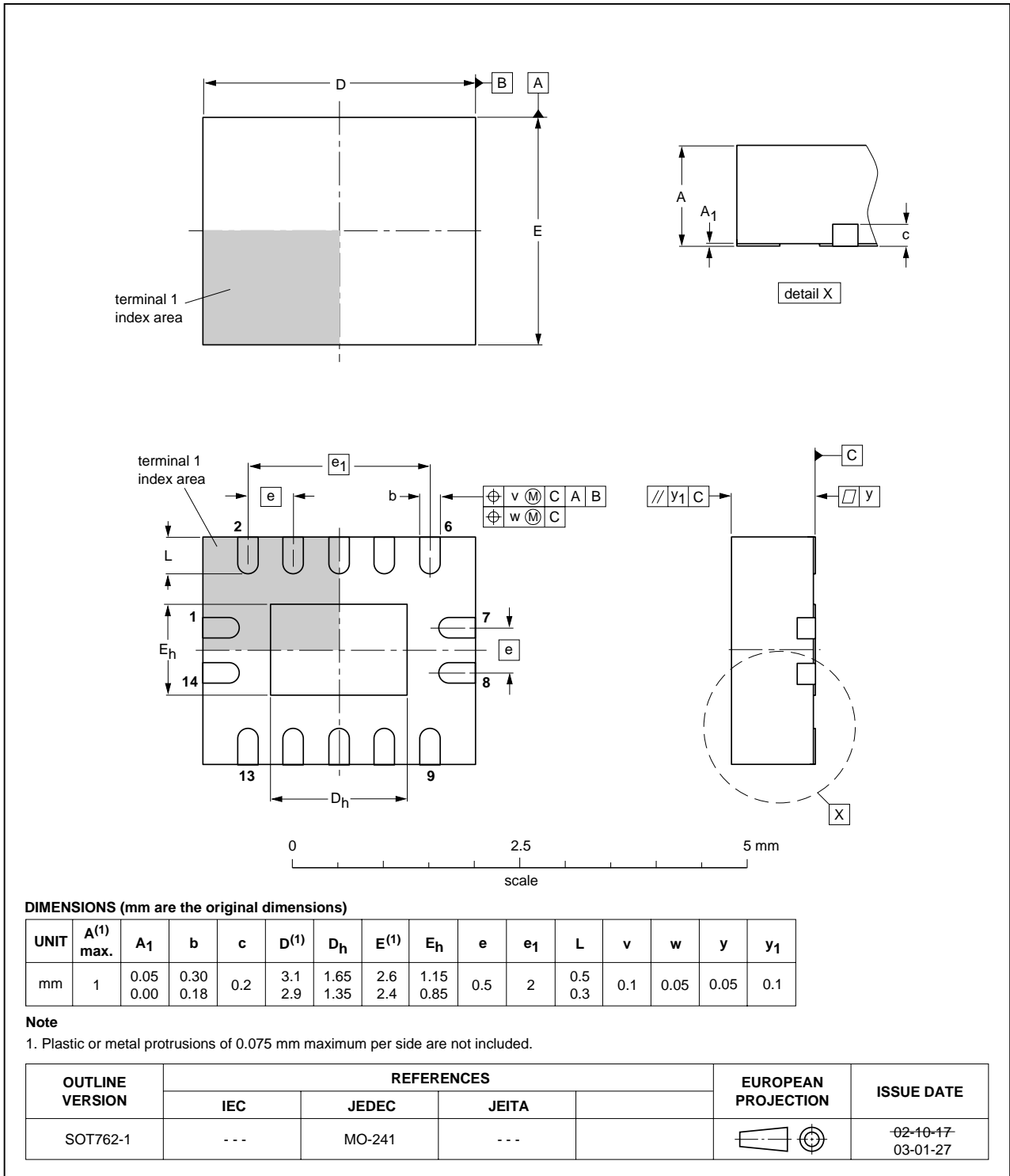


Fig 13. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC74A_6	20070604	Product data sheet	-	74LVC74A_5
Modifications:	<ul style="list-style-type: none"> Change of hold time in Table 8 "Dynamic characteristics". Minimum values changed to 1.0 ns. 			
74LVC74A_5	20070525	Product data sheet	-	74LVC74A_4
74LVC74A_4	20030526	Product specification	-	74LVC74A_3
74LVC74A_3	20020618	Product specification	-	74LVC74A_2
74LVC74A_2	19980617	Product specification	-	74LVC74A_1
74LVC74A_1	19980617	Product specification	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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