1. Overview for the Arria II Device Family

AIIGX51001-4.4

The Arria® II device family is designed specifically for ease-of-use. The cost-optimized, 40-nm device family architecture features a low-power, programmable logic engine and streamlined transceivers and I/Os. Common interfaces, such as the Physical Interface for PCI Express® (PCIe®), Ethernet, and DDR3 memory are easily implemented in your design with the Quartus® II software, the SOPC Builder design software, and a broad library of hard and soft intellectual property (IP) solutions from Altera. The Arria II device family makes designing for applications requiring transceivers operating at up to 6.375 Gbps fast and easy.

This chapter contains the following sections:

Arria II Device Feature

The Arria II device features consist of the following highlights:

- 40-nm, low-power FPGA engine
  - Adaptive logic module (ALM) offers the highest logic efficiency in the industry
  - Eight-input fracturable look-up table (LUT)
  - Memory logic array blocks (MLABs) for efficient implementation of small FIFOs
- High-performance digital signal processing (DSP) blocks up to 550 MHz
  - Configurable as 9 x 9-bit, 12 x 12-bit, 18 x 18-bit, and 36 x 36-bit full-precision multipliers as well as 18 x 36-bit high-precision multiplier
  - Hardcoded adders, subtractors, accumulators, and summation functions
  - Fully-integrated design flow with the MATLAB and DSP Builder software from Altera
- Maximum system bandwidth
  - Up to 24 full-duplex clock data recovery (CDR)-based transceivers supporting rates between 600 Mbps and 6.375 Gbps
  - Dedicated circuitry to support physical layer functionality for popular serial protocols, including PCIe Gen1 and PCIe Gen2, Gbps Ethernet, Serial RapidIO® (SRIO), Common Public Radio Interface (CPRI), OBSAI, SD/HD/3G/ASI Serial Digital Interface (SDI), XAUI and Reduced XAUI (RXAUI), HiGig/HiGig+, SATA/Serial Attached SCSI (SAS), GPON, SerialLite II, Fiber Channel, SONET/SDH, Interlaken, Serial Data Converter (JESD204), and SFI-5.

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- Complete PIPE protocol solution with an embedded hard IP block that provides physical interface and media access control (PHY/MAC) layer, Data Link layer, and Transaction layer functionality
- Optimized for high-bandwidth system interfaces
  - Up to 726 user I/O pins arranged in up to 20 modular I/O banks that support a wide range of single-ended and differential I/O standards
  - High-speed LVDS I/O support with serializer/deserializer (SERDES) and dynamic phase alignment (DPA) circuitry at data rates from 150 Mbps to 1.25 Gbps
- Low power
  - Architectural power reduction techniques
  - Typical physical medium attachment (PMA) power consumption of 100 mW at 3.125 Gbps.
  - Power optimizations integrated into the Quartus II development software
- Advanced usability and security features
  - Parallel and serial configuration options
  - On-chip series (R_S) and on-chip parallel (R_T) termination with auto-calibration for single-ended I/Os and on-chip differential (R_D) termination for differential I/O
  - 256-bit advanced encryption standard (AES) programming file encryption for design security with volatile and non-volatile key storage options
  - Robust portfolio of IP for processing, serial protocols, and memory interfaces
  - Low cost, easy-to-use development kits featuring high-speed mezzanine connectors (HSMC)
- Emulated LVDS output support with a data rate of up to 1152 Mbps

Table 1–1 lists the Arria II device features.

Table 1–1. Features in Arria II Devices

Feature	Arria II GX Devices						Arria II GZ Devices		
	EP2AGX45	EP2AGX65	EP2AGX95	EP2AGX125	EP2AGX190	EP2AGX260	EP2AGZ225	EP2AGZ300	EP2AGZ350
Total Transceivers *(1)*	8	8	12	12	16	16	16 or 24	16 or 24	16 or 24
ALMs	18,050	25,300	37,470	49,640	76,120	102,600	89,600	119,200	139,400
LEs	42,959	60,214	89,178	118,143	181,165	244,188	224,000	298,000	348,500
PCIe hard IP blocks	1	1	1	1	1	1	1	1	1
M9K Blocks	319	495	612	730	840	950	1,235	1,248	1,248
M144K Blocks	—	—	—	—	—	—	—	24	36
Total Embedded Memory in M9K Blocks (Kbits)	2,871	4,455	5,508	6,570	7,560	8,550	11,115	14,688	16,416
Total On-Chip Memory (M9K +M144K + MLABs) (Kbits)	3,435	5,246	6,679	8,121	9,939	11,756	13,915	18,413	20,772
Embedded Multipliers (18 x 18) *(2)*	232	312	448	576	656	736	800	920	1,040
General Purpose PLLs	4	4	6	6	6	6	6 or 8	4, 6, or 8	4, 6, or 8
Transceiver TX PLLs *(3)*, *(4)*	2 or 4	2 or 4	4 or 6	4 or 6	6 or 8	6 or 8	8 or 12	8 or 12	8 or 12
User I/O Banks *(5)*, *(6)*	6	6	8	8	12	12	16 or 20	8, 16, or 20	8, 16, or 20
High-Speed LVDS SERDES (up to 1.25 Gbps) *(7)*	8, 24, or 28	8, 24, or 28	24, 28, or 32	24, 28, 32	28 or 48	24 or 48	42 or 86	0 *(8)*, 42, or 86	0 *(8)*, 42, or 86

Notes to Table 1–1:

(1) The total number of transceivers is divided equally between the left and right side of each device, except for the devices in the F780 package. These devices have eight transceiver channels located only on the right side of the device.

(2) This is in four multiplier adder mode.

(3) The FPGA fabric can use these phase locked-loops (PLLs) if they are not used by the transceiver.

(4) The number of PLLs depends on the package. Transceiver transmitter (TX) PLL count = (number of transceiver blocks) × 2.

(5) Banks 3C and 8C are dedicated configuration banks and do not have user I/O pins.

(6) For Arria II GZ devices, the user I/Os count from pin-out files includes all general purpose I/O, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

(7) For Arria II GZ devices, total pairs of high-speed LVDS SERDES take the lowest channel count of RX/TX. For more information, refer to the *High-Speed I/O Interfaces and DPA in Arria II Devices* chapter.

(8) The smallest pin package (780-pin package) does not support high-speed LVDS SERDES.

Table 1–2 and Table 1–3 list the Arria II device package options and user I/O pin counts, high-speed LVDS channel counts, and transceiver channel counts for Ultra FineLine BGA (UBGA) and FineLine BGA (FBGA) devices.

Table 1–2. Package Options and I/O Information for Arria II GX Devices *(Note 1), (2), (3), (4), (5), (6), (7)*

Device	358-Pin Flip Chip UBGA 17 mm x 17 mm			572-Pin Flip Chip FBGA 25 mm x 25 mm			780-Pin Flip Chip FBGA 29 mm x 29 mm			1152-Pin Flip Chip FBGA 35 mm x 35 mm		
	I/O	LVDS *(8)*	XCVRs	I/O	LVDS *(8)*	XCVRs	I/O	LVDS *(8)*	XCVRs	I/O	LVDS *(8)*	XCVRs
EP2AGX45	156	33(R_D or eTX) + 32(RX, TX, or eTX)	4	252	57(R_D or eTX) + 56(RX, TX, or eTX)	8	364	85(R_D or eTX) + 84(RX, TX, or eTX)	8	—	—	—
EP2AGX65	156	33(R_D or eTX) + 32(RX, TX, or eTX)	4	252	57(R_D or eTX) + 56(RX, TX, or eTX)	8	364	85(R_D or eTX) +84(RX,TX, eTX)	8	—	—	—
EP2AGX95	—	—	—	260	57(R_D or eTX) + 56(RX, TX, or eTX)	8	372	85(R_D or eTX) +84(RX, TX, or eTX)	12	452	105(R_D or eTX) + 104(RX, TX, or eTX)	12
EP2AGX125	—	—	—	260	57(R_D or eTX) + 56(RX,TX, or eTX)	8	372	85(R_D or eTX) +84(RX,TX, or eTX)	12	452	105(R_D or eTX) + 104(RX, TX, or eTX)	12
EP2AGX190	—	—	—	—	—	—	372	85(R_D or eTX) +84(RX, TX, or eTX)	12	612	145(R_D or eTX) + 144(RX, TX, or eTX)	16
EP2AGX260	—	—	—	—	—	—	372	85(R_D, eTX) +84(RX, TX, or eTX)	12	612	145(R_D, eTX) + 144(RX, TX, or eTX)	16

Notes to Table 1–2:

(1) The user I/O counts include clock pins.

(2) The arrows indicate packages vertical migration capability. Vertical migration allows you to migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

(3) R_D = True LVDS input buffers with on-chip differential termination (R_D OCT) support.

(4) RX = True LVDS input buffers without R_D OCT support.

(5) TX = True LVDS output buffers.

(6) eTX = Emulated-LVDS output buffers, either `LVDS_E_3R` or `LVDS_E_1R`.

(7) The LVDS channel count does not include dedicated clock input pins and PLL clock output pins.

(8) These numbers represent the accumulated LVDS channels supported in Arria II GX row and column I/O banks.

Table 1–3. Package Options and I/O Information for Arria II GZ Devices *(Note 1)*, *(2)*, *(3)*, *(4)*, *(5)*

Device	780-Pin Flip Chip FBGA 29 mm x 29 mm			1152-Pin Flip Chip FBGA 35 mm x 35 mm			1517-Pin Flip Chip FBGA 40 mm x 40 mm		
	I/O	LVDS *(6)*	XCVRs	I/O	LVDS *(7)*	XCVRs	I/O	LVDS *(7)*	XCVRs
EP2AGZ225	—	—	—	554	135 (RX or eTX) + 140 (TX or eTX)	16	734	179 (RX or eTX) + 184 (TX or eTX)	24
EP2AGZ300	281	68 (RX or eTX) + 72 eTX	16	554	135 (RX or eTX) + 140 (TX or eTX)	16	734	179 (RX or eTX) + 184 (TX or eTX)	24
EP2AGZ350	281	68 (RX or eTX) + 72 eTX	16	554	135 (RX or eTX) + 140 (TX or eTX)	16	734	179 (RX or eTX) + 184 (TX or eTX)	24

Notes to Table 1–3:

(1) The user I/O counts include clock pins.

(2) RX = True LVDS input buffers without R_D OCT support for row I/O banks, or true LVDS input buffers without R_D OCT support for column I/O banks.

(3) eTX = Emulated-LVDS output buffers, either `LVDS_E_3R` or `LVDS_E_1R`.

(4) The LVDS RX and TX channels are equally divided between the left and right sides of the device.

(5) The LVDS channel count does not include dedicated clock input pins.

(6) For Arria II GZ 780-pin FBGA package, the LVDS channels are only supported in column I/O banks.

(7) These numbers represents the accumulated LVDS channels supported in Arria II GZ device row and column I/O banks.

Arria II devices are available in up to four speed grades: –3 (fastest), –4, –5, and –6 (slowest). Table 1–4 lists the speed grades for Arria II devices.

Table 1–4. Speed Grades for Arria II Devices

Device	358-Pin Flip Chip UBGA	572-Pin Flip Chip FBGA	780-Pin Flip Chip FBGA	1152-Pin Flip Chip FBGA	1517-Pin Flip Chip FBGA
EP2AGX45	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	—	—
EP2AGX65	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	—	—
EP2AGX95	—	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	—
EP2AGX125	—	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	—
EP2AGX190	—	—	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	—
EP2AGX260	—	—	C4, C5, C6, I3, I5	C4, C5, C6, I3, I5	—
EP2AGZ225	—	—	—	C3, C4, I3, I4	C3, C4, I3, I4
EP2AGZ300	—	—	C3, C4, I3, I4	C3, C4, I3, I4	C3, C4, I3, I4
EP2AGZ350	—	—	C3, C4, I3, I4	C3, C4, I3, I4	C3, C4, I3, I4

Arria II Device Architecture

Arria II devices include a customer-defined feature set optimized for cost-sensitive applications and offer a wide range of density, memory, embedded multiplier, I/O, and packaging options. Arria II devices support external memory interfaces and I/O protocols required by wireless, wireline, broadcast, computer, storage, and military markets. They inherit the 8-input ALM, M9K and M144K embedded RAM block, and high-performance DSP blocks from the Stratix® IV device family with a cost-optimized I/O cell and a transceiver optimized for 6.375 Gbps speeds.

Figure 1–1 and Figure 1–2 show an overview of the Arria II GX and Arria II GZ device architecture, respectively.

Figure 1–1. Architecture Overview for Arria II GX Devices

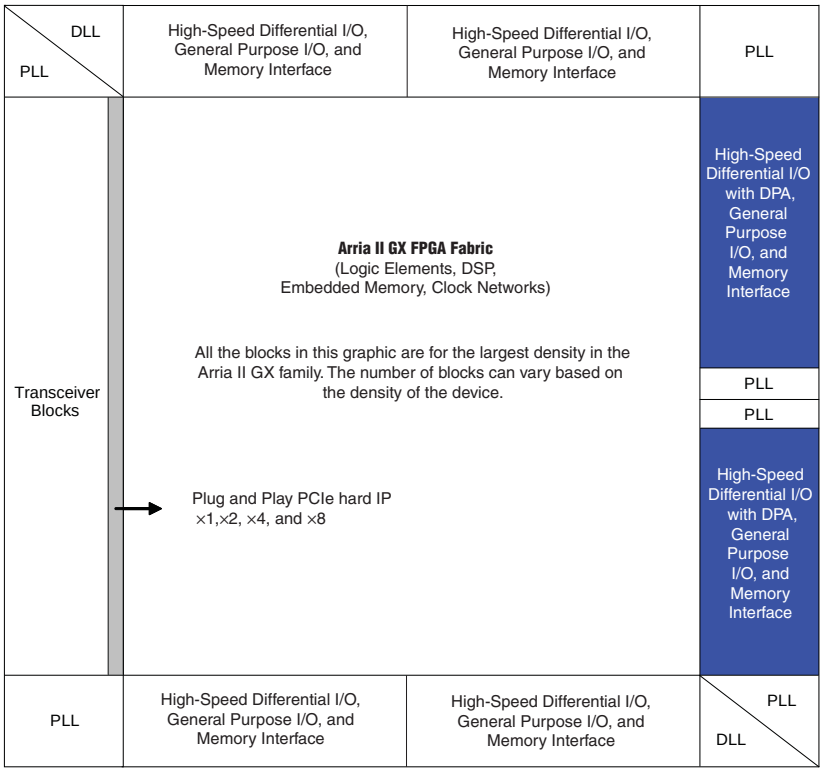
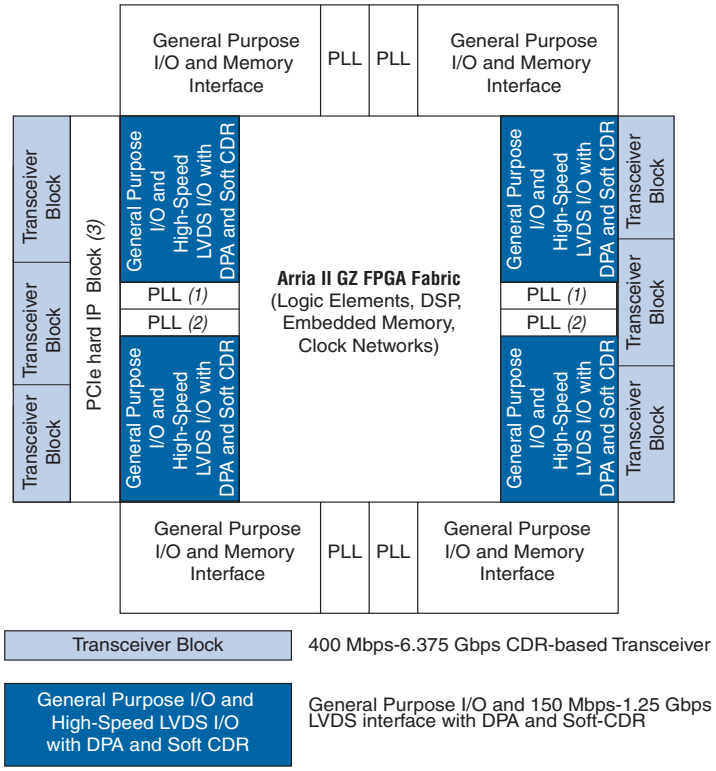


Figure 1–2. Architecture Overview for Arria II GZ Device



Notes to Figure 1–2:

(1) Not available for 780-pin FBGA package.

(2) Not available for 780-pin and 1152-pin FBGA packages.

(3) The PCIe hard IP block is located on the left side of the device only (IOBANK_QL).

High-Speed Transceiver Features

Arria II GX devices integrate up to 16 transceivers and Arria II GZ devices up to 24 transceivers on a single device. The transceiver block is optimized for cost and power consumption. Arria II transceivers support the following features:

- Configurable pre-emphasis and equalization, and adjustable output differential voltage
- Flexible and easy-to-configure transceiver datapath to implement proprietary protocols
- Signal integrity features
  - Programmable transmitter pre-emphasis to compensate for inter-symbol interference (ISI)
  - User-controlled receiver equalization with up to 7 dB (Arria II GX) and 16 dB (Arria II GZ) of high-frequency gain
  - On-die power supply regulators for transmitter and receiver PLL charge pump and voltage-controlled oscillator (VCO) for superior noise immunity
  - Calibration circuitry for transmitter and receiver on-chip termination (OCT) resistors

- Diagnostic features
  - Serial loopback from the transmitter serializer to the receiver CDR for transceiver physical coding sublayer (PCS) and PMA diagnostics
  - Parallel loopback from the transmitter PCS to the receiver PCS with built-in self test (BIST) pattern generator and verifier
  - Reverse serial loopback pre- and post-CDR to transmitter buffer for physical link diagnostics
  - Loopback master and slave capability in PCIe hard IP blocks
  - Support for protocol features such as MSB-to-LSB transmission in a SONET/SDH configuration and spread-spectrum clocking in a PCIe configuration

Table 1–5 lists common protocols and the Arria II dedicated circuitry and features for implementing these protocols.

Table 1–5. Sample of Supported Protocols and Feature Descriptions for Arria II Devices

Supported Protocols	Feature Descriptions

PCIe	■ Complete PCIe Gen1 and Gen2 protocol stack solution compliant to PCIe Base Specification 2.0 that includes PHY/MAC, Data Link, and Transaction layer circuitry embedded in the PCIe hard IP blocks.
	■ PCIe Gen1 has x1, x2, x4, and x8 lane configurations. PCIe Gen2 has x1, x2, and x4 lane configurations. PCIe Gen2 does not support x8 lane configurations
	■ Built-in circuitry for electrical idle generation and detection, receiver detect, power state transitions, lane reversal, and polarity inversion
	■ 8B/10B encoder and decoder, receiver synchronization state machine, and ±300 parts per million (PPM) clock compensation circuitry
	■ Options to use:
	  ■ Hard IP Data Link Layer and Transaction Layer
	  ■ Hard IP Data Link Layer and custom Soft IP Transaction Layer

XAUI/HiGig/HiGig+	■ Compliant to IEEE P802.3ae specification ■ Embedded state machine circuitry to convert XGMII idle code groups (||I||) to and from idle ordered sets (||A||, ||K||, ||R||) at the transmitter and receiver, respectively ■ 8B/10B encoder and decoder, receiver synchronization state machine, lane deskew, and ±100 PPM clock compensation circuitry
GbE	■ Compliant to IEEE 802.3 specification ■ Automatic idle ordered set (/I1/, /I2/) generation at the transmitter, depending on the current running disparity ■ 8B/10B encoder and decoder, receiver synchronization state machine, and ±100 PPM clock compensation circuitry
CPRI/OBSAI	■ Transmit bit slipper eliminates latency uncertainty to comply with CPRI/OBSAI specifications ■ Optimized for power and cost for remote radio heads and RF modules

For other protocols supported by Arria II devices, such as SONET/SDH, SDI, SATA and SRIO, refer to the *Transceiver Architecture in Arria II Devices* chapter.

PCIe Gen2 protocol is only available in Arria II GZ devices.

The following sections provide an overview of the various features of the Arria II FPGA.

PCIe Hard IP Block

Every Arria II device includes an integrated hard IP block which implements PCIe PHY/MAC, data link, and transaction layers. This PCIe hard IP block is highly configurable to meet the requirements of the majority of PCIe applications. PCIe hard IP makes implementing PCIe Gen1 and PCIe Gen2 solution in your Arria II design simple and easy.

You can instantiate PCIe hard IP block using the PCI Compiler MegaWizard™ Plug-In Manager, similar to soft IP functions, but does not consume core FPGA resources or require placement, routing, and timing analysis to ensure correct operation of the core. Table 1–6 lists the PCIe hard IP block support for Arria II GX and GZ devices.

Table 1–6. PCIe Hard IP Block Support

Support	Arria II GX Devices	Arria II GZ Devices
PCIe Gen1	x1, x4, x8	x1, x4, x8
PCIe Gen2	—	x1, x4
Root Port and endpoint configurations	Yes	Yes
Payloads	128-byte to 256-byte	128-byte to 2K-byte

Logic Array Block and Adaptive Logic Modules

- Logic array blocks (LABs) consists of 10 ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines
- ALMs expand the traditional four-input LUT architecture to eight-inputs, increasing performance by reducing logic elements (LEs), logic levels, and associated routing
- LABs have a derivative called MLAB, which adds SRAM-memory capability to the LAB
- MLAB and LAB blocks always coexist as pairs, allowing up to 50% of the logic (LABs) to be traded for memory (MLABs)

Embedded Memory Blocks

- MLABs, M9K, and M144K embedded memory blocks provide up to 20,836 Kbits of on-chip memory capable of up to 540-MHz performance. The embedded memory structure consists of columns of embedded memory blocks that you can configure as RAM, FIFO buffers, and ROM.
- Optimized for applications such as high-throughput packet processing, high-definition (HD) line buffers for video processing functions, and embedded processor program and data storage.

- The Quartus® II software allows you to take advantage of MLABs, M9K, and M144K memory blocks by instantiating memory using a dedicated megafunction wizard or by inferring memory directly from VHDL or Verilog source code.

Table 1–7 lists the Arria II device memory modes.

Table 1–7. Memory Modes for Arria II Devices

Port Mode	Port Width Configuration
Single Port	x1, x2, x4, x8, x9, x16, x18, x32, x36, x64, and x72
Simple Dual Port	x1, x2, x4, x8, x9, x16, x18, x32, x36, x64, and x72
True Dual Port	x1, x2, x4, x8, x9, x16, x18, x32, and x36

DSP Resources

- Fulfills the DSP requirements of 3G and Long Term Evolution (LTE) wireless infrastructure applications, video processing applications, and voice processing applications
- DSP block input registers efficiently implement shift registers for finite impulse response (FIR) filter applications
- The Quartus II software includes megafunctions you can use to control the mode of operation of the DSP blocks based on user-parameter settings
- You can directly infer multipliers from the VHDL or Verilog HDL source code

I/O Features

- Contains up to 20 modular I/O banks
- All I/O banks support a wide range of single-ended and differential I/O standards listed in Table 1–8.

Table 1–8. I/O Standards Support for Arria II Devices

Type	I/O Standard
Single-Ended I/O	LVTTL, LVCMOS, SSTL, HSTL, PCIe, and PCI-X
Differential I/O	SSTL, HSTL, LVPECL, LVDS, mini-LVDS, Bus LVDS (BLVDS) *(1)*, and RSDS

Note to Table 1–8:

(1) BLVDS is only available for Arria II GX devices.

- Supports programmable bus hold, programmable weak pull-up resistors, and programmable slew rate control
- For Arria II devices, calibrates OCT or driver impedance matching for single-ended I/O standards with one OCT calibration block on the I/O banks listed in Table 1–9.

Table 1–9. Location of OCT Calibration Block in Arria II Devices

Device	Package Option	I/O Bank
Arria II GX	All pin packages	Bank 3A, Bank 7A, and Bank 8A
Arria II GZ	780-pin flip chip FBGA	Bank 3A, Bank 4A, Bank 7A, and Bank 8A
	1152-pin flip chip FBGA	Bank 1A, Bank 3A, Bank 4A, Bank 6A, Bank 7A, and Bank 8A
	1517-pin flip chip FBGA	Bank 1A, Bank 2A, Bank 3A, Bank 4A, Bank 5A, Bank 6A, Bank 7A, and Bank 8A

- Arria II GX devices have dedicated configuration banks at Bank 3C and 8C, which support dedicated configuration pins and some of the dual-purpose pins with a configuration scheme at 1.8, 2.5, 3.0, and 3.3 V. For Arria II GZ devices, the dedicated configuration pins are located in Bank 1A and Bank 1C. However, these banks are not dedicated configuration banks; therefore, user I/O pins are available in Bank 1A and Bank 1C.
- Dedicated VCCIO, VREF, and VCCPD pin per I/O bank to allow voltage-referenced I/O standards. Each I/O bank can operate at independent V_{CCIO}, V_{REF}, and V_{CCPD} levels.

High-Speed LVDS I/O and DPA

- Dedicated circuitry for implementing LVDS interfaces at speeds from 150 Mbps to 1.25 Gbps
- R_D OCT for high-speed LVDS interfacing
- DPA circuitry and soft-CDR circuitry at the receiver automatically compensates for channel-to-channel and channel-to-clock skew in source-synchronous interfaces and allows for implementation of asynchronous serial interfaces with embedded clocks at up to 1.25 Gbps data rate (SGMII and GbE)
- Emulated LVDS output buffers use two single-ended output buffers with an external resistor network to support LVDS, mini-LVDS, BLVDS (only for Arria II GZ devices), and RSDS standards.

Clock Management

- Provides dedicated global clock networks, regional clock networks, and periphery clock networks that are organized into a hierarchical structure that provides up to 192 unique clock domains
- Up to eight PLLs with 10 outputs per PLL to provide robust clock management and synthesis
  - Independently programmable PLL outputs, creating a unique and customizable clock frequency with no fixed relation to any other clock
  - Inherent jitter filtration and fine granularity control over multiply and divide ratios
  - Supports spread-spectrum input clocking and counter cascading with PLL input clock frequencies ranging from 5 to 500 MHz to support both low-cost and high-end clock performance
- FPGA fabric can use the unused transceiver PLLs to provide more flexibility

Auto-Calibrating External Memory Interfaces

- I/O structure enhanced to provide flexible and cost-effective support for different types of memory interfaces
- Contains features such as OCT and DQ/DQS pin groupings to enable rapid and robust implementation of different memory standards
- An auto-calibrating megafunction is available in the Quartus II software for DDR SDRAM, DDR2 SDRAM, DDR3 SDRAM, RLDRAM II memory interface PHYs; the megafunction takes advantage of the PLL dynamic reconfiguration feature to calibrate based on the changes of process, voltage, and temperature (PVT).

For the maximum clock rates supported in Altera's FPGA devices, refer to the External Memory Interface Spec Estimator online tool.

For more information about the external memory interfaces support, refer to the *External Memory Interfaces in Arria II Devices* chapter.

Nios II

- Arria II devices support all variants of the NIOS® II processor
- Nios II processors are supported by an array of software tools from Altera and leading embedded partners and are used by more designers than any other configurable processor

Configuration Features

- Configuration
  - Supports active serial (AS), passive serial (PS), fast passive parallel (FPP), and JTAG configuration schemes.
- Design Security
  - Supports programming file encryption using 256-bit volatile and non-volatile security keys to protect designs from copying, reverse engineering, and tampering in FPP configuration mode with an external host (such as a MAX® II device or microprocessor), or when using the AS, FAS, or PS configuration scheme
  - Decrypts an encrypted configuration bitstream using the AES algorithm, an industry standard encryption algorithm that is FIPS-197 certified and requires a 256-bit security key

- Remote System Upgrade
  - Allows error-free deployment of system upgrades from a remote location securely and reliably without an external controller
  - Soft logic (either the Nios II embedded processor or user logic) implementation in the device helps download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to start a reconfiguration cycle
  - Dedicated circuitry in the remote system upgrade helps to avoid system down time by performing error detection during and after the configuration process, recover from an error condition by reverting back to a safe configuration image, and provides error status information

SEU Mitigation

- Offers built-in error detection circuitry to detect data corruption due to soft errors in the configuration random access memory (CRAM) cells
- Allows all CRAM contents to be read and verified to match a configuration-computed cyclic redundancy check (CRC) value
- You can identify and read out the bit location and the type of soft error through the JTAG or the core interface

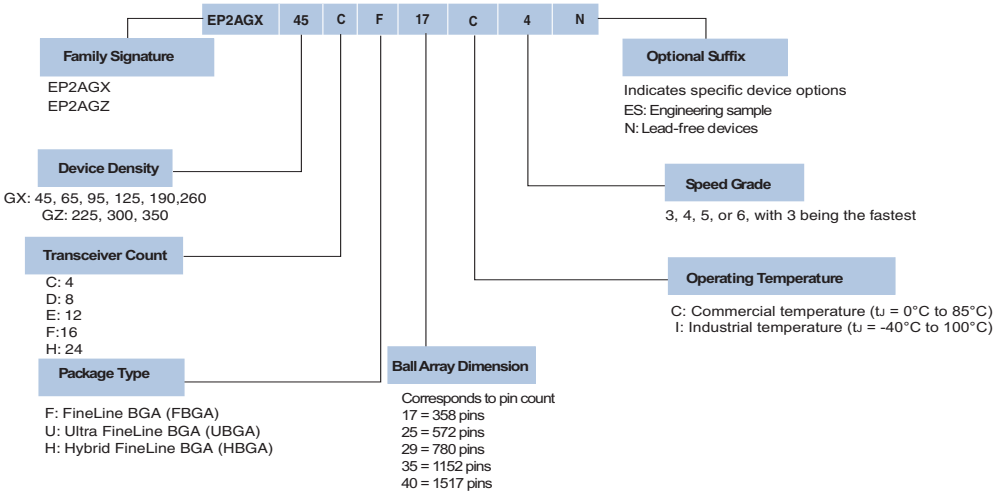
JTAG Boundary Scan Testing

- Supports JTAG IEEE Std. 1149.1 and IEEE Std. 1149.6 specifications
- IEEE Std. 1149.6 supports high-speed serial interface (HSSI) transceivers and performs boundary scan on alternating current (AC)-coupled transceiver channels
- Boundary-scan test (BST) architecture offers the capability to test pin connections without using physical test probes and capture functional data while a device is operating normally

Reference and Ordering Information

Figure 1–3 shows the ordering codes for Arria II devices.

Figure 1–3. Packaging Ordering Information for Arria II Devices



Document Revision History

Table 1–10 lists the revision history for this chapter.

Table 1–10. Document Revision History (Part 1 of 2)

Date	Version	Changes
July 2012	4.4	Replaced Table 1-10. External Memory Interface Maximum Performance for Arria II Devices with link to the External Memory Interface Spec Estimator online tool.
December 2011	4.3	Updated Table 1–4 and Table 1–9.
June 2011	4.2	Updated Table 1–2.
June 2011	4.1	■ Updated Figure 1–2. ■ Updated Table 1–10. ■ Updated the “Arria II Device Feature” section. ■ Added Table 1–6. ■ Minor text edits.
December 2010	4.0	■ Updated for the Quartus II software version 10.0 release ■ Added information about Arria II GZ devices ■ Updated Table 1–1, Table 1–4, Table 1–5, Table 1–6, Table 1–7, and Table 1–9 ■ Added Table 1–3 ■ Added Figure 1–2 ■ Updated Figure 1–3 ■ Updated “Arria II Device Feature” and “Arria II Device Architecture” section

Table 1–10. Document Revision History (Part 2 of 2)

Date	Version	Changes
July 2010	3.0	Updated for the Quartus II software version 10.0 release: ■ Added information about –I3 speed grade ■ Updated Table 1–1, Table 1–3, and Table 1–7 ■ Updated Figure 1–2 ■ Updated "Highlights" and "High-Speed LVDS I/O and DPA"section ■ Minor text edits
November 2009	2.0	■ Updated Table 1–1, Table 1–2, and Table 1–3 ■ Updated "Configuration Features" section
June 2009	1.1	■ Updated Table 1–2. ■ Updated "I/O Features" section.
February 2009	1.0	Initial release.

Стандарт Электрон Связь

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