SSM3J35AFS

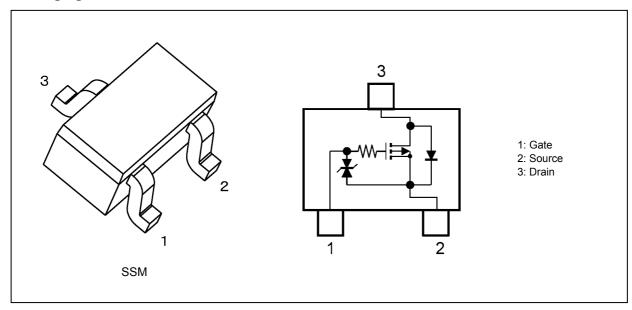
1. Applications

Analog Switches

2. Features

- (1) 1.2 V drive
- (2) ESD(HBM) level 2 kV
- (3) Low drain-source on-resistance : $R_{DS(ON)} = 3.2 \Omega$ (typ.) (@V_{GS} = -1.2 V)
 - $R_{DS(ON)} = 2.3 \Omega (typ.) (@V_{GS} = -1.5 V)$
 - $R_{DS(ON)} = 2.0 \ \Omega \ (typ.) \ (@V_{GS} = -1.8 \ V)$ $R_{DS(ON)} = 2.0 \ \Omega \ (typ.) \ (@V_{GS} = -1.8 \ V)$
 - $R_{DS(ON)} = 2.5 \Omega (typ.) (@V_{GS} = -2.5 V)$ $R_{DS(ON)} = 1.5 \Omega (typ.) (@V_{GS} = -2.5 V)$
 - $R_{DS(ON)} = 1.1 \Omega (typ.) (@V_{GS} = -4.5 V)$

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V _{DSS}	-20	V
Gate-source voltage		V _{GSS}	±10	
Drain current (DC)	(Note 1)	Ι _D	-250	mA
Drain current (pulsed)	(Note 1)	I _{DP}	-600	
Power dissipation	(Note 2)	PD	150	mW
Power dissipation	(Note 3)		500	
Channel temperature		T _{ch}	150	°C
Storage temperature		T _{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- Note 1: Ensure that the channel temperature does not exceed 150 °C.
- Note 2: Mounted on an FR4 board (25.4 mm \times 25.4 mm \times 1.6 mm, Cu pad: 0.36 mm² \times 3)
- Note 3: Mounted on an FR4 board (25.4 mm \times 25.4 mm \times 1.6 mm, Cu pad: 645 mm²)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

- Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.
- Note: The channel-to-ambient thermal resistance, R_{th(ch-a)}, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V	—	_	±1	μA
Drain cut-off current		I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	—		-1	
Drain-source breakdown voltage		V _{(BR)DSS}	I _D = -1 mA, V _{GS} = 0 V	-20	_	_	V
Drain-source breakdown voltage	(Note 1)	V _{(BR)DSX}	$I_{\rm D}$ = -1 mA, $V_{\rm GS}$ = 10 V	-10	_	_	
Gate threshold voltage	(Note 2)	V _{th}	V_{DS} = -10 V, I _D = -100 µA	-0.3	—	-1	
Drain-source on-resistance	(Note 3)	R _{DS(ON)}	I _D = -10 mA, V _{GS} = -1.2 V	_	3.2	20	Ω
			I _D = -20 mA, V _{GS} = -1.5 V	_	2.3	4.0	
			I _D = -50 mA, V _{GS} = -1.8 V	—	2.0	2.9	
			I _D = -150 mA, V _{GS} = -2.5 V	—	1.5	2.1	
			I _D = -150 mA, V _{GS} = -4.5 V	—	1.1	1.4	
Forward transfer admittance	(Note 3)	Y _{fs}	V _{DS} = -10 V, I _D = -100 mA	_	430	—	mS

Note 1: If a reverse bias is applied between gate and source, this device enters V_{(BR)DSX} mode. Note that the drainsource breakdown voltage is lowered in this mode.

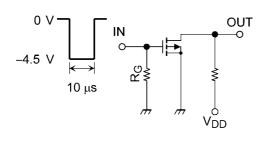
Note 3: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25$ °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V,	_	21	42	pF
Reverse transfer capacitance	C _{rss}	f = 1 MHz		2	_	
Output capacitance	C _{oss}			6	_	
Switching time (rise time)	tr	V _{DD} = -10 V, I _D = -50 mA,	_	42	_	ns
Switching time (turn-on delay time)	t _{d(on)}	V _{GS} = 0 to -4.5 V, R _G = 10 Ω Duty ≤ 1%, V _{IN} : t _r , t _f < 5 ns,		17	_	
Switching time (fall time)	t _f	Common source, See Chapter 5.3.		145	_	
Switching time (turn-off delay time)	t _{d(off)}			420	_	

0 V

5.3. Switching Time Test Circuit



-4.5 V $V_{DS(ON)}$ V_{DD} V_{DD} U_{DD} U_{DD}

Fig. 5.3.1 Switching Time Test Circuit

Fig. 5.3.2 Input Waveform/Output Waveform

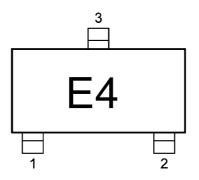
Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-100 μ A for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th} , and $V_{GS(OFF)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$. Take this into consideration when using the device.

5.4. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25$ °C)

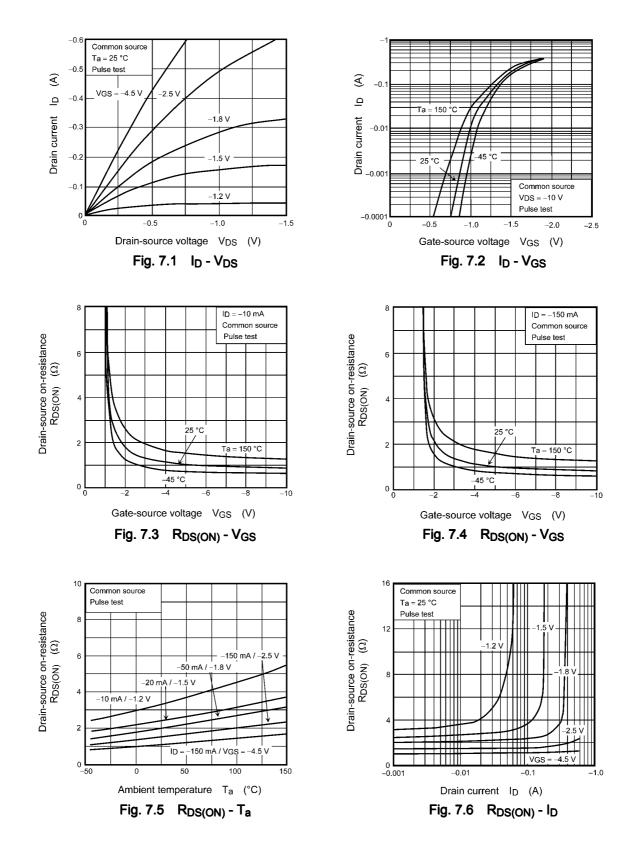
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	(Note 1)	V_{DSF}	$I_{\rm D}$ = 100 mA, $V_{\rm GS}$ = 0 V	_	0.83	1.2	V

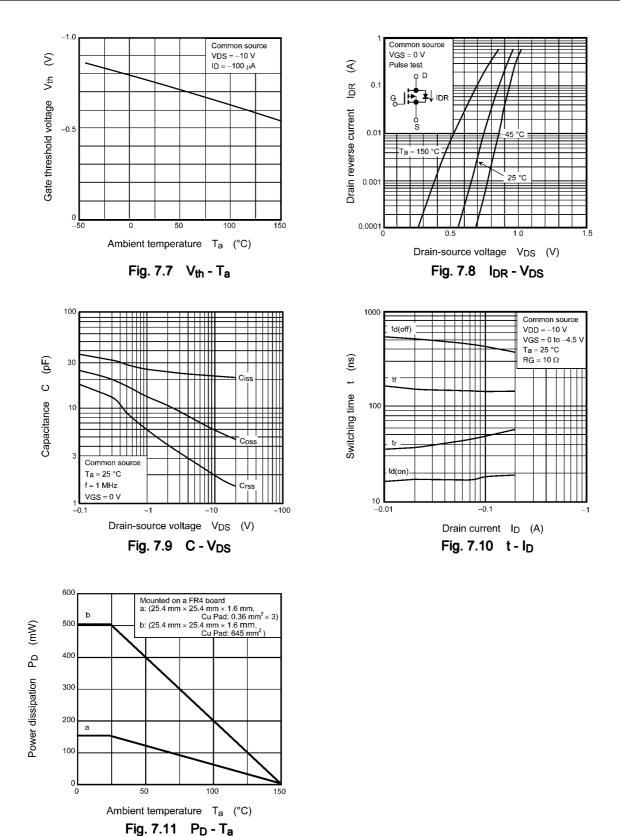
Note 1: Pulse measurement.

6. Marking



7. Characteristics Curves (Note)





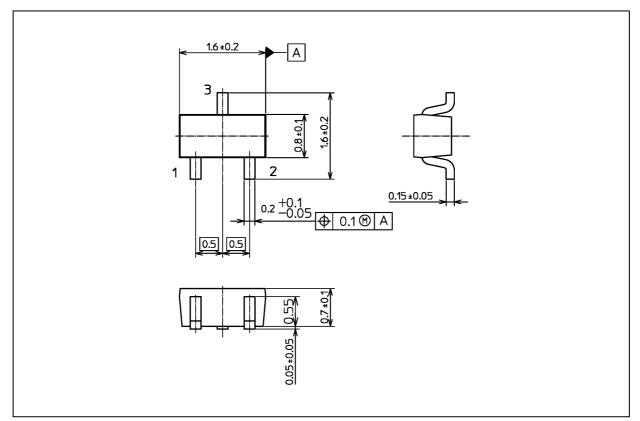
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



SSM3J35AFS

Package Dimensions

Unit: mm



Weight: 2.4 mg (typ.)

	Package Name(s)	
JEDEC: SOT-416		
Nickname: SSM		

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